



STP78N75F4

N-channel 75 V, 0.0092 Ω typ., 78 A STripFET™ DeepGATE™ Power MOSFET in TO-220 package

Datasheet — production data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STP78N75F4	75 V	< 0.011 Ω	78 A

- N-channel enhancement mode
- 100% avalanche rated
- Low gate charge
- Very low on-resistance

Application

- Switching applications

Description

This device is an N-channel Power MOSFET developed using ST's STripFET™ DeepGATE™ technology. The device has a new gate structure and is specially designed to minimize on-state resistance to provide superior switching performance.

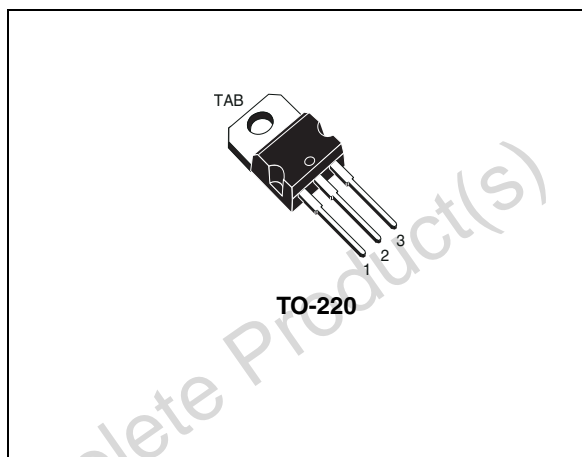


Figure 1. Internal schematic diagram

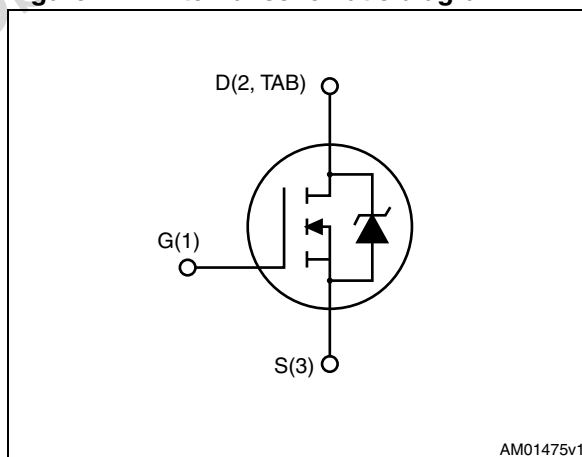


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP78N75F4	78N75F4	TO-220	Tube

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	78	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	55	A
$I_{DM}^{(1)}$	Drain current (pulsed)	312	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
	Derating factor	1	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	185	mJ
T_{stg}	Storage temperature	- 55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Pulse width limited by safe operating area

2. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 35\text{ A}$, $V_{DD} = 50\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown voltage	I _D = 250 μA, V _{GS} = 0	75			V
I _{DSS}	Zero gate voltage	V _{DS} = 75 V			1	μA
	Drain current (V _{GS} = 0)	V _{DS} = 75 V, T _C = 125 °C			100	μA
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2		4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 39 A		0.0092	0.011	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance			5015		pF
C _{oss}	Output capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	382	-	pF
C _{rss}	Reverse transfer capacitance			218		pF
Q _g	Total gate charge	V _{DD} = 37.5 V, I _D = 78 A, V _{GS} = 10 V		76		nC
Q _{gs}	Gate-source charge	(see Figure 14)	-	23	-	nC
Q _{gd}	Gate-drain charge			18.5		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 37.5 V, I _D = 39 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13)		25		ns
t _r	Rise time			33		ns
t _{d(off)}	Turn-off-delay time			61		ns
t _f	Fall time			14		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		78	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		312	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 78 \text{ A}, V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 78 \text{ A}, V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s},$ $T_j = 150 \text{ }^\circ\text{C}$ <i>(see Figure 15)</i>	-	67		ns
Q_{rr}	Reverse recovery charge			183		nC
I_{RRM}	Reverse recovery current			5.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

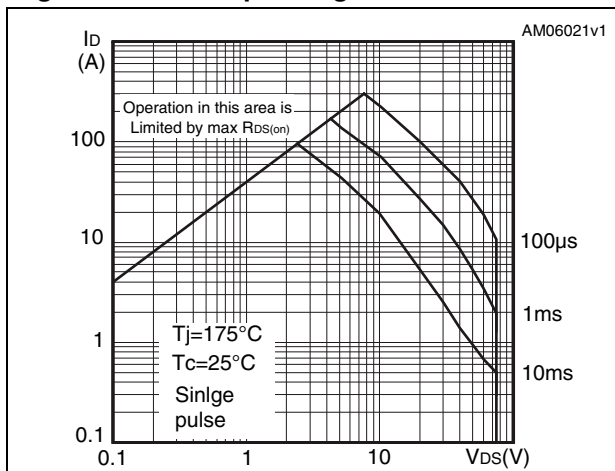


Figure 3. Thermal impedance

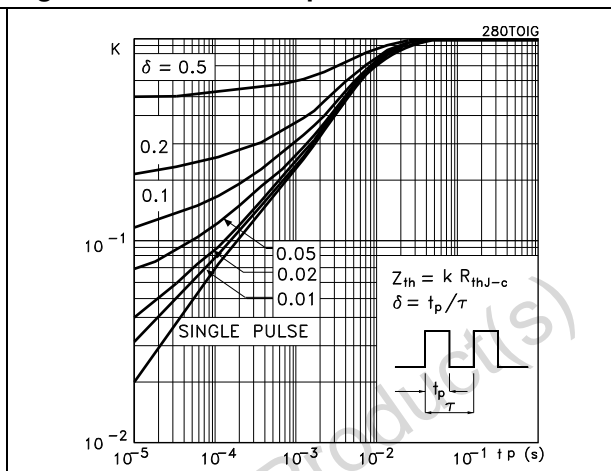


Figure 4. Output characteristics

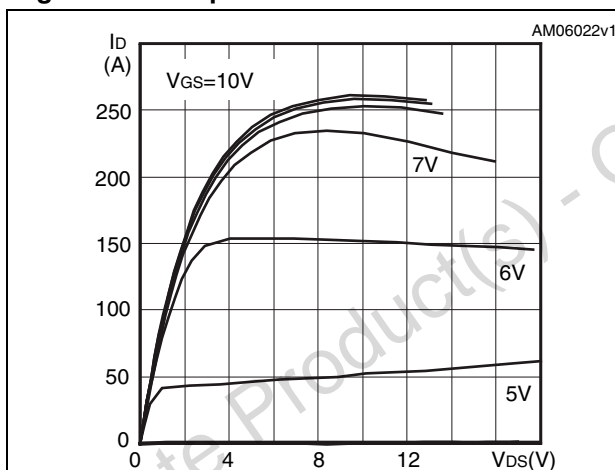


Figure 5. Transfer characteristics

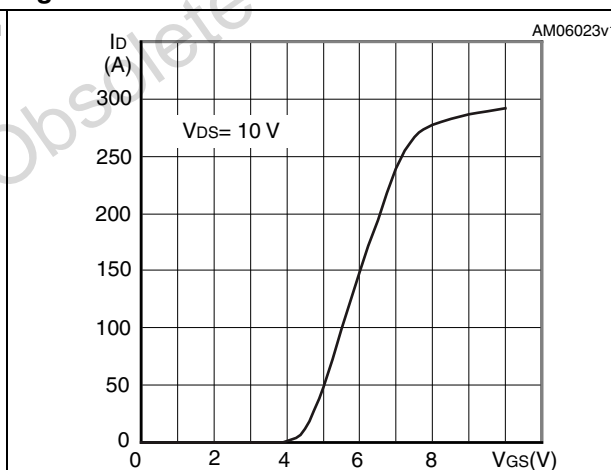


Figure 6. Normalized BV_{DSS} vs temperature

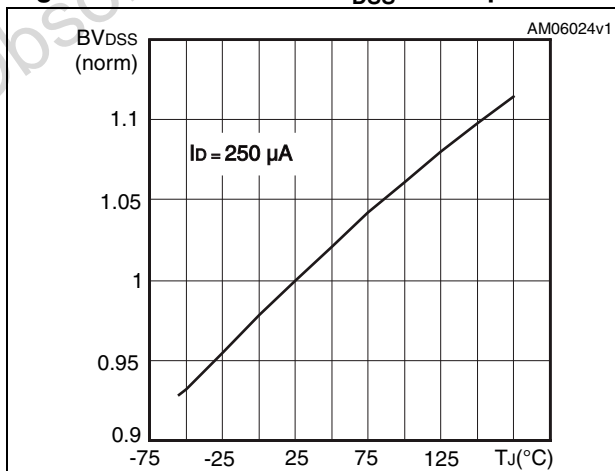


Figure 7. Static drain-source on-resistance

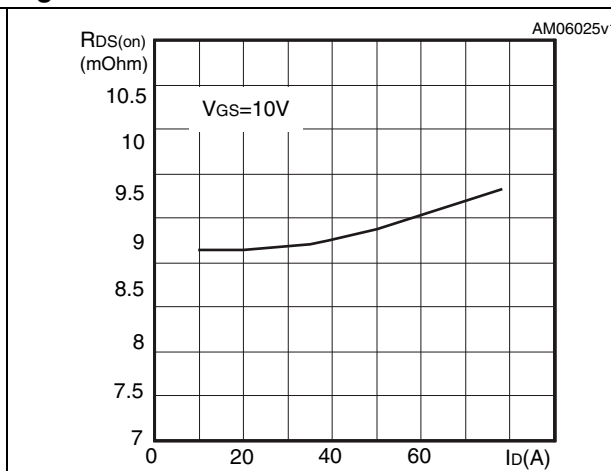


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

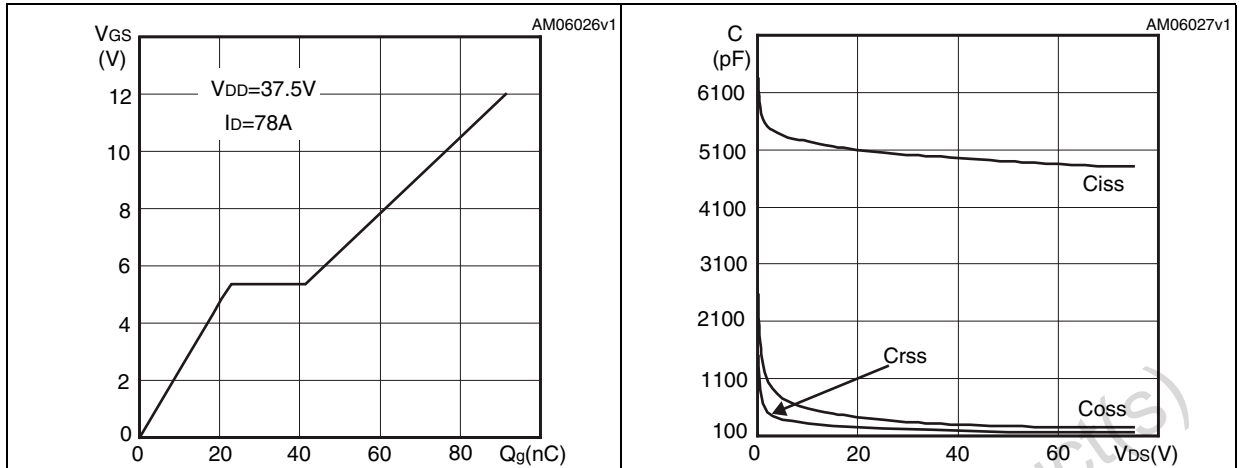


Figure 10. Normalized on-resistance vs temperature

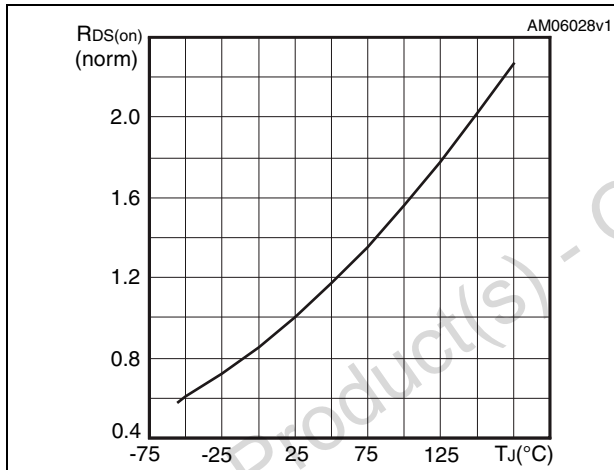


Figure 11. Normalized gate threshold voltage vs temperature

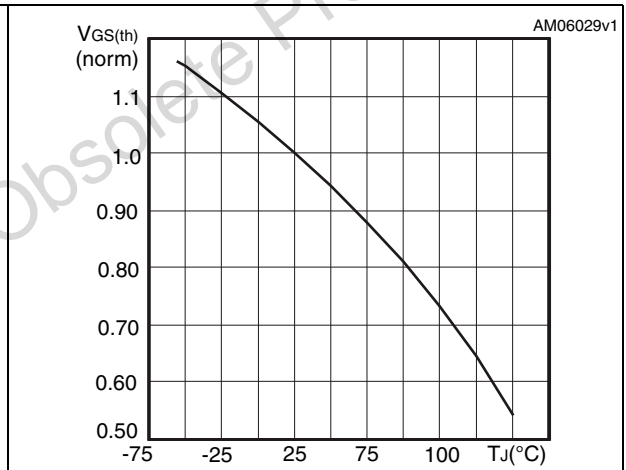
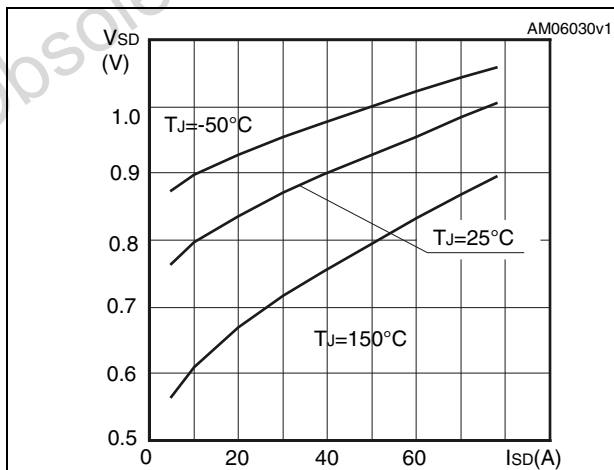
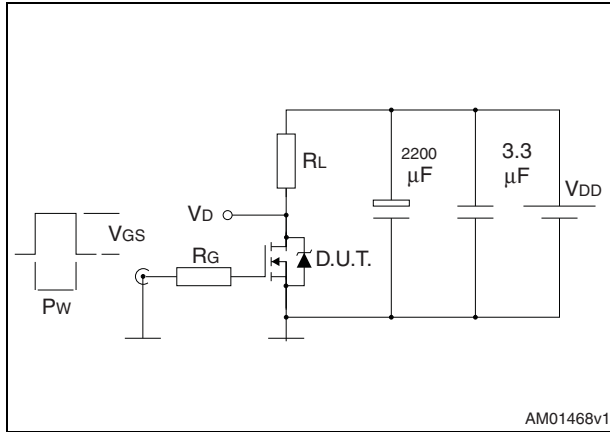


Figure 12. Source-drain diode forward characteristics



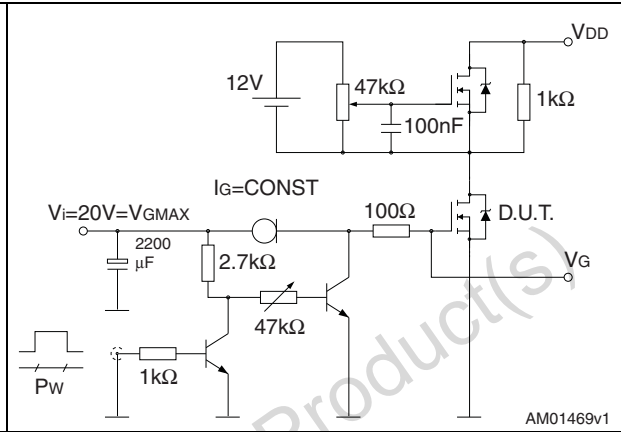
3 Test circuits

Figure 13. Switching times test circuit for resistive load



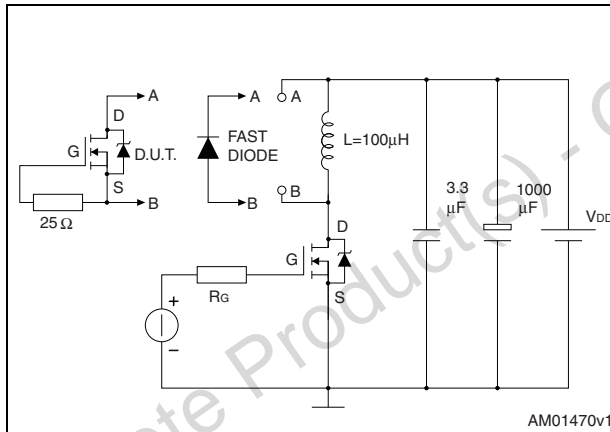
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Figure 14. Gate charge test circuit



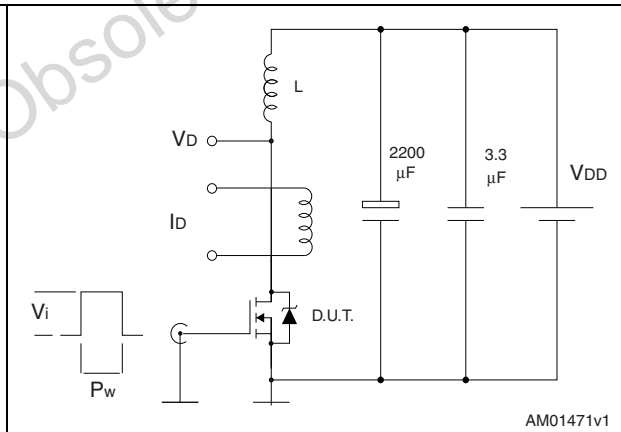
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Figure 15. Test circuit for inductive load switching and diode recovery times



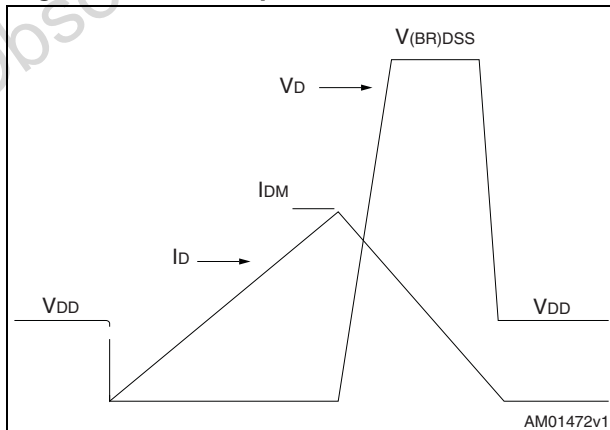
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Figure 16. Unclamped inductive load test circuit



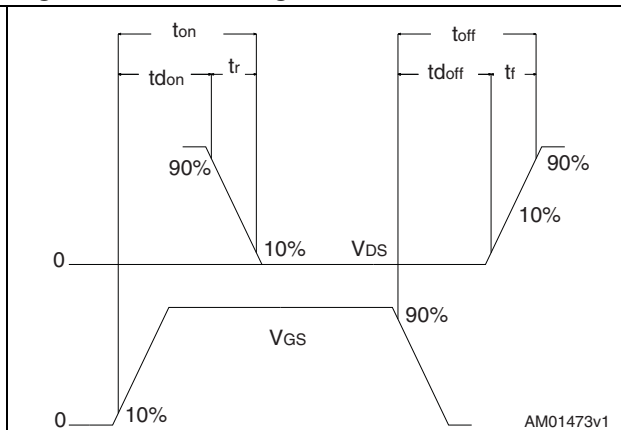
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Figure 17. Unclamped inductive waveform



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Figure 18. Switching time waveform



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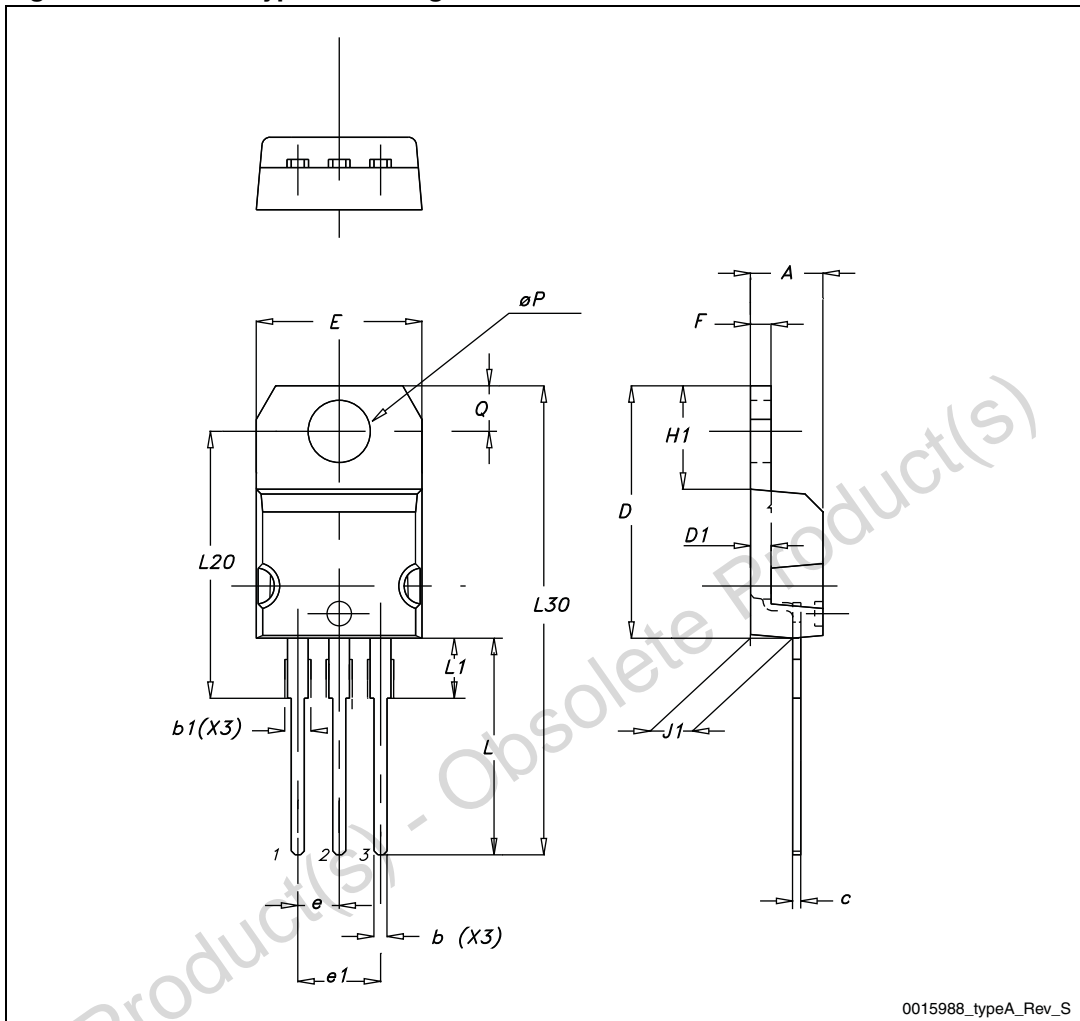
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 19. TO-220 type A drawing



0015988_typeA_Rev_S

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-May-2009	1	First release.
26-Nov-2009	2	Document status promoted from preliminary data to datasheet (see Section 2.1: Electrical characteristics (curves)).
24-Jul-2012	3	Minor text changes on the cover page. Updated Section 4: Package mechanical data .

Obsolete Product(s) - Obsolete Product(s)

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