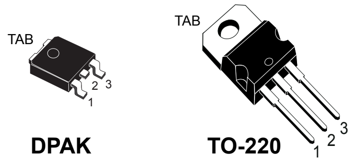
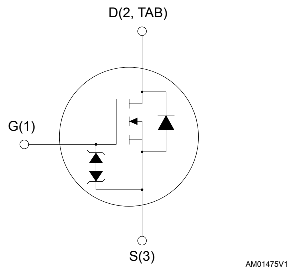
STD7N52K3, STP7N52K3

Datasheet

N-channel 525 V, 0.72 Ω typ., 6 A, MDmesh™ K3 Power MOSFETs in DPAK and TO-220 packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD7N52K3	525 V	0.85 Ω	6 A	90 W
STP7N52K3				

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

These MDmesh™ K3 Power MOSFETs are the result of improvements applied to STMicroelectronics’ MDmesh™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

Product status links
STD7N52K3
STP7N52K3

Product summary	
STD7N52K3	
Order code	STD7N52K3
Marking	7N52K3
Package	DPAK
Packing	Tape and reel
STP7N52K3	
Order code	STP7N52K3
Marking	7N52K3
Package	TO-220
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	6	A
	Drain current (continuous) at T_C = 100 °C	3.8	A
I_{DM}(1)	Drain current (pulsed)	24	A
P_{TOT}	Total dissipation at T_C = 25 °C	90	W
I_{AR}(2)	Avalanche current, repetitive or non-repetitive	3	A
E_{AS}(3)	Single pulse avalanche energy	100	mJ
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	2.5	kV
dv/dt(4)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Pulse width is limited by T_{Jmax}.*
3. *Starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V*
4. *$I_{SD} \leq 6$ A, di/dt ≤ 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*

Table 2. **Thermal data**

Symbol	Parameter	Value		Unit
		DPAK	TO-220	
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.39		°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50		°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	525			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 525 V			1	µA
		V_{GS} = 0 V, V_{DS} = 525 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3 A		0.72	0.85	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	870	-	pF
C_{oss}	Output capacitance			70		
C_{rss}	Reverse transfer capacitance			13		
$C_{oss(tr)}$(1)	Equivalent output capacitance	V_{DS} = 0 to 420 V, V_{GS} = 0 V,	-	53	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 420 V, I_D = 6 A, V_{GS} = 0 to 10 V (see Figure 17. Test circuit for gate charge behavior)	-	33	-	nC
Q_{gs}	Gate-source charge			6		
Q_{gd}	Gate-drain charge			21		

1. *$C_{oss(tr)}$ is defined as the constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 420 V.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 260 V, I_D = 3 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	13	-	ns
t_r	Rise time			11		
$t_{d(off)}$	Turn-off delay time			36		
t_f	Fall time			19		

Table 6. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
I_{SDM}(1)	Source-drain current (pulsed)				24	
V_{SD}(2)	Forward on voltage	I_{SD} = 6 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	220		ns
Q_{rr}	Reverse recovery charge			1.8		µC
I_{RRM}	Reverse recovery current			16		A
t_{rr}	Reverse recovery time	I_{SD} = 6 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 18. Test circuit for inductive load switching and diode recovery times)	-	250		ns
Q_{rr}	Reverse recovery charge			2.2		µC
I_{RRM}	Reverse recovery current			18		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

Table 7. **Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for DPAK

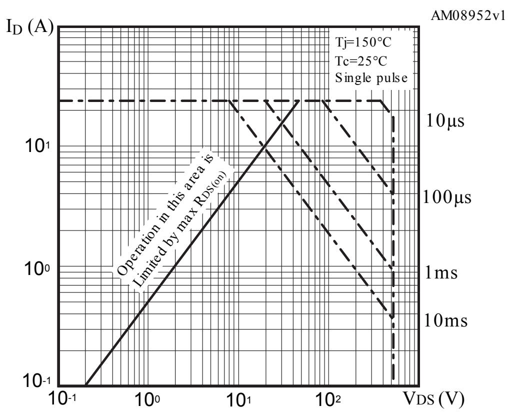


Figure 2. Thermal impedance for DPAK

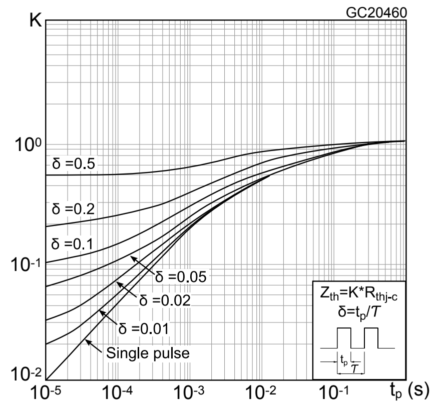


Figure 3. Safe operating area for TO-220

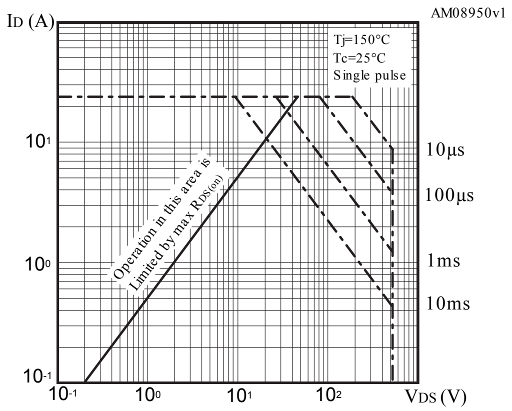


Figure 4. Thermal impedance for TO-220

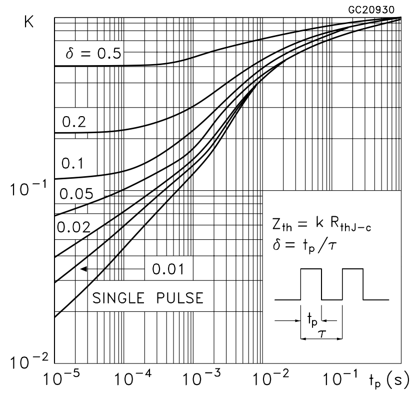


Figure 5. Output characteristics

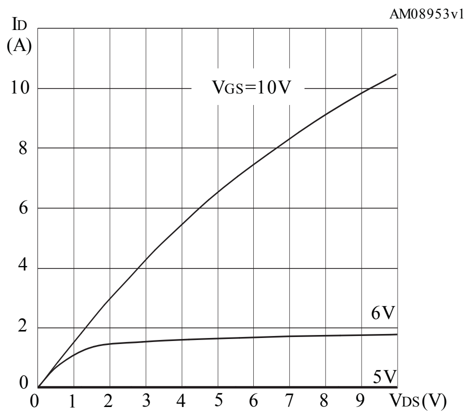


Figure 6. Transfer characteristics

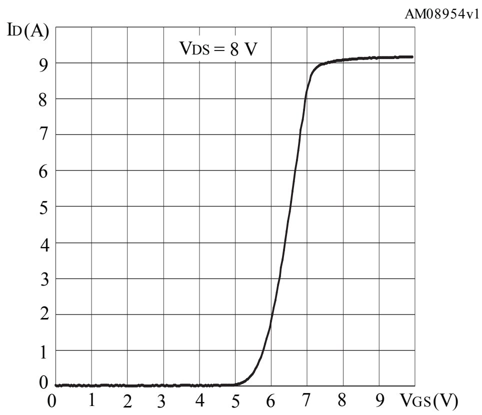


Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

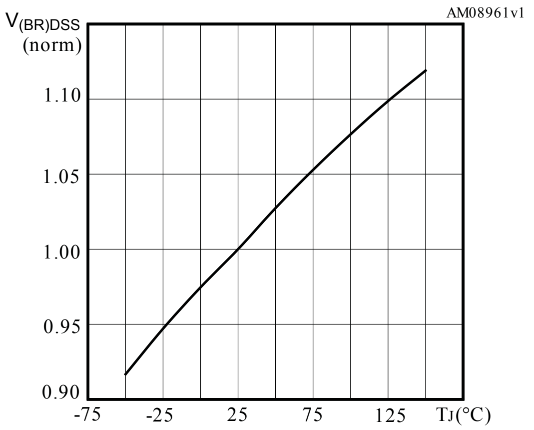


Figure 8. Static drain-source on-resistance

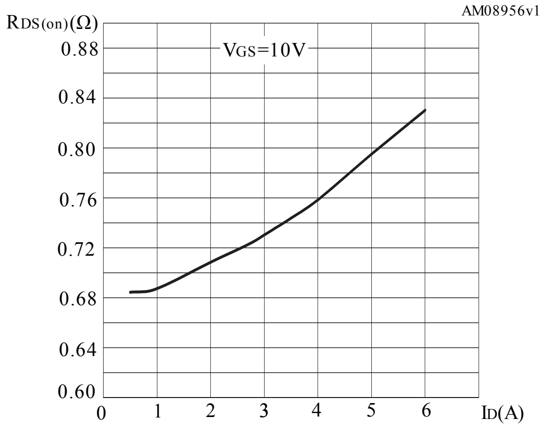


Figure 9. Output capacitance stored energy

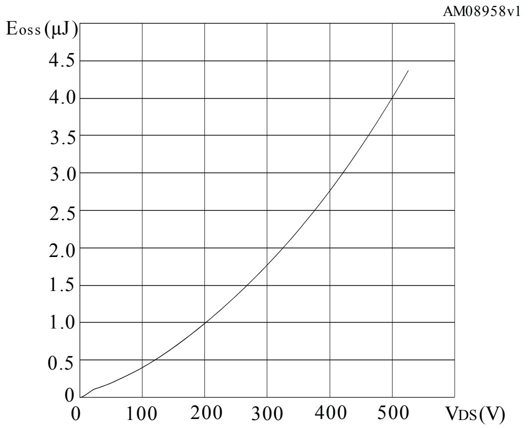


Figure 10. Capacitance variations

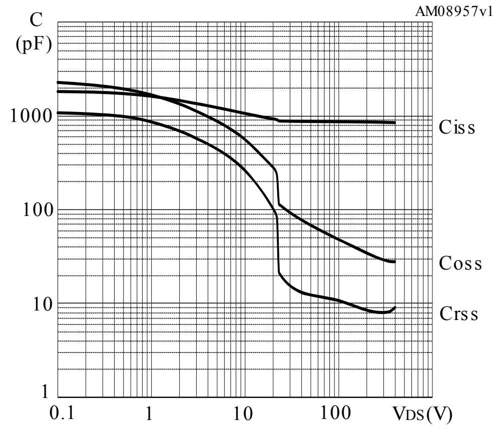


Figure 11. Gate charge vs gate-source voltage

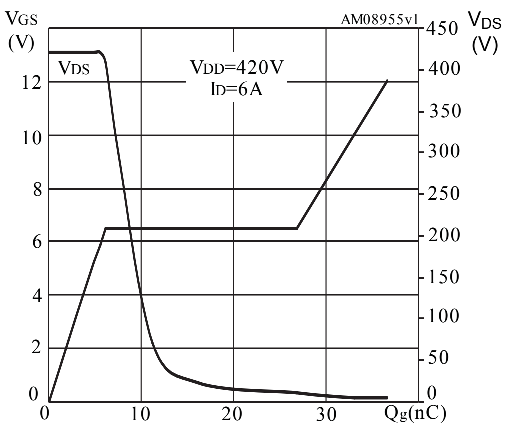


Figure 12. Normalized on-resistance vs temperature

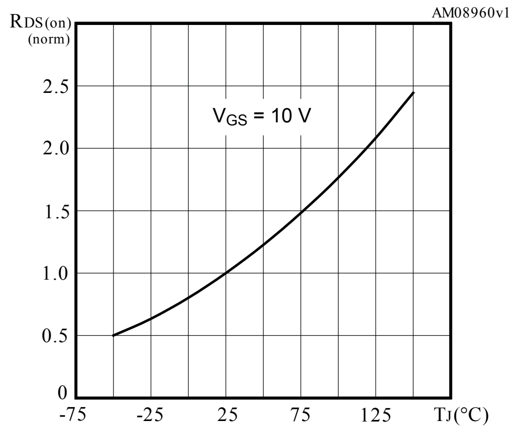


Figure 13. Normalized gate threshold voltage vs temperature

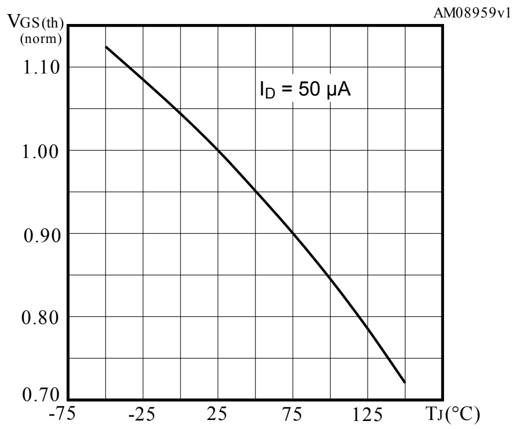


Figure 14. Maximum avalanche energy vs temperature

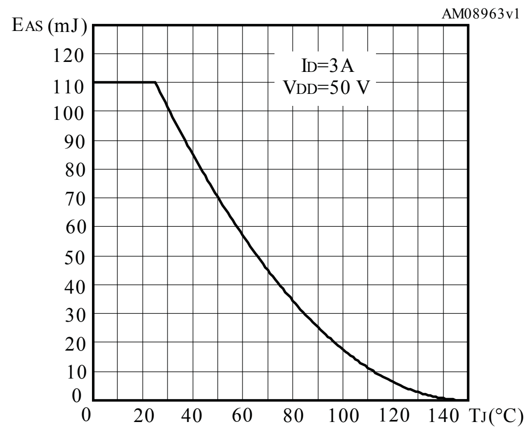
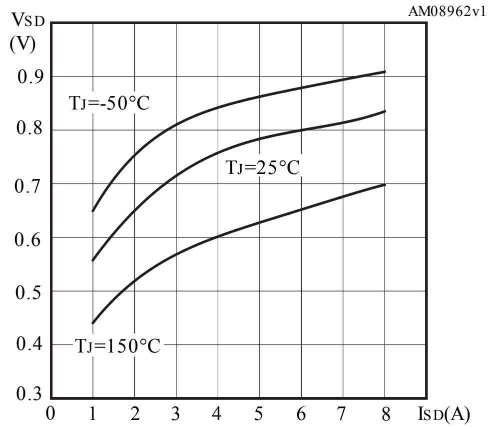


Figure 15. Source-drain diode forward characteristics



3 Test circuits

Figure 16. Test circuit for resistive load switching times

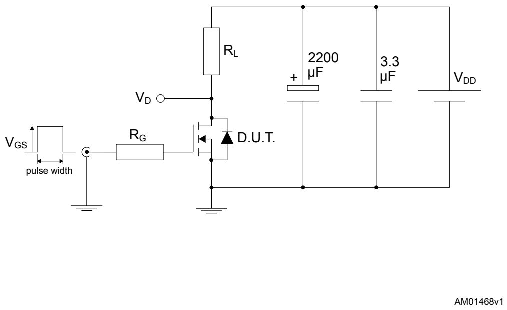


Figure 17. Test circuit for gate charge behavior

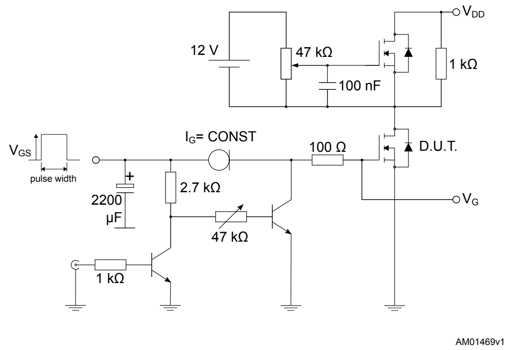


Figure 18. Test circuit for inductive load switching and diode recovery times

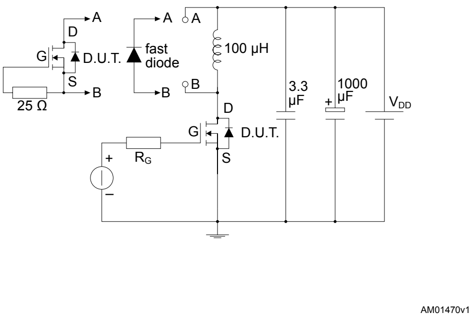


Figure 19. Unclamped inductive load test circuit

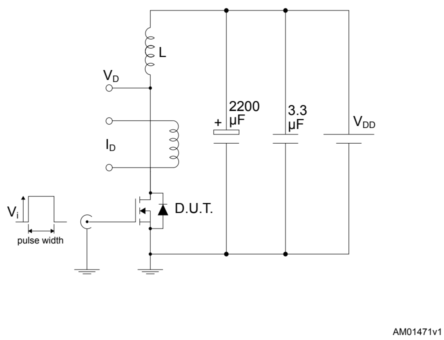


Figure 20. Unclamped inductive waveform

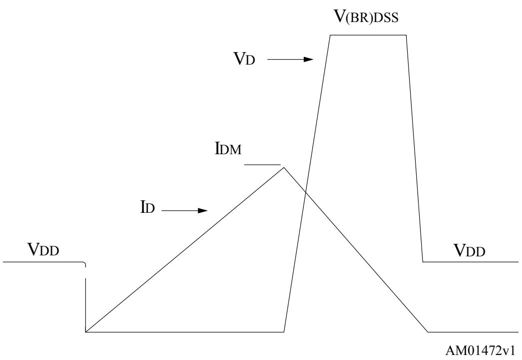
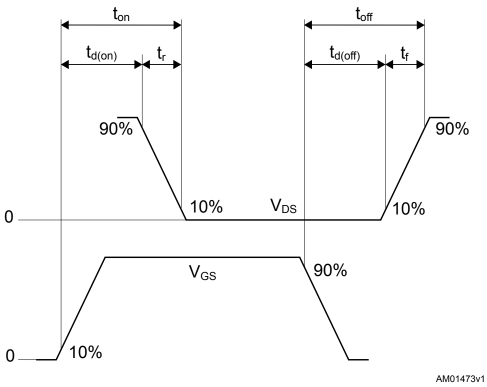


Figure 21. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 22. **DPAK (TO-252) type A2 package outline**

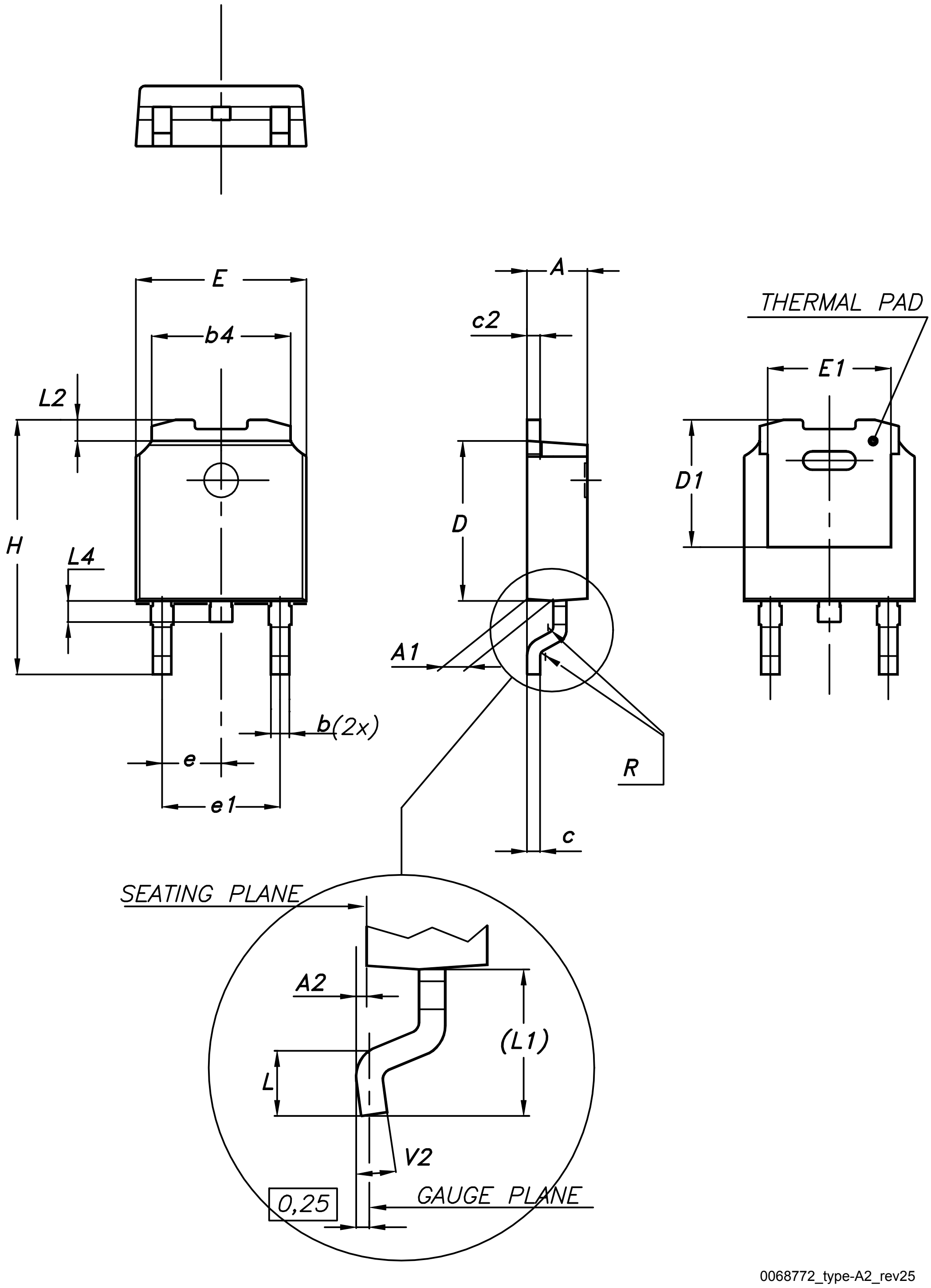


Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 23. **DPAK (TO-252) type C2 package outline**

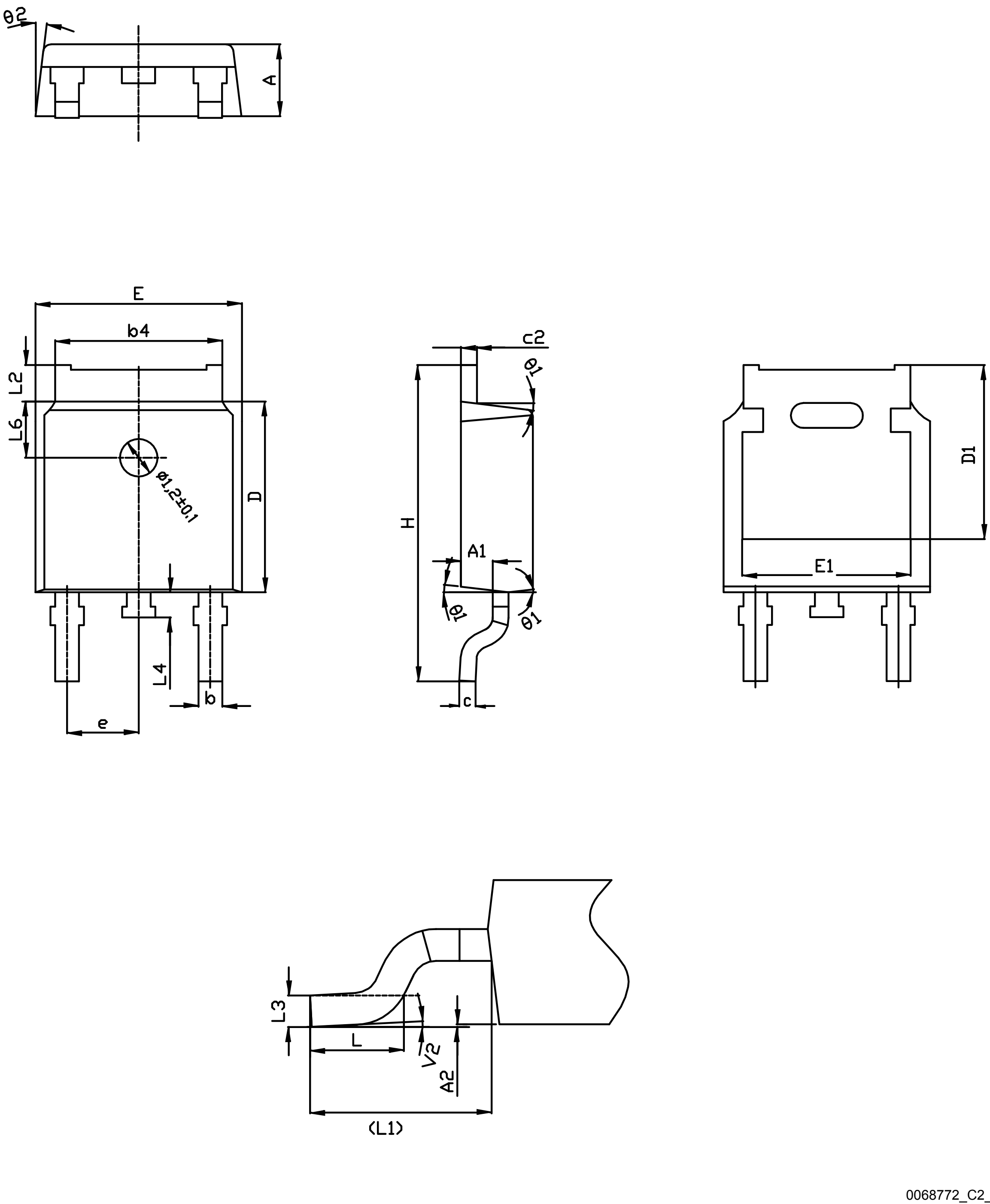
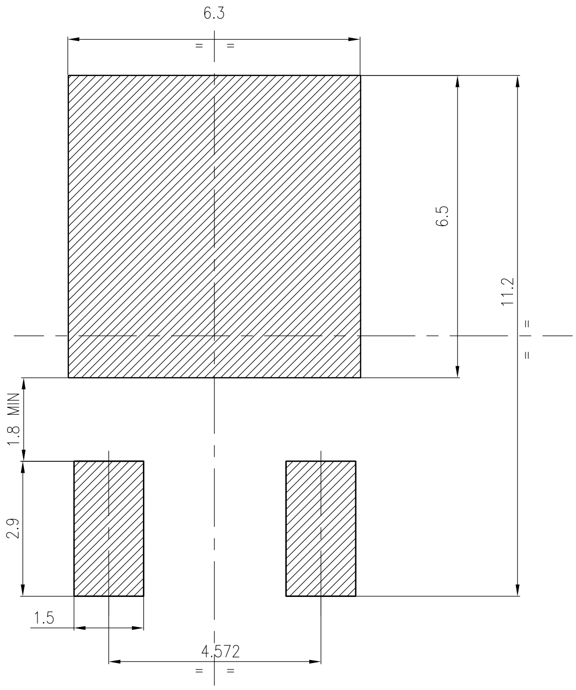


Table 9. **DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



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4.3 DPAK (TO-252) packing information

Figure 25. DPAK (TO-252) tape outline

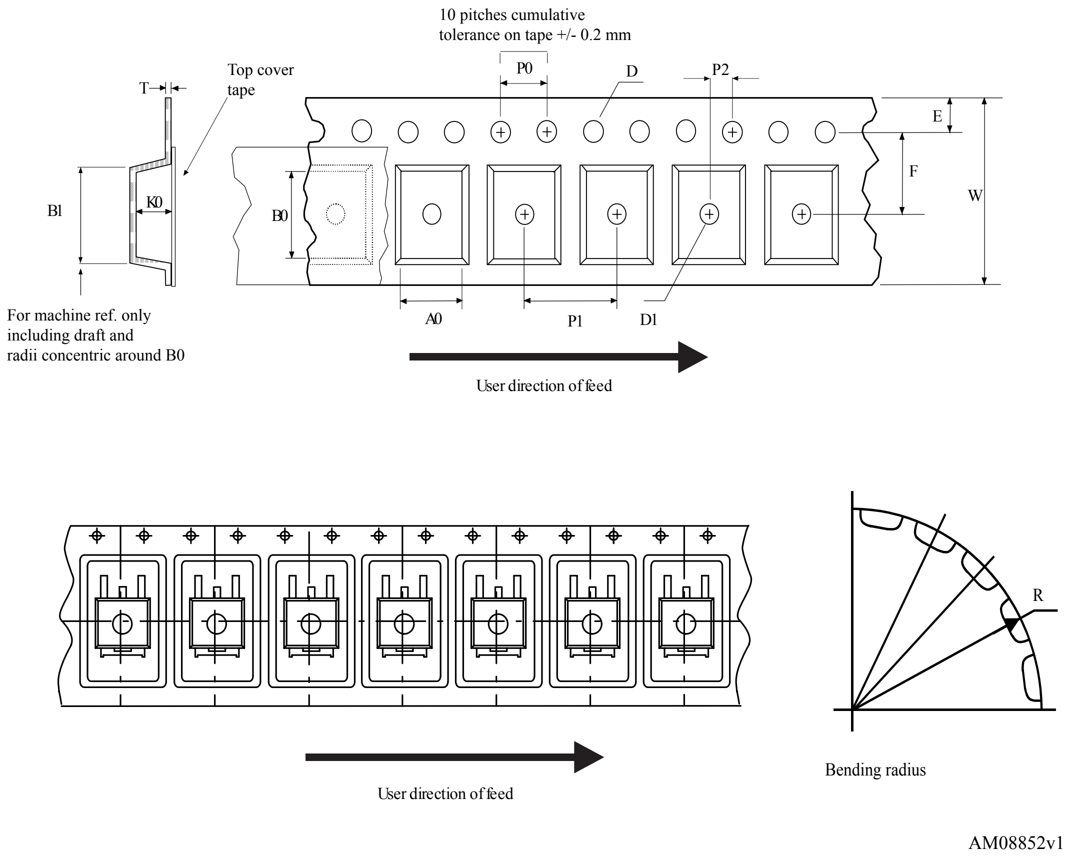

Figure 26. **DPAK (TO-252) reel outline**

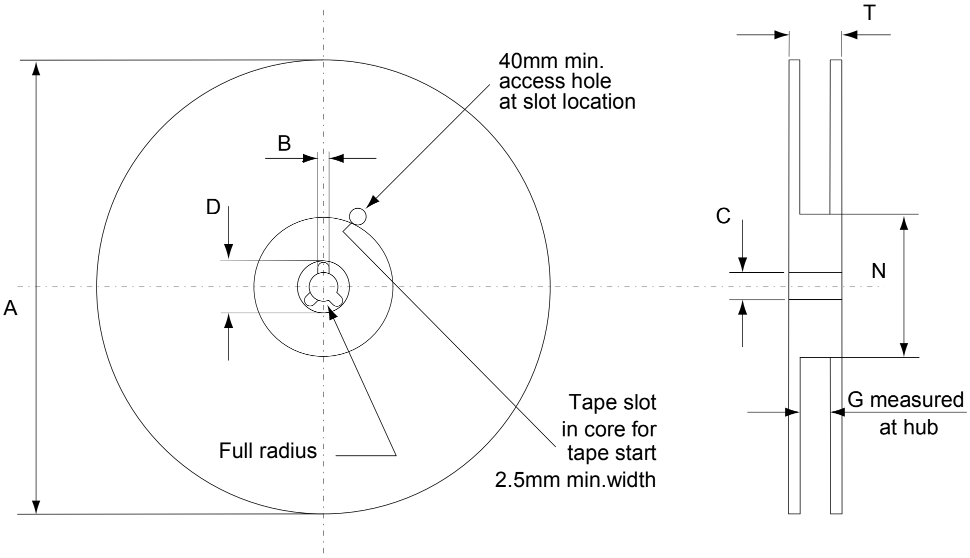

Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 27. TO-220 type A package outline

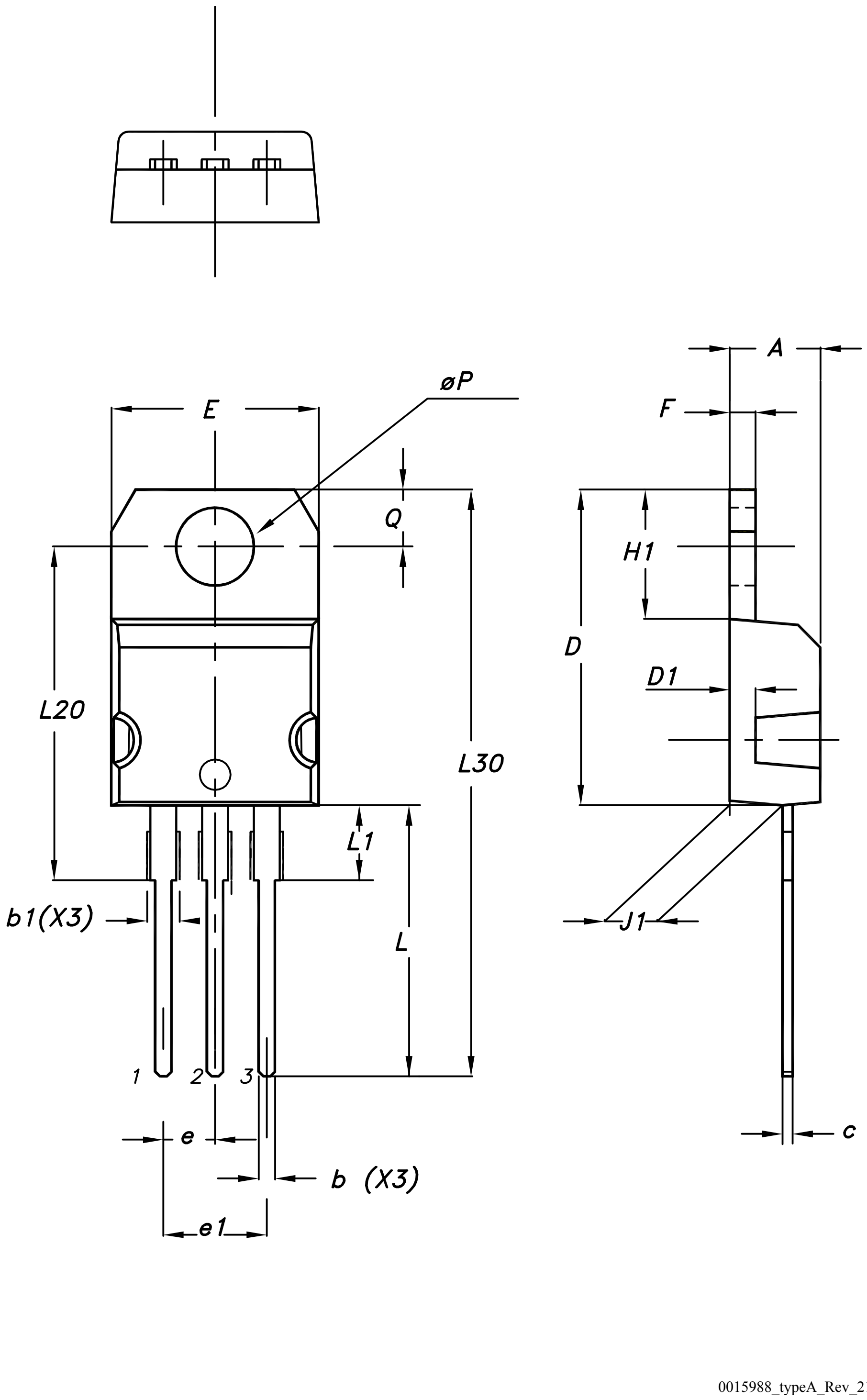

Table 11. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

Revision history

Table 12. **Document revision history**

Date	Version	Changes
07-Jul-2008	1	First release.
10-Sep-2009	2	Document status promoted from preliminary data to datasheet.
27-Jun-2011	3	*Section 2.1: Electrical characteristics (curves)* has been updated.
07-Mar-2012	4	Updated *Section 4: Package mechanical data*. Minor text changes.
11-Jul-2018	5	Part numbers STB7N52K3 and STF7N52K3 have been moved to a different datasheet, and the document has been updated accordingly. Updated features and description on cover page. Updated *Table 1. Absolute maximum ratings*. Updated *Section 4.1 DPAK (TO-252) type A2 package information*. Minor text changes.
01-Aug-2018	6	Updated Table 1. Absolute maximum ratings.

Contents