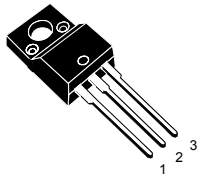
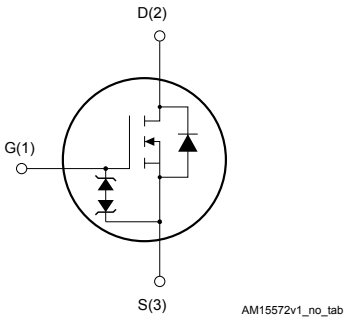
N-channel 400 V, 0.85 Ω typ., 5.4 A SuperMESH Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP7NK40ZFP	400 V	1 Ω	5.4 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STP7NK40ZFP

Product summary	
Order code	STP7NK40ZFP
Marking	P7NK40ZFP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	400	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	400	V
V_{GS}	Gate-source voltage	±30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	5.4	A
	Drain current (continuous) at T_C = 100 °C	3.4	
I_{DM}(1)(2)	Drain current (pulsed)	21.6	A
P_{TOT}	Total power dissipation at T_C = 25 °C	70	W
ESD	Gate-source, human body model (R = 1.5 kΩ, C = 100 pF)	3	kV
dv/dt(3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *This value is limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 5.4 A, di/dt ≤ 200 A/µs, V_{DD} < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	5	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	5.4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	130	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	400			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 400 V			1	µA
		V_{GS} = 0 V, V_{DS} = 400 V, T_C = 125 °C(1)			50	
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 2.7 A		0.85	1	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	535		pF
C_{oss}	Output capacitance		-	82		pF
C_{rss}	Reverse transfer capacitance		-	18		pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 320 V	-	53		pF
Q_g	Total gate charge	V_{DD} = 320 V, I_D = 5.4 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	19	26	nC
Q_{gs}	Gate-source charge		-	4		nC
Q_{gd}	Gate-drain charge		-	10		nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 200 V, I_D = 2.7 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	15	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	12	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 320 V, I_D = 5.4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	12	-	ns
t_f	Fall time		-	10	-	ns
t_c	Crossover time		-	20	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		5.4	A
I_{SDM}(1)	Source-drain current (pulsed)		-		21.6	A
V_{SD}(2)	Forward on voltage	I_{SD} = 5.4 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 5.4 A, di/dt = 100 A/µs,	-	220		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 50 V, T_J = 150 °C	-	990		nC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*
2. *Pulse width is limited by safe operating area.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

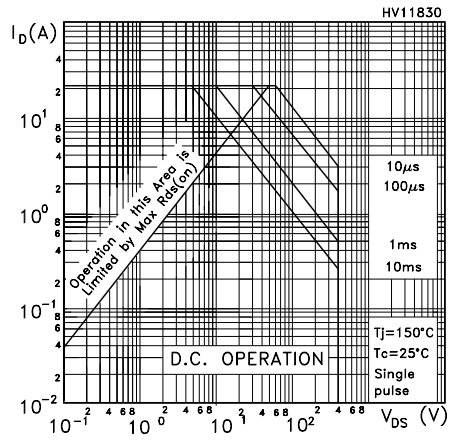


Figure 2. Thermal impedance

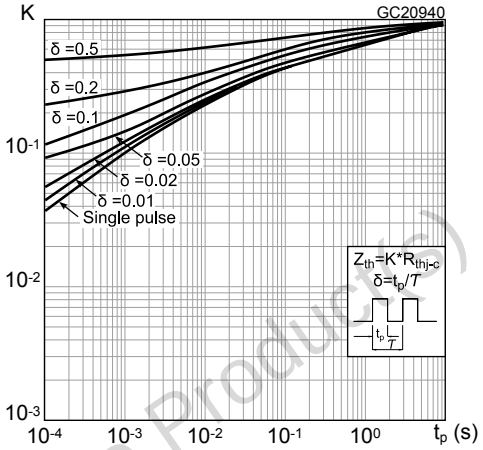


Figure 3. Output characteristics

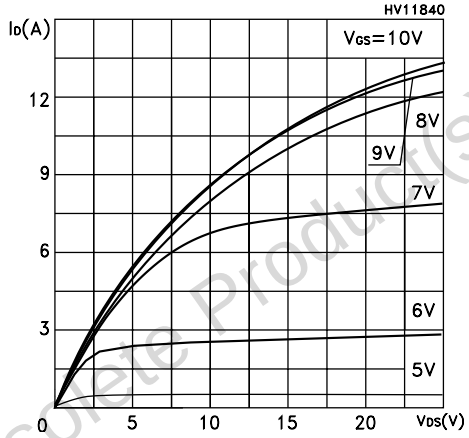


Figure 4. Transfer characteristics

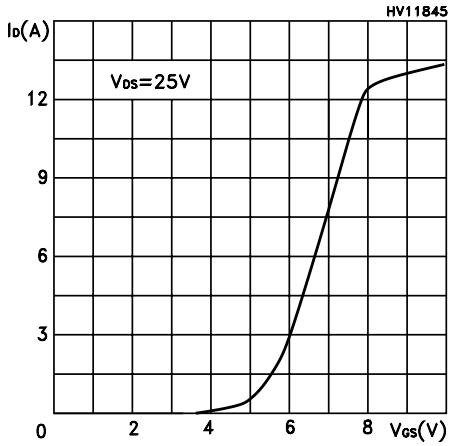


Figure 5. Static drain-source on-resistance

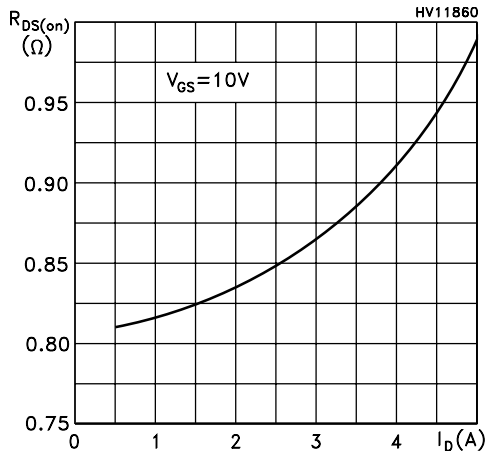


Figure 6. Gate charge vs gate-source voltage

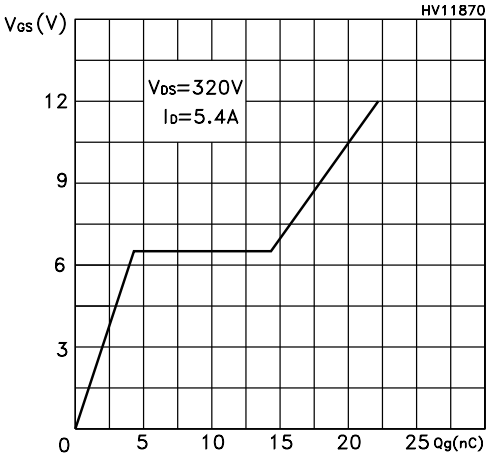


Figure 7. Capacitance variations

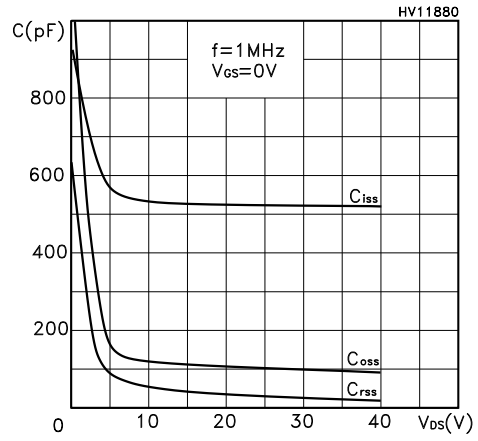


Figure 8. Normalized gate threshold voltage vs temperature

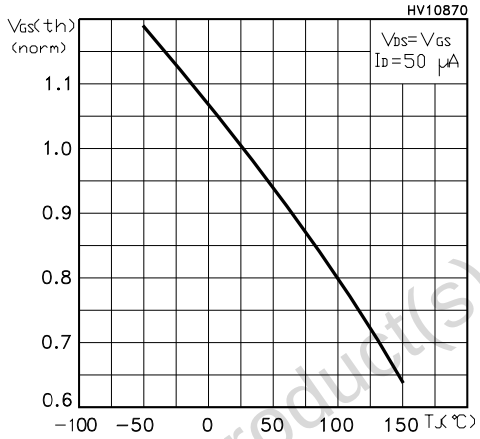


Figure 9. Normalized on-resistance vs temperature

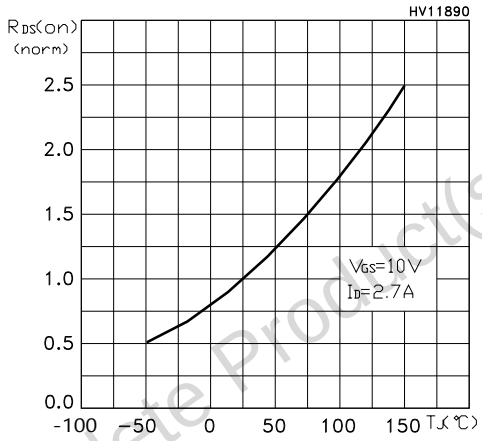


Figure 10. Source-drain diode forward characteristics

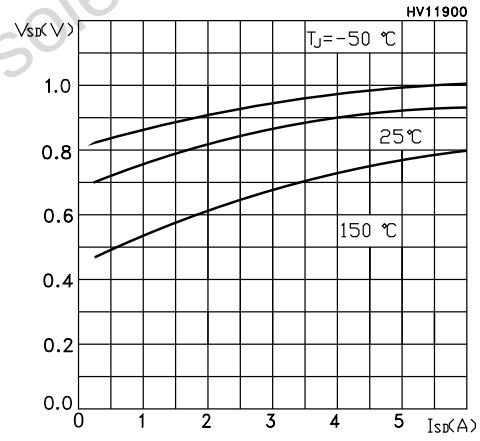


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

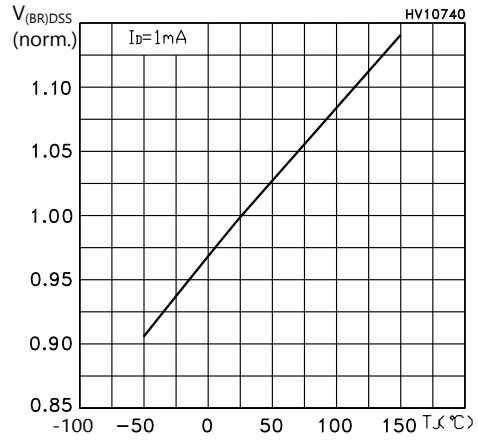
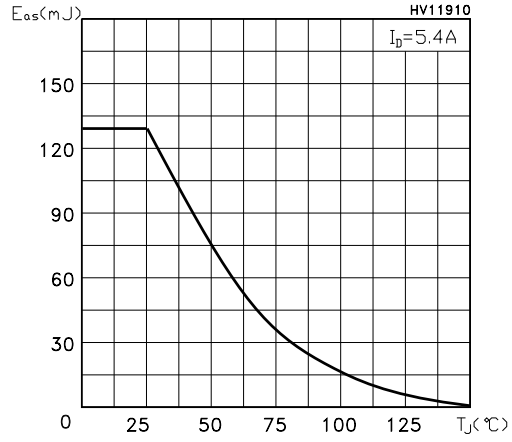
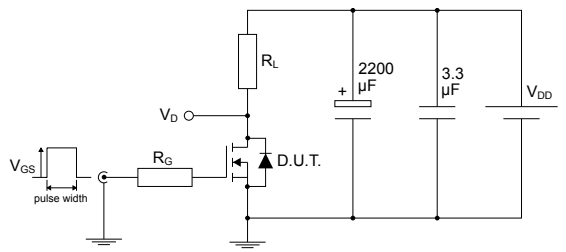


Figure 12. Maximum avalanche energy vs temperature



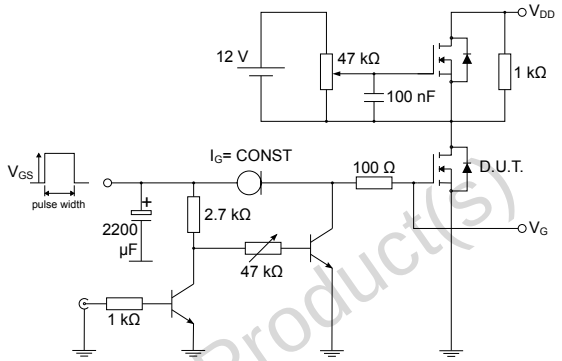
3 Test circuits

Figure 13. Test circuit for resistive load switching times



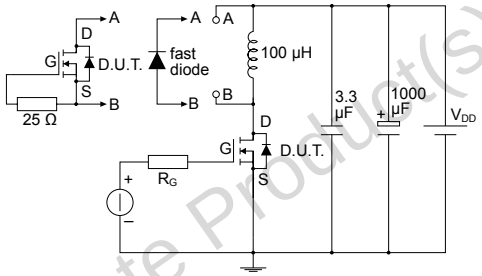
AM01468v1

Figure 14. Test circuit for gate charge behavior



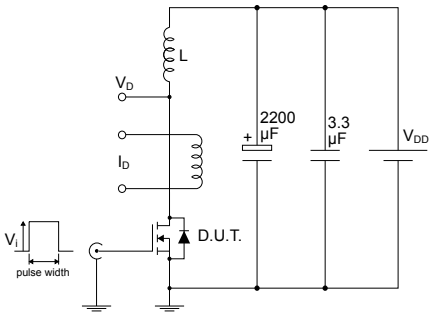
AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times



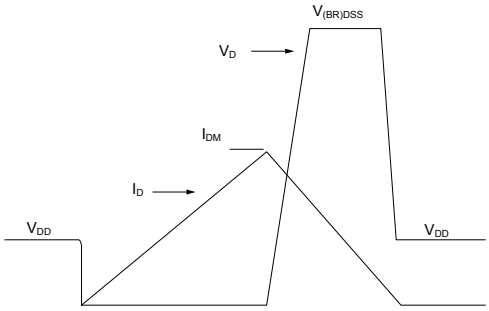
AM01470v1

Figure 16. Unclamped inductive load test circuit



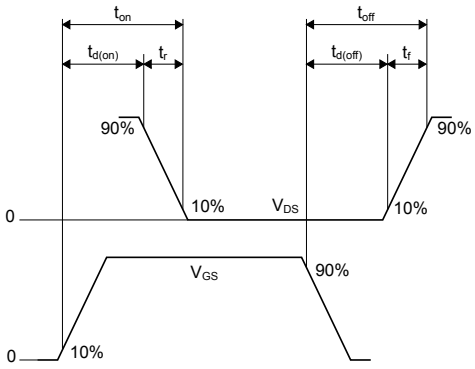
AM01471v1

Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline

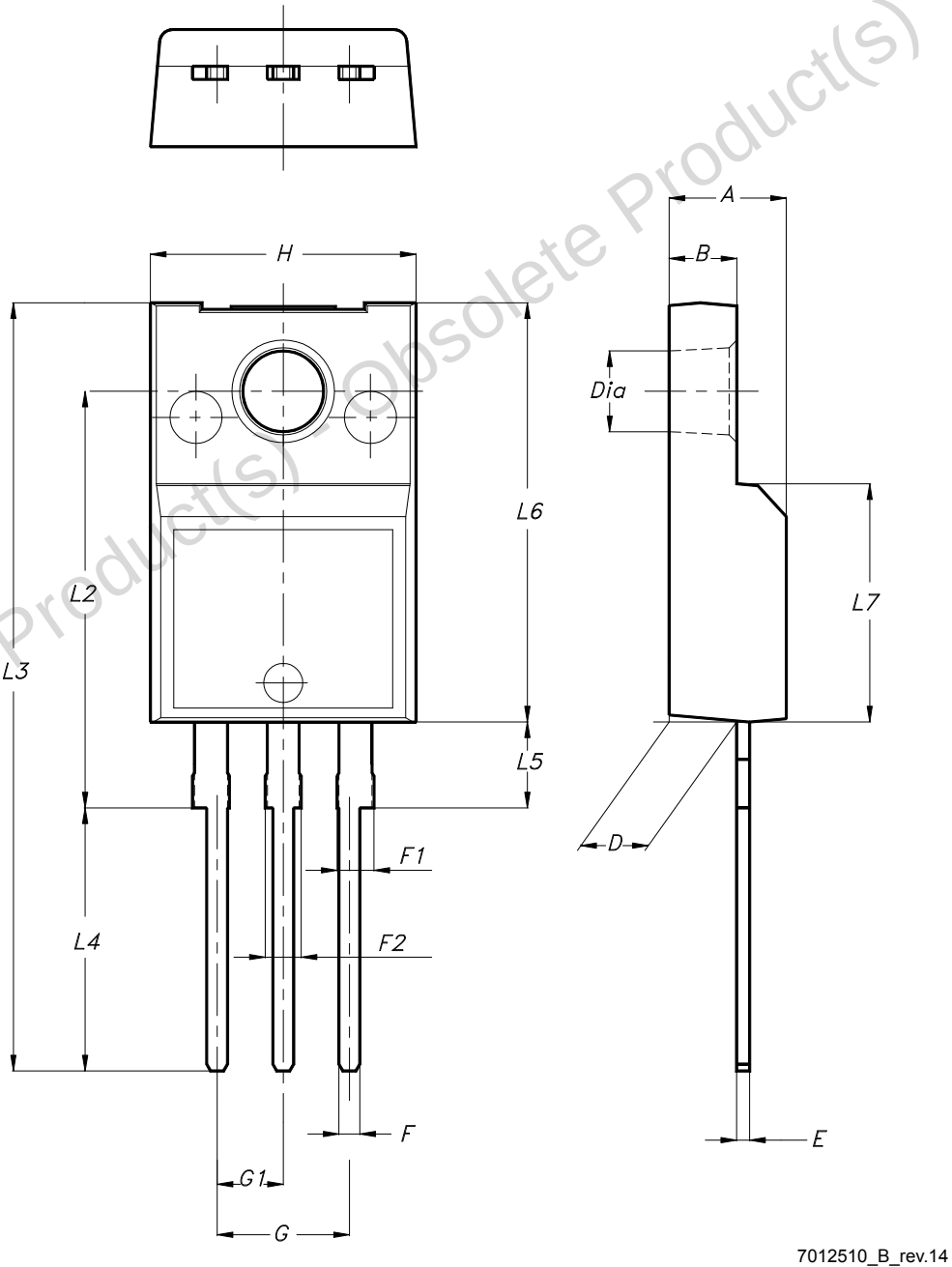


Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
25-May-2023	1	First release. The part number STP7NK40ZFP was previously inserted in the DS2855.

Contents