

STP80NS04ZB

N-CHANNEL CLAMPED 7.5mΩ - 80A TO-220 FULLY PROTECTED MESH OVERLAY™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS} R _D		I _D
STP80NS04ZB	CLAMPED	<0.008 Ω	80 A

- TYPICAL $R_{DS}(on) = 0.0075 \Omega$
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 °C MAXIMUM JUNCTION TEMPERATURE

DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout.

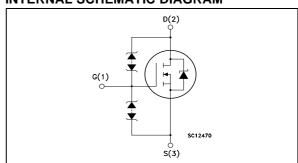
The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS, SOLENOID DRIVERS
- MOTOR CONTROL
- DC-DC CONVERTERS



INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	CLAMPED	V
V_{DG}	Drain-gate Voltage	CLAMPED	V
V _{GS}	Gate- source Voltage	CLAMPED	V
I _D	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	60	Α
I _{DG}	Drain Gate Current (continuous)	± 50	mA
I _{GS}	Gate SourceCurrent (continuous)	± 50	mA
I _{DM} (•)	Drain Current (pulsed)	320	A
P _{tot}	Total Dissipation at T _C = 25°C	200	W
	Derating Factor	1.33	W/°C
V _{ESD(G-S)}	Gate-Source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
V _{ESD(G-D)}	Gate-Drain ESD (HBM - C = 100pF, R=1.5 k Ω)	4	kV
V _{ESD(D-S)}	Drain-source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
T _{stg}	Storage Temperature	-65 to 175	°C
Tj	Max. Operating Junction Temperature	-40 to 175	°C

^(•) Pulse width limited by safe operating area.

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THERMAL DATA

Rthj-case Rthj-amb T _I		Max Max	0.75 62.5 300	°C/W °C/W °C
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AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	80	А
E _{AS}	Single Pulse Avalanche Energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 30$ V)	500	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Clamped Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$ -40 < T_J < 175 °C	33			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	$V_{DS} = 16 \text{ V}$ $T_c = 25 \text{ °C}$ $V_{DS} = 16 \text{ V}$ $T_J = 150 \text{ °C}$ $V_{DS} = 16 \text{ V}$ $T_J = 175 \text{ °C}$			10 50 100	μΑ μΑ μΑ
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 10 V T _J =175 °C V _{GS} = ± 16 V T _J =175 °C			50 150	μA μA
V _{GSS}	Gate-Source Breakdown Voltage	I _{GS} = 100 μA	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_{D} = 1 \text{ mA}$ $-40 < T_{J} < 150 ^{\circ}\text{C}$	1.7	3	4.2	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 40 A V _{GS} = 16 V I _D = 40 A		8 7.5	9 8	$m\Omega$ $m\Omega$
I _{D(on)}	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $V_{GS} = 10V$	80			А

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
9fs ^(*)	Forward Transconductance	$V_{DS}>I_{D(on)}xR_{DS(on)max}$ $I_{D}=40A$	30	50		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V$, $f = 1$ MHz, $V_{GS} = 0$		2700 1275 285	3300 1600 350	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 20 V I _D = 80 A V _{GS} = 10V		80 20 27	105	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t _{r(Voff)} t _f t _c	Off-voltage Rise Time Fall Time Cross-over Time	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$		115 80 210	150 105 280	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} (•)	Source-drain Current Source-drain Current (pulsed)					80 320	A A
V _{SD} (*)	Forward On Voltage	I _{SD} = 80 A	$V_{GS} = 0$			1.5	V
t _{rr} Q _{rr} I _{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I _{SD} = 80 A V _{DD} = 25 V (see test circuit	di/dt = $100A/\mu s$ $T_j = 150$ °C t, Figure 5)		90 0.18 4		ns μC A

^(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

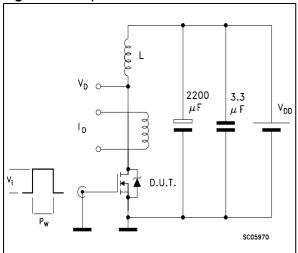


Fig. 3: Switching Times Test Circuits For Resistive Load

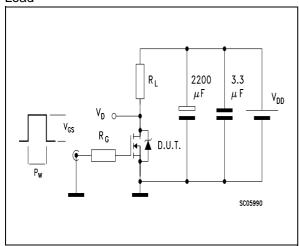


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

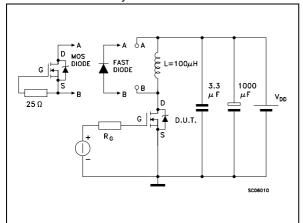


Fig. 2: Unclamped Inductive Waveform

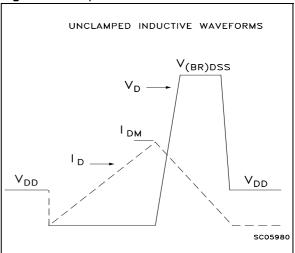
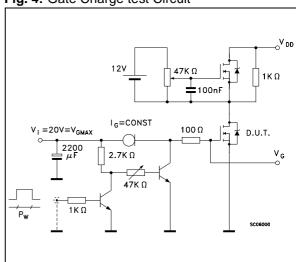
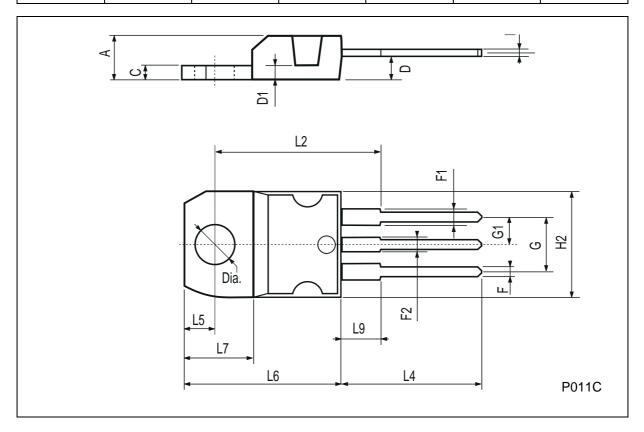


Fig. 4: Gate Charge test Circuit



TO-220 MECHANICAL DATA

DIM.		mm			inch	
DINI.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	4.40		4.60	0.173		0.181
С	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
Е	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



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