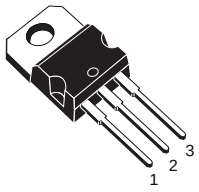
STP80NS04ZB

N-CHANNEL CLAMPED 7.5mΩ - 80A TO-220
FULLY PROTECTED MESH OVERLAY™ MOSFET

PRELIMINARY DATA

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STP80NS04ZB	CLAMPED	<0.008 Ω	80 A

- TYPICAL $R_{DS}(on)$ = 0.0075 Ω
- 100% AVALANCHE TESTED
- LOW CAPACITANCE AND GATE CHARGE
- 175 ^{o}C MAXIMUM JUNCTION TEMPERATURE



TO-220

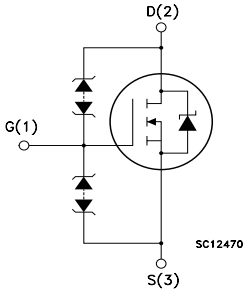
DESCRIPTION

This fully clamped Mosfet is produced by using the latest advanced Company's Mesh Overlay process which is based on a novel strip layout.
The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions such as those encountered in the automotive environment. Any other application requiring extra ruggedness is also recommended.

APPLICATIONS

- ABS, SOLENOID DRIVERS
- MOTOR CONTROL
- DC-DC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	CLAMPED	V
V_{DG}	Drain-gate Voltage	CLAMPED	V
V_{GS}	Gate- source Voltage	CLAMPED	V
I_D	Drain Current (continuous) at T_C = 25°C	80	A
I_D	Drain Current (continuous) at T_C = 100°C	60	A
I_{DG}	Drain Gate Current (continuous)	± 50	mA
I_{GS}	Gate SourceCurrent (continuous)	± 50	mA
I_{DM}(•)	Drain Current (pulsed)	320	A
P_{tot}	Total Dissipation at T_C = 25°C	200	W
	Derating Factor	1.33	W/°C
$V_{ESD(G-S)}$	Gate-Source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
$V_{ESD(G-D)}$	Gate-Drain ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
$V_{ESD(D-S)}$	Drain-source ESD (HBM - C = 100pF, R=1.5 kΩ)	4	kV
T_{stg}	Storage Temperature	-65 to 175	°C
T_j	Max. Operating Junction Temperature	-40 to 175	°C

(•) Pulse width limited by safe operating area.

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.75	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	80	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 30 V)	500	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Clamped Voltage	I_D = 1 mA, V_{GS} = 0 -40 < T_J < 175 °C	33			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = 16 V T_c=25 °C V_{DS} = 16 V T_J =150 °C V_{DS} = 16 V T_J =175 °C			10 50 100	µA µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 10 V T_J =175 °C V_{GS} = ± 16 V T_J =175 °C			50 150	µA µA
V_{GSS}	Gate-Source Breakdown Voltage	I_{GS} = 100 µA	18			V

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ I_D = 1 mA -40 < T_J < 150 °C	1.7	3	4.2	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 40 A V_{GS} = 16 V I_D = 40 A		8 7.5	9 8	mΩ mΩ
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$, V_{GS} = 10V	80			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	$V_{DS} > I_{D(on)} x R_{DS(on)max}$ I_D=40A	30	50		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		2700 1275 285	3300 1600 350	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 20 V I_D= 80 A V_{GS}= 10V		80 20 27	105	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 30 V I_D = 80 A R_G = 4.7Ω, V_{GS} = 10 V (Inductive Load, Figure 5)		115 80 210	150 105 280	ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				80 320	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 80 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 80 A di/dt = 100A/µs V_{DD} = 25 V T_j = 150°C (see test circuit, Figure 5)		90 0.18 4		ns µC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

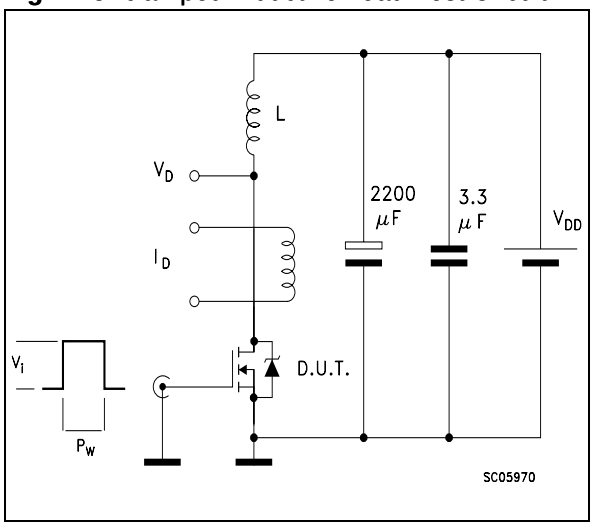


Fig. 2: Unclamped Inductive Waveform

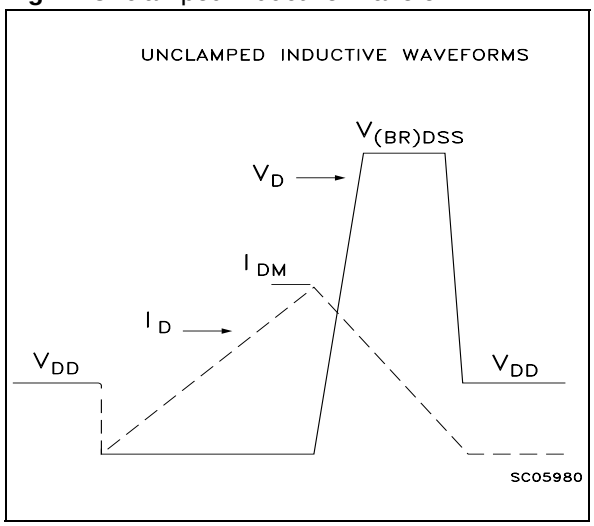


Fig. 3: Switching Times Test Circuits For Resistive Load

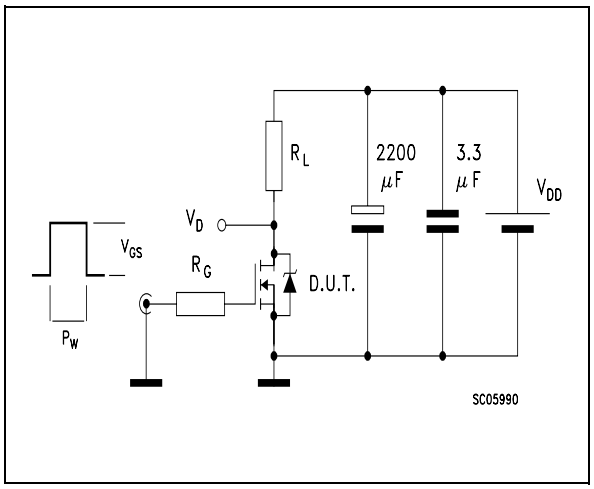


Fig. 4: Gate Charge test Circuit

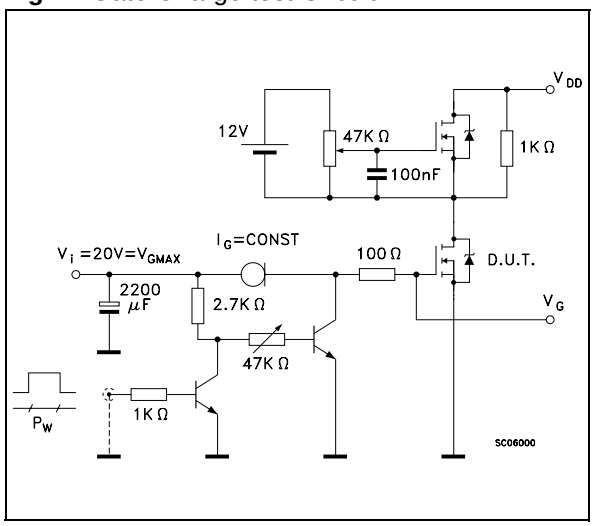
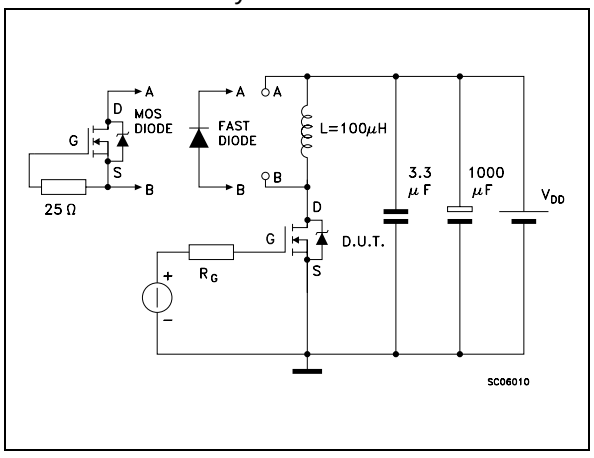


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151