



STB85N15F4 STP85N15F4

N-channel 150 V, 0.015 Ω , 85 A TO-220, D²PAK
STripFET™ DeepGATE™ Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STB85N15F4	150 V	< 0.019 Ω	85 A
STP85N15F4	150 V	< 0.019 Ω	85 A

- Exceptional dv/dt capability
- Extremely low on-resistance R_{DS(on)}
- 100% avalanche tested

Application

- Switching applications

Description

This Power MOSFET is among the latest developments that use an advanced technology (STripFET™ DeepGATE™ technology), which has been especially tailored to minimize on-state resistance, provide superior switching performance and withstand high energy pulse in avalanche and commutation mode. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

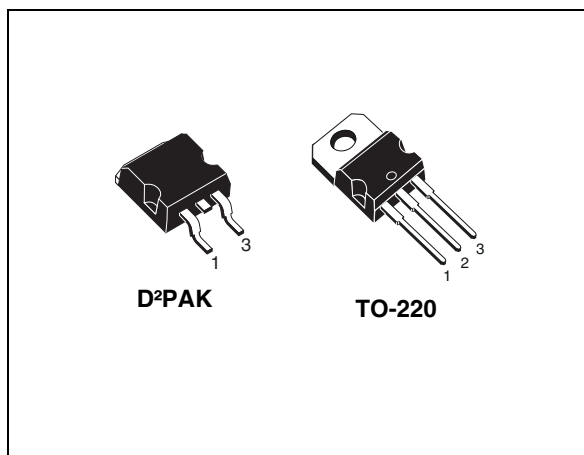
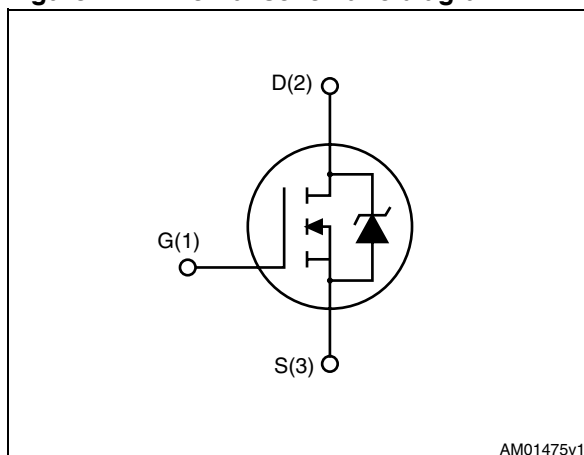


Figure 1. Internal schematic diagram



AM01475v1

Table 1. Device summary

Order codes	Marking	Package	Packaging
STB85N15F4	85N15F4	D ² PAK	Tape and reel
STP85N15F4	85N15F4	TO-220	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	150	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	85	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	340	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
	Derating factor	2.0	W/ $^{\circ}\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	TBD	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	TBD	mJ
T_{stg}	Storage temperature	- 55 to 175	$^{\circ}\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 50\text{ A}$, $di/dt \leq 600\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

3. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = 50\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	D ² PAK	
$R_{thj-case}$	Thermal resistance junction-case max	0.5		$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	--	35 ⁽¹⁾	$^{\circ}\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	62.5	--	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^{\circ}\text{C}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	150			V
I_{DSS}	Zero gate voltage Drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$		0.015	0.019	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		8320		pF
C_{oss}	Output capacitance			600		pF
C_{rss}	Reverse transfer capacitance			230		pF
Q_g	Total gate charge	$V_{DD} = 80\text{ V}$, $I_D = 85\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 3)		140		nC
Q_{gs}	Gate-source charge			TBD		nC
Q_{gd}	Gate-drain charge			TBD		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 75\text{ V}$, $I_D = 40\text{ A}$ $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD TBD		ns ns
$t_{d(off)}$ t_f	Turn-off-delay time Fall time	$V_{DD} = 75\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD TBD		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current				85	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				340	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 85\text{ A}$, $V_{GS} = 0$			TBD	V
t_{rr}	Reverse recovery time	$I_{SD} = 85\text{ A}$, $V_{DD} = 25\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^{\circ}\text{C}$ <i>(see Figure 4)</i>		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

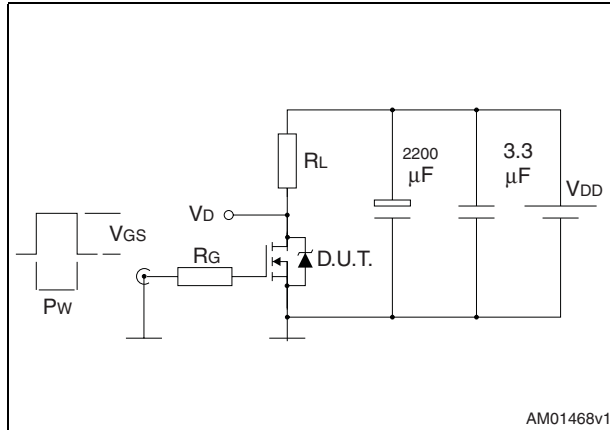


Figure 3. Gate charge test circuit

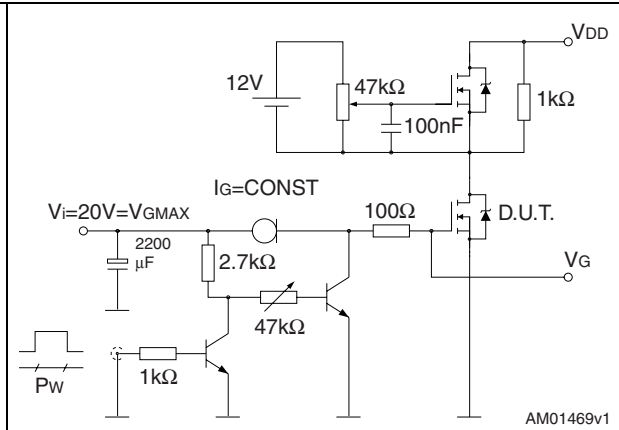


Figure 4. Test circuit for inductive load switching and diode recovery times

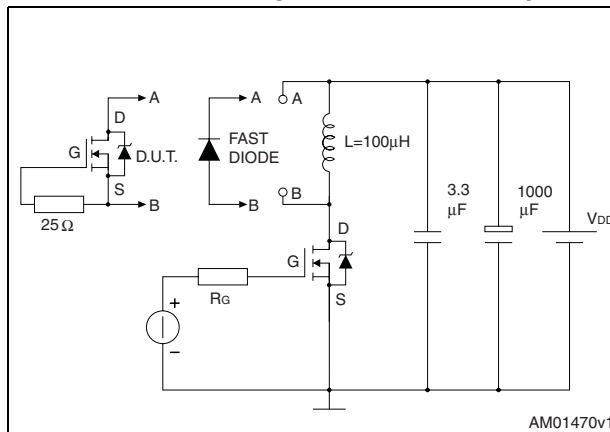


Figure 5. Unclamped inductive load test circuit

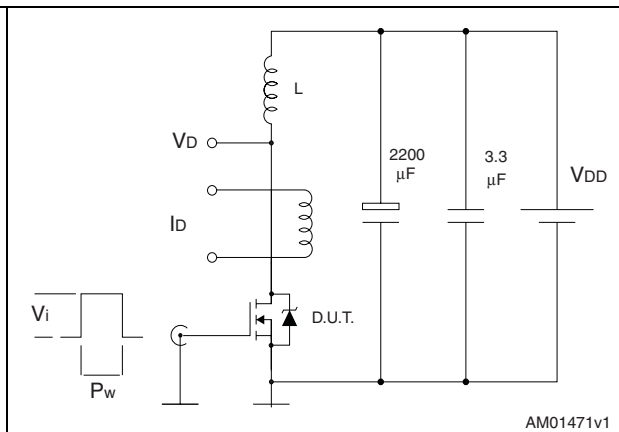


Figure 6. Unclamped inductive waveform

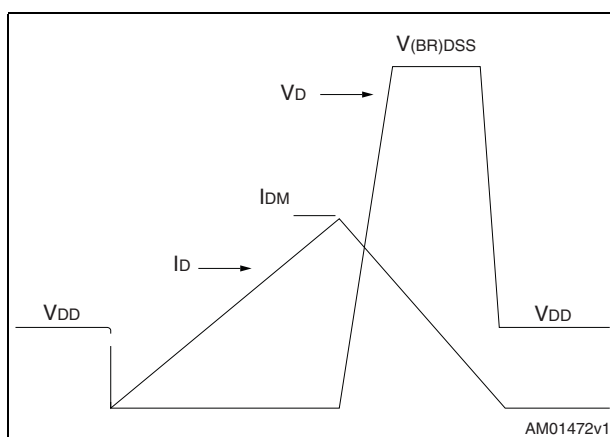
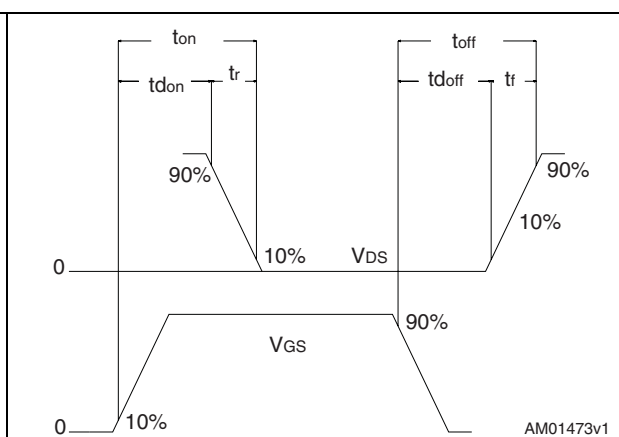


Figure 7. Switching time waveform

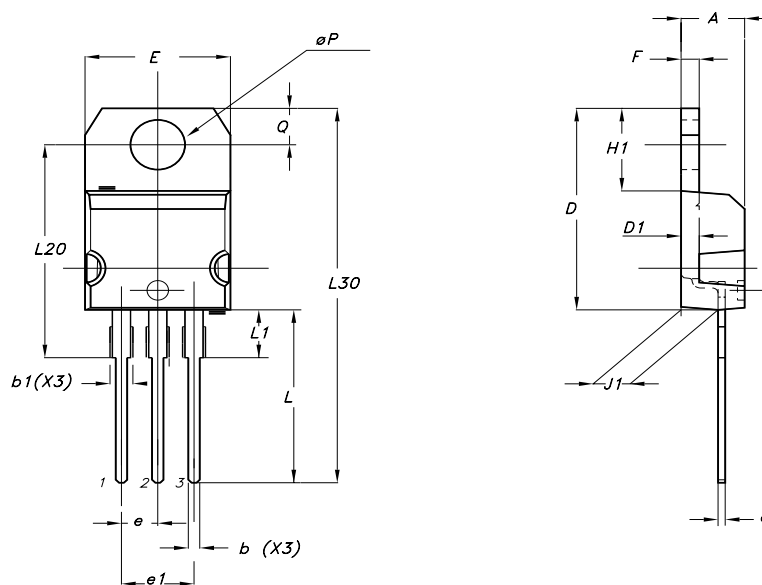


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

TO-220 mechanical data

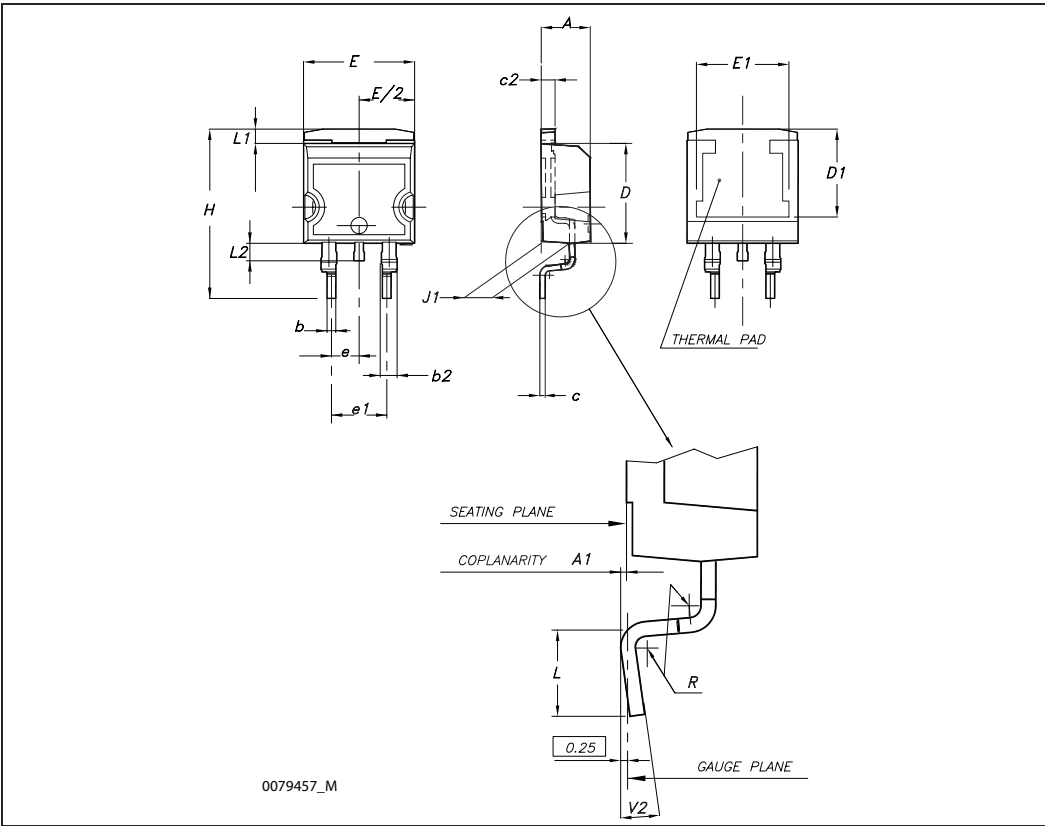
Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.14		1.70	0.044		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.6		0.62
D1		1.27			0.050	
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.051
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
ØP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



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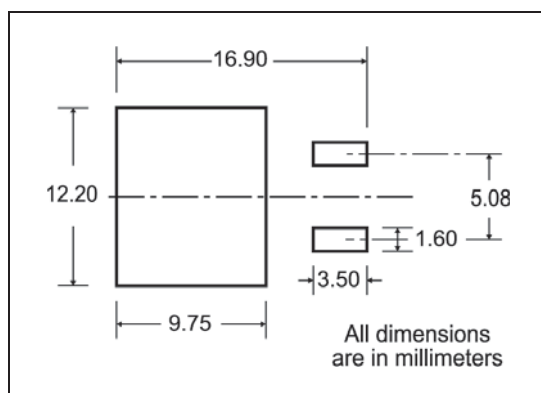
D²PAK (TO-263) mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	4.40		4.60	0.173		0.181
A1	0.03		0.23	0.001		0.009
b	0.70		0.93	0.027		0.037
b2	1.14		1.70	0.045		0.067
c	0.45		0.60	0.017		0.024
c2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1	7.50			0.295		
E	10		10.40	0.394		0.409
E1	8.50			0.334		
e		2.54			0.1	
e1	4.88		5.28	0.192		0.208
H	15		15.85	0.590		0.624
J1	2.49		2.69	0.099		0.106
L	2.29		2.79	0.090		0.110
L1	1.27		1.40	0.05		0.055
L2	1.30		1.75	0.051		0.069
R		0.4			0.016	
V2	0°		8°	0°		8°

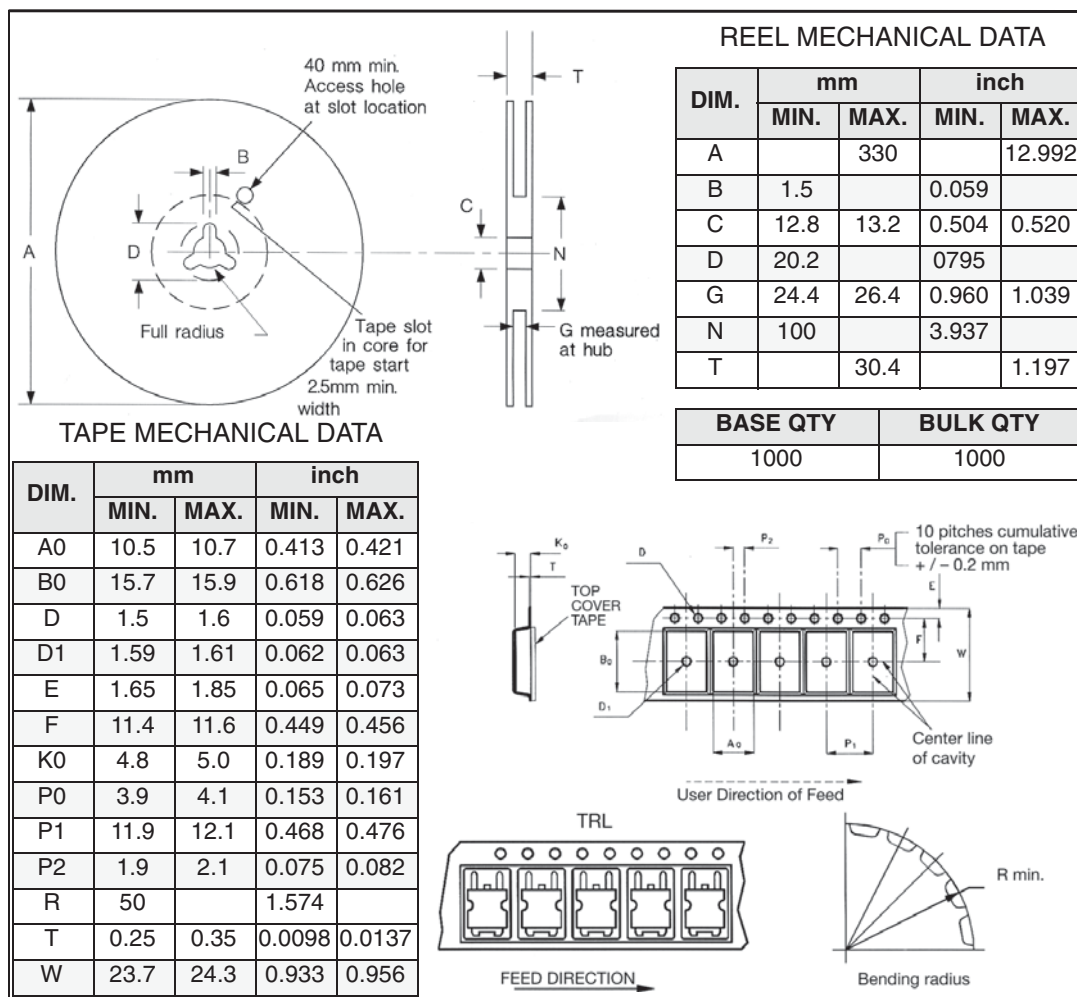


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
12-Jan-2009	1	First release

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