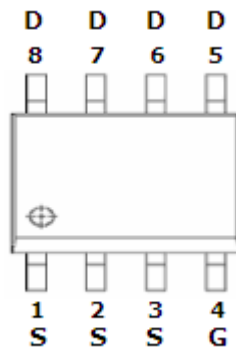


**DESCRIPTION**

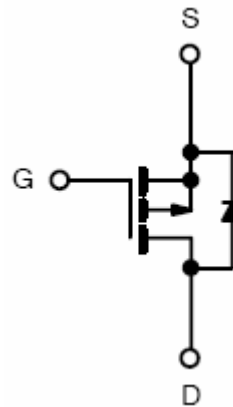
STP9437 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management, and other battery powered circuits where high-side switching.

**PIN CONFIGURATION  
SOP-8**

**FEATURE**

- -30V/-5.7A,  $R_{DS(ON)} = 45m\Omega$  (Typ.) @ $V_{GS} = -10V$
- -30V/-5.0A,  $R_{DS(ON)} = 50m\Omega$  @ $V_{GS} = -4.5V$
- -30V/-4.4A,  $R_{DS(ON)} = 65m\Omega$  @ $V_{GS} = -2.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING  
SOP-8**


**Y: Year Code**  
**A: Date Code**





**STP9437** 

P Channel Enhancement Mode MOSFET

- 5.7A

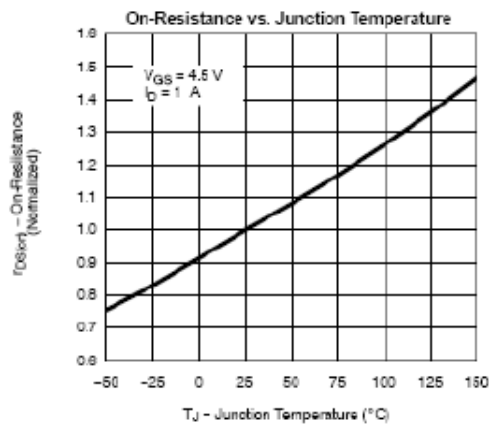
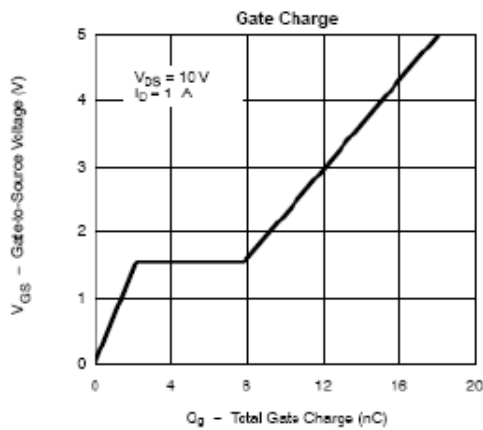
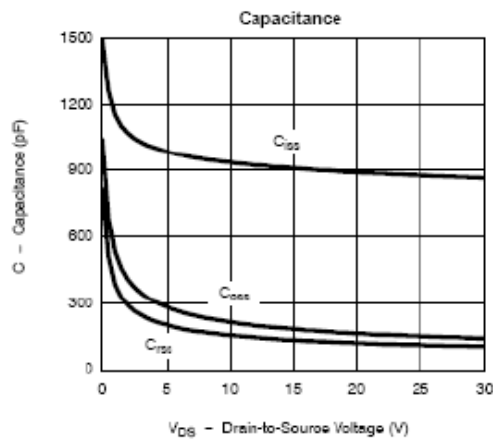
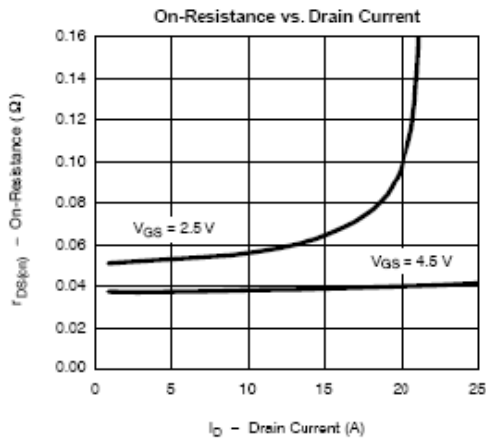
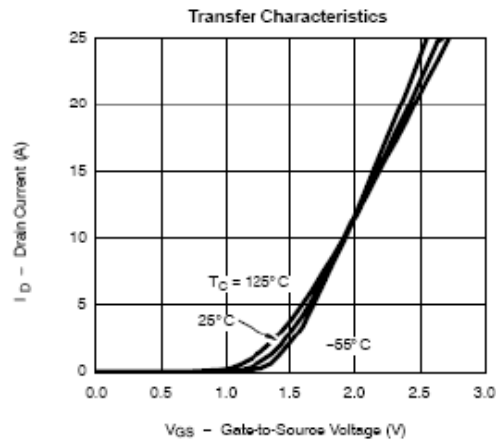
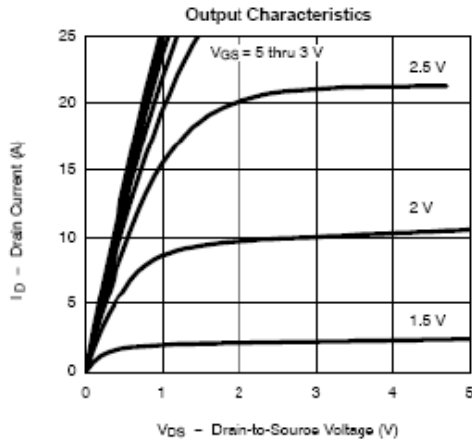
**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	-30	V
Gate-Source Voltage	VGSS	±12	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C -6.8	A
		TA=70°C -4.6	
Pulsed Drain Current	IDM	-30	A
Continuous Source Current (Diode Conduction)	IS	-2.3	A
Power Dissipation	PD	TA=25°C 2.8	W
		TA=70°C 1.8	
Operation Junction Temperature	TJ	-55/150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	70	°C/W

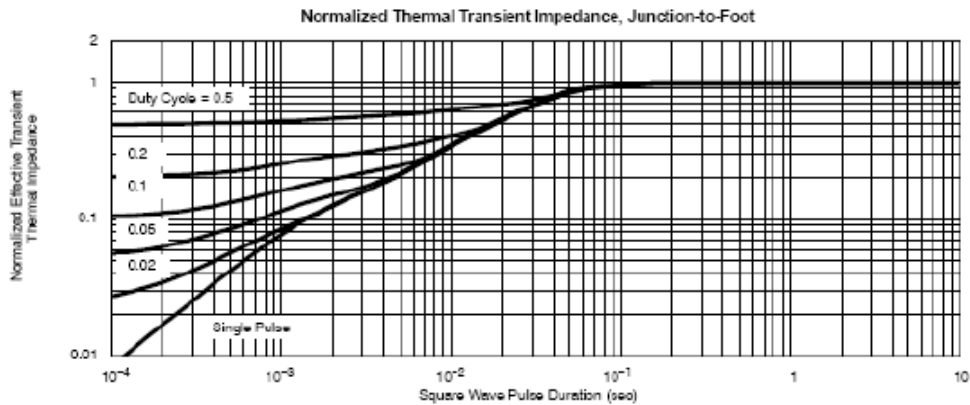
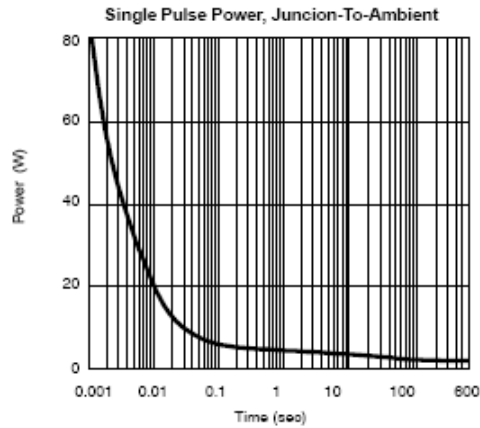
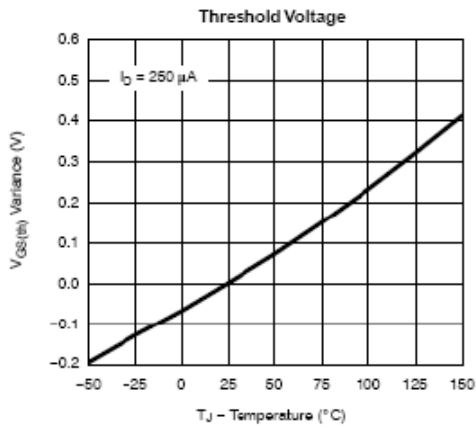
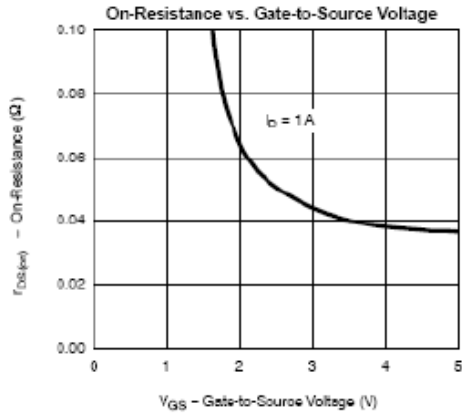
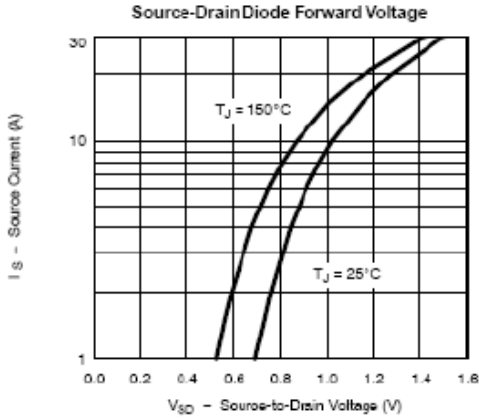
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

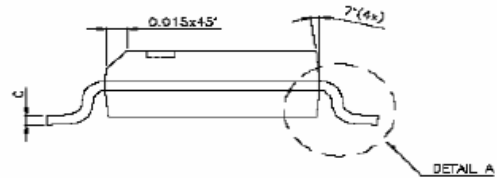
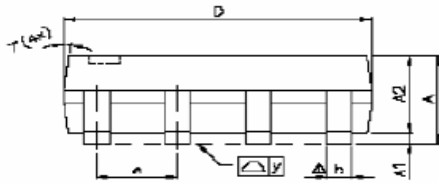
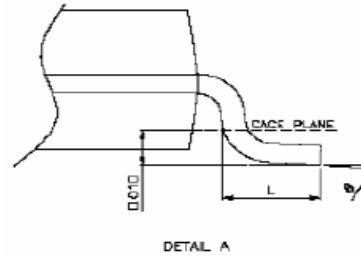
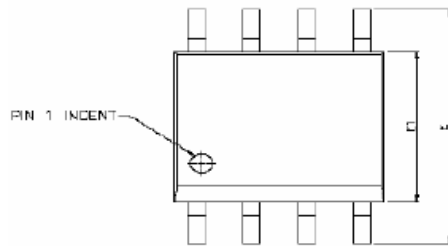
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4		-1.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=85^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-5.7A$		0.035	0.045	$\Omega$
		$V_{GS}=-4.5V, I_D=-5.0A$		0.040	0.050	
		$V_{GS}=-2.5V, I_D=-4.4A$		0.050	0.065	
Forward Transconductance	$g_{fs}$	$V_{DS}=-15V, I_D=-5.7V$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=-2.3A, V_{GS}=0V$		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-3.5A$		16	24	nC
Gate-Source Charge	$Q_{gs}$			2.3		
Gate-Drain Charge	$Q_{gd}$			4.5		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		680		pF
Output Capacitance	$C_{oss}$			120		
Reverse Transfer Capacitance	$C_{rss}$			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1A, V_{GEN}=-10V$ $R_G=6\Omega$		14	25	nS
	$t_r$			16	26	
Turn-Off Time	$t_{d(off)}$			42	70	
	$t_f$			30	50	

**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS**



**PACKAGE OUTLINE SOP-8P**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\phi$	0°	—	8°	0°	—	8°