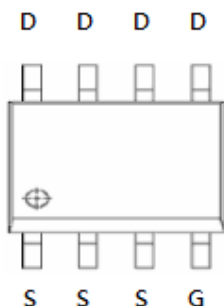


suSCRIPTION

STP9527 is the P-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook power management and ther battery powered circuits where high-side witching.

PIN CONFIGURATION SOP-8



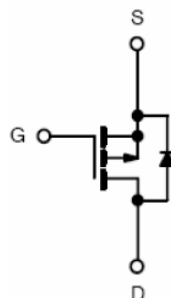
FEATURE

- -40V/-10.0A, $R_{DS(ON)} = 32m\Omega$ (Typ.)
@ $V_{GS} = -10V$
- -40V/-8.0A, $R_{DS(ON)} = 38m\Omega$
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING SOP-8



Y : Year Code A : Process code



ORDERING INFORMATION

Part Number	Package	Part Marking
STP9527	SOP-8	STP9527

※ Process Code : A ~ Z ; a ~ z



STP9527 

P Channel Enhancement Mode MOSFET

-10.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-40	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	T _A =25°C T _A =70°C	I _D	-10.0 -8.0	A
Pulsed Drain Current		I _{DM}	-30	A
Continuous Source Current (Diode Conduction)		I _S	-2.3	A
Power Dissipation	T _A =25°C T _A =70°C	P _D	2.8 1.8	W
Operation Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	70	°C/W



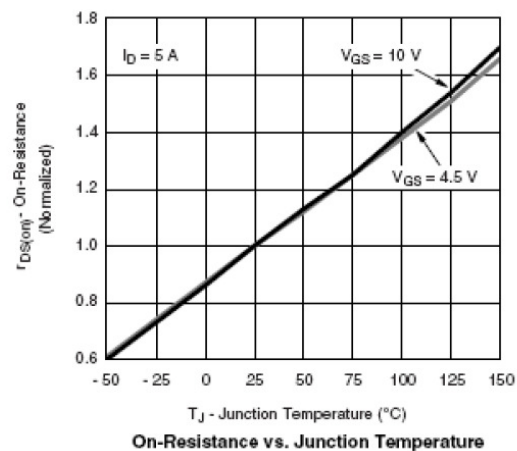
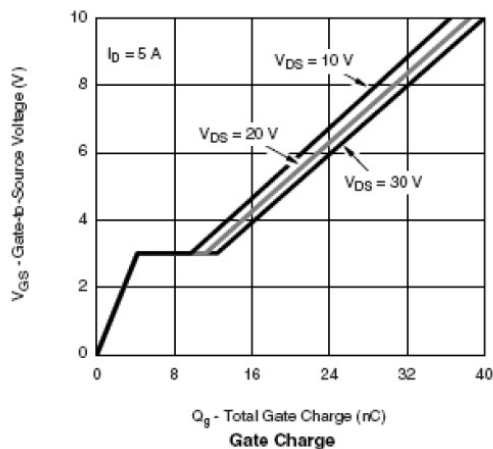
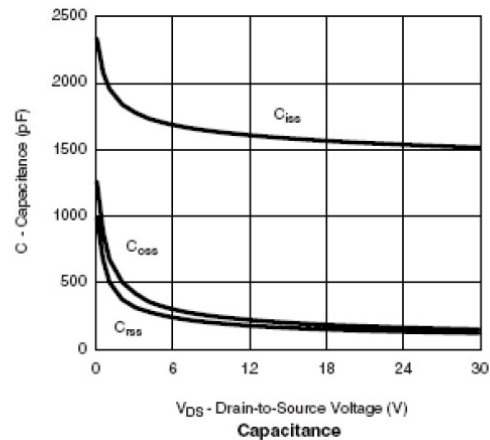
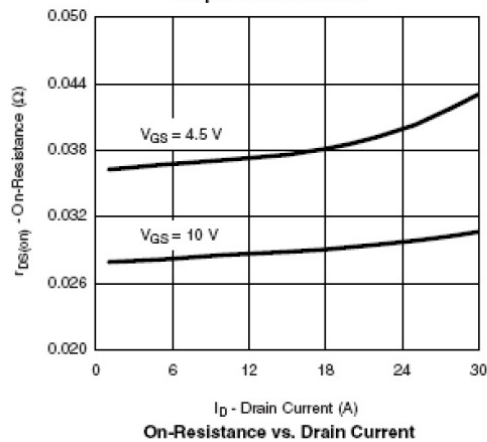
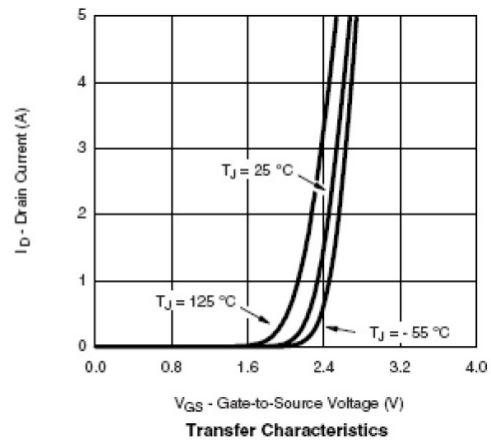
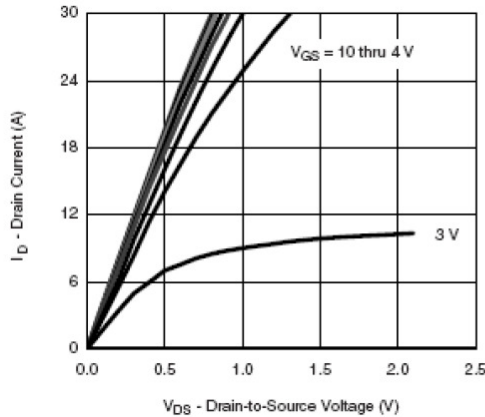
STP9527 

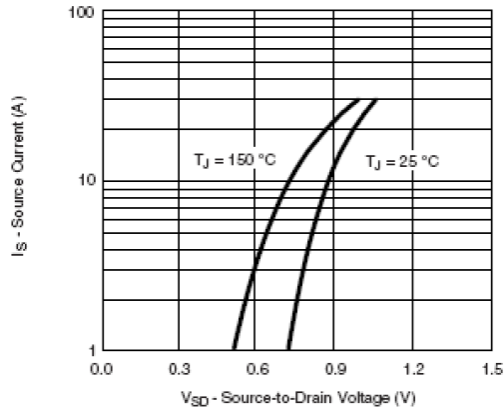
P Channel Enhancement Mode MOSFET

-10.0A

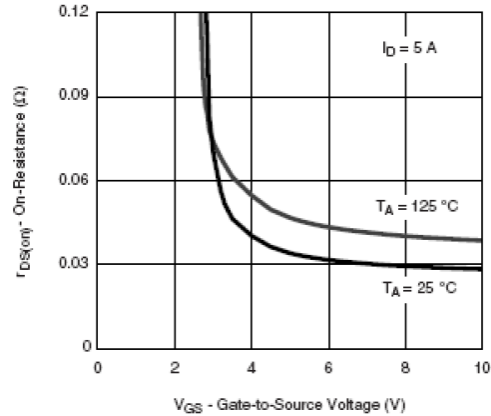
ELECTRICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V,I _D =-250uA	-40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =-250 uA	-0.8		-2.5	V
Gate Leakage Current	I _{GSS}	V _{DS} =0V,V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-36V,V _{GS} =0V			-1	uA
		V _{DS} =-36V,V _{GS} =0V T _J =85°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} =-5V,V _{GS} =4.5	-10			A
Drain-source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-10A V _{GS} =-4.5V, I _D =-8A		0.032 0.038	0.040 0.050	Ω
Forward Tran Conductance	g _{fs}	V _{DS} =-15V,I _D =-5.7A		13		S
Diode Forward Voltage	V _{SD}	I _S =-2.3A,V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-20V,V _{GS} =-4.5 I _D ≡-5.0A		13	20	nC
Gate-Source Charge	Q _{gs}			4.5		
Gate-Drain Charge	Q _{gd}			6.5		
Input Capacitance	C _{iss}	V _{DS} =-20V,V _{GS} =0V f=1MHz		1100		pF
Output Capacitance	C _{oss}			145		
Reverse TransferCapacitance	C _{rss}			115		
Turn-On Time	t _{d(on)} tr	V _{DD} =20V,R _L =4Ω I _D =-5.0A,V _{GEN} =-4.5 R _G =1Ω		40	80	nS
				55	100	
Turn-Off Time	t _{d(off)} tf			30	60	
				12	20	

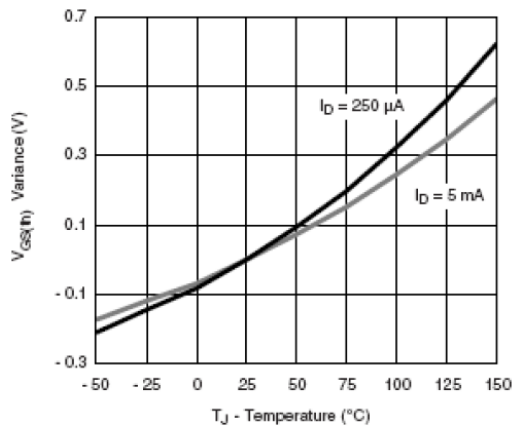
TYPICAL CHARACTERISTICS


TYPICAL CHARACTERISTICS


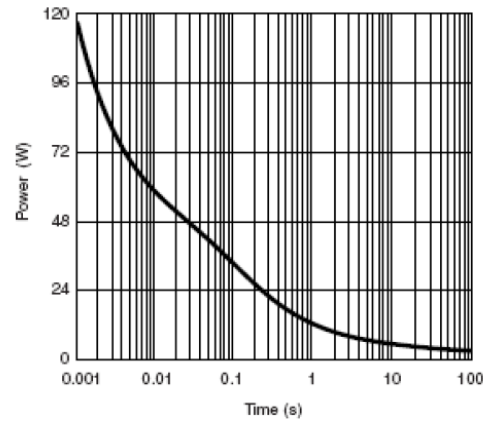
Source-Drain Diode Forward Voltage



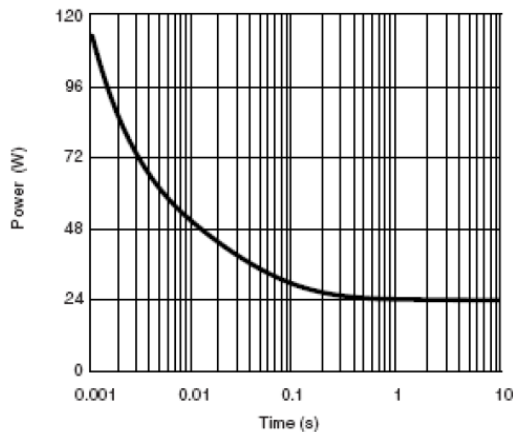
On-Resistance vs. Gate-to-Source Voltage



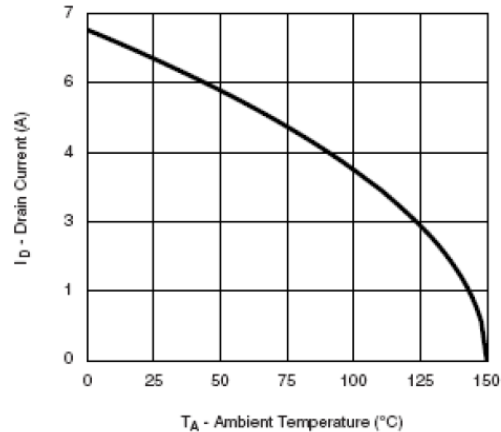
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Single Pulse Power, Junction-to-Case



Current Derating*, Junction-to-Ambient

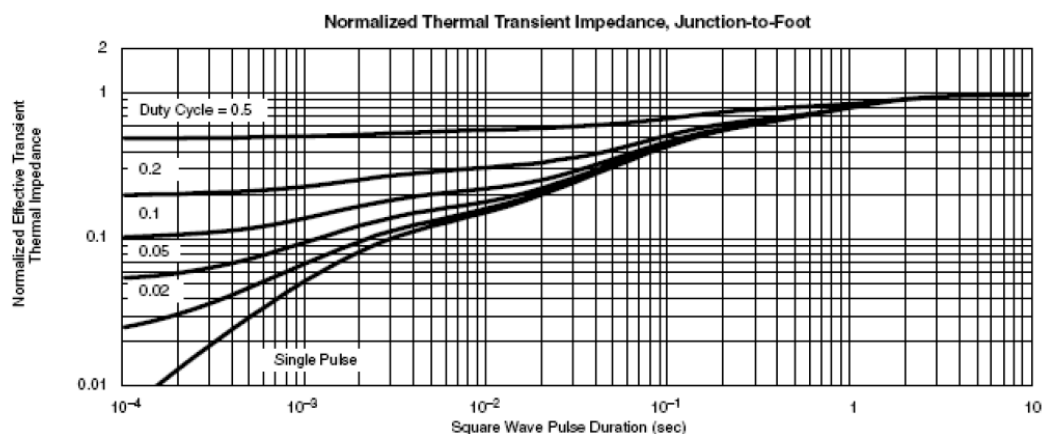
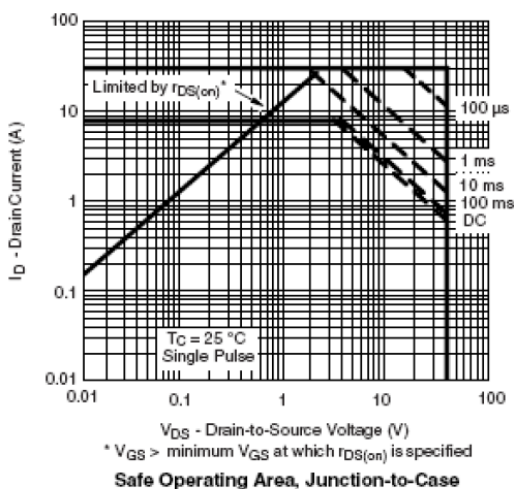
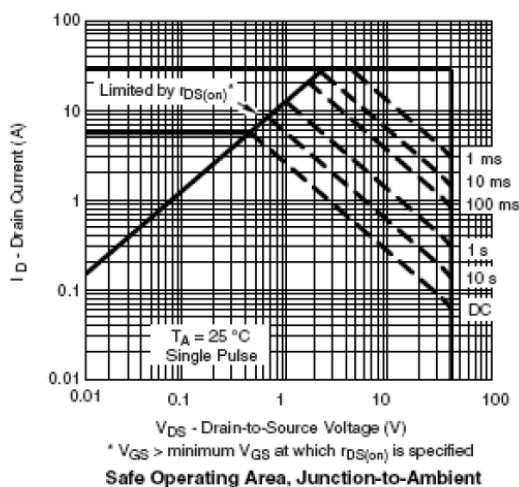


STP9527 

P Channel Enhancement Mode MOSFET

-10.0A

TYPICAL CHARACTERISTICS



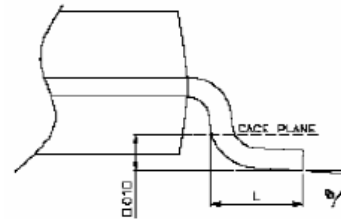
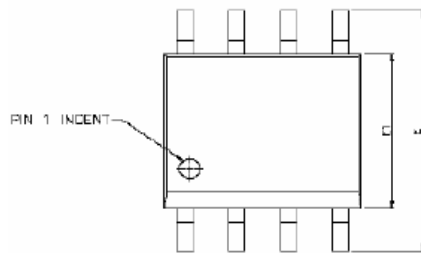


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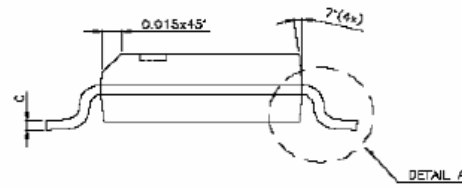
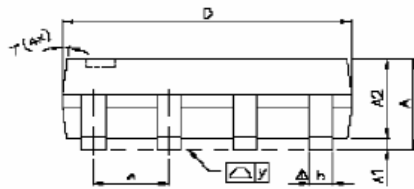
P Channel Enhancement Mode MOSFET

-10.0A

SOP-8 PACKAGE OUTLINE



DETAIL A



DETAIL A

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
 y	—	—	0.076	—	—	0.003
⌀	0°	—	8°	0°	—	8°

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