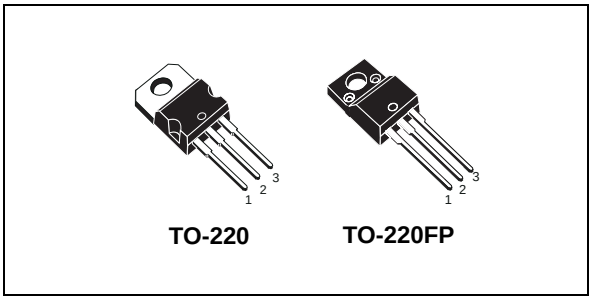
STF9NK60ZD, STP9NK60ZD

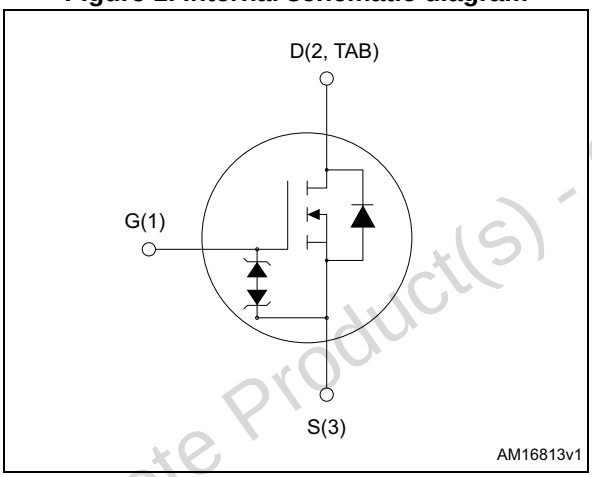
N-channel 600 V - 0.85 Ω - 7 A - TO-220FP, TO-220 SuperFREDMesh™ Power MOSFET

Datasheet - obsolete product



TO-220 **TO-220FP**

Figure 1. Internal schematic diagram



Features

Type	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF9NK60ZD	600 V	< 0.95 Ω	7 A	30 W
STP9NK60ZD	600 V	< 0.95 Ω	7 A	125 W

- Very high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Low intrinsic capacitances
- Fast internal recovery diode

Application

- Switching applications

Description

The SuperFREDMesh™ series associates all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

Table 1. Device summary

Order code	Marking	Package	Packaging
STF9NK60ZD	F9NK60ZD	TO-220FP	Tube
STP9NK60ZD	P9NK60ZD	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
V_{DS}	Drain-source voltage	600		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at T_C = 25 °C	7	7(1)	A
I_D	Drain current (continuous) at T_C = 100 °C	4.3	4.3(1)	A
I_{DM}(2)	Drain current (pulsed)	28	28(1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	125	30	W
	Derating factor	1	0.24	W/°C
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100 pF, R=1.5 kΩ)	4000		V
dv/dt (3)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)		2500	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 7$ A, di/dt $\leq$ 500 A/µs, $V_{DD} = 80\%V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$R_{thj\text{-}pcb}$	Thermal resistance junction-pcb max. (when mounted on minimum footprint)	30		°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case max.	1	4.16	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max.	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Max. value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max.)	7	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	235	mJ

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max. rating V_{DS} = max. rating, T_C = 125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.5 A		0.85	0.95	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 3.5 A	-	5.3		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1110 135 30		pF pF pF
$C_{oss\ eq}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	72		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 7 A, V_{GS} = 10 V *(see Figure 17)*	-	41 8.7 21	53	nC nC nC

1. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.
2. $C_{oss\ eq}$. is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 300 V, I_D = 3.5 A R_G= 4.7 Ω, V_{GS} = 10 V *Figure 16*	-	11.4 13.6 23.1 15	-	ns ns ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-overtime	V_{DD} = 480 V, I_D = 7 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 16*	-	11 8 20	-	ns ns ns

Table 8. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)		-		7 28	A A
V_{SD}(2)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100 A/µs V_{DD} = 30 V *Figure 21*	-	130 550 8.4		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 7 A, di/dt = 100 A/µs V_{DD} = 30 V, T_j = 150 °C *Figure 21*	-	176 880 10		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}(1)	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

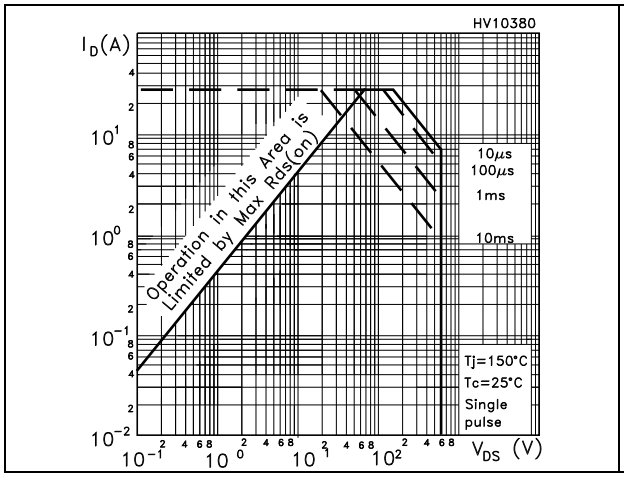


Figure 3. Thermal impedance for TO-220

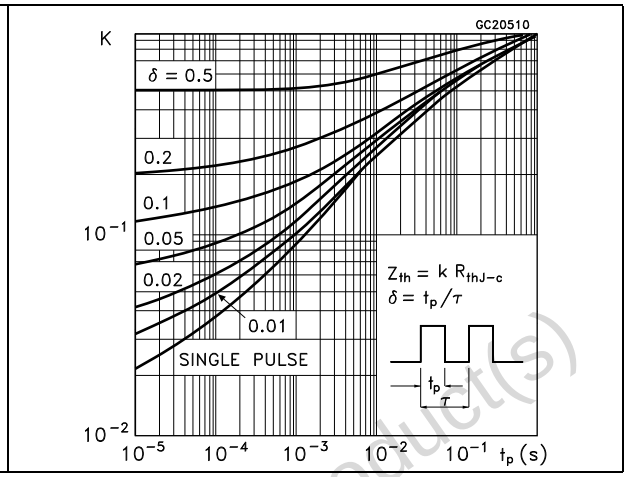


Figure 4. Safe operating area for TO-220FP

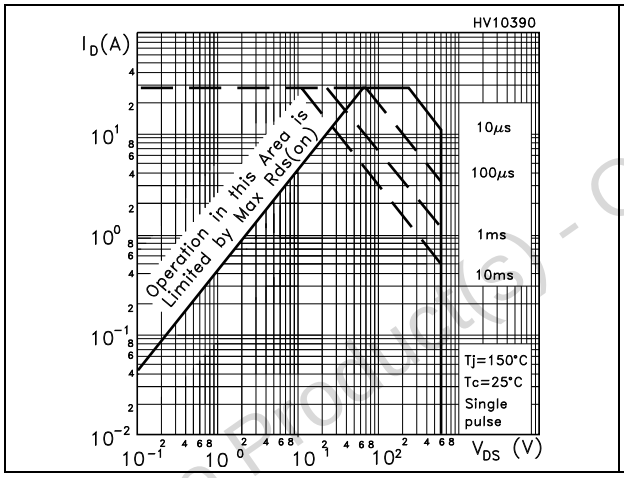


Figure 5. Thermal impedance for TO-220FP

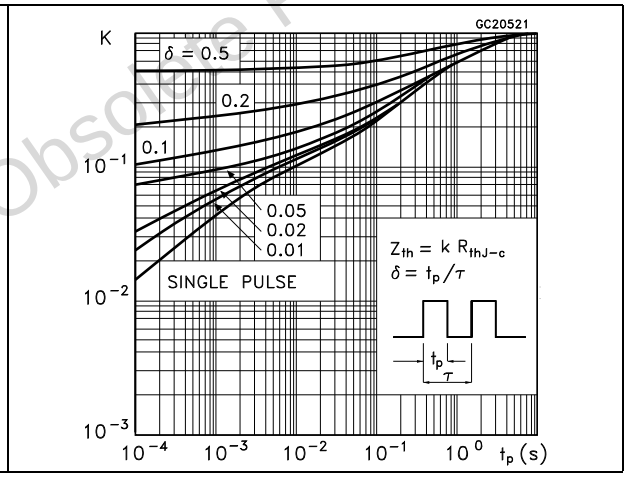


Figure 6. Output characteristics

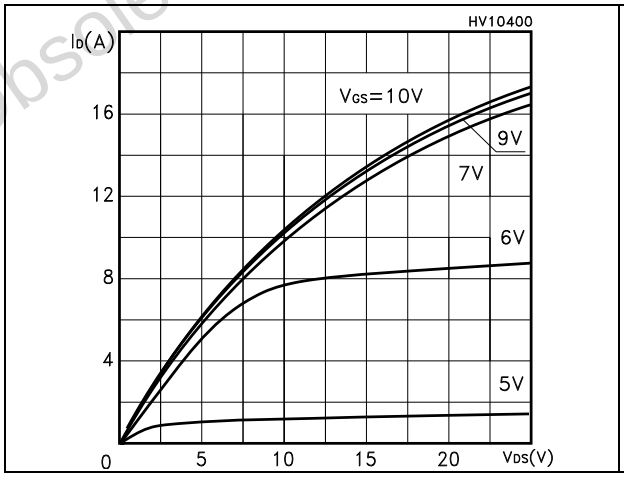


Figure 7. Transfer characteristics

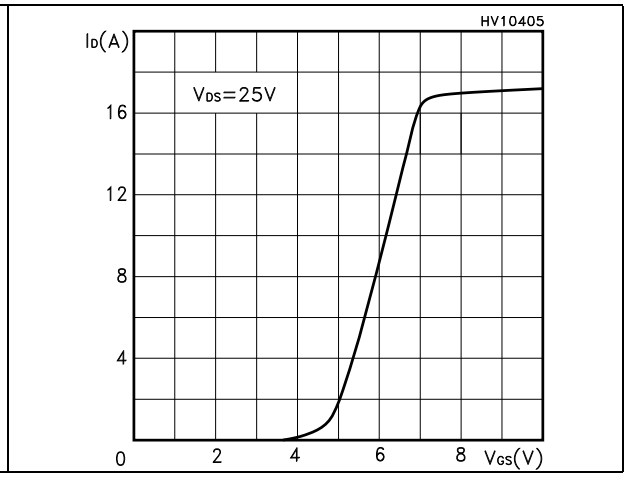


Figure 8. Normalized B_{VDSS} vs temperature

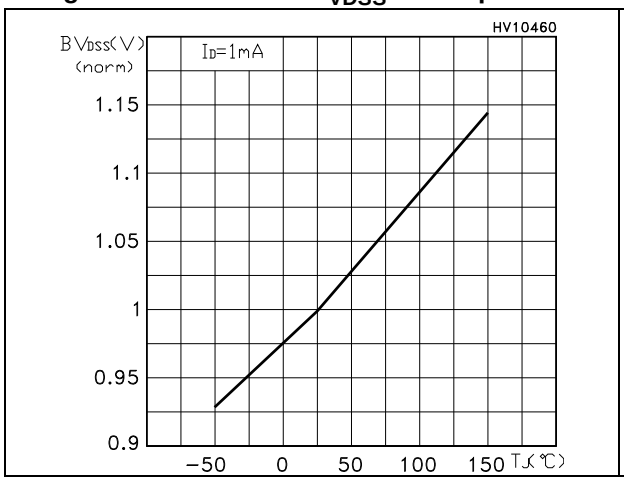


Figure 9. Static drain-source on-resistance

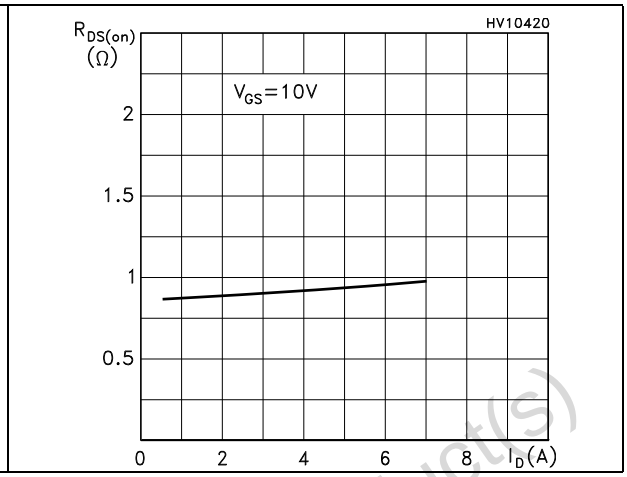


Figure 10. Gate charge vs gate-source voltage

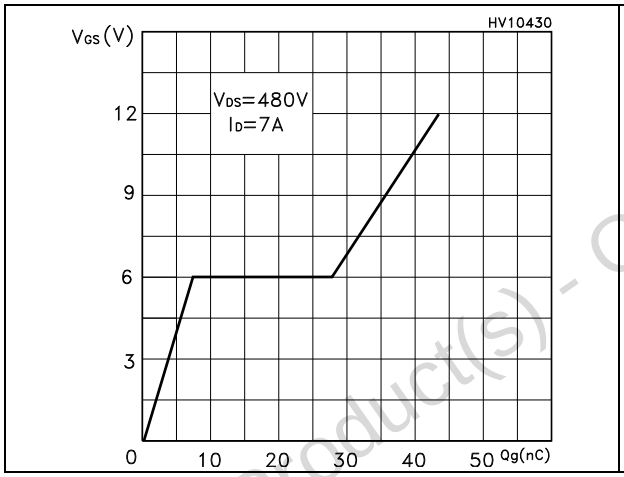


Figure 11. Capacitance variations

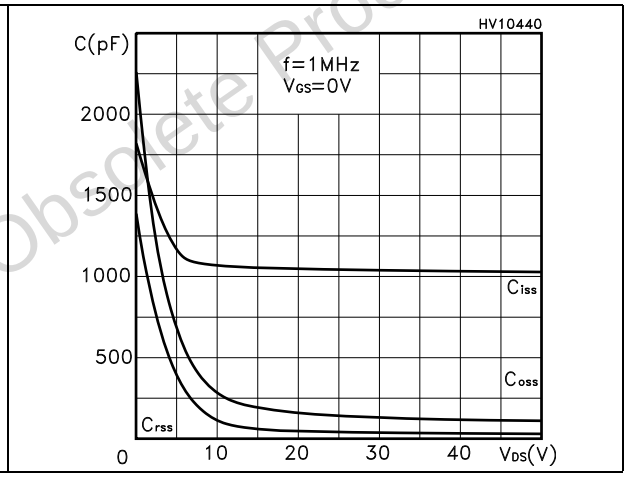


Figure 12. Normalized gate threshold voltage vs temperature

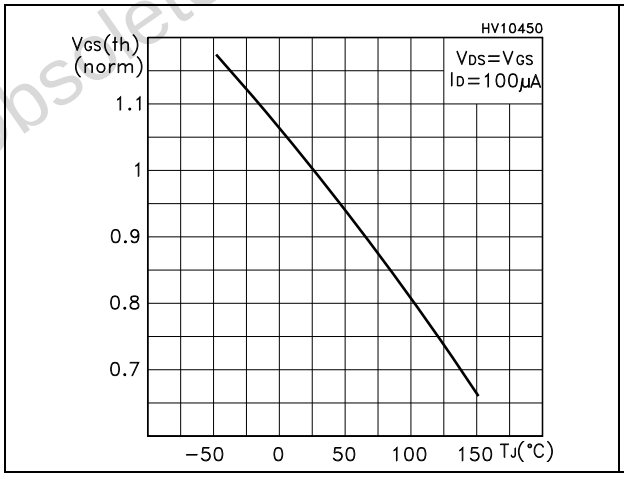


Figure 13. Normalized on-resistance vs temperature

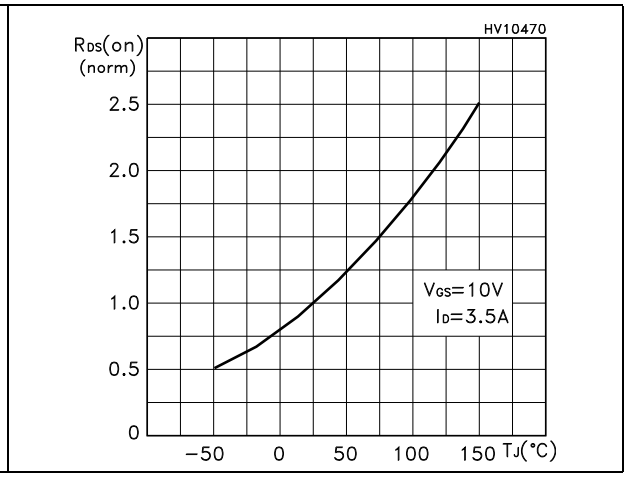


Figure 14. Source-drain diode forward characteristics

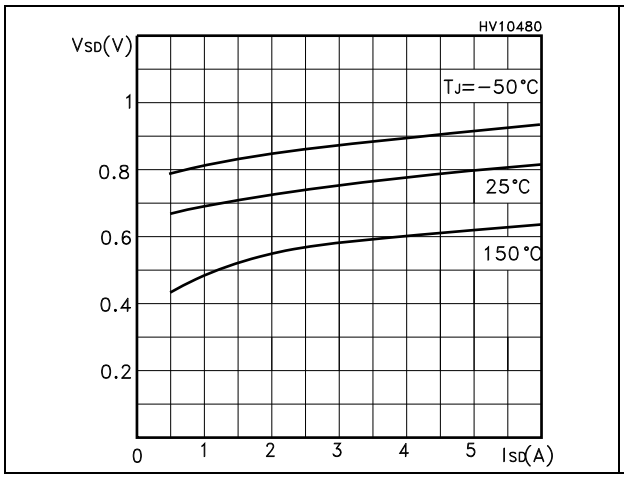
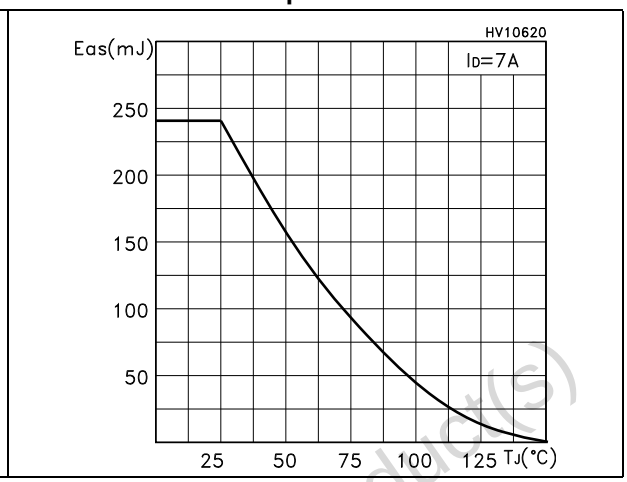


Figure 15. Maximum avalanche energy vs temperature



3 Test circuits

Figure 16. Switching time test circuit for resistive load

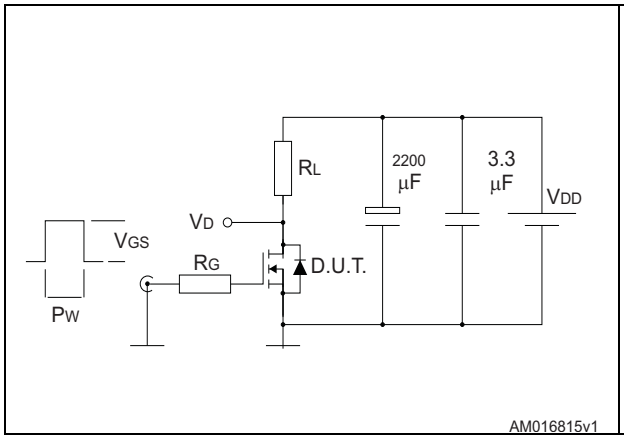


Figure 17. Gate charge test circuit

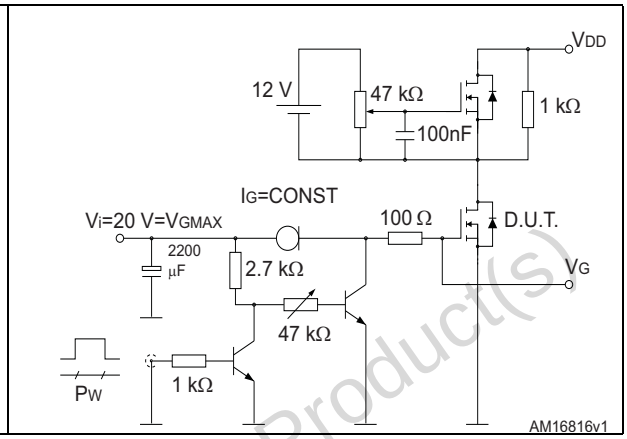


Figure 18. Test circuit for inductive load switching and diode recovery times

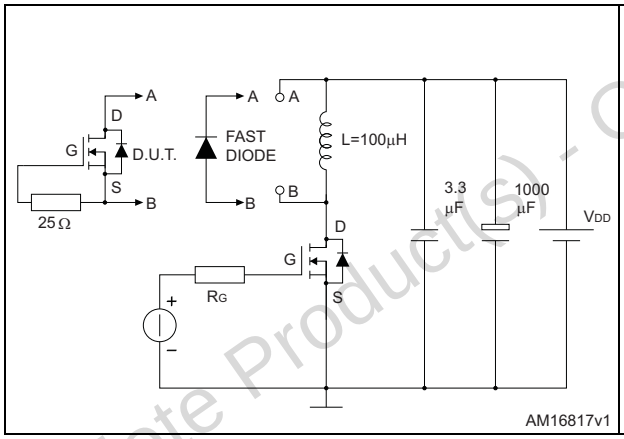


Figure 19. Unclamped inductive load test circuit

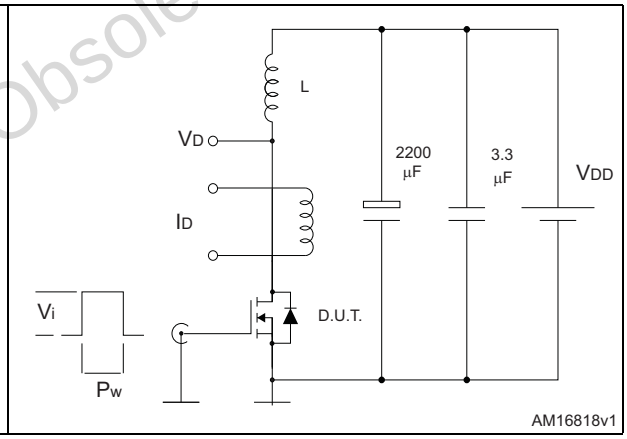


Figure 20. Unclamped inductive waveform

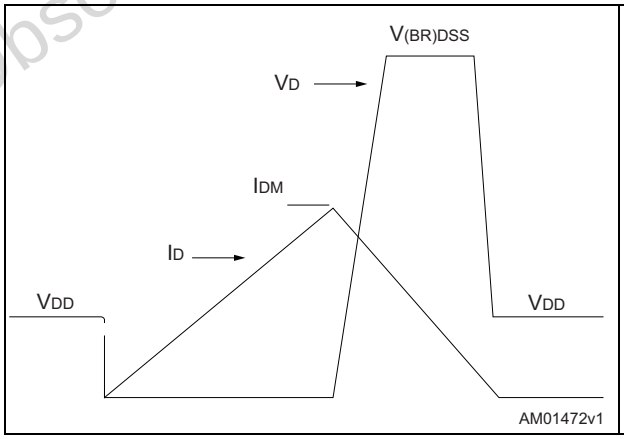
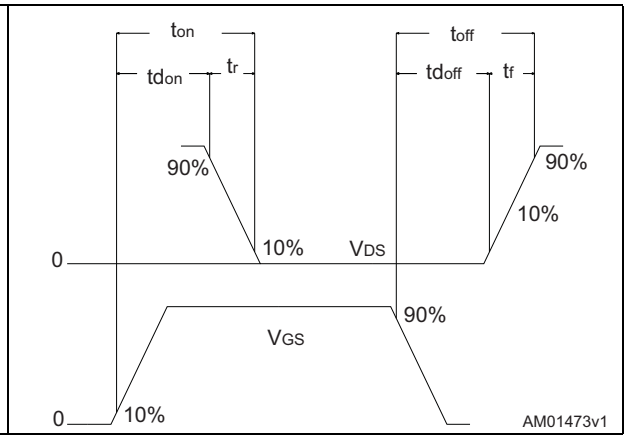


Figure 21. Switching time waveform



4 Package mechanical data

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Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 22. TO-220 drawing

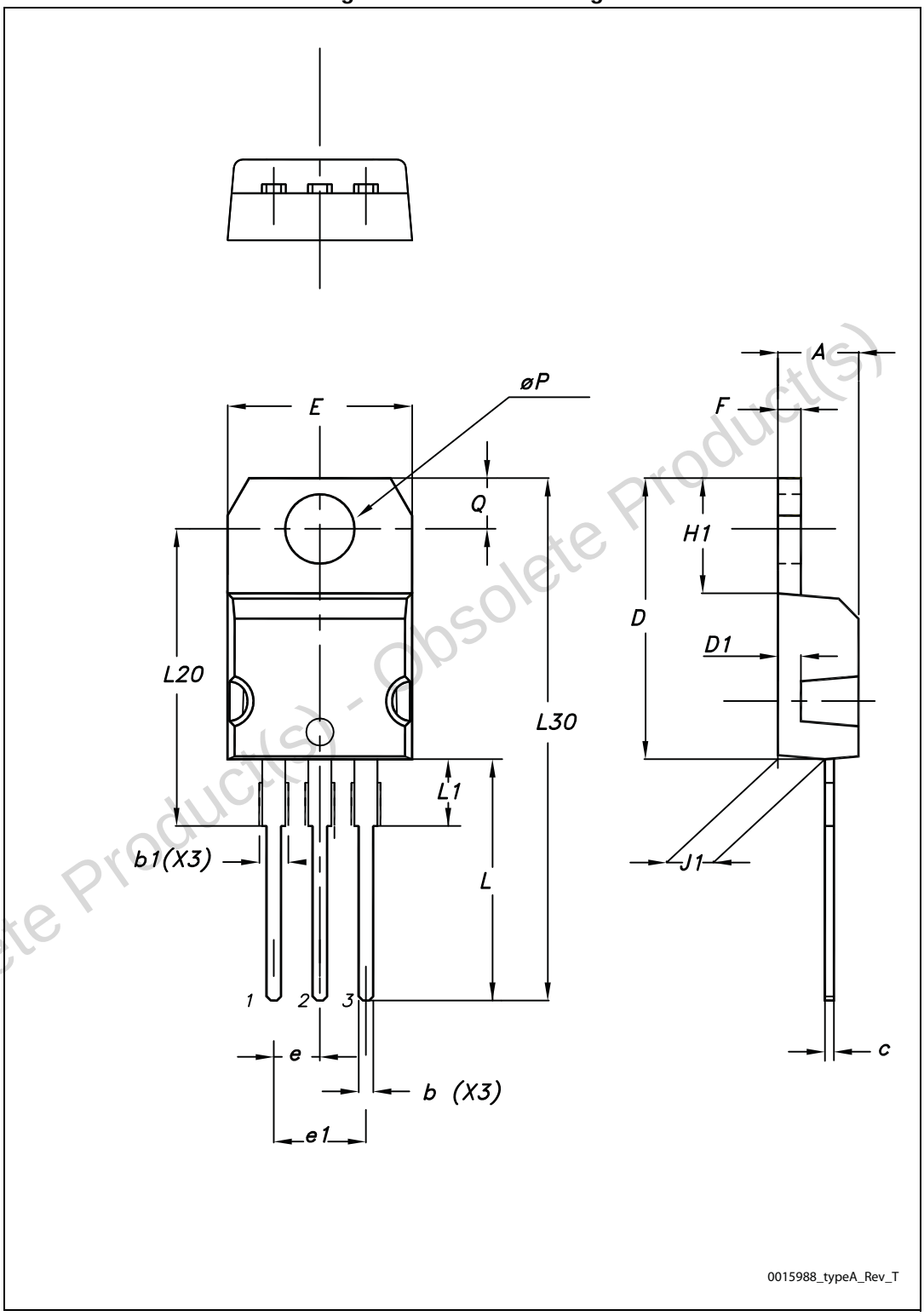
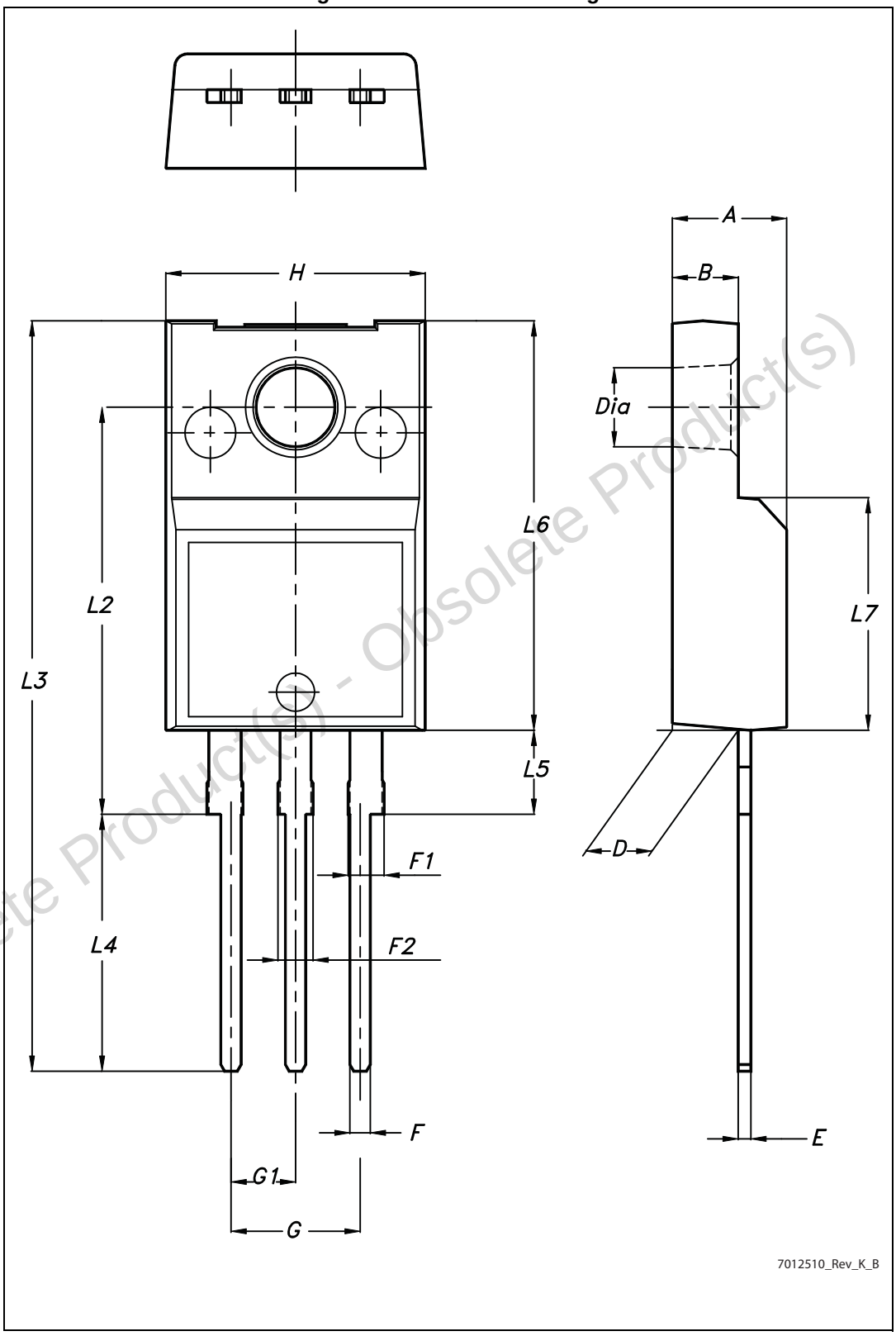


Table 11. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 23. TO-220FP drawing



5 Revision history

Table 12. Document revision history

Date	Revision	Changes
19-Jul-2013	1	First release. The part numbers STF9NK60ZD and STP9NK60ZD were previously included in datasheet with DocID9573.

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