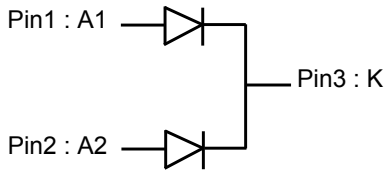
STPS80A150CHR

Datasheet

Rad-Hard 2 x 40 A - 150 V Schottky rectifier

SMD.5

The upper metallic lid is not internally connected to any pin, nor to the IC die inside the package



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Features

- Forward current: 2 x 40 A
- Repetitive peak reverse voltage: 150 V
- Low forward voltage drop: 0.88 V max. at 80 A / 125 °C
- dV/dt up to 10 kV/µs
- Monolithic dual die - common cathode
- Ceramic hermetic package
- TID and SEE characterized
- Package mass: 0.92 g
- ESCC qualified : 5106/023

Description

The STPS80A150CHR is package and screened to comply with the ESCC5000 specification for Rad-Hard products. It is a dual monolithic Schottky rectifier assembled in an SMD.5 hermetic package and characterized in total dose at high dose rate and in single event effect to be used in aerospace applications. It is ESCC qualified.

The complete ESCC specification for this device is available from the European Space Agency web site. ST guarantees full compliance of qualified parts with the ESCC detailed specification.

Product status link
STPS80A150CHR

Product summary	
$I_{F(AV)}$	2 x 40 A
V_{RRM}	150 V
T_j(max)	175 °C
$V_{F(max)}$ at 2 x 40 A / 125 °C	0.88 V

1 Characteristics

1.1 Absolute maximum ratings

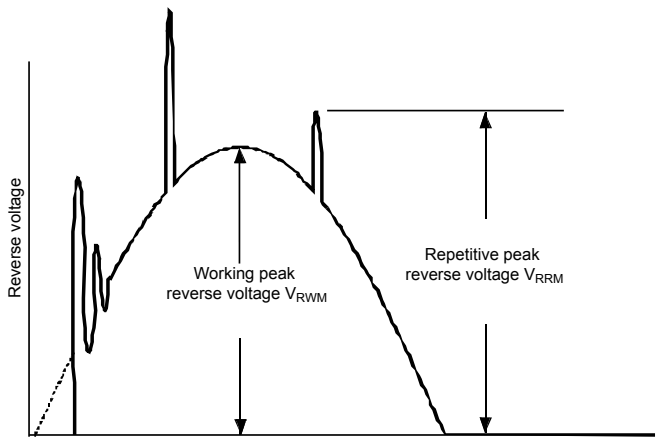
The absolute maximum ratings are limiting values at 25°C, per diode unless otherwise notified. Values provided in Table 1 shall not be exceeded at any time during use or storage

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{RWM}(1)	Working peak reverse voltage	150	V
V_{RRM}	Repetitive peak reverse voltage	150	V
I_O(2)	Average output rectified current per diode per package	 40 80	A
I_{FSM}	Forward surge current	190	A
dV/dt(3)	Reverse voltage maximum rise rate (4)	10	kV/µs
T_{op}	Operating temperature range (case temperature)	-65 to +175	°C
T_j(5)	Maximum junction temperature	+175	°C
T_{stg}	Storage temperature range	-65 to +175	°C
T_{sol}(6)	Soldering temperature	+245	°C
ESD	Electrostatic discharge - Human body model	8	kV

1. *See Figure 1.*
2. *Per diode: at T_{case} > +33.5 °C, derate linearly to 0 A at +175 °C. Per package: at T_{case} > -8 °C, derate linearly to 0 at +175°C.*
3. *Evaluated by characterization. Tested in production at 25 °C on 5 parts per wafer lot.*
4. *V_{RRM} from stationary no-conduction state to V_{RRM} < V_{RRM} max*
5. *$(dP_{tot}/dT_j) < (1/R_{th(j-a)})$ condition to avoid thermal runaway for a diode on its own heatsink.*
6. *Duration 5 seconds maximum with at least 3 minutes between consecutive temperature peaks.*

Figure 1. V_{RRM} and V_{WRM} definition - Schematics



1.2 Thermal parameters

Table 2. Thermal parameters

Symbol	Parameter		Typ. value	Max. value	Unit
$R_{th(j-c)}$	Thermal resistance, junction to case[1]	Per diode	-	3.4	°C/W
		Per package	-	2.2	

1. *When only 1 diode is used, the dissipation is made from a part of the die, hence to a higher thermal resistance.*

1.3 Electrical characteristics

Limiting value per diodes, unless otherwise specified.

Table 3. Static electrical characteristics

Symbol	Parameter	MIL-STD-750 test method	Test conditions		Min.	Typ.	Max.	Unit
I_R (1)	Reverse leakage current	4016	DC method, V_R = 150 V	T_j = 25 °C	-		14	µA
				T_j = 125 °C	-	2.0	8	mA
V_{F1} (2)(3)	Forward voltage drop	4011	I_F = 20 A	T_j = -55 °C	-	1.27	1.44	V
				T_j = 25 °C	-	0.85	0.93	
				T_j = 125 °C	-	0.70	0.78	
			I_F = 30 A	T_j = -55 °C	-	1.65	1.87	
				T_j = 25 °C	-	0.90	0.99	
				T_j = 125 °C	-	0.76	0.83	
			I_F = 40 A	T_j = -55 °C	-	2.05	2.33	
				T_j = 25 °C	-	0.95	1.04	
				T_j = 125 °C	-	0.81	0.88	
C (3)	Junction capacitance	4001	V_R = 10 V, F = 1 MHz	T_{case} = 25 °C	-	237	310	pF

1. *100% tested at 25°C. Compliance with the 125 °C specification is supported by simulation, characterization and, as per STMicroelectronics wafer lot acceptance procedure, by sampling on 5 parts per wafer lot, with an acceptance criteria of 0. In case of fail, a 100% test is performed.*
2. *Pulse width 680 µs, duty cycle ≤ 2%*
3. *Compliance with the specification is supported by simulation, characterization and, as per STMicroelectronics wafer lot acceptance procedure, by sampling on 5 parts per wafer lot, with an acceptance criteria of 0. In case of fail, a 100% test is performed.*

1.4 Characteristics (curves)

Figure 2. Average forward current versus case temperature (DC, per diode)

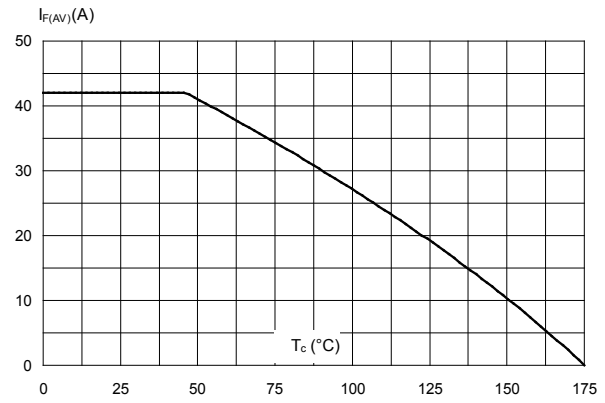


Figure 3. Forward voltage drop versus forward current (typical values, per diode)

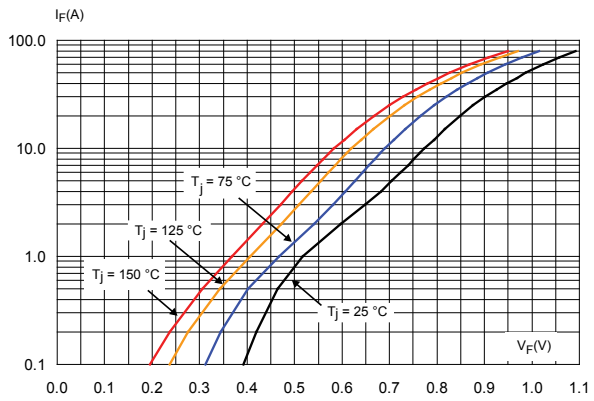


Figure 4. Reverse leakage current versus reverse voltage (typical values, per diode)

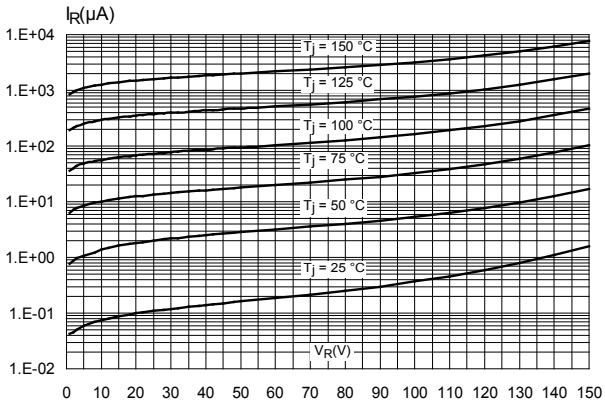


Figure 5. Relative variation of $Z_{th(j-c)}$ versus pulse duration

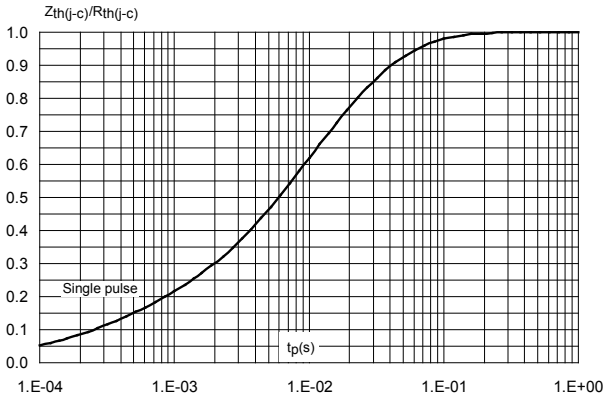
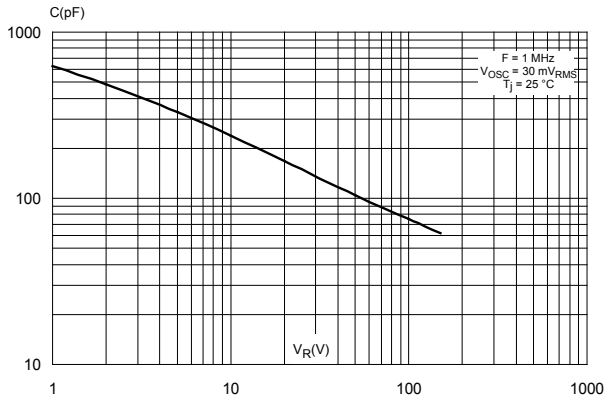


Figure 6. Junction capacitance versus reverse voltage (typical values, per diode)



2 Radiation

The technology of the STMicroelectronics Rad-Hard rectifier's diodes is intrinsically highly resistant to radiative environments.

The product radiation hardness assurance is supported by a total ionisation dose (TID) test at high dose rate and a single effect event (SEE) characterization.

2.1 Total dose radiation (TID) testing

The part has been characterized in total ionizing dose at high dose rate on 12 parts packaged in SMD.5, 4 parts unbiased, 4 parts reverse biased and 4 parts forward biased. All parts were from the same wafer lot.

The irradiation has been done according to the ESCC 22900 specification, standard window.

Both pre-irradiation and post-irradiation performances have been tested using the same circuitry and test conditions for a direct comparison can be done (T_{amb} = 22 ±3 °C unless otherwise specified).

The following parameters were measured :

- Before irradiation
- After irradiation at final dose 3 Mrad (Si)
- After 168 hrs at room temperature
- after 168 hrs at 100 °C anneal

Based on this characterization, the device is deemed able to sustain 3 Mrad(Si) while maintaining all its parameters within its specifications.

2.2 Single event effect

The Single Event Effect (SEE) relevant to power rectifiers are characterized, i.e. the Single Event Burnout (SEB).

The tests are performed as per ESCC 25100, each one on 3 pieces from 1 wafer at room temperature.

The accept/reject criteria are :

- SEB (Destructive mode):

  The diode is reverse biased during irradiation. The test is stopped as soon as a SEB occurs or when the reverse leakage current is above the specification or when the overall fluency on the component reaches 1E7 cm².
- Post irradiation stress test (PIST):

  After the irradiation, a stress is applied to the diode in order to reveal any latent damage on the irradiated devices.

  The reverse voltage value is increased from 0 V to 100% of $V_R$max. and then decreased from 100% of the $V_R$max. to 0 V. At each step, the reverse leakage current value is measured.

Table 4. Radiation hardness assurance summary

Type	Conditions	Result
Total ionisation dose	High dose rate 4 reverse biased + 4 forward biased + 4 unbiased	Immune up to 3 Mrad(Si)
Single effect burnout	LET : 61.2 MeV.cm/mg V_r : 30 V	No burnout

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 SMD.5 package information

Figure 7. Surface mount SMD.5 package outline (3-terminal)

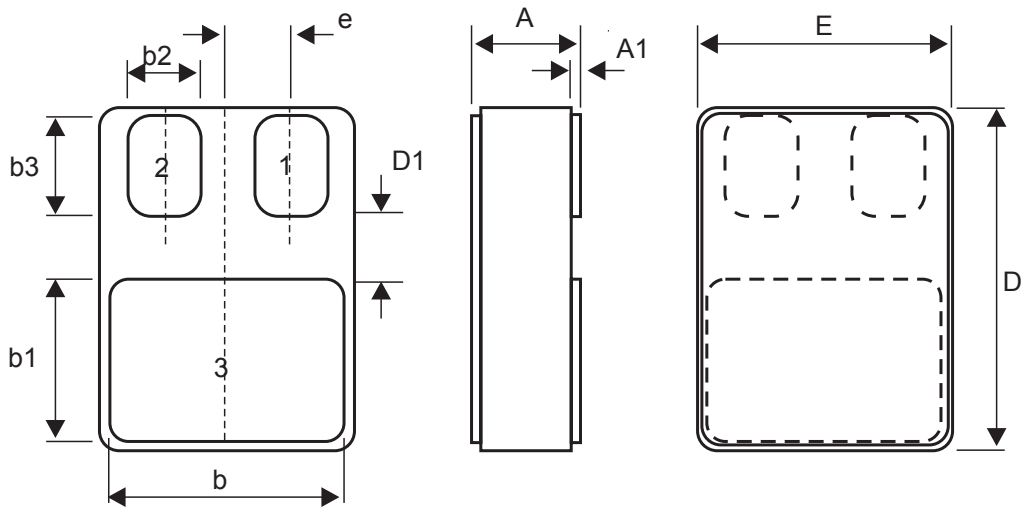


Table 5. SMD.5 package mechanical data

Symbols	Dimensions (mm)			Dimensions (inches)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.84		3.15	0.112		0.124
A1	0.25		0.51	0.010		0.200
b	7.13		7.39	0.281		0.291
b1	5.58		5.84	0.220		0.230
b2[(1)]	2.28		2.54	0.090		0.100
b3	2.92		3.18	0.115		0.125
D	10.03		10.28	0.395		0.405
D1	0.76			0.030		
E	7.39		7.64	0.291		0.301
e		1.91 BSC			0.075	

1. 2 locations

4 Ordering information

Table 6. Ordering information

Order codes	ESCC detail specification	Quality level	Package	Lead finishing	Marking(1)	Weight	Packing
STPS80A150CS1	-	engineering model	SMD.5	Gold	STPS80A150CS1	0.92 g	Strip pack
STPS80A150CSG	5106/023/01	Flight model			510602301		

1. *Specific marking only. The full marking includes in addition:*
   - *For the Engineering Models: ST logo, date code, country of origin (FR)*
   - *For flight parts: ST logo, date code, country of origin (FR), ESA logo, serial number of the part within the assembly lot*

5 Other information

5.1 Traceability information

The date code in formation is structured as described in the table below.

Table 7. Date codes

Model	Date code[1]
EM	3yywwN
ESCC	yywwN

1. *yy = year, ww = week number, N = lot index in the week.*

5.2 Documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The documentation is provided on printed paper in a dedicated envelop.

Table 8. Default documentation provided with the parts

Quality level	Documentation
Engineering Model	Certificate of Conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference data sheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID
ESCC Flight	Certificate of Conformance including: • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Diffusion line (plant + wafer size) • Diffusion run (wafer lot number) and wafer ID • Reference of the applicable ESCC Qualification maintenance lot • Reference to the ESCC detail specification • ST Rennes assembly lot ID

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
26-Jun-2020	1	First issue.
20-Oct-2020	2	Updated Table 8.
06-Dec-2021	3	Updated Table 1 and Table 8. Added Figure 1.