STR-W6200D Series PWM Off-Line Switching Regulator ICs

General Description

The STR-W6200D series are power ICs for switching power supplies, incorporating a power MOSFET and a current mode PWM controller IC in one package. Including a startup circuit and a standby function in the controller, the product achieves low power consumption, low standby power, and high cost-effectiveness in power supply systems, while reducing external components.

Features and Benefits

- TO-220 fully-molded package with 6 pins
- Current mode PWM control
- PWM and frequency modulation functions: reduces EMI noise, simplifies EMI filters, and cuts cost by external part reduction
- Built-in Slope Compensation circuit: avoids subharmonic oscillation
- Automatic Standby Mode function (Input Power < 40 mW at no load)
  - Normal operation: PWM mode
  - Light load operation: Standby mode (burst oscillation)
- Built-in Audible Noise Suppression function during Standby mode
- Built-in startup circuit: reduces power consumption in standby operation, and eliminates external components
- Bias-Assist function: improves startup operation, suppresses VCC pin voltage drop in operation, and allows use of smaller V_{CC} capacitor
- Built-in Leading Edge Blanking function
- Protection Functions:
  - Overcurrent Protection function (OCP); pulse-by-pulse, built-in compensation circuit to minimize OCP point variation on AC input voltage
  - Overload Protection function (OLP); auto restart, built-in timer, reduces heat during overload condition, and few external components required
  - External Latch Protection function (ELP): latched shutdown by external signal
  - Overvoltage Protection function (OVP): latched shutdown
  - Thermal Shutdown function (TSD); latched shutdown

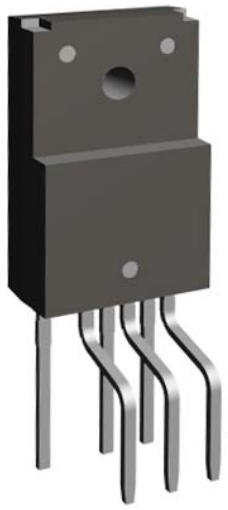

Figure 1. STR-W6200 series packages are fully molded TO-220 package types. Pin 2 is deleted for greater isolation. A flange is provided for heatsink mounting.

Applications

Switching power supplies for electronic devices such as:

- White goods
- Consumer electronics
- Office automation
- Industrial equipment
- Communications equipment

The product lineup for the STR-W6200D series provides the following options:

Part Number	f_{OSC} (kHz)	MOSFET V_{DSS}(min) (V)	$R_{DS(on)}$ (max) (Ω)	P_{OUT}* (W)	
				230 VAC	85 to 265 VAC
STR-W6251D	67	650	3.95	45	30
STR-W6252D			2.8	60	40
STR-W6253D			1.9	90	60

*The listed output power is based on the thermal ratings, and the peak output power can be 120% to 140% of the value stated here. At low output voltage and short duty cycle, the output power may be less than the value stated here.

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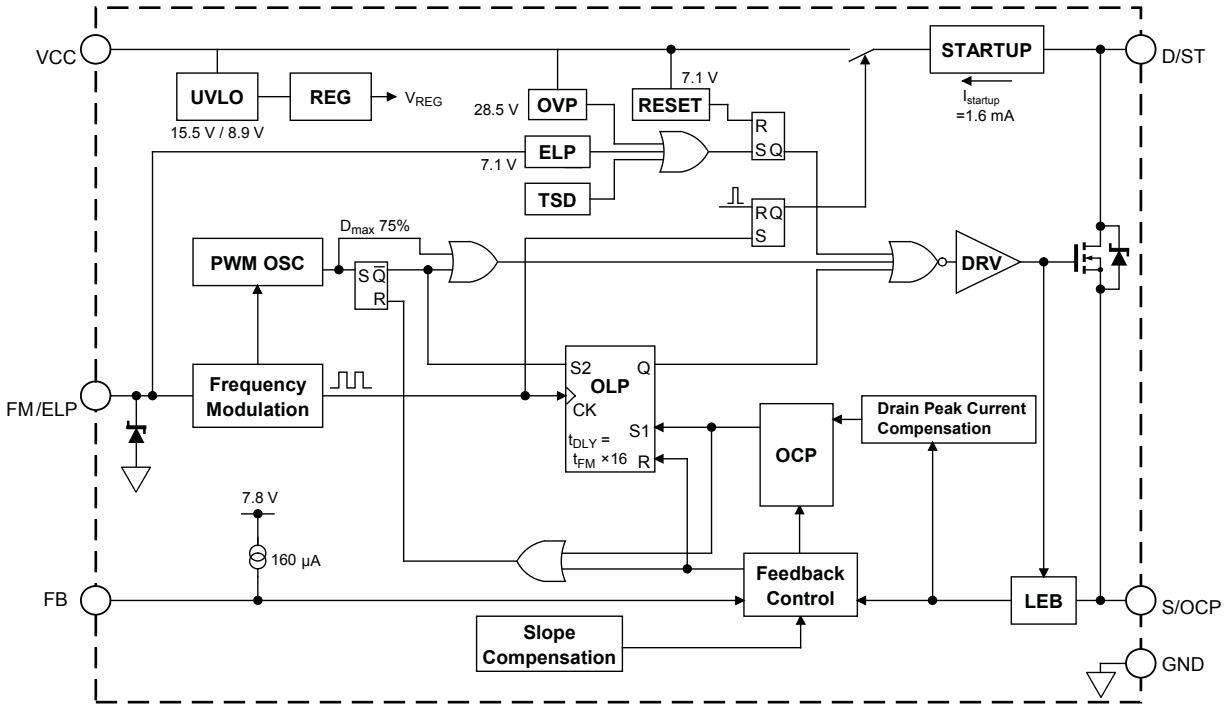


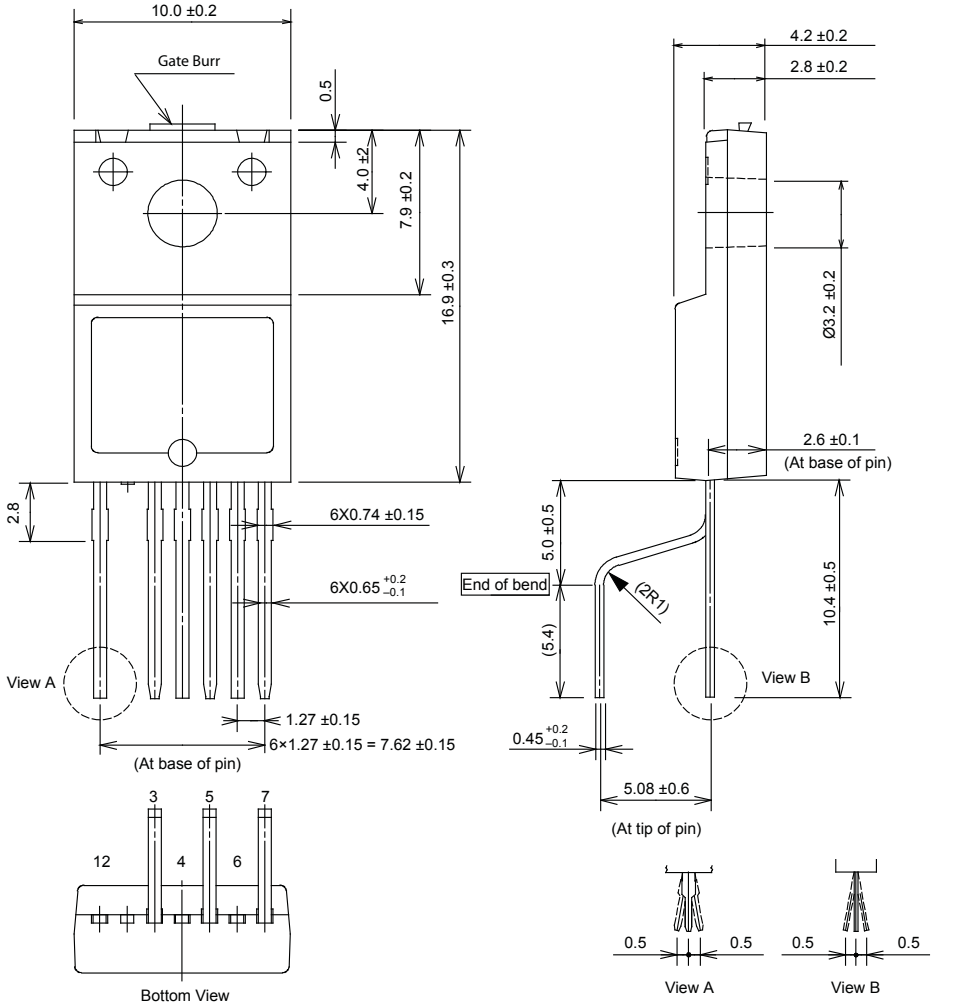
Pin List Table

Number	Name	Function
1	D/ST	MOSFET drain and input of the startup current
2	–	(Pin removed)
3	S/OCP	MOSFET source and input of Overcurrent Protection (OCP) signal
4	VCC	Power supply voltage input for Control Part and input of Overvoltage Protection (OVP) signal
5	GND	Ground
6	FB	Input for constant voltage control signal
7	FM/ELP	Capacitor connection pin for frequency modulation and input of External Latch Protection

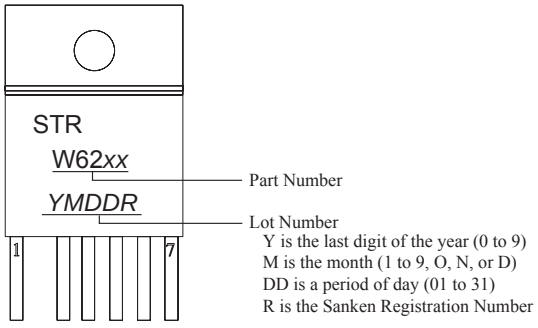
Table of Contents

Package Diagram

TO-220F-6L package
Leadform: 2003



Unit: mm
Dashed line at Gate Burr indicates protrusion of 0.3 mm (max)



Pin treatment Pb-free. Device composition compliant with the RoHS directive.

Electrical Characteristics

- This section provides separate sets of electrical characteristic data for each product.
- The polarity value for current specifies a sink as "+ ," and a source as "–," referencing the IC.

Absolute Maximum Ratings Unless specifically noted, valid at T_A = 25°C

Characteristic	Symbol	Note			Pin	Rating	Unit
Drain Peak Current	I_{DPEAK}	STR-W6251D	Single Pulse		1-3	2.6	A
		STR-W6252D				3.2	A
		STR-W6253D				10	A
Maximum Switching Current	I_{DMAX}	STR-W6251D	T_A = –20°C to 125°C		1-3	2.6	A
		STR-W6252D				3.2	A
		STR-W6253D				10	A
Avalanche Energy	E_{AS}	STR-W6251D	I_{LPEAK} = 2 A	Single Pulse, V_{DD} = 99 V, L = 20 mH	1-3	47	mJ
		STR-W6252D	I_{LPEAK} = 2.3 A			62	mJ
		STR-W6253D	I_{LPEAK} = 2.7 A			86	mJ
S/OCP Pin Voltage	V_{OCP}				3-5	–6 to 6	V
FM/ELP Pin Voltage	V_{FM}				7-5	–0.3 to 12	V
FM/ELP Pin Sink Current	I_{FM}				7-5	3	mA
FB Pin Voltage	V_{FB}	FB pin is open			6-5	–0.3 to 9	V
Controller Part Input Voltage	V_{CC}				4-5	0 to 32	V
MOSFET Power Dissipation	P_{D1}	STR-W6251D	With infinite heatsink		1-3	25	W
		STR-W6252D				26	W
		STR-W6253D				27.5	W
		Without heatsink				1.3	W
Controller Part Power Dissipation	P_{D2}				4-5	0.8	W
Internal Frame Temperature in Operation	T_F	Recommended operating temperature is T_F = 105°C (max)			–	–20 to 115	°C
Operating Ambient Temperature	T_{op}				–	–20 to 115	°C
Storage Temperature	T_{stg}				–	–40 to 125	°C
Channel Temperature	T_{ch}				–	150	°C

Electrical Characteristics of Control Part Unless specifically noted, T_A is 25°C, V_{CC} = 18 V

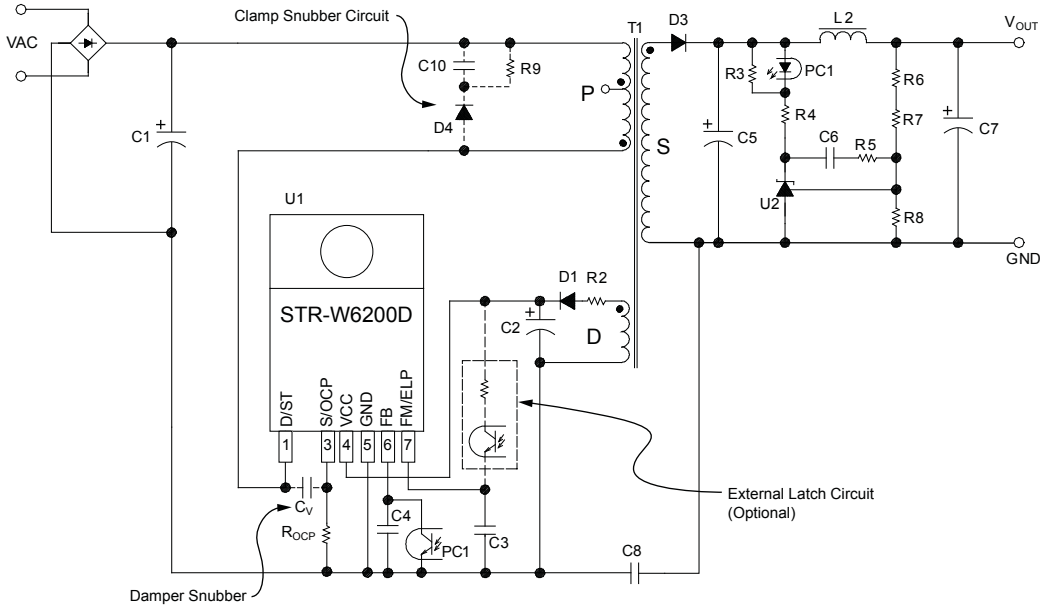
Characteristic	Symbol	Pin	Min.	Typ.	Max	Unit
Power Supply Startup Operation						
Operation Start Voltage	$V_{CC(ON)}$	4-5	13.9	15.5	17.1	V
Operation Stop Voltage	$V_{CC(OFF)}$	4-5	8.0	8.9	9.8	V
Circuit Current in Operation	$I_{CC(ON)}$	4-5	–	1.4	2.8	mA
Circuit Current in Non-Oscillation	$I_{CC(STOP)}$	4-5	–	0.8	1.3	mA
Circuit Current in Non-Operation	$I_{CC(OFF)}$	4-5	–	5	20	μA
Startup Current	$I_{STARTUP}$	4-5	–0.9	–1.6	–2.3	mA
Bias Assist Voltage	$V_{CC(BIAS)}$	4-5	13.6	15.2	16.8	V
Normal Operation						
FM/ELP Pin High Threshold Voltage	$V_{FM(H)}$	7-5	4.0	4.5	5.0	V
FM/ELP Pin Low Threshold Voltage	$V_{FM(L)}$	7-5	2.4	2.8	3.2	V
FM/ELP Pin Voltage Difference	ΔV_{FM}	7-5	1.4	1.7	1.8	V
FM/ELP Pin Source Current	$I_{FM(SRC)}$	7-5	–17.4	–13	–8.6	μA
FM/ELP Pin Sink Current	$I_{FM(SNK)}$	7-5	8.6	13	17.4	μA
Average Switching Frequency	$f_{OSC(AVG)}$	1-5	60	67	74	kHz
Frequency Modulation Deviation	Δf	1-5	4.8	6.9	9	kHz
Maximum Duty Cycle (On-duty)	D_{MAX}	1-5	71	75	79	%
FB Pin Maximum Feedback Current	$I_{FB(MAX)}$	6-5	–220	–160	–100	μA
Standby Operation Startup Voltage	V_{STBY}	6-5	0.99	1.10	1.21	V
Slope Compensation Startup Duty Cycle	D_{SLP}	6-5	–	27	–	%
Slope Compensation Rate	SLP	6-5	–22	–17	–12	mV/μs
Protection Operation						
OCP Threshold Voltage at Zero Duty Cycle (0% On-duty)	V_{OCP1}	3-5	0.71	0.78	0.86	V
Drain Peak Current Compensation Coefficient	D_{PC}	–	1.5	1.9	2.3	mV/D%
OCP Threshold Voltage After Compensation	V_{OCP2}	3-5	0.82	0.93	1.04	V
LEB Time	t_{BW}	1-5	280	400	520	ns
OLP Delay Time*	t_{DLY}	1-5	–	200	–	ms
Circuit Current in OLP-Operation	$I_{CC(OLP)}$	4-5	–	410	700	μA
OVP Threshold Voltage	$V_{CC(OVP)}$	4-5	27	28.5	30	V
Latch Circuit Holding Current	$I_{CC(La.H)}$	4-5	–	140	220	μA
Latch Circuit Release Voltage	$V_{CC(La.OFF)}$	4-5	6.4	7.1	7.8	V
ELP Threshold Voltage	V_{ELP}	7-5	6.4	7.1	7.8	V
Sink Current in ELP Operation	I_{ELP}	7-5	–	55	100	μA
Thermal Shutdown Activating Temperature	$T_{J(TSD)}$	–	135	–	–	°C

*Reference value of 47 nF capacitor between FM/ELP and GND Pins.

Electrical Characteristics of MOSFET Unless specifically noted, T_A is 25°C

Characteristic	Symbol	Note		Pin	Min.	Typ.	Max.	Unit
Drain-to-Source Breakdown Voltage	V_{DSS}			1-3	650	–	–	V
Drain Leakage Current	I_{DSS}			1-3	–	–	300	μA
On-Resistance	$R_{DS(ON)}$	STR-W6251D		1-3	–	–	3.95	Ω
		STR-W6252D			–	–	2.8	Ω
		STR-W6253D			–	–	1.9	Ω
Switching Time	t_r			1-3	–	–	400	ns
Thermal Resistance	$R_{\theta ch-F}$	STR-W6251D	Between channel and internal frame	–	–	–	2.23	°C/W
		STR-W6252D			–	–	2.04	°C/W
		STR-W6253D			–	–	1.75	°C/W

Typical Application Circuit



The following design feature should be observed: In applications having a power supply specified such that V_{DS} has large transient surge voltages, a clamp snubber circuit of a capacitor-resistor-diode (CRD) combination should be added on the primary winding, P, or a damper snubber circuit of a capacitor (C) or a resistor-capacitor (CR) combination should be added between the D/ST pins and the S/OCP pin.

Functional Description

With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).

Startup Operation

Figure 2 shows the VCC pin peripheral circuit. The built-in startup circuit is connected to the D/ST pin, and it generates a constant current, $I_{STARTUP}$ (–1.6 mA typical) to charge capacitor C2 connected to the VCC pin. During this process, when the VCC pin voltage reaches $V_{CC(ON)}$ (15.5 V typical), the control circuit starts operation. After that, the startup circuit stops automatically, in order to eliminate its own power consumption.

The startup time is determined by the C2 capacitance, and a value of 10 to 47 µF is generally recommended. The approximate startup time, t_{START}, can be calculated as follows:

$$t_{STARTUP}\,(s) = C_2\,(\mu F) \times \frac{V_{CC(ON)}\,(V) - V_{CC(INT)}\,(V)}{|I_{STARTUP}|\,(mA)} \quad (1)$$

where $V_{CC(INT)}$ is the initial voltage on the VCC pin.

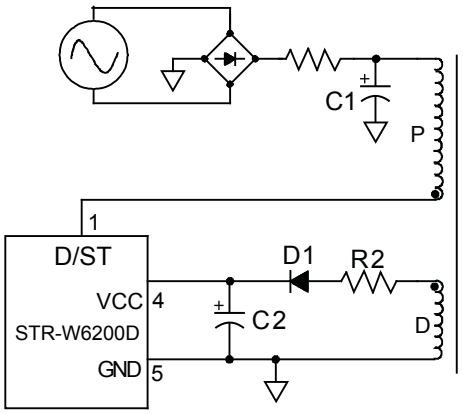


Figure 2. VCC pin peripheral circuit

Figure 3 shows the relationship of V_{CC} and I_{CC}. When the VCC pin voltage increases to $V_{CC(ON)}$, the control circuit starts operation and the circuit current, I_{CC}, increases. In operation, when the VCC pin voltage decreases to $V_{CC(OFF)}$ (8.9 V typical), the control circuit stops operation, by the UVLO (Undervoltage Lockout) circuit, and reverts to the state before startup.

The rectified voltage from the auxiliary winding, D (figure 2), becomes a power source to the control circuit after the operation start.

The VCC pin voltage should become as follows within the specification of input voltage range and the output load range of power supply, taking account of the winding turns of the D winding; the target voltage of the VCC pin voltage is about 15 to 20 V:

$$V_{CC(OFF)} = 9.8\ V\ (max) < V_{CC} < V_{CC(OVP)} = 27.0\ V\ (min) \quad (2)$$

Figure 4 shows the VCC pin voltage behavior during the startup period. When the VCC pin voltage reaches $V_{CC(ON)}$, the control circuit starts operation, the circuit current, I_{CC}, increases, and thus the VCC pin voltage begins dropping. At the same time, the auxiliary winding voltage, V_D, increases in proportion to the output voltage rise. Thus, the VCC pin voltage is set by the balance between dropping by the increase of I_{CC} and rising by the increase of the auxiliary winding voltage, V_D.

Just at the turning-off of the power MOSFET, a surge voltage occurs at the output winding. If the feedback control is activated by the surge voltage on light load condition at startup, and the VCC pin voltage decreases to $V_{CC(OFF)}$, a startup failure can occur, because the output power is restricted and the output voltage decreases.

In order to prevent this, when the VCC pin voltage falls to the Bias Assist Voltage, $V_{CC(BIAS)}$ (15.2 V typical), the Bias

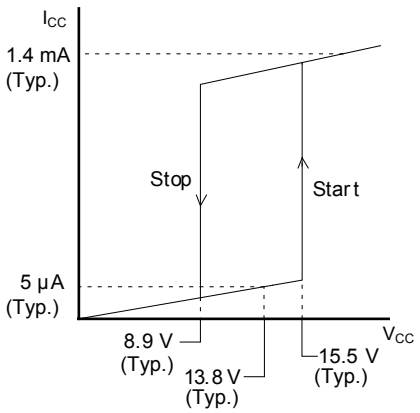


Figure 3. VCC versus ICC

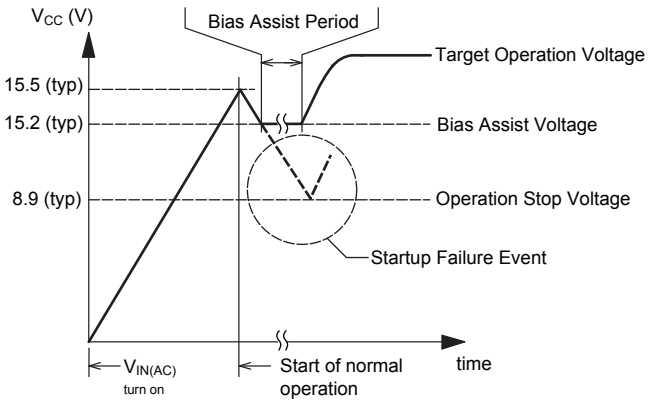


Figure 4. VCC during startup period

Assist function is activated. While this function is operating, the decrease of the VCC pin voltage is suppressed by providing the startup current, $I_{STARTUP}$, from the startup circuit. By this function, the use of a small value C2 capacitor is allowed, resulting in shortened startup time. Also, because the increase of VCC pin voltage becomes faster when the output runs with excess voltage, the response time of the OVP function can also be shortened.

After the IC starts switching operation, the Bias Assist function is available until the FM/ELP pin voltage reaches the FM/ELP pin High Threshold Voltage, $V_{FM(H)}$ (4.5 V typical), and at this voltage, this function stops.

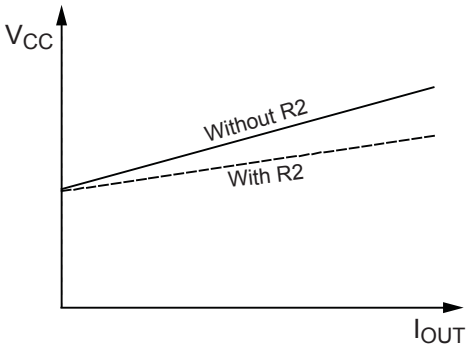


Figure 5. V_{CC} versus I_{OUT} with and without resistor R2

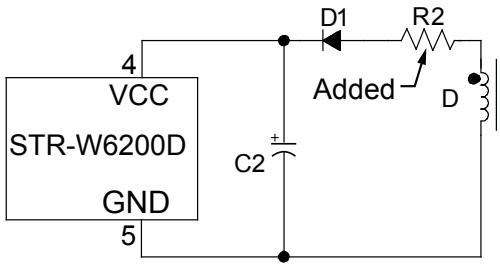
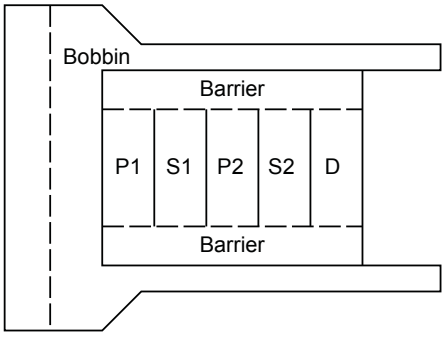


Figure 6. VCC pin peripheral circuit with R2

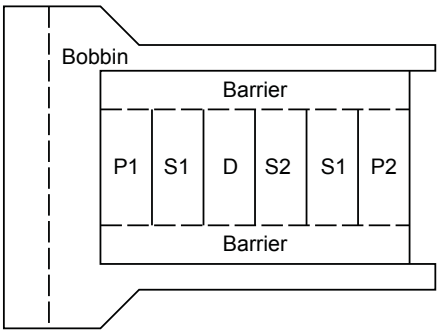
In actual power supply circuits, there are cases in which the VCC pin voltage fluctuates in proportion to the output of the SMPS (see figure 5), and the Overvoltage Protection (OVP) on the VCC pin may be activated. This happens because C2 is charged to a peak voltage on the auxiliary winding D, which is caused by the transient surge voltage coupled from the primary winding when the power MOSFET turns off.

For alleviating C2 peak charging, it is effective to add some value R2, of several tenths of ohms to several ohms, in series with D1 (see figure 6). The optimal value of R2 should be determined using a transformer matching what will be used in the actual application, because the variation of the auxiliary winding voltage is affected by the transformer structural design.



P_1 ,P_2 Primary winding
S_1 Secondary output winding controlled to constant voltage
S_2 Secondary output winding
D Auxiliary winding for VCC

Figure 7. Winding structural example (a)



P_1 ,P_2 Primary winding
S_1 Secondary output winding controlled to constant voltage
S_2 Secondary output winding
D Auxiliary winding for VCC

Figure 8. Winding structural example (b)

The variation of VCC pin voltage becomes worse if:

• The coupling between the primary and secondary windings of the transformer gets worse and the surge voltage increases (low output voltage, large current load specification, for example).

• The coupling of the auxiliary winding, D, and the secondary side stabilization output winding (winding of the output line which is controlling constant voltage) gets worse and it is subject to surge voltage.

In order to reduce the influence of surge voltages on the VCC pin, alternative structures of the auxiliary winding, D, can be used; as examples of transformer structural designs see figures 7 and 8.

• Winding structural example (a): Separating the auxiliary winding D from the primary side windings P1 and P2.

The primary side winding is divided into two windings, P1 and P2.

• Winding structural example (b): Placing the auxiliary winding D within the secondary winding S1 in order to improve the coupling of those windings.

The output winding S1 is a stabilized output winding, controlled to constant voltage.

Frequency Modulation Function

The frequency modulation is superposed on the PWM frequency, helping to reduce the conductive EMI noise, and simplify noise filtering on input lines.

Figure 9 shows the V_{DS} and I_D waveforms at an average frequency of 67 kHz and an internally-fixed fluctuation width, Δf, of 6.9 kHz typical. Figure 10 shows the relationship between the FM/ELP pin voltage and the frequency modulation period.

The C3 connected to the FM/ELP pin is charged by the constant source current, $I_{FM(SRC)}$ (–13 µA typical), until its voltage increases to about 4.5 V. After that, it is discharged by the

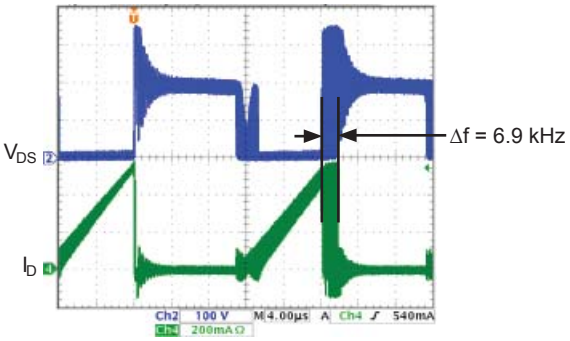


Figure 9. V_{DS} and I_D waveforms in frequency modulation

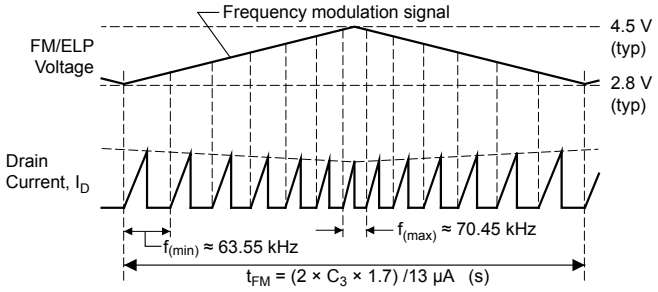


Figure 10. FM/ELP pin voltage and frequency modulation period

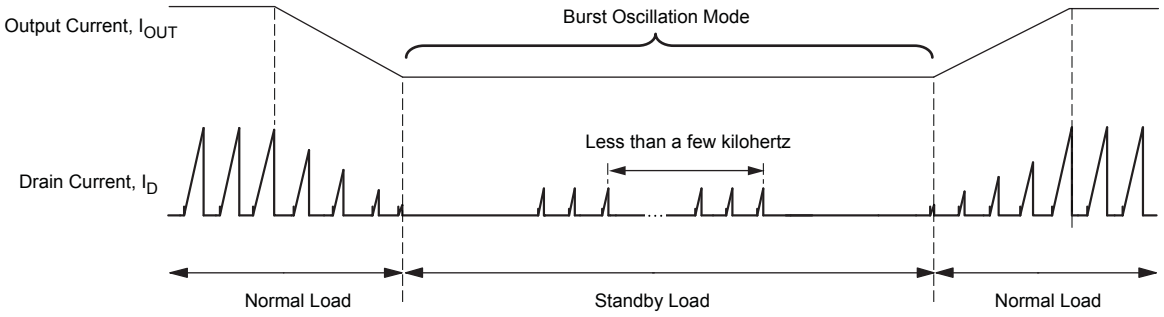


Figure 11. Automatic-Standby mode operation

constant sink current, $I_{FM(SNK)}$ (13 µA typical), until its voltage decreases to about 2.8 V, and then the mode is reverted to the constant charge by $I_{FM(SRC)}$. The repetition of this makes the frequency modulation signal a triangle waveform on the FM/ELP pin. By inputting this signal to the PWM oscillation circuit, the frequency modulation occurs.

The frequency modulation period, t_{FM}, can be adjusted by the value of C3. The t_{FM} can be calculated as follows.

$$t_{FM}\ (\mathrm{s}) = 2 \times \frac{C_3 \times \Delta V_{FM}}{13\ (\mu\mathrm{A})} \qquad (3)$$

where ΔV_{FM} is 1.7 V typical.

In general, a C_3 value in the range of 0.01 to 0.047 µF is recommended, and should be determined based on actual operation in the application.

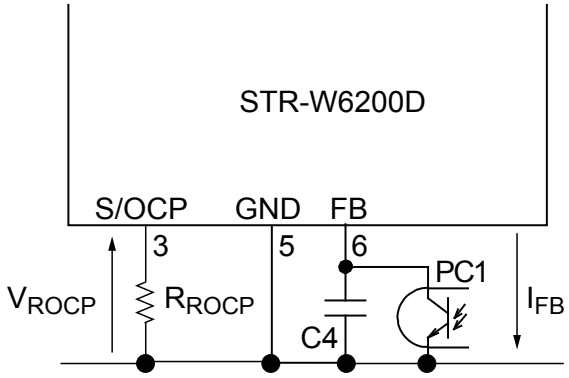


Figure 12. FB pin peripheral circuit

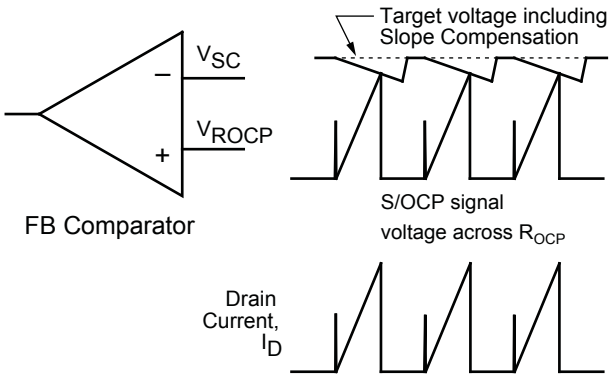


Figure 13. Drain current, I_D, and FB comparator operation in steady operation

Automatic Standby Mode Function

The Automatic Standby mode is activated automatically when the drain current, I_D, reduces under light load conditions, at which I_D is less than 15% of the maximum drain current (it is in the Overcurrent Protection state).

The operation mode becomes burst oscillation, as shown in figure 11. Burst oscillation reduces switching losses and improves power supply efficiency because of periodic non-switching intervals. Generally, to improve efficiency under light load conditions, the frequency of the burst oscillation becomes just a few kilohertz. When the burst oscillation frequency is in the human audible range (20 Hz to 20 kHz), audible noise may occur from the transformer.

This IC keeps the peak drain current low during burst oscillation mode, and suppresses the audible noise of the transformer.

Constant Output Voltage Control

The constant output voltage control function uses current-mode control (peak current mode), which enhances response speed and provides stable operation. This IC compares the voltage, V_{ROCP}, of the current detection resistor with the target voltage, V_{SC}, by the internal FB comparator, and controls the peak value of V_{ROCP} so that it gets close to V_{SC}. V_{SC} is internally generated by inputting the FB pin voltage to the feedback control (see the Functional Block diagram) and adding the slope compensation value (refer to figures 12 and 13).

• Light load conditions When load conditions become lighter, the output voltage, V_{OUT}, rises, and the feedback current from the error amplifier on the secondary side also increases. The feedback current is sunk at the FB pin, transferred through a

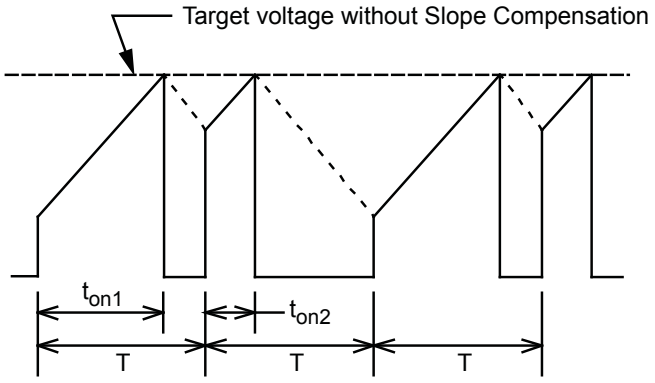


Figure 14. Drain current, I_D, waveform in subharmonic oscillation

photo-coupler, PC1, and the FB pin voltage decreases. Thus, V_{SC} decreases, the peak value of V_{ROCP} is controlled to be low, and the peak drain current of I_D decreases. This control prevents the output voltage from increasing.

• Heavy load conditions When load conditions become greater, the control circuit performs the inverse operation to that described above. Thus, V_{SC} increases and the peak drain current of I_D increases. This control prevents the output voltage from decreasing.

In the current-mode control method, when the drain current waveform becomes trapezoidal in continuous operating mode, even if the peak current level set by the target voltage is constant, the on-time fluctuates based on the initial value of the drain current. This results in the on-time fluctuating in multiples of the fundamental operating frequency as shown in figure 14. This is called the *subharmonics* phenomenon.

In order to avoid this, the IC incorporates the Slope Compensation function. Because the target voltage is added, a down-slope compensation signal that reduces the peak drain current as the on-duty gets wider relative to the FB pin signal to compensate V_{SC}, the subharmonics phenomenon is suppressed.

Even if subharmonic oscillations occur when the IC has some excess supply being out of feedback control, such as during startup and load shorted, this does not affect performance during normal operation.

In the current-mode control method, the FB comparator and/or the OCP comparator may respond to the surge voltage resulting from the drain surge current in turning-on the power MOSFET, and may turn off the power MOSFET irregularly. Leading Edge Blanking, t_{BW} (400 ns typical), is built-in to prevent malfunctions caused by surge voltage in turning-on the power MOSFET.

Fault Latch

When the OVP, ELP, and TSD functions are activated, the latch circuit is also activated, and then the IC stops switching operation, in latch mode.

After that, the VCC pin voltage decreases to $V_{CC(OFF)}$ (8.9 V typical), and then the startup circuit is activated. When the VCC pin voltage increases to $V_{CC(ON)}$ (15.5 V typical), the circuit current increases, and the VCC pin voltage decreases again. As a result, the VCC pin voltage fluctuates between 8.9 V typical and 15.5 V typical as shown in figure 15, and it prevents the VCC pin voltage from increasing.

Releasing the latched state is done by turning off the input voltage and allowing the VCC pin voltage to drop below $V_{CC(La.OFF)}$ (7.1 V typical).

External Latch Protection Function (ELP)

This function forces a latched shutdown if more than the ELP Threshold Voltage, V_{ELP} (7.1 V typical), is applied between the FM/ELP and the GND pins. The applied voltage should be within –0.3 to 12 V (the Absolute Maximum Rating of the FM/ELP pin voltage).

The Typical Application Circuit shows an example, whereby a current limitation resistor and a latch trigger switch (that is, a photocoupler), are inserted between the VCC and FM/ELP pins. Because the FM/ELP pin has a built-in Zener diode, the current limitation resistor value should be such that the current going into the FM/ELP pin would be below the Absolute Maximum Rating of 3 mA for I_{FM}.

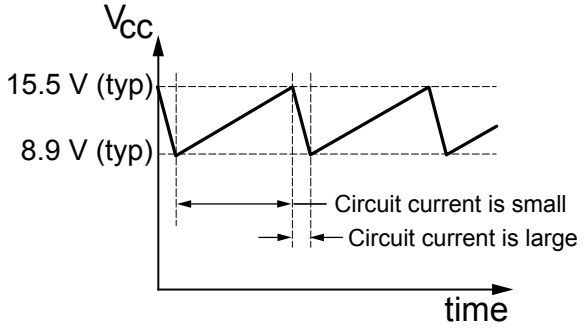


Figure 15. VCC pin voltage at fault latch

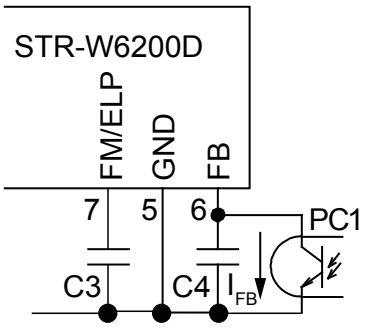


Figure 16. FB pin and FM/ELP pin peripheral circuit

Overload Protection Function (OLP)

When the peak drain current of I_D is limited by OCP operation, the output voltage, V_{OUT}, decreases and the feedback current from the secondary photo-coupler, I_{FB} (see figure 16), becomes zero. When this state remains for the OLP Delay Time, t_{DLY}, the OLP function is activated, and the IC stops switching operation.

When the VCC pin voltage decreases to $V_{CC(OFF)}$, the control circuit stops its operation by the UVLO circuit, and reverts to the state before startup. After that, the VCC pin voltage increases to $V_{CC(ON)}$ because the startup circuit is activated. As a result, the operation becomes the intermittent oscillation mode by UVLO as shown in figure 17, during OLP operation.

This operation reduces stresses on the power MOSFET and on the secondary rectifier diode, furthermore, it reduces power consumption because it reduces the frequency of the intermittent oscillation and the ratio of the switching period, by lowering the circuit current to $I_{CC(OLP)}$ (410 µA typical) during OLP operation. The approximate value of t_{DLY} is equal to 16 times the charge-discharge cycle of C3, connected to the FM/ELP pin (see figure 16), and its equation is:

$$t_{DLY}\,(s) = t_{FM} \times 16 = \frac{2 \times C_3\,(\mu F) \times 1.7\,(V)}{13\,(\mu A)\,(typ)} \times 16 \qquad (4)$$

where t_{FM} is determined by equation 3.

The Delay Time, t_{DLY}, should be longer than the period from a point where the VCC pin voltage increases to $V_{CC(ON)}$, to other where the output voltage reaches its target value, in order to prevent startup failure caused by OLP operation.

In general, a C3 value is recommended to be about 0.01 to 0.047 µF, and the optimal value should be determined based on actual operation in the application.

Overvoltage Protection Function (OVP)

When the voltage between the VCC pin and the GND pin increases to $V_{CC(OVP)}$ (28.5 V typical) or more, the OVP function is activated and stops switching operation. When the auxiliary winding supplies the VCC pin voltage, the OVP function is able to detect an excessive output voltage, such as when the detection circuit for output control is open on the secondary side, because the VCC pin voltage is proportional to the output voltage.

The secondary side output voltage, which initiates OVP operation, is calculated approximately as follows:

$$V_{OUT(OVP)} = \frac{V_{OUT}(\text{normal operation})}{V_{CC}(\text{normal operation})} \times 28.5\ (V)\ (typ.) \qquad (5)$$

Overcurrent Protection Function (OCP)

The OCP function detects each peak drain current level of a power MOSFET on a pulse-by-pulse basis, by monitoring the voltage across the current detection resistor R_{OCP} between the S/OCP pin and the GND pin, and limits the output power accordingly. When the voltage drop on both sides of R_{OCP} increases to the OCP threshold voltage, the power MOSFET is turned off.

ICs with PWM control usually have some detection delay time on OCP detection. The steeper the slope of the actual drain current at a high AC input voltage is, the later the actual detection point is, compared to the internal OCP threshold voltage, V_{OCP}. Thus, the actual OCP point limiting the output current usually has some variation depending on the AC input voltage, as shown in figure 18.

The IC incorporates a built-in AC Input Compensation function that superposes a signal with a defined slope into the detection signal from the S/OCP pin as shown in figures 19 and 20. When the AC input voltage is lower and the duty cycle is higher, the OCP compensation level of this function is increased. Therefore, the OCP point in low AC input voltage is increased to minimize the difference of OCP points between low AC input voltage and high AC input voltage, without additional external components.

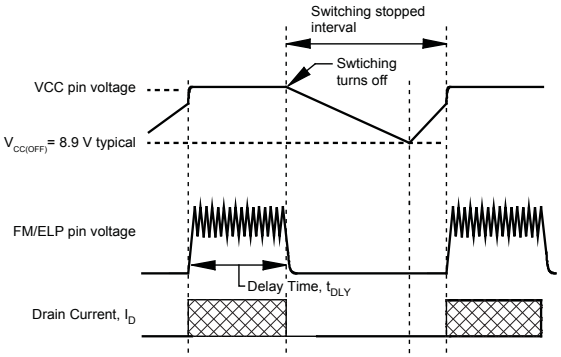


Figure 17. Waveforms during OLP operation

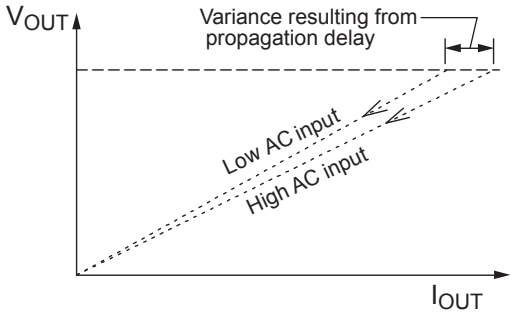


Figure 18. Output current at OCP without input compensation

Because the compensation signal level is designed to depend upon the duty cycle, the OCP threshold voltage after compensation, $V_{OCP(D\%)}$, is calculated as follows:

$$V_{OCP(D\%)}\ (V) = V_{OCP1}\ (V) + D_{PC}\ (mV/duty\%) \times D\ (\%) \qquad (6)$$

where

V_{OCP1} is the OCP threshold voltage at zero duty cycle (V), 0.78Vtypical,

D_{PC} is the OCP compensation coefficient (mV/D%), 1.9 mV/D% typical, and

D is the duty cycle.

Assuming an AC input voltage of 85 V, if the transformer is designed so the duty cycle, D, at a maximum load is 50%, then, according to equation 6, $V_{OCP(50\%)}$ = 0.875 V typical.

Thermal Shutdown Function (TSD)

When the controller chip temperature increases to 135°C (min) or more, the IC stops switching operation, in latch mode.

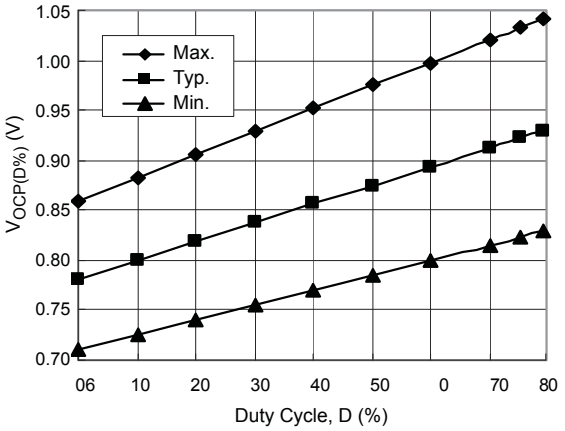


Figure 19. Duty Cycle versus OCP Threshold Voltage After Compensation

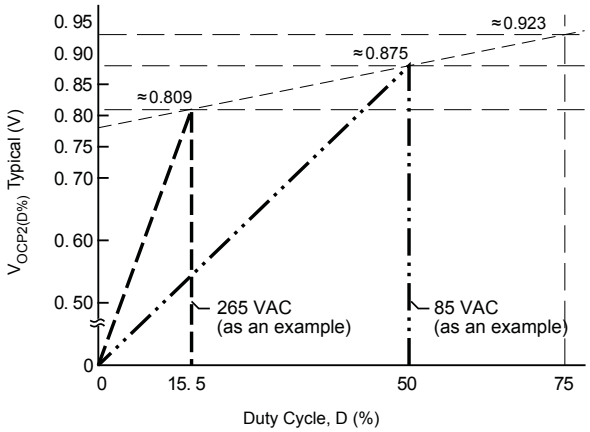


Figure 20. Duty Cycle versus typical value of OCP Threshold Voltage After Compensation relative to input voltage, for examaple

Design Notes

Peripheral Components

Take care to use the proper rating and proper type of components.

- Input and output electrolytic capacitors
  - Apply proper design margin to accommodate ripple current, voltage, and temperature rise.
  - Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.
- Transformer
  - Apply proper design margin to core temperature rise by core loss and copper loss.
  - Because the switching circuits contain high frequency currents, the skin effect may become a consideration.
  - In consideration of the skin effect, choose a suitable wire gauge in consideration of the rms current and a current density of about 3 to 4 A/mm^2.
  - If measures to further reduce temperature are still necessary, use paralleled wires or litz wires to increase the total surface area of the wiring.
- Current detection resistor, R_{OCP}
  - A high frequency switching current flows to R_{OCP}, and may cause poor operation if a high inductance resistor is used.
  - Choose a low inductance and high surge tolerant type.

Phase Compensation

A typical phase compensation circuit with a secondary shunt regulator (U2) is shown in figure 21. The value for C6 is recommended to be about 0.047 to 0.47 µF, and should be selected based on actual operation in the application.

Place C4 between the FB pin and the GND pin, as shown in figure 22, to perform high frequency noise reduction and phase compensation. The value for C4 is recommended to be about 2200 pF to 0.01 µF, and should be selected based on actual operation in the application.

Capacitance of External Capacitor at FM/ELP Pin

The capacitor C3 at the FM/ELP pin determines the frequency of frequency modulation, f_{FM}, and the OLP delay time t_{DLY}. Figure 23 shows the relationship between them and the C3 value. A C3 value of 0.01 to 0.047 µF is recommended, and should be selected based on actual operation in the application.

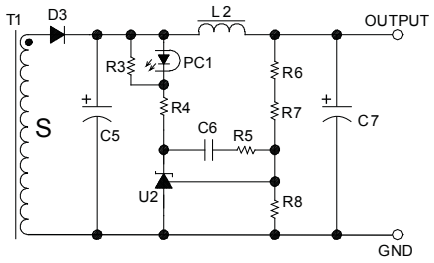


Figure 21. Peripheral circuit around secondary shunt regulator (U2)

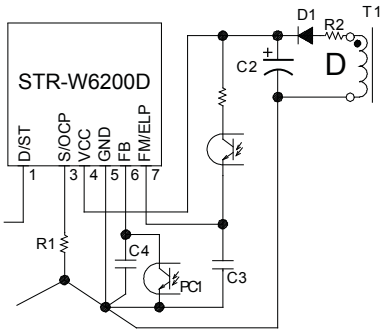


Figure 22. FB pin peripheral circuit

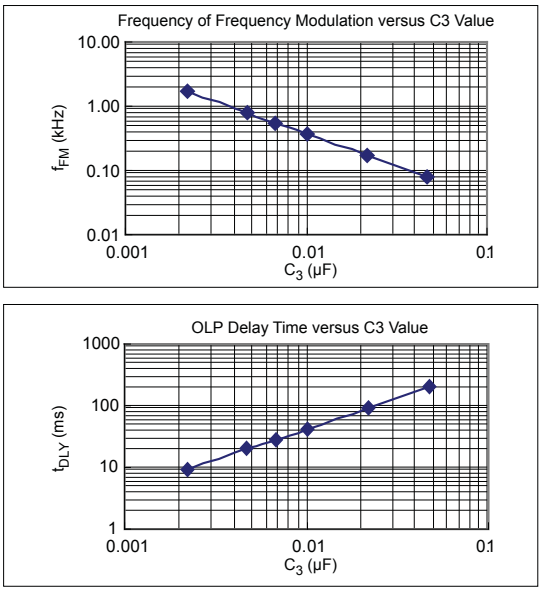


Figure 23. The relationship between t_{FM}, t_{DLY}, and C3 (calculated values)

Secondary Diode EMI Measure

A ceramic capacitor, C_{DI}, parallel to the secondary rectifier as shown in figure 24, may become necessary in some cases to reduce EMI noise reduction. If ringing occurs on the drain current, it is recommended to connect a damper resistor, R_{DI}, in series with C_{DI}, as shown in figure 25, in order to reduce ringing waveforms, and to stabilize switching operation. Note: The values chosen for R_{DI} and C_{DI} should take those temperature rises into consideration, based on actual operation in the application.

PCB Trace Layout and Component Placement

PCB circuit trace design and component layout significantly affect operation, EMI noise, and power dissipation. Therefore, pay extra attention to these designs. In general, where high frequency current traces form a loop, as shown in figure 26, wide, short traces, and small circuit loops are important to reduce line impedance. In addition, earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switch-mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines. Furthermore, because the incorporated power MOSFET has a positive thermal coefficient of $R_{DS(ON)}$, consider it when preparing a thermal design.

Figure 27 shows a circuit layout design example for the IC peripheral circuit and secondary smoothing circuit.

• **S/OCP Trace Layout:** S/OCP pin to R_{OCP} to C1 to T1 (winding P) to D/ST pin. This is the main trace containing switching currents, and thus it should be as wide and short as possible. If C1 and the IC are distant from each other, an electrolytic capacitor or film capacitor (about 0.1 µF and with proper voltage rating) near the IC or the transformer is recommended to reduce impedance of the high frequency current loop.

• **GND Trace Layout:** GND pin to C2 (negative pin) to T1 (winding D) to R2 to D1 to C2 (positive pin) to VCC pin. This trace also must be as wide and short as possible. If C2 and the IC are distant from each other, placing a capacitor (approximately 0.1 to 1.0 µF film capacitor) close to the VCC pin and the GND pin is recommended.

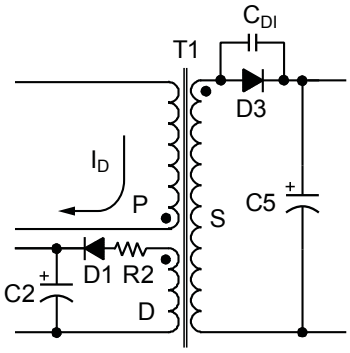


Figure 24. Rectifier measure example

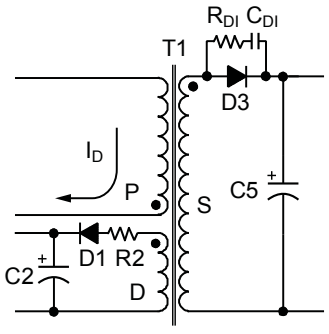


Figure 25. Damper resistor example

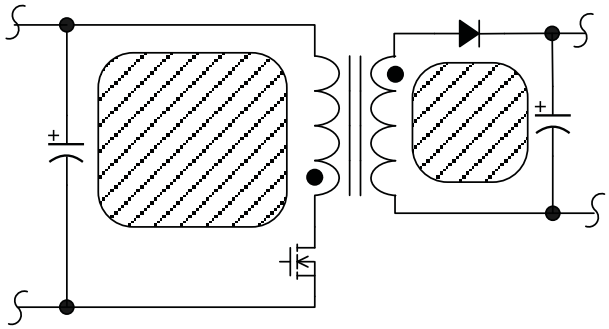


Figure 26. High-frequency current loops (hatched areas)

• **R_{OCP} Trace Layout:** R_{OCP} should be placed as close as possible to the S/OCP pin. The connection between the power ground of the main trace and the control circuit ground should be at a single point ground (A in figure 27) to remove common impedance, and to avoid interference from switching currents to the control circuit.

• **Secondary Smoothing Circuit Trace Layout:** T1 (winding S) to D3 to C5. This trace should be as wide and short as possible. If the loop distance is lengthy, leakage inductance resulting from the long loop may increase surge voltage at turning off the incorporated power MOSFET. Proper secondary trace layout helps to increase margin against the power MOSFET breakdown voltage, and reduces stress on the clamp snubber circuit and losses in it.

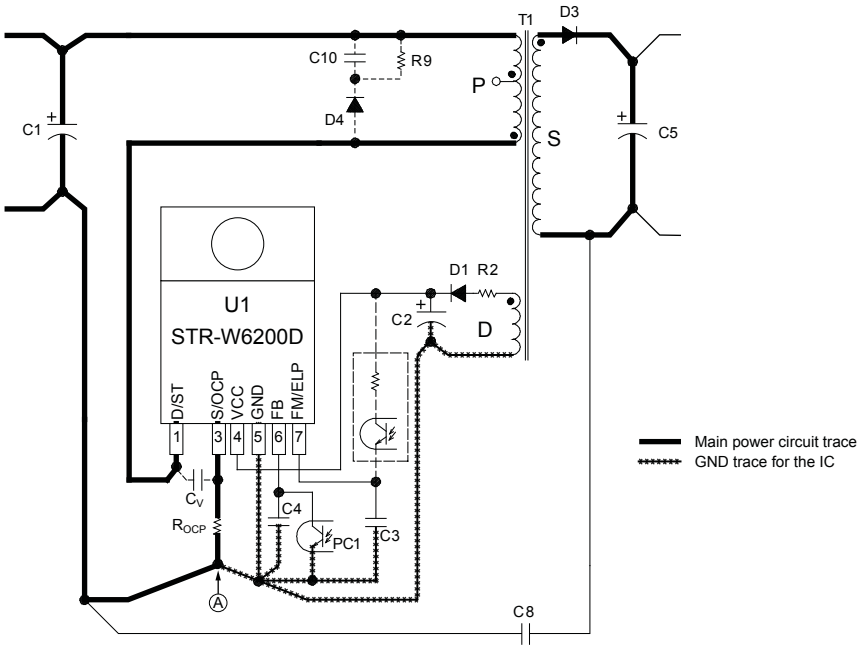


Figure 27. Peripheral circuit example around the IC

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