STR-W6700 Series

Application Note (Ver0.3)

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Preliminary

SANKEN ELECTRIC CO., LTD.

Application Engineering Department -1

Semiconductor Operations

STR-W6700 Series

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1 Introduction

The STR-W6700 series is a Hybrid IC (HIC) designed for Quasi-Resonant type Switching Mold Power Supply built-in a Power MOSFET and Control IC. At the normal operation, the HIC provides high efficiency and low noises by the Bottom-Skip Quasi-Resonant Operation, and low power consumption is also achieved by the blocking (intermittent) oscillation at stand-by mode.

The HIC adopts 6 pins full-mold package (TO220F-6L, Sanken Package Type No.: FM207) and is suitable for downsizing and standardizing of a SMPS having a limited mounting space. Furthermore, the HIC is made possible to ease circuit design with a small number of external parts, and it also makes possible to miniaturize and standardize the SMPS.

2 Features

1). The operation mode turns blocking oscillation by reducing output voltage at stand-by mode.
2). In addition to the existing Quasi-Resonant Operation, the Bottom-Skip Function is added in order to be efficient from light to medium load.
3). Soft-Start Operation is provided at the SMPS start-up.
4). Switching noise is reduced by Step-Drive Function.
5). Avalanche energy of the MOSFET is guaranteed.
6). Overcurrent Protection (OCP), Overvoltage Protection (OVP), Overload Protection (OLP), and Maximum ON-Time control circuits are incorporated.
7). It is possible to save the SMPS design time by utilizing the present designs and evaluation processes.

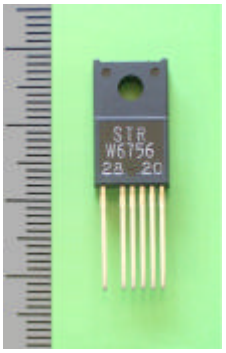
3 STR-W6700 Series Line-up

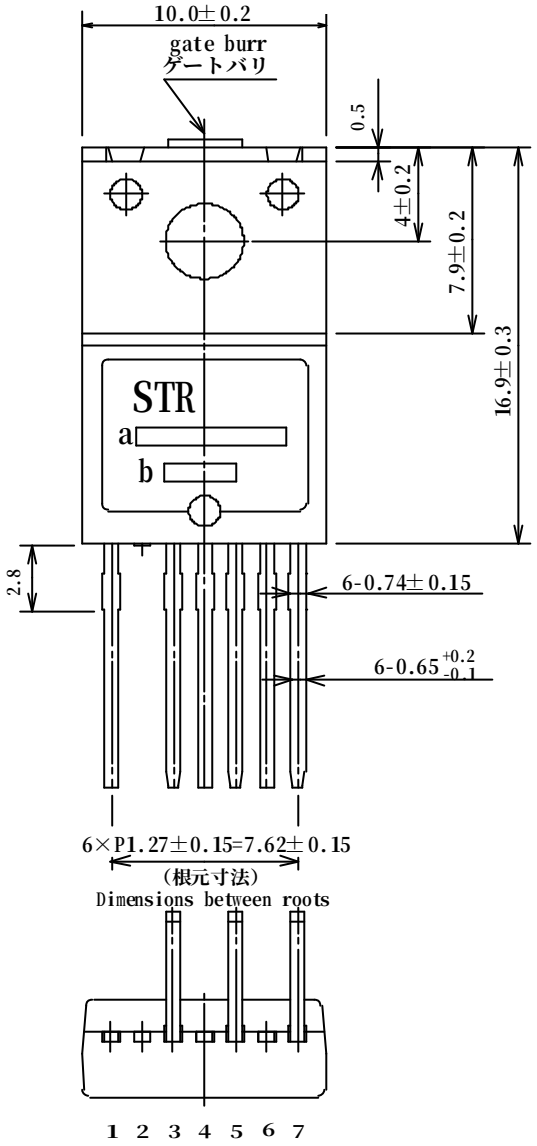
Type	MOSFET V_{DSS}[V]	$R_{DS(ON)}$ MAX[Ω]	$V_{ACINPUT}$[V]	Pout [W] ※1	Mass-Production	Engineering Sample
STR-W6754	650	1.00 ※2	WIDE	100 ※2	2Q/2003	4Q/2002
			220	200 ※2		
STR-W6756	650	0.73 ※2	WIDE	140 ※2	2Q/2003	4Q/2002
			220	280 ※2		

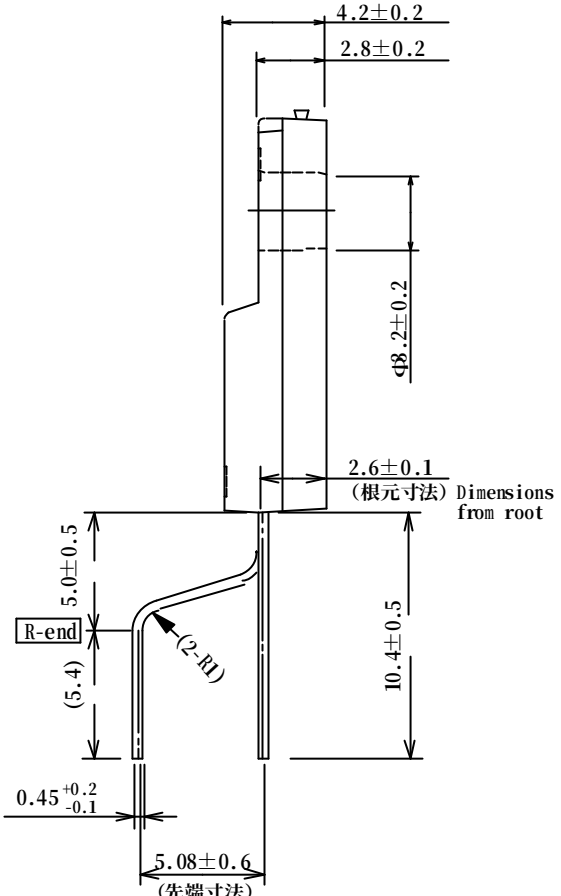
※1. The listed output power represents a thermal rating value, and the peak output power can be obtained up to 120% - 140% to the thermal rating value. In case of low output power and narrow ON duty, the output power shall be lower than that of the above listed.

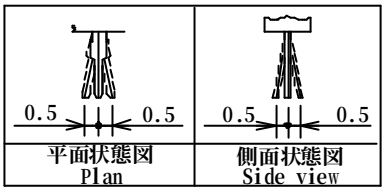
※2. The value is still tentative because of the underdevelopment parts.

4 Outline Drawings (LF2003)









端子の材質： Ｃｕ
Material of terminal:Cu
端子の処理：Ｎｉメッキ＋半田ディップ
Treatment of terminal: Ni plating+solder dip
製品質量 :約2.3ｇ
Weight : Approx. 2.3g

注記 Note
－－－ 部は高さ0.3maxのゲートバリ発生個所をしめす。
shows a point where 0.3max gate burr is produced.

図番 :
DWG.No. :

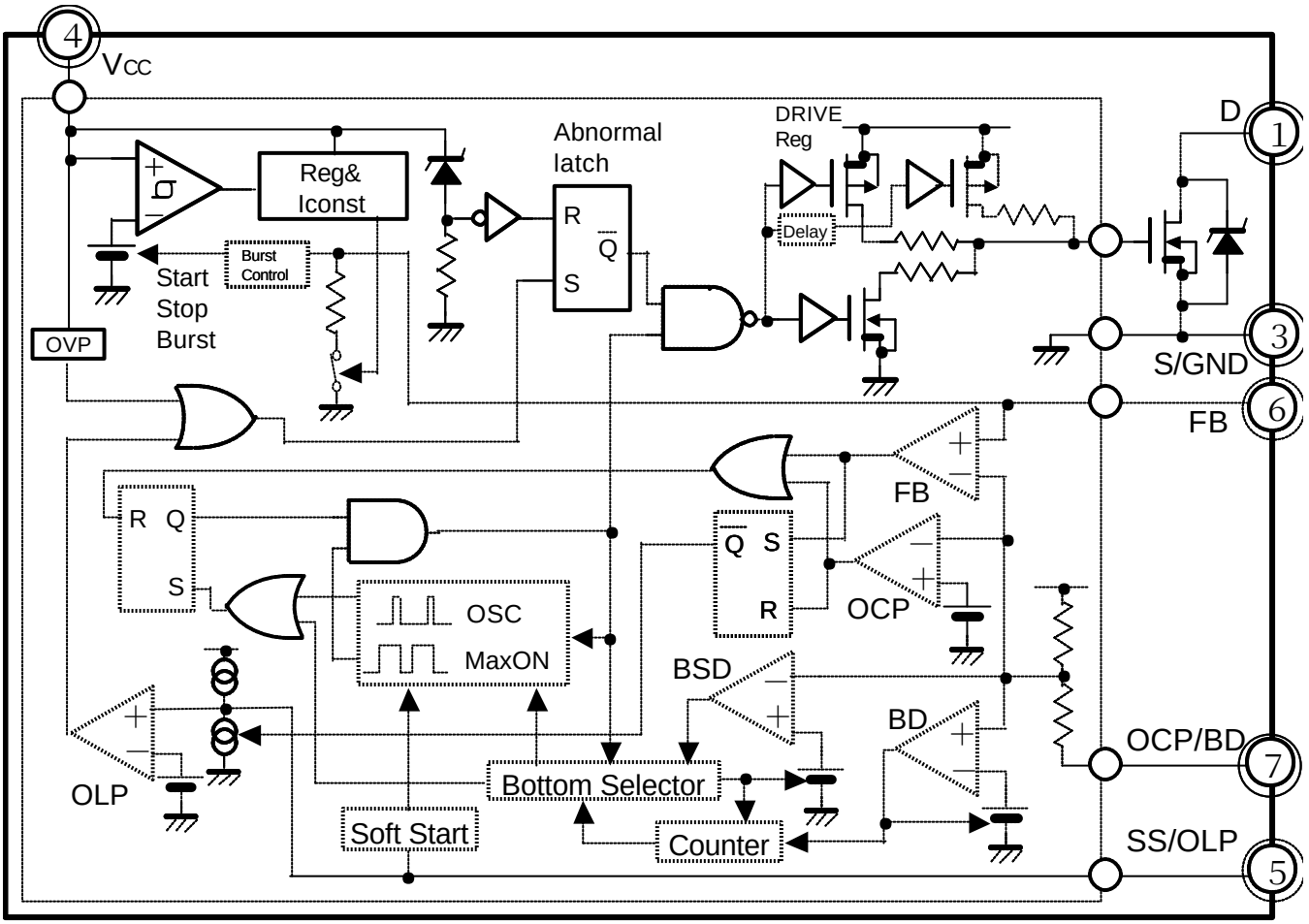
単位：mm
Dimensions in mm

a. 品名標示 W6700
Type Number

b. ロット番号
Lot Number
第１文字 西暦年号下一桁
1st letter The last digit of year
第２文字 製造月
2nd letter Month
１～９月 アラビア数字
１０月 O
１１月 N
１２月 D
(1 to 9 for Jan. to Sept.,
O for Oct. N for Nov. D for Dec.)
第３、４文字 製造日
3rd &4th letter Day
０１～３１ アラビア数字
Arabic numerals

※注：参考図です。詳細は、各製品仕様書を御参照下さい。

5 Block Diagram



Functions of Each Terminal

Terminal No.	Symbols		Terminal Descriptions	Functions
	STR-W6700 [TO220F-6L]	STR-X6700※1 [TO3PF-7L]		
1	D		Drain Terminal	MOSFET Drain
2	—※2	S	Source/Grand Terminal	MOSFET Source and Ground
3	S/GND	GND		
4	Vcc		Power Supply Terminal	Control Circuit Power Supply Input
5	SS/OLP		Delay at Overload/Soft-Start set up Terminal	Overload Protection and Soft-Start Operation Time set up
6	FB		Feedback Terminal	Constant Voltage Control Signal Input, Blocking Oscillation Control
7	OCP/BD		Overcurrent Protection Input/Bottom Detection Terminal	Overcurrent Detection Signal Input / Bottom Detection Signal Input

※1. STR-X6700 is a HIC which has a different package from STR-W6700.

※2. Terminated Pin (Refer to the Outline Drawings)

6 Electrical Characteristics (Example: STR-W6756)

6.1 Absolute Maximum Ratings (Ta＝25℃)

Parameters	Terminal	Symbols	Ratings	Units	Conditions
Drain Current	1 - 3	I_{Dpeak}※1		A	Single Pulse
Maximum Switching Current	1 - 3	I_{DMAX}※2		A	Ta=-20～+125℃
Avalanche Energy Capacity	1 - 3	E_{AS}※3		mJ	Single Pulse V_{DD}=99V,L=20mH I_L= A
Control Part Power Supply Voltage	4 - 3	V_{CC}	35	V	
SS/OLP Terminal Voltage	5 - 3	V_{OLPSS}	-0.5～6	V	
FB Terminal Inflow Current	6 - 3	I_{FB}	10	mA	※Under examination
FB Terminal Voltage	6 - 3	V_{FB}	-0.5～7.5	V	
OCP/BD Terminal Voltage	7 - 3	V_{OCPBD}	-1.5～5	V	
MOS FET part Permissive Loss	1 - 3	P_{D1}※4		W	With Indefinite Heat-sink
					Without Heat-sink
Control part Permissive Loss (MIC)	4 - 3	P_{D2}※5		W	Regulated at Vcc x Icc
Operational Internal Frame Temperature	—	T_F	−20～+125	℃	Refer to Recommended Operational Temperature
Operational Ambient Temperature	—	Top	−20～+125	℃	
Storage Temperature	—	Tstg	−40～+125	℃	
Channel Temperature	—	Tch	+150	℃	

※1. Refer to the MOSFET A.S.O. curve listed on the specification sheet.
※2. Maximum Switching Current listed on the specification sheet.
Maximum Switching Current represents Drain Current which is determined by IC internal drive voltage and MOSFET Vth.
※3. Refer to the MOSFET Tch-E_{AS} curve listed in the specification sheet.
※4. Refer to the MOSFET Ta – P_{D1} curve listed in the specification.
※5. Refer to the MIC TF-P_{D2} curve listed in the specification sheet.

6.2 Electrical Characteristics in Power MOS FET (Ta = 25℃)

Parameters	Terminal	Symbols	Ratings			Units	Conditions
			MIN	TYP	MAX		
Drain-Source Voltage ※7	1 - 3	V_{DSS}	650	—	—	V	※6
Drain Leakage Current	1 - 3	I_{DSS}	—	—	300	μA	
ON Resistance ※7	1 - 3	$R_{DS(ON)}$	—	—	0.73	Ω	
Switching Time	1 - 3	tf	—	—		Nsec	
Thermal Resistance ※7	—	θch-F	—	—		℃/W	Channel – Internal Frame

※6. Refer to the specifications of each product for the details.
※7. The ratings shall be different to each product. Refer to the specifications for the detail.

6.3 Electrical Characteristics (Ta = 25℃)

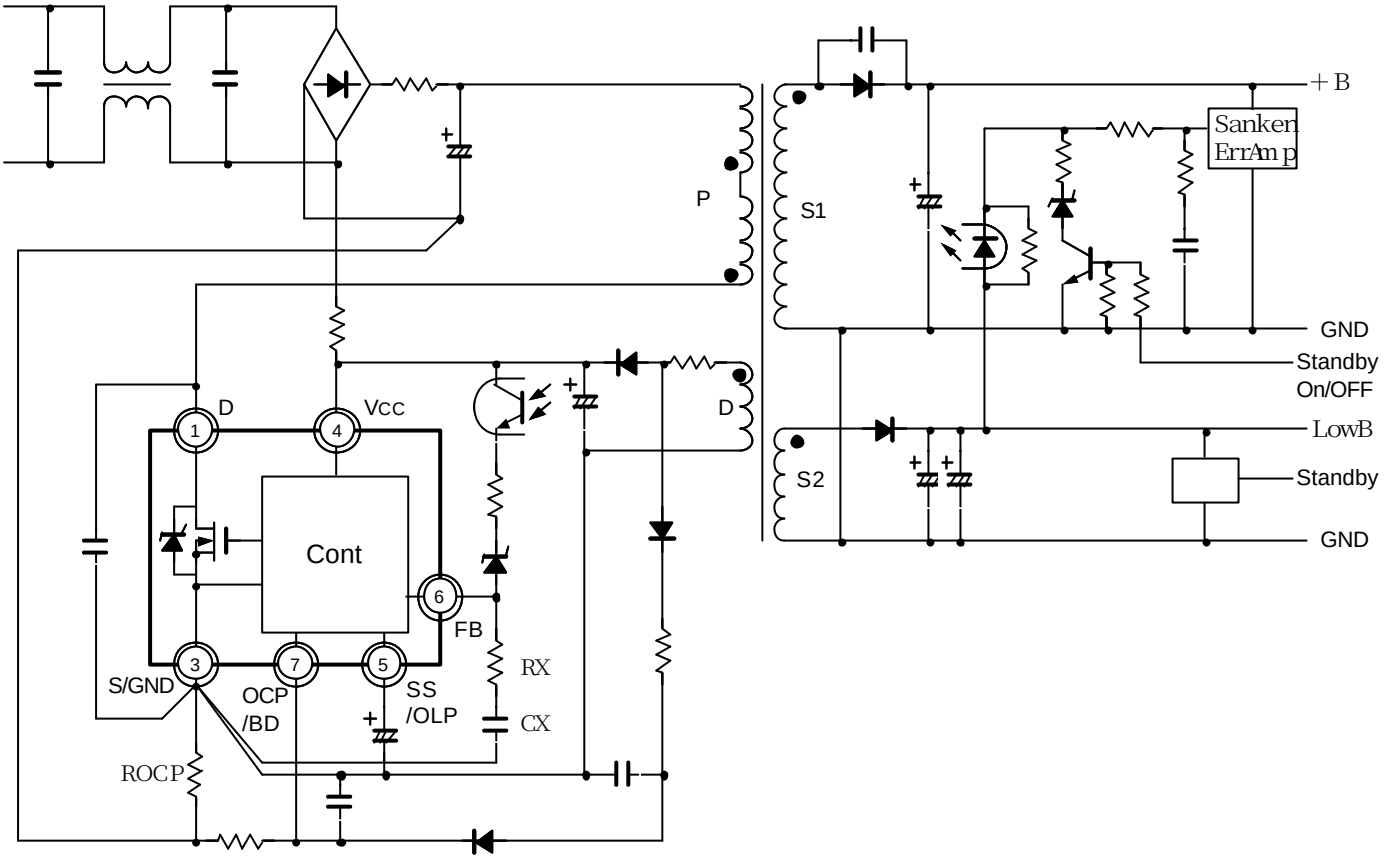
Parameters	Terminal	Symbols	Ratings			Units	Conditions
			MIN	TYP	MAX		
Power Supply Start-up Operation							※8
Operation Start-up Voltage	4 - 3	VCC(ON)		18.2		V	
Operation Stop Voltage	4 - 3	VCC(OFF)		9.6		V	
Operation Circuit Current	4 - 3	ICC(ON)	—	—	6	mA	
Non Operation Circuit Current	4 - 3	ICC(OFF)	—	—	100	μA	
Oscillation Frequency	1 - 3	fOSC		22		kHz	
Soft-Start Operation Stop Voltage	5 - 3	VSSOLP(SS)		1		V	
Soft-Start Operation Charging Current	5 - 3	ISSOLP(SS)		-450		μA	
Normal Operation							
Overcurrent Detection Threshold Voltage	7 - 3	VOCPBD(LIM)		-0.95		V	
Bottom-Skip Operation Threshold Voltage 1	7 - 3	VOCPBD(BS1)		-0.66		V	
Bottom-Skip Operation Threshold Voltage 2	7 - 3	VOCPBD(BS2)		-0.44		V	
OCP/BD Terminal Outflow Current	7 - 3	IOCPBD				μA	
Quasi-Resonant Operation Threshold Voltage 1	7 - 3	VOCPBD(TH1)		0.4		V	
Quasi-Resonant Operation Threshold Voltage 2	7 - 3	VOCPBD(TH2)		0.8		V	
Minimum Quasi-Resonant Signal Input Time	7 - 3	TOFF(MIN)	—	—	1	μsec	
FB Terminal Threshold Voltage	6 - 3	VFB(OFF)		1.5		V	
FB Terminal Inflow Current (Normal Operation)	6 - 3	IFB(ON)				mA	
Stand-by Operation							
Stand-by Operation Start-up Power Supply Voltage	4 - 3	VCC(S)		11.2		V	
Stand-by Power Supply Voltage Interval	4 - 3	VCC(SK)		1.5		V	
Stand-by Non-Operational Circuit Current	4 - 3	ICC(S)		30		μA	
FB Stand-by Operation Threshold Voltage	6 - 3	VFB(S)				V	
FB Terminal Inflow Current (Stand-by)	6 - 3	IFB(S)				μA	
Minimum ON Time	1 - 3	TON(MIN)		1		μsec	
Protection Operation							
Maximum ON Time	1 - 3	TON(MAX)		34		μS	
OLP Operation Threshold Voltage	5 - 3	VSSOLP(OLP)		5		V	
OLP Operation Charging Current	5 - 3	ISSOLP(OLP)		-10		μA	
Normal Operation Discharging Current	5 - 3	ISSOLP(NOR)		40		μA	
OLP Delay Time	1 - 3	TOLP				ms	
OVP Operational Voltage	4 - 3	VCC(OVP)		27.5		V	
Latch Circuit Holding Current ※10	4 - 3	ICC(H)	—	—	150	μA	
Latch Circuit Releasing Power Supply Voltage ※10	4 - 3	VCC(La.OFF)		7.3		V	

※8. Refer to the specifications for the details.

※9. The current rating is based on the HIC's standards, and plus(+) represents sink and minas(-) represents source.

※10. Latch circuit is the circuit operated by OVP and OLP.

7 Applicable Circuit (Example)



8 Functions of Each Terminal

8.1. Vcc Terminal (Pin 4)

8.1.1. Start-up Circuit

The start-up circuit detects Vcc terminal (No.4 pin) voltage, and makes a control IC start and stop. The power supply of the control IC (Vcc terminal input) employs a circuit as shown in Fig.1. At start-up, C3 is charged through a start-up resistor R2. The R2 value needs to be set more than the holding current of the latch circuit (150 μA Max), which is described later, to be flown at the minimum AC input.

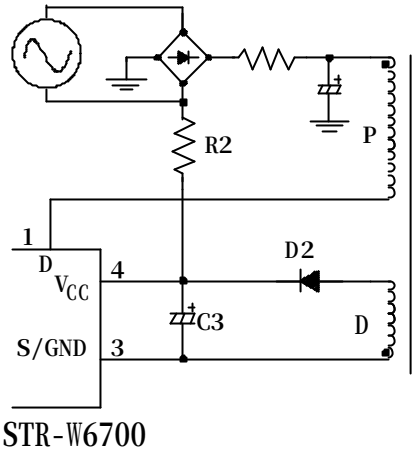


Fig.1. Start-up Circuit

However, where the R2 value is too high, the current charging to C3 shall be reduced after AC input. Consequently, it takes much time to reach the operation start-up voltage, so it is required to monitor the capacity of C3 that is mentioned later simultaneously. The Vcc terminal voltage falls immediately after the control circuit starts its operation; however the voltage drop is reduced by the increase of the C3 capacity. Therefore, even if the auxiliary drive winding voltage is delayed in rising, the Vcc terminal voltage does not fall up to the operation stop voltage to maintain the start-up operation. However, with larger capacity of C3, it takes much time, after AC input, to reach the operation start since the certain time is required to charge C3. In general, SMPS performs its operation properly with the value, C3 is 10 to 47 μF, R2 is 47k to 150k Ohm for 100V wide input, and 82K to 330K Ohm for 200V narrow input for its start up.

As shown in Fig.2, the circuit current which makes the control circuit start is regulated at **100 μA MAX** (Vcc = 15V, Ta = 25C), and higher value resister R2 is applicable to the circuit. Once the Vcc terminal voltage reaches 18.2V (TYP), the control circuit starts its operation by the **Start-up Circuit**, and current consumption shall be increased. Once the Vcc terminal voltage falls and it becomes lower than the operation stop voltage **9.6V (TYP)** with the decrease of the Vcc terminal voltage, **Under Voltage Lock Out (UVLO)** circuits stops the controlling operation and returns to the start-up mode.

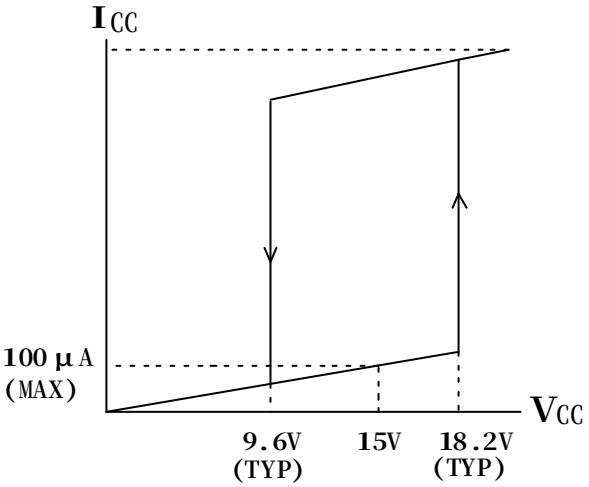


Fig.2. Vcc Terminal Vol. – Circuit Cur. Icc

8.1.2. Auxiliary/Drive Winding

After the control circuit starts its operation, the power supply is gained by rectifying and smoothing the voltage of the auxiliary winding D. Fig.3 shows the start-up voltage waveform of the Vcc Terminal. The auxiliary winding voltage does not rise up to the set voltage after the control circuit starts its operation, and the Vcc terminal voltage starts falling. However, because the operation stop voltage is set as low as **10.6V (Max)**, the auxiliary winding voltage D reaches stabilizing voltage before falling to the operation stop voltage, and the control circuit continues its operation.

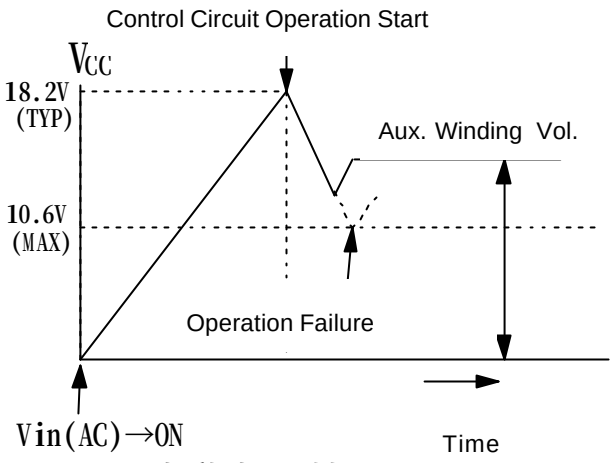


Fig.3. Waveform of VCC Terminal Vol. at Start-up

The auxiliary winding voltage, at the normal power supply operation, is to be set the number of windings for both the ends voltage of C3 to be higher than the operation stop voltage [Vcc(OFF) 10.6V(MAX)] and lower than the OVP operation voltage [Vcc(OVP) 25.5V(MIN)].

Besides, in an actual power supply circuit, the Vcc terminal voltage might be varied by the value of secondary output current as shown in Fig.4. This is caused by the small circuit current of STR-W6700 itself and C3 is charged up to the peak value by the surge voltage generated instantly after the MOSFET is turned OFF.

In order to prevent this, it is effective to add a resistor having several to several tens ohms (R7) in series to a rectifier diode as shown in Fig.5. The optimum value of the additional resistor should be determined in accordance with the specs of a transformer since the Vcc terminal voltage is varied by the structure difference of transformers.

Furthermore, the variation ratio of the Vcc terminal voltage becomes worse due to an inaccurate coupling between primary and secondary windings of the transformer (the coupling between the auxiliary winding D and the stabilizing output winding for the constant voltage control). Thus, for designing the transformer, the winding position of the auxiliary winding D needs to be studied carefully.

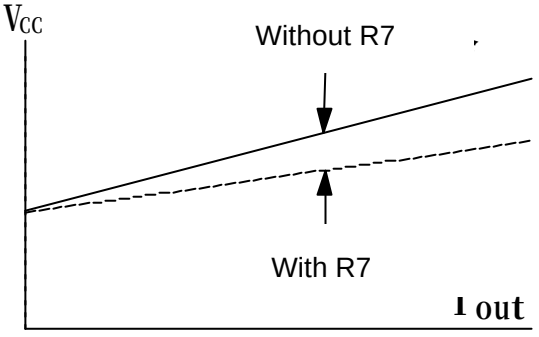


Fig.4. Output Current IOUT – VCC Terminal Vol.

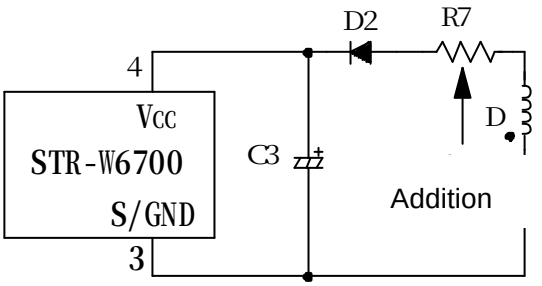


Fig.5. Auxiliary Power Supply Circuit not affected by Output Current IOUT

8.1.3. Overvoltage Protection Circuit

Where the voltage exceeding 27.5V(TYP) is imposed on between Vcc and GND terminals, the OVP circuit of the control IC starts its operation and turns latch-mode, and the control IC stops its oscillation. Generally, the Vcc terminal voltage is supplied from the auxiliary winding of the transformer, and the voltage is in proportion to the output voltage; thus, the circuit also operates at that time when the overvoltage output of the secondary side comes out such as the voltage detection circuit open.

The secondary output voltage at the Overvoltage Protection circuit operation is obtained form the following formula:

$$V_{OUT}(OVP) = \frac{V_{OUT} \text{ at Normal Operation}}{\text{Vcc Terminal Voltage at Normal Operation}} \times 27.5V\ (TYP) \quad \ldots\ldots (1)$$

8.1.4. Latch Circuit

The latch circuit is a circuit that holds the oscillator output low and stops the power supply circuit operation when OVP or OLP circuit operates. The holding current of the latch circuit is 150 μA MAX (Ta = 25C) when the Vcc terminal voltage is minus 0.3V to the operation stop.

In order to avoid improper operations caused by noises, etc., the delay-time is provided with a timer circuit incorporated in the HIC, and thereafter, the latch circuit starts its operation when OVP or OLP circuit operates for more than the set time. While, the Vcc terminal voltage drops even after the latch circuit starts its operation because the constant voltage (Reg) circuit of the control circuit continues its operation with higher circuit current.

Where the Vcc terminal voltage falls lower than the operation stop voltage (9.6V(TYP)), the voltage starts rising as the circuit current becomes lower than 150 μA (Ta = 25C). Where the Vcc terminal voltage reaches the operation start voltage (18.2V(TYP)), it falls as the circuit current is increased again. Consequently, the latch circuit prevents the Vcc terminal voltage from rising abnormally by controlling the voltage between 9.6V (TYP) and 18.2V(TYP). The Fig.6 indicates the voltage waveform when the latch circuit is under operation. The latch circuit operation is cancelled by reducing the Vcc terminal voltage below 7.3V (TYP), and generally, it is restarted by AC input switch-off of the power supply.

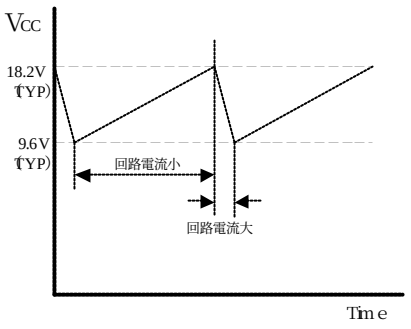


Fig.6. VCC Terminal Vol. Waveform at Latch-mode

8.2 SS/OLP Terminal (Pin 5)

The operation of SS/OLP terminal is classified as Soft-Start and Overload Protection, and the SS/OLP terminal is generally connected to a condenser having the value of 0.47μF to 3.3μF.

8.2.1. Soft-Start Operation at Start-up of Power Supply

At the power supply start-up, an external condenser is charged up to the threshold operating charging voltage ($V_{SSOLP(SS)}$) by the Soft-Start operating charging current ($I_{SSOLP(SS)}$) flowing from SS/OLP. The Soft-Start is provided at power supply start-up by utilizing the changing of SS/OLP terminal voltage from 0V to 1.0V. The timing chart of the Soft-Start is shown in Fig.7. Comparing the oscillation waveforms between OLP terminal voltage and the oscillation waveform of the internal control part, the Soft-Start widen the ON width. Besides, at the burst stand-by, the Soft-Start is operated every time; so, the magnetostriction noises from transformers are controlled with the increase of the drain current gradually.

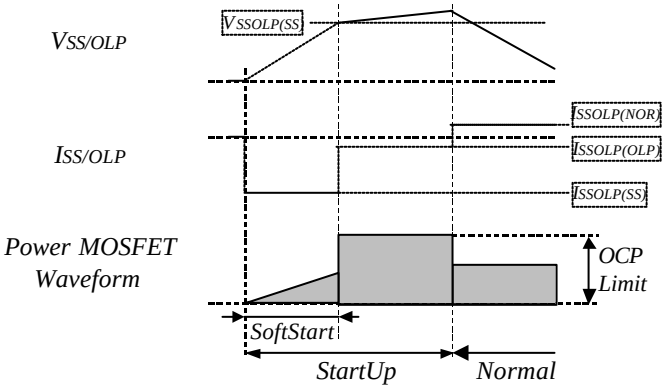


Fig.7. Soft-Start Operation

8.2.2. Overload Protection

The output characteristics of the secondary side at the time when the OCP circuit operates, due to the overload of the secondary side output, is shown in Fig.8. Where the output voltage falls below the overload mode, the auxiliary winding voltage of the primary side also falls proportionally, and the Vcc terminal voltage falls below shutdown voltage to stop the operation. In that case, as the circuit current is also decreased simultaneously, the Vcc terminal voltage rise again by the start-up resistor Rs 's charging current, and the circuit re-operates intermittently at the operation start-up voltage. However, where the transformer has lots of output windings and the coupling is not sufficient, and even if the output voltage is reduced in overload mode, the operation may not be intermittent because the primary side auxiliary winding voltage does not fall. Although the intermittent operation is not provided, the operation itself can be protected by the OLP circuit.

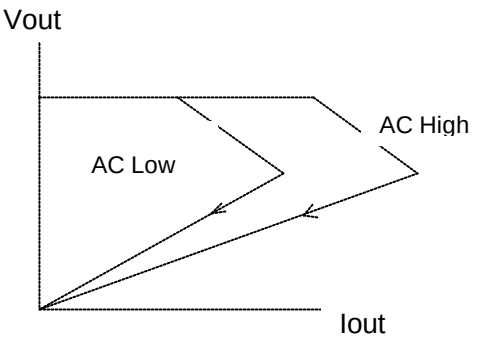


Fig.8. SMPS Output Overload Characteristics

In the overload mode (the mode in which the drain current is controlled by OCP operation), the secondary side output voltage falls. Thus, the error-amplifier and photo-coupler in secondary side need to be cut off. The STR-W6700 series recognizes the circumstances continuing OCP operation without FB signal as overload mode, and the SS/OLP terminal voltage starts rising by $I_{SSOLP(OLP)}$ as shown in Fig.9, and after the SS/OLP terminal voltage continues rising to reach $V_{SSOLP(OLP)}$ TYP 5V, the oscillation is stopped and turns the latch protection operation.

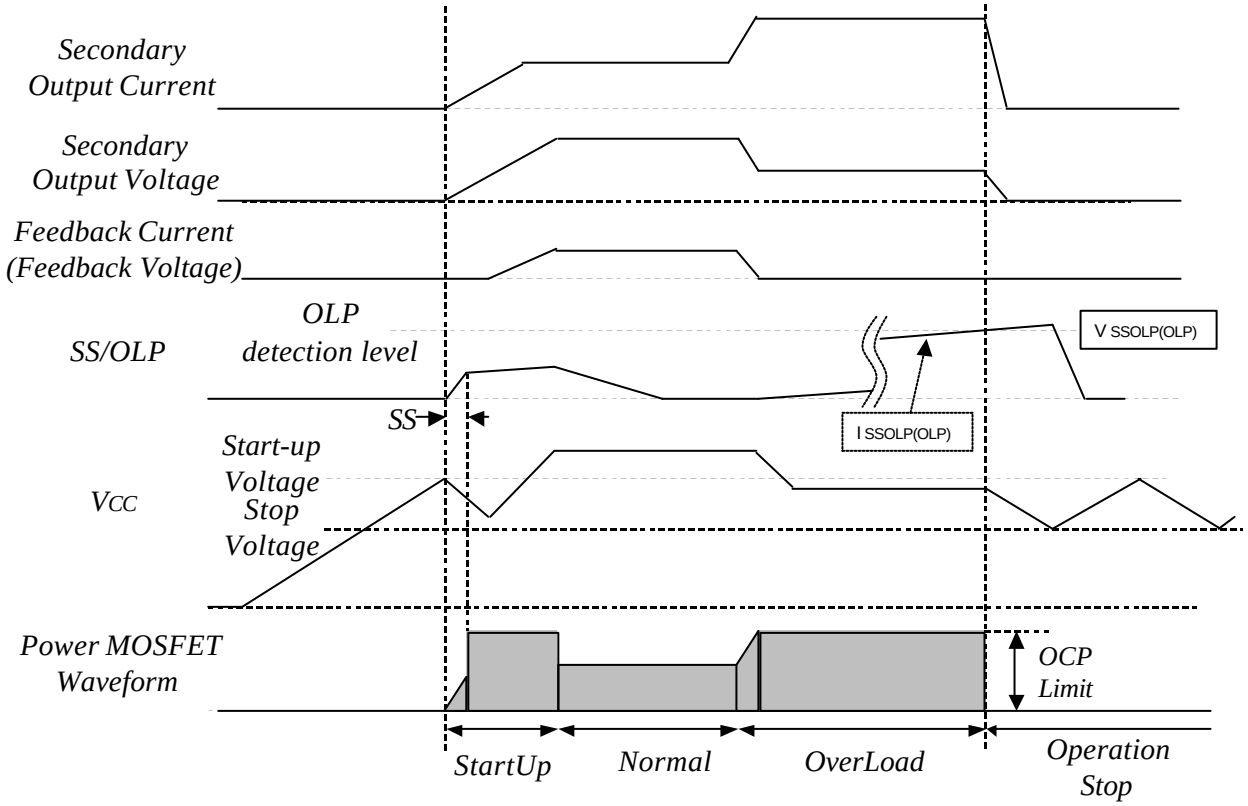


Fig.9. Timing-Chart at Overload

The time until the latch protection operation starts its operation can be calculated from the following formula since the $I_{SSOLP(OLP)}$ is a constant current circuit. That is,

C (Condenser Capacity) x ⊿V(Condenser Charging Voltage: approx. 5V) = $I_{SSOLP(OLP)}$ x t (time) …… (2)

While, the $I_{SSOLP(OLP)}$ contains the voltage dependent characteristics on SS/OLP terminal voltage, and $I_{SSOLP(OLP)}$ falls when SS/OLP terminal voltage rises. The actual value does not match to the value calculated from the formula (2) completely, so it is recommended to monitor the actual load conditions. Furthermore, the power supply start-up voltage turning OCP operation is also needed to confirm.

8.2.3. Operation at Power Supply OFF

The voltage of the condenser mounted externally to SS/OLP terminal is discharged by the internal reset circuit of the HIC at power OFF. The reset circuit does not start its operation at normal operation (i.e., while the internal constant voltage circuit operates).

8.2.4. Cancellation of OLP Circuit

The OLP operation is cancelled by inserting a resistor having 47K ohms (or Zener diodes) into SS/OLP terminal at start-up or overload maintaining Soft-Start operation effectively.

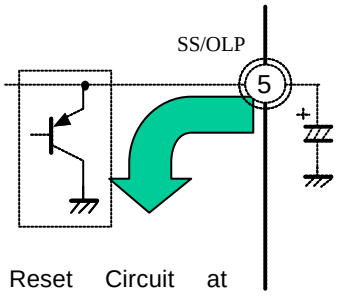


Fig.10. Reset Circuit

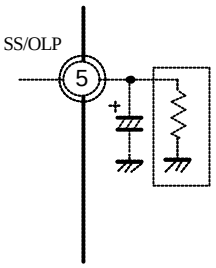


Fig.11. OLP Cancellation Circuit

8.3 FB Terminal (Pin. 6)

The operation of FB terminal is divided into normal (constant voltage control circuit operation) and stand-by operation control. Refer to item No. 8.6 for the controlling at stand-by operation.

8.3.1. Constant Voltage Control Circuit

The STR-W6700 series adopts the current mode controlling circuit for the constant voltage control, which proves its superiority in a heavy load. The MOSFET drain current peak value (ON time) is varied comparing FB terminal voltage and HIC's internal V_{OCPM}. During the OFF-time, Quasi-Resonant operation synchronized to the reset signal from a transformer is applied. While, where no reset signal is supplied from the transformer, the fixed oscillation frequency (approx. 22kHz) is applied by the HIC's internal oscillation circuit. The timing chart is shown in Fig.12, and the internal circuit diagram at the constant voltage control is shown in Fig. 13. respectively.

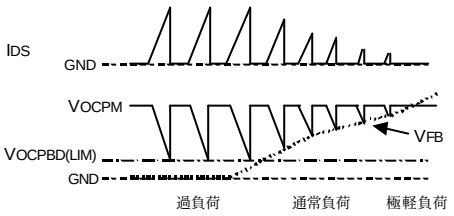


Fig.12. Constant Control Voltage

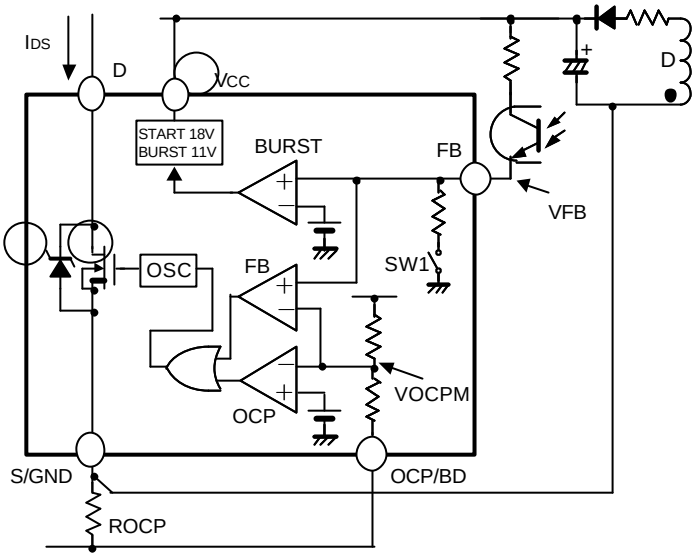


Fig.13. Constant Voltage Control Circuit (Theory)

The constant voltage controlling circuit makes the control signal (FB current) flowing from the secondary side error-amplifier input to No.6 terminal by the photo-coupler. The input FB current is transformed into Feedback voltage V_{FB} by the HIC internal resistor (SW1 is ON at normal). While, the reversed voltage waveform (V_{OCPM}) of the drain current waveform is input to the input terminal of the FB comparator. It is the current mode controlling circuit that controls the peak value of the drain current by the FB comparator.

The FB current shall be decreased to nil value at the overload in Fig.12. At that time, the drain current is controlled under the current value regulated by the Overcurrent Protection Circuit. At the transition period from the normal load to the lowest load in Fig.12, the drain current is decreased since the FB current increases and V_{FB} rises. Where the V_{FB} exceeds the FB terminal threshold voltage ($V_{FB(OFF)}$, 1.5V TYP) such as at the lowest load, the thinned-out oscillating operation starts and the HIC controls the secondary side output voltage so as not to raise the secondary side output voltage.

8.4 OCP/BD Terminal (Pin 7)

The functions of OCP/BD terminal are categorized as Overcurrent Protection (OCP), Bottom-Skip, and Quasi-Resonant Operation control. Refer to item No. 8.5 for Bottom-Skip and Quasi-Resonant operation.

8.4.1. Minus-Detection Type OCP Circuit

The OCP of the STR-W6700 series is pulse-by-pulse type Overcurrent protection circuit, which detects the peak value of the MOSFET drain current per pulse and reverses oscillator output. As shown in Fig.14, overcurrent detecting resistors, R5, R4, and C5 are mounted externally. R4 and C5 construct the filter circuit that prevents malfunctions caused by the surge current generating at the MOSFET Turn-ON. As the Overcurrent Protection Circuit operation (OCP), it turns OFF the MOSFET at that time when OCP/BD terminal threshold voltage reaches $V_{OCPBD(LIM)}$ by the voltage generated at the overcurrent detecting resistor R5 after the switching current flows at the MOSFET ON.

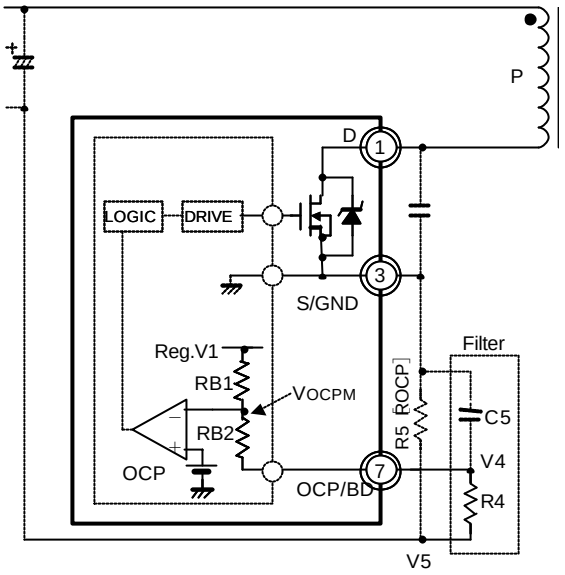


Fig.14. Minus-Detection OCP Circuit

The threshold voltage $V_{OCPBD(LIM)}$ of the OCP/BD terminal is set at –0.95V (Typ). The OCP circuit adopts the minus-detection circuit, which provides the detecting voltage V_{OCPM} in the MIC by dividing the voltage (between V1 and R5) with RB1, RB2, and R4. Since the RB1 and RB2 are resistors incorporated in the HIC, taking the distributions of RB1 and RB2 (regulated as b_{CPBD} in the specs) into consideration, the value of R4 is to be between 100 to 330 Ohms in order to lower the influence from the distributions between RB1 and RB2.

8.5 Quasi-Resonant and Bottom-Skip Operation

8.5.1. Quasi-Resonant Operation

The Quasi-Resonant operation is to match the timing of the MOSFET Turn-ON to the bottom point of the voltage resonant waveform after a transformer releases the energy (i.e., 1/2 cycle of the resonant-frequency).

As shown in Fig.15, the voltage resonant condenser C4 is connected between the drain and source, and the delay circuit, C10, D3, D4, and R9 are connected between the auxiliary winding D and OCP/BD terminal (Pin No.7). Where the MOSFET is turned OFF, the Quasi-Resonant signal is made of the fly-back voltage generated in the auxiliary winding, which operates BD comparator, and it provides the Quasi-Resonant operation. Due to the operation of the delay circuit, even if the energy of the transformer is released to complete, the Quasi-Resonant signal imposed on Pin No. 7 terminal does not fall immediately. This is why the C10 is discharged by R4, and after a certain period, the voltage falls to the threshold voltage $V_{OCPBD(TH1)}$ 0.4V and below. Consequently, the delay-time needs to be set by adjusting C10 monitoring the operating waveform in order to turn ON the MOSFET at that time when the V_{DS} of the MOSFET reaches the lowest point.

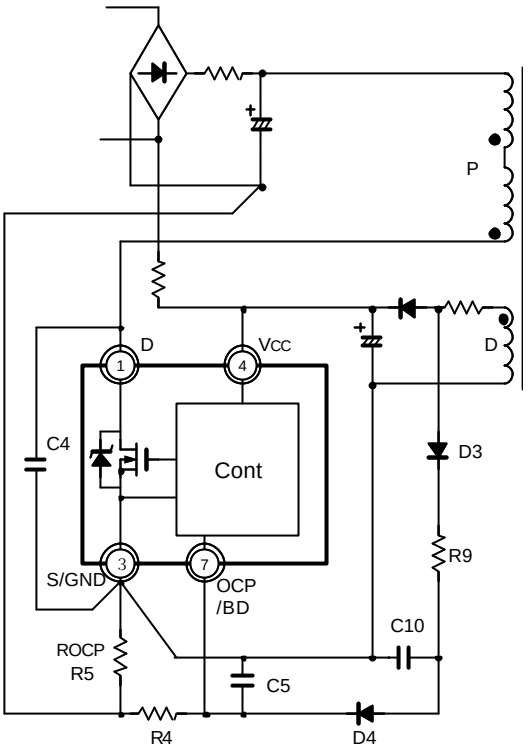


Fig.15. Quasi-Resonant and Delay Circuit

In addition to the Quasi-Resonant operation, in order to control the increase of the oscillating frequency at light to medium load, the Bottom-Skip operation widening OFF time is built-in in accordance with the load volumes. The switching timing between the Quasi-Resonant and Bottom-Skip operation is described in the item No. 8.5.2.

Where the Quasi-Resonant signal voltage imposed on OCP/BD terminal is below $V_{OCPBD(TH2)}$ 0.8V, the internal oscillator starts PWM operation with the fixed oscillating frequency (22kHz).

The PWM operation is also provided at power supply start-up or low auxiliary winding voltage such as winding-short, which lowers oscillating frequency, and the stress of the MOSFET is fairly reduced. After the Quasi-Resonant signal is over $V_{OCPBD(TH2)}$ 0.8V, the MOSFET remains OFF while $V_{OCPBD(TH1)}$ 0.4V and more is imposed on. That is, the gap between $V_{OCPBD(TH1)}$ and $V_{OCPBD(TH2)}$ prevents the HIC from operating improperly.

While, in the setting up R9 and R4, the Quasi-Resonant signal imposed on the OCP/BD terminal needs to be 5V or below since the OCP/BD terminal voltage is maximum 5V. At the normal condition, it should be 1.5V approximately.

8.5.2. Bottom-Skip Operation (Switching from Quasi-Resonant Operation)

The basic bottom-skip operation is that the load of the secondary side is detected by the drain current value (actually OCP/BD terminal voltage), which switches to the Quasi-Resonant (at heavy load) and the Bottom-Skip operation (at light load). The timing of distinguishing is made by taking the OCP/BD terminal voltage in at start-down of the MOSFET gate voltage of the HIC. Furthermore, the number of start-down (OCP/BD terminal voltage is under $V_{OCPBD(TH1)}$) is measured, which makes the MOSFET turn ON in accordance with the mode described above.

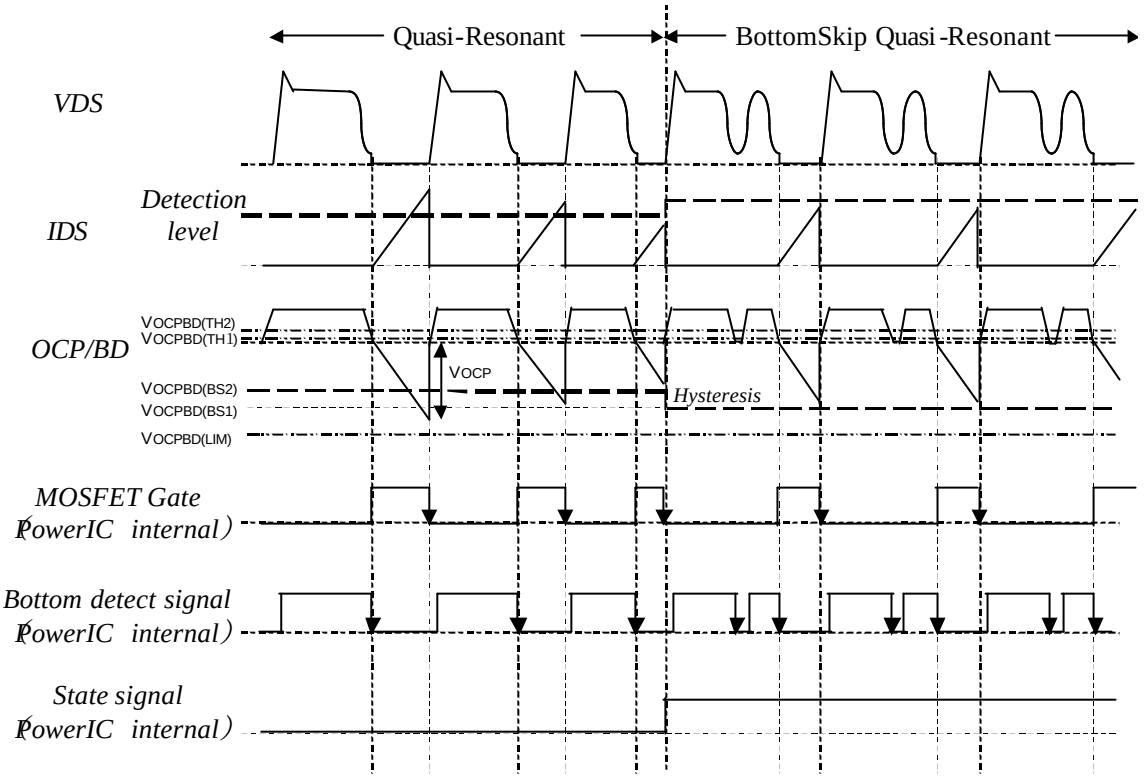


Fig.16. Bottom-Skip Quasi-Resonant Operation Timing Chart

1). Quasi-Resonant Operation ⇒ Bottom-Skip Operation

The Quasi-Resonant is operated under the mode that V_{OCP} is higher than $V_{OCPBD(BS2)}$ at the absolute rating. Where the load becomes lighter than that of the mode, the drain current falls. As the result, the mode is switched to the Bottom-Skip operation when the V_{OCP} becomes lower than $V_{OCPBD(BS2)}$ at the absolute rating, and the standard voltage is automatically changed to $V_{OCPBD(BS1)}$. Fig 16 shows the switching timing chart from the Quasi-Resonant to the Bottom-Skip operation.

2). Bottom-Skip Operation ⇒ Quasi-Resonant Operation

The Bottom-Skip is operated under the mode that V_{OCP} is lower than $V_{OCPBD(BS1)}$ at the absolute rating. Where the load becomes higher than that of the mode, the drain current rises. As the result, the mode is switched to the Quasi-Resonant operation when V_{OCP} becomes higher than $V_{OCPBD(BS1)}$ at the absolute rating, and the standard voltage is automatically changed to $V_{OCPBD(BS2)}$.

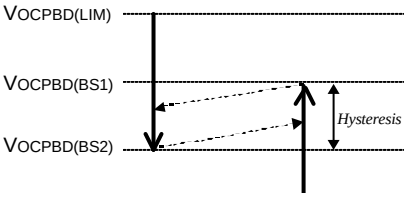


Fig.17. Operation Mode switching

Besides, the V_{OCP} is OCP/BD terminal voltage at that time when the MOSFET gate voltage starts down.

As described above, the standard voltage ($V_{OCPBD(BS1)}$, $V_{OCPBD(BS2)}$) realizing the Bottom-Skip operation provides the hysteresis operation automatically and makes it possible to have the stabilized operation. Fig.17 shows the above operation switching changing mode.

8.6 Stand-By Operation

The STR-W6700 series contains the burst-mode switching function to reduce the power dissipation at stand-by mode. At the stand-by with a remote controller, the switching mode is set in the secondary side, which makes the HIC switch to the burst-mode automatically by reducing the output voltage.

The transformer winding voltage falls reducing the output voltage by switching in the secondary side, and it reduces the primary side auxiliary winding voltage, which cuts off the power supply from the auxiliary winding to V_{CC} terminal (Pin No. 4), and the V_{CC} terminal voltage is reduced by the HIC's dissipation current itself. Where the V_{CC} terminal (Pin No.4) voltage reaches the operation stop power supply voltage (9.6V TYP), the HIC stops its operation, and the dissipation current of the HIC turns circuit current ($I_{CC(S)}$) at stand-by non-operation, and with the charging to the back-up condenser through a start-up resistor, the V_{CC} terminal voltage (Pin No.4) rises again, and the HIC starts its operation immediately after the V_{CC} terminal voltage reaches the operation start-up power supply voltage. Repeating the above cycles, the HIC has the power supply continue the burst-mode.

In order to reduce the transformer's magnetostriction noises at the burst-mode, by lowering the voltage gap between the operation start-up power supply voltage at the stand-by and the operation stop voltage, the operation frequency is increased and switched to the mode controlling the switching current as low as possible without increasing the loss at the start-up resistor.

This switching is made by detecting that the FB terminal voltage exceeds the FB stand-by operation threshold voltage $V_{FB(S)}$, and the operation voltage width of the V_{CC} terminal is determined as "the power supply voltage interval 1.5V(TYP) at stand-by" and the width is approximately one fifth compared to the normal operation.

In the transition period from the normal to stand-by operation, the output voltage continues falling because the HIC's oscillation is suspended by the feedback current. Thus, it is inevitable to secure the voltage exceeding the required output voltage of secondary side in the period until the HIC starts the stand-by operation.

Meanwhile, in the transition period from the stand-by to normal operation, the output voltage continues falling because the HIC's oscillation is suspended until the Vcc terminal voltage (Pin 4) reaches the operation start-up voltage 18V (TYP). Thus it is required to secure the voltage exceeding the required output voltage of secondary side.

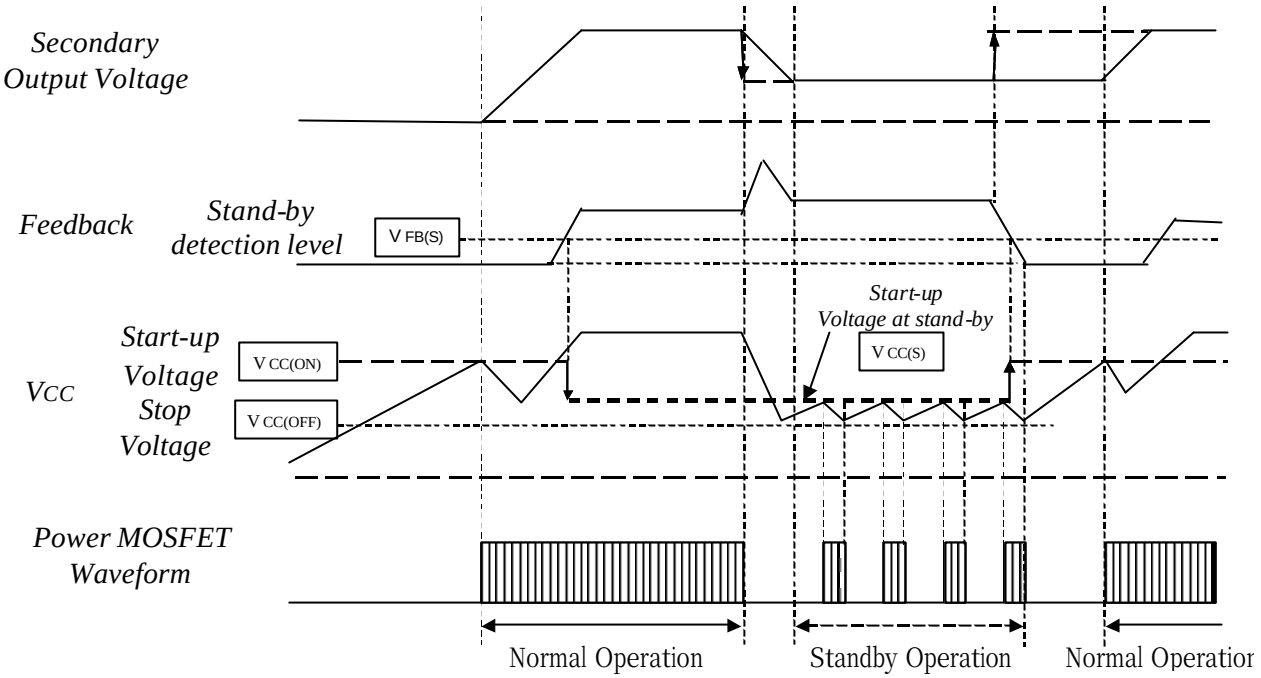


Fig.18. Timing-Chart at Operation Switching

At the stand-by mode, as mentioned above, due to the burst-mode of the HIC's intermittent operation, the output voltage falls since the HIC stops its operation during the oscillation stop period. While, during the stand-by operation, the intermittent operation repeating oscillation and stop through the start-up resistor is provided because the transformer's auxiliary winding voltage supplying the power supply to the HIC is extremely decreased. Accordingly, the load except stand-by load cannot be taken out at the stand-by operation (the period of intermittent operation). Where the load excluding the stand-by load is imposed on the transition period from the stand-by to normal operation, the incomplete start-up might be occurred. Thus, for the switching to the normal mode, it is required to have the sequence (no load at stand-by should be imposed on the normal mode), and the switching needs to be made after the power supply is completely turned to the normal mode.

8.7 Step-Drive Circuit

The STR-W6700 series reduces noises at Turn-ON by adopting the step-drive circuit for the MOSFET drive circuit as shown in Fig. 19. The drive current at Turn-ON is controlled at low by RG1 first, and it makes the gate voltage increase gradually, and the gate voltage is increased rapidly through RG1 + RG2 after 0.8µsec approximately. While, the MOSFET drive voltage adopts the constant voltage drive circuit maintained at V_{DRM}=7.6Vtyp, and it is not affected to V_{CC}. The MOSFET gate electric charge is discharged rapidly through RG3 when the MOSFET is turned OFF.

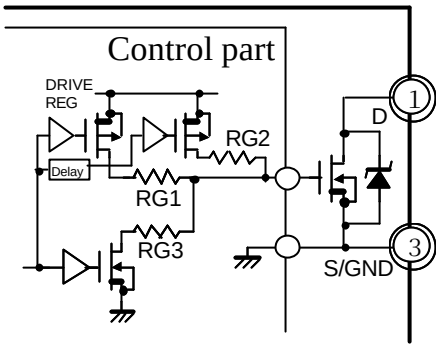


Fig.19. Step-Drive Circuit

That is, in the STR-W6700 series' drive circuit, the gate voltage imposed on the MOSFET is shifted with the two steps, which lowers the gate voltage at Turn ON and controls the surge current flowing at Turn ON, and provides the ideal drive circuit securing the sufficient gate voltage at normal drive mode.

8.8 Maximum ON Time Controlling Function

The MOSFET ON Time is controlled in the transition mode such as a low input voltage or AC input ON and OFF. The maximum ON Time is set at about 80% of the oscillation cycle (= 1/f_{OSC} approx. 45 µsec) and approximately 35 µsec (TYP). While, for the design of power supply, it is also required to monitor the MOSFET ON time at maximum load and input voltage minimum.

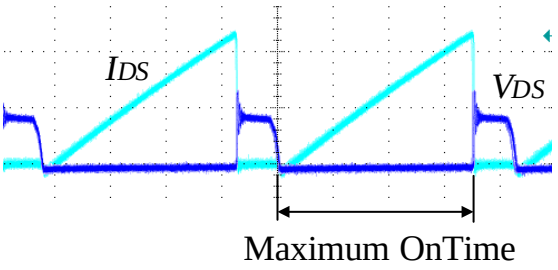


Fig.20. Maximum ON Time