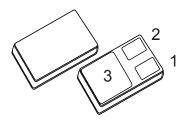
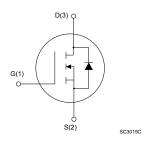


Rad-Hard 100 V, 6 A, N-channel Power MOSFET



SMD.5



Product status link

STRH8N10

Features

V _{DS}	I _D	R _{DS(on)} typ.	Q _g typ.
100 V	6 A	0.27 Ω	18.5 nC

- Fast switching
- 100 % avalanche tested
- · Hermetic package
- 50 krad TID
- SEE radiation hardened

Description

The STRH8N10 is a N-channel Power MOSFET able to operate under severe environment conditions and radiation exposure. It provides high reliability performance and immunity to the total ionizing dose (TID) and single event effects (SEE).

Qualified as per ESCC detail specification No. 5205/023 and available in SMD.5 hermetic package it is specifically recommended for space and harsh environment applications and suitable for in-Satellite power conversion, motor control and power switch circuits.

In case of discrepancies between this datasheet and the relevant agency specification, the latter takes precedence.

Device summary

Product summary					
Part numbers	Quality level	ESCC Part number	Package	Lead finish	Radiation level
STRH8N10S1	Engineering model	5205/022	CMD 5	Gold	-
STRH8N10SG	ESCC	5205/023	SMD.5		50 krad
STRH8N10ST	flight			Solder-dip	JU KIAU

Note: See Table 8 for ordering information.



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS} ⁽¹⁾	Drain-source voltage (V _{GS} = 0)	100	V
V _{GS} ⁽²⁾	Gate-source voltage	±20	V
I _D ⁽³⁾	Drain current (continuous)	6	Α
I _D	Drain current (continuous) at T _{amb} = 100 °C	4.1	Α
I _{DM} ⁽⁴⁾	Drain current (pulsed)	24	Α
P _{TOT}	Total dissipation at T _C = 25 °C	62.5	W
P _{TOT}	Total dissipation at T _a = 25 °C	2.4	W
dv/dt ⁽⁵⁾	Peak diode recovery voltage slope	6.4	V/ns
T _{op}	Operating temperature range	-55 to 150	°C
Tj	Max. operating junction temperature range	150	°C

- 1. This rating is guaranteed at $T_J \ge 25$ °C (see Figure 9. Normalized $V_{(BR)DSS}$ vs temperature).
- 2. This value is guaranteed over the full range of temperature.
- 3. Rated according to the $R_{thj\text{-case}} + R_{thc\text{-s.}}$
- 4. Pulse width limited by safe operating area.
- 5. $I_{SD} \le 6 \text{ A}$, $di/dt \le 1060 \text{ A/}\mu\text{s}$, $V_{DD} = 80 \% V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	2	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	52	°C/W

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2 Avalanche data

Table 3. Avalanche data

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive $ (\text{pulse width limited by } T_j \text{ max.}) $	4	Α
E _{AS} ⁽¹⁾	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	457	mJ
E _{AS}	Single pulse avalanche energy (starting T_j = 110 °C, I_D = I_{AR} , V_{DD} = 50 V)	134	1113
E _{AR}	Repetitive avalanche $(V_{DD} = 50 \text{ V}, I_{AR} = 4 \text{ A}, f = 100 \text{ KHz},$ $T_{J} = 25 ^{\circ}\text{C}, \text{ duty cycle} = 10 \%)$	4.3	ml
⊢AR	Repetitive avalanche $(V_{DD} = 50 \text{ V}, I_{AR} = 4 \text{ A}, f = 100 \text{ KHz},$ $T_J = 110 ^{\circ}\text{C}, \text{ duty cycle} = 10 ^{\circ}\text{M})$	1.4	- mJ

^{1.} Maximum rating value.

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3 Electrical characteristics

Table 4. Electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Max.	Unit				
		100 % V _{(BR)DSS}		1	mA				
I_{DSS}	Zero gate voltage drain current (V _{GS} = 0)	80 % V _{(BR)DSS}		10	μA				
	(vGS = 0)	80 % V _{(BR)DSS} , T _C = 125 °C		100	μA				
		V _{GS} = 20 V		100					
lana	Gate body leakage current,	V _{GS} = -20 V	-100		nA				
I _{GSS}	(V _{DS} = 0)	V _{GS} = 20 V, T _C = 125 °C	200	nA.					
		V _{GS} = -20 V, T _C = 125 °C	-200						
		$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	2	4.5					
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 1 mA, T _C = 125 °C	1.5	3.7	V				
		V _{DS} = V _{GS} , I _D = 1 mA, T _C = -55 °C	2.1	5.5					
Р	Otatia daria assura as assistante	V _{GS} = 12 V, I _D = 4 A		0.3	Ω				
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 12 V, I _D = 4 A, T _a = 125 °C		0.72					
C _{iss}	Input capacitance			791	pF				
C _{oss} (1)	Output capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	76	114	pF				
C _{rss}	Reverse transfer capacitance		31	47	pF				
Qg	Total gate charge		15	22	nC				
Q _{gs}	Gate-to-source charge	V _{DD} = 50 V, I _D = 4 A, V _{GS} = 12 V	2.5	4.5	nC				
Q_{gd}	Gate-to-drain ("Miller") charge		4.3	6.5	nC				
t _{d(on)}	Turn-on delay time		5	10					
t _r	Rise time	V = 50 V L = 4 A B = 4 7 O V = 40 V	2	9					
t _{d(off)}	Turn-off delay time	V_{DD} = 50 V, I_{D} = 4 A, R_{G} = 4.7 Ω , V_{GS} = 12 V		30	ns				
t _f	Fall time		2.5	7.5					
I _{SD}	Source-drain current			6	Α				
I _{SDM} ⁽²⁾	Source-drain current (pulsed)			24	Α				
V	Diada farmanda "	I _{SD} = 8 A, V _{GS} = 0 V		1.5	,,				
V_{SD}	Diode forward voltage	I _{SD} = 8 A, V _{GS} = 0 V, T _a = 125 °C		1.275	V				
t _{rr} ⁽¹⁾	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/ μ s, V_{DD} = 50 V, T_{j} = 25 °C	196	294	ns				

^{1.} Not tested in production, garanteed by process.

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^{2.} Pulse width limited by safe operating area.

^{3.} Pulsed: pulse duration = 300 µs, duty cycle ≤ 1.5%



4 Radiation characteristics

This products is guaranteed in radiation as per ESCC 5205/023 and ESCC 22900 specification at 50 krad. Each lot tested in radiation is accepted according to the characteristics as per Table 5.

4.1 Total dose radiation (TID) testing

The bias with V_{GS} = + 15 V and V_{DS} = 0 V is applied during irradiation exposure.

The parameters listed in Table 5 are measured:

- · Before irradiation
- After irradiation
- After 24 hrs at room temperature
- after 168 hrs at 100 °C anneal

Table 5. Post-irradiation electrical characteristics (T_{amb} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Drift values Δ	Unit	
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	80 % V _{(BR)DSS}	+1	μA	
la-a-	Gate body leakage current, (V _{DS} = 0)	V _{GS} = 20 V	1.5		
I _{GSS}	Gate body leakage culterit, (VDS = 0)	V _{GS} = -20 V	-1.5	nA	
V _{(BR)DSS}	Drain-to-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	-25%	V	
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$	-60% / +30%	V	
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 4 A	±10%	Ω	
V _{SD}	Diode forward voltage	I _{SD} = 8 A, V _{GS} = 0 V	±2%	V	

^{1.} Pulsed: pulse duration = 300 μs, duty cycle ≤ 1.5%

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4.2 Single event effect RBSOA

The STRH8N10 is extremely resistant to heavy ions exposure as per MIL-STD-750E, test method 1080, bias circuit of Figure 2.

SEB and SEGR tests are performed with a fluence of 3e+5 ions/cm² with the following acceptance criteria:

- SEB test: drain voltage checked, trigger level is set to VDS = 5 V. Stop condition: as soon as a SEB occurs or if the fluence reaches 3e+5 ions/cm².
- SEGR test: the gate current is monitored every 200 ms. A gate stress is performed before and after irradiation. Stop condition: as soon as the gate current reaches 100 nA (during irradiation or during PIGS test) or if the fluence reaches 3e+5 ions/cm².

Table 6. Single event effect (SEE), reverse biased safe operating area (RBSOA)

lon	Let (Mev/(mg/cm²)	Energy (MeV)	Range (µm)
Kr	32	768	94
Xe	60	1217	89

Figure 1. Single event effect, RBSOA

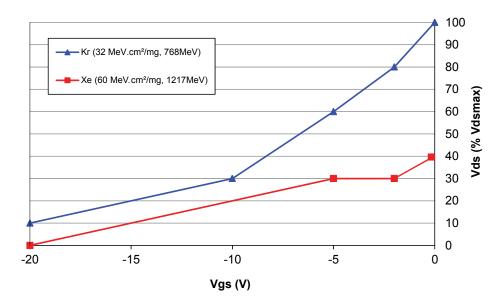
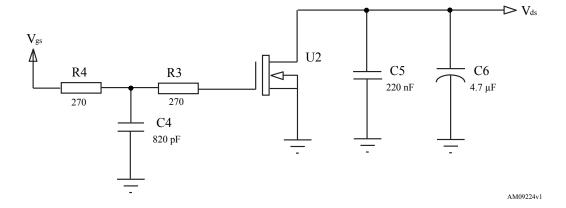


Figure 2. Single event effect, bias circuit



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5 Electrical characteristics (curves)

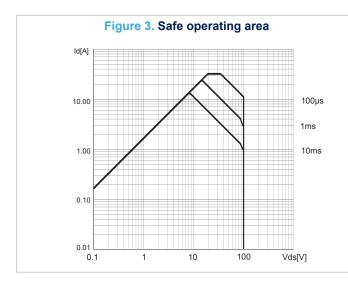


Figure 5. Output characteristics

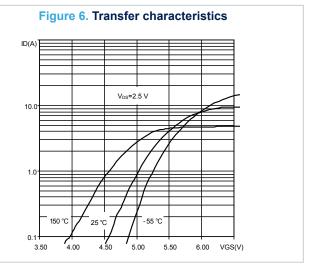
ID
(A)
VGS = 10 V

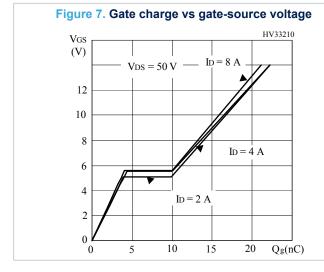
VGS = 7 V

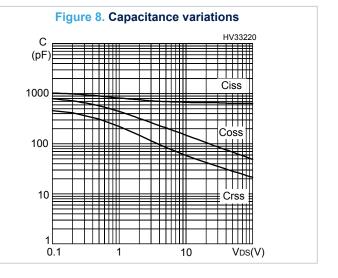
VGS = 6 V

VGS = 5 V

O
10
20
VDS(V)







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Figure 9. Normalized V_{(BR)DSS} vs temperature

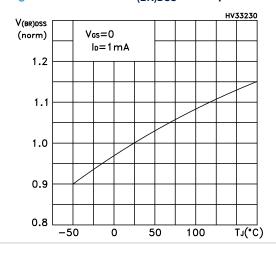


Figure 10. Static drain-source on-resistance

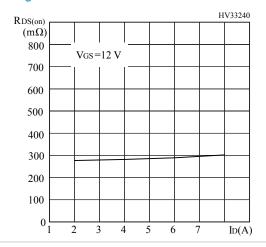


Figure 11. Normalized gate threshold voltage vs temperature

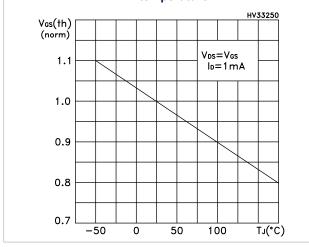


Figure 12. Normalized on-resistance vs temperature

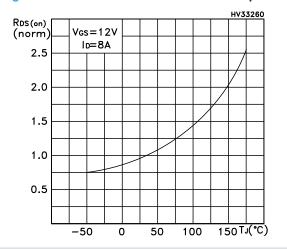
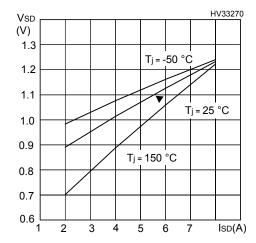


Figure 13. Source drain-diode forward characteristics

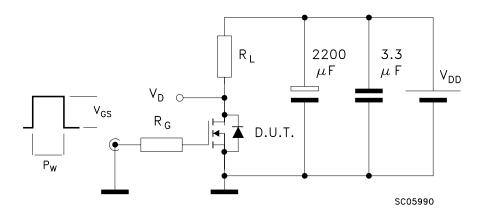


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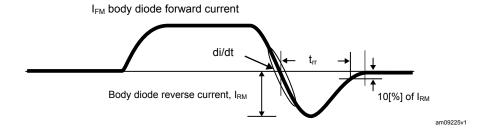
6 Test circuits

Figure 14. Switching times test circuit for resistive load



Note: $Max driver V_{GS} slope = 1 V/ns (no DUT)$

Figure 15. Source drain diode waveform



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7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 SMD.5 package information

Pin n° 1 identification ⊕ .014 (M) C A 2 pls b2 2 pls b3 2 pls D1 D b1 □.004 C > ← В ⊕ .014 M C A Bottom view Top view

Figure 16. SMD.5 package outline

7386434_REV7

Table 7. SMD.5 package mechanical data

Dim.		mm					
Diili.	Min.	Тур.	Max.				
A	2.84		3.30				
A1	0.25	0.38	0.51				
b	7.13	7.26	7.39				
b1	5.58	5.72	5.84				
b2	2.28	2.41	2.54				
b3	2.92	3.05	3.18				
D	10.03	10.16	10.28				
D1	0.76						
E	7.39	7.52	7.64				
е		1.91					

Note: The lid is not connected to any pin.

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8 Order codes

Table 8. Ordering information

Part number	Agency specification	Quality level	Radiation level	Package	Weight	Lead finish	Marking ⁽¹⁾	Packing
STRH8N10S1	-	Engineering model	-	CMD 5	4 -	Gold	STRH8N10S1	Chuin nach
STRH8N10SG	5205/023/01	ESCC	50 krad	SMD.5	1 g		520502301F	Strip pack
STRH8N10ST	5205/023/02	flight	50 KIAU			Solder-dip	520502302F	

Specific marking only. The full marking includes in addition: For the Engineering Models: ST logo, date code; country of origin (FR). For ESCC flight parts: STlogo, date code, country of origin (FR), ESA logo, serial number of the part within the assembly lot.

Contact ST sales office for information about specific conditions for products in die form.

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9 Other information

Table 9. Traceability and documentation

Screening type	Date code ⁽¹⁾	Radiation level	Documentation
Engineering model	3yywwN	-	Certificate of conformance
Flight model	yywwN	50 krad	Certificate of conformance ESCC qualification maintenance lot reference Radiation verification test (RVT) report at 10 / 20 / 30 / 50 krad at 0.1 rad / s.

^{1.} yy = year, ww = week number, N = lot index in the week.

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Revision history

Table 10. Document revision history

Date	Revision	Changes
20-May-2011	1	First release.
09-Nov-2011	2	Updated dynamic values on Table 6: Dynamic, Table 7: Switching times.
03-Jun-2013	3	Added new package and mechanical data: SMD.5 Removed TO-39 package.
16-Dec-2013	4	Updated Description Minor text changes
09-Apr-2014	5	Document status promoted from preliminary data to production data Modified: Figure 2. Minor text changes.
26-May-2014	6	Updated Figure 1.
04-Mar-2016	7	Updated: Features, Table 5, Table 6, Table 9, Table 10, Table 11 and Table 15. Updated Section 6: Package information. Minor text changes.
10-Feb-2017	8	Updated Table 6: Dynamic and Table 8: Source drain diode.
04-Oct-2021	9	Updated Description. Minor text changes.
19-May-2022	10	Updated Table 4, Figure 15 and Section 9 Other information.
18-Jan-2024	11	Updated Table 4. Electrical characteristics (T _{amb} = 25 °C unless otherwise specified). Minor text changes.

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