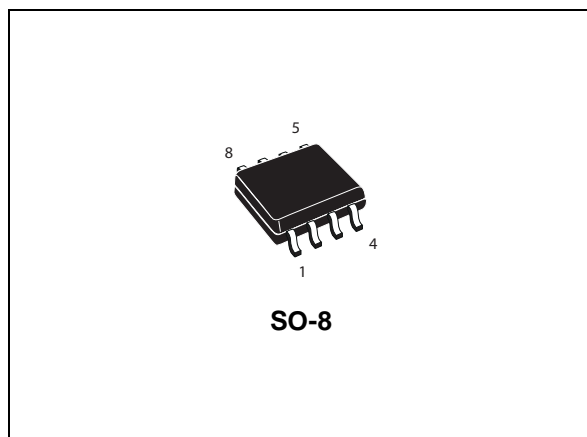
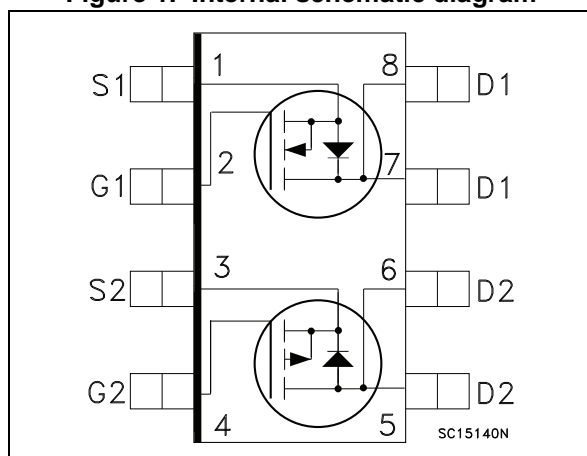


N-channel 30 V, 0.018  $\Omega$  typ., 8 A, P-channel 30 V, 0.045  $\Omega$  typ., 5 A  
Power MOSFET in a SO-8 package

Datasheet - production data



**Figure 1. Internal schematic diagram**



## Features

Order code	Channel	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STS8C5H30L	N	30 V	0.022 $\Omega$	8 A
	P		0.055 $\Omega$	5 A

- Conduction losses reduced
- Switching losses reduced
- Low threshold drive
- Standard outline for easy automated surface mount assembly

## Applications

- Switching applications

## Description

This device is a complementary N-channel and P-channel Power MOSFET developed using STripFET™ II (P-channel) and STripFET™ V (N-channel) technologies. The resulting transistors show extremely high packing density for low on-resistance and rugged avalanche characteristics.

**Table 1. Device summary**

Order code	Marking	Packages	Packaging
STS8C5H30L	8C5H30L	SO-8	Tape and reel

Contents

1      **Electrical ratings** ..... 3

2      **Electrical characteristics** ..... 4

      2.1    Electrical characteristics (curves) ..... 7

3      **Test circuits** ..... 11

4      **Package mechanical data** ..... 12

5      **Packaging mechanical data** ..... 15

6      **Revision history** ..... 17



# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		N-channel	P-channel	
$V_{DS}$	Drain-source voltage	30		V
$V_{GS}$	Gate- source voltage	±16	±16	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$ single operating	8	5.4	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$ single operating	6.4	4.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	32	21.6	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$ dual operating	1.6		W
	Total dissipation at $T_C = 25^\circ\text{C}$ single operating	2		W
$T_{stg}$	Storage temperature	-55 to 150		°C
$T_j$	Operating junction temperature	150		°C

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-a}^{(1)}$	Thermal resistance junction-ambient single operating	62.5	°C/W
$R_{thj-a}^{(1)}$	Thermal resistance junction-ambient dual operating	78	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10$  sec

**Note:** For the p-channel MOSFET actual polarity of voltages and current has to be reversed

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$	N	30			V
			P	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 30\text{ V}$	N			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 30\text{ V}, T_C = 125\text{ }^{\circ}\text{C}$	P			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 16\text{ V}$	N			$\pm 100$	nA
		$V_{DS} = 0, V_{GS} = \pm 16\text{ V}$	P			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N	1	1.6	2.5	V
			P	1	1.6	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 4\text{ A}$	N		0.018	0.022	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$	P		0.045	0.055	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$	N		0.020	0.025	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 2.5\text{ A}$	P		0.070	0.075	$\Omega$

Table 5. Dynamic

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit		
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 4\text{ A}$	N	-	8.5		S		
		$V_{DS} = 15\text{ V}, I_D = 2.5\text{ A}$	P	-	10		S		
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 25\text{ V},$ $f = 1\text{ MHz}$	N	-	857		pF		
			P	-	1350		pF		
$C_{oss}$	Output capacitance		N	-	147		pF		
			P	-	490		pF		
$C_{rss}$	Reverse transfer capacitance		N	-	20		pF		
			P	-	130		pF		
$Q_g$	Total gate charge		N-channel $V_{DD} = 24\text{ V}$ $I_D = 8\text{ A}$ $V_{GS} = 5\text{ V}$ P-channel $V_{DD} = 24\text{ V}$ $I_D = 4\text{ A}$ $V_{GS} = 5\text{ V}$ <i>(see Figure 27)</i>	N	-	7	10	nC	
				P	-	12.5	16	nC	
$Q_{gs}$	Gate-source charge			N	-	2.5		nC	
				P	-	5		nC	
$Q_{gd}$	Gate-drain charge			N	-	2.3		nC	
				P	-	3		nC	

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5.

For the p-channel MOSFET actual polarity of voltages and current has to be reversed

Table 6. Switching times

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	N-channel $V_{DD} = 15\text{ V}$ , $I_D = 4\text{ A}$ $R_G=4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ P-channel $V_{DD} = 15\text{ V}$ , $I_D = 2\text{ A}$ $R_G=4.7\ \Omega$ , $V_{GS} = 4.5\text{ V}$ <i>Figure 26</i>	N	-	12	-	ns
			P	-	25	-	ns
$t_r$	Rise time		N	-	14.5	-	ns
			P	-	35	-	ns
$t_{d(off)}$	Turn-off delay time		N	-	23	-	ns
			P	-	125	-	ns
$t_f$	Fall time		N	-	8	-	ns
			P	-	35	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Channel	Min.	Typ.	Max.	Unit	
I <sub>SD</sub>	Source-drain current		N	-		8	A	
			P	-		5	A	
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		N	-		32	A	
			P	-		20	A	
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage		I <sub>SD</sub> = 8 A, V <sub>GS</sub> = 0	N	-		1.5	V
			I <sub>SD</sub> = 5 A, V <sub>GS</sub> = 0	P	-		1.2	V
t <sub>rr</sub>	Reverse recovery time		N-channel	N	-	15		ns
			I <sub>SD</sub> = 8 A, di/dt = 100 A/μs	P	-	45		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> =15 V, T <sub>j</sub> =150 °C	N	-	5.7		nC	
		P-channel	P	-	36		nC	
I <sub>RRM</sub>	Reverse recovery current	I <sub>SD</sub> = 5 A, di/dt = 100 A/μs	N	-	0.76		A	
		V <sub>DD</sub> =15 V, T <sub>j</sub> =150 °C <i>Figure 28</i>	P	-	1.6		A	

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu$ s, duty cycle 1.5%

*Note:* For the p-channel MOSFET actual polarity of voltages and current has to be reversed

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area n-ch

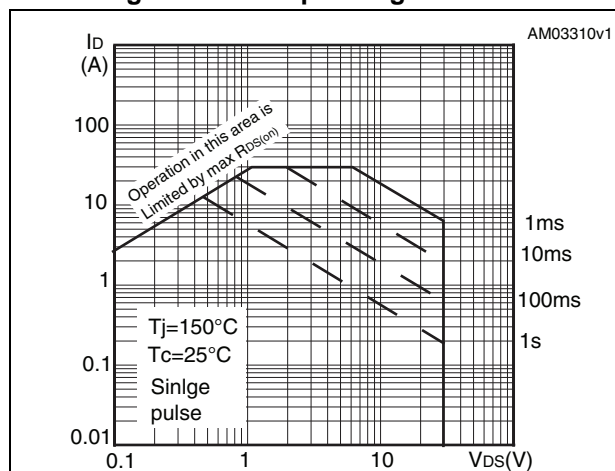


Figure 3. Thermal impedance n-ch

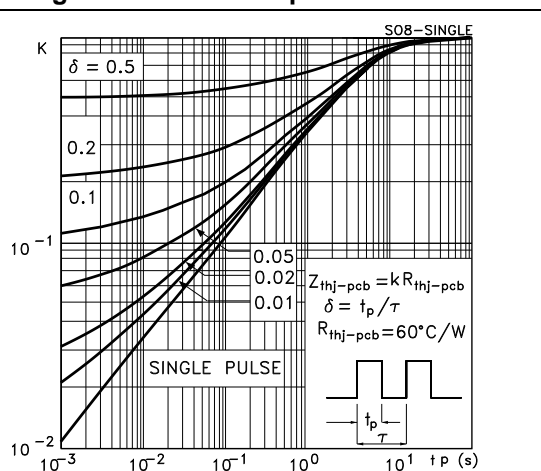


Figure 4. Output characteristics n-ch

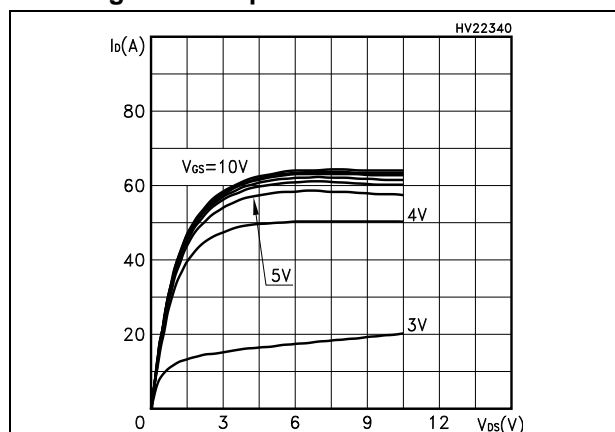


Figure 5. Transfer characteristics n-ch

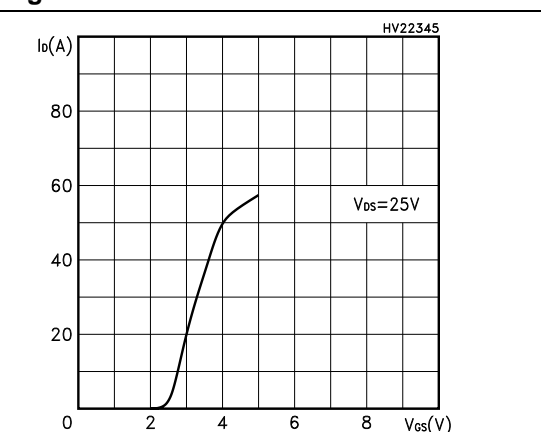


Figure 6. Transconductance n-ch

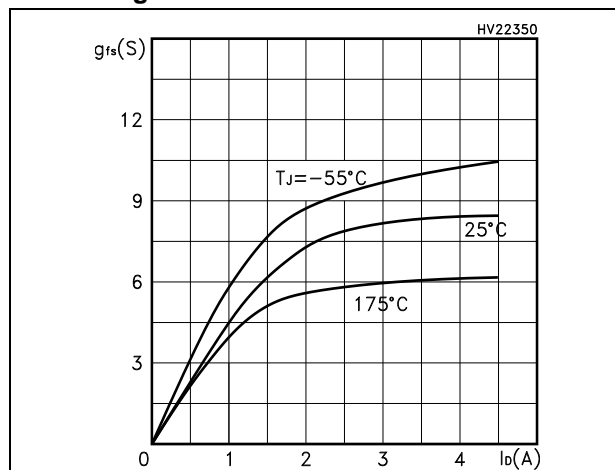


Figure 7. Static drain-source on resistance n-ch

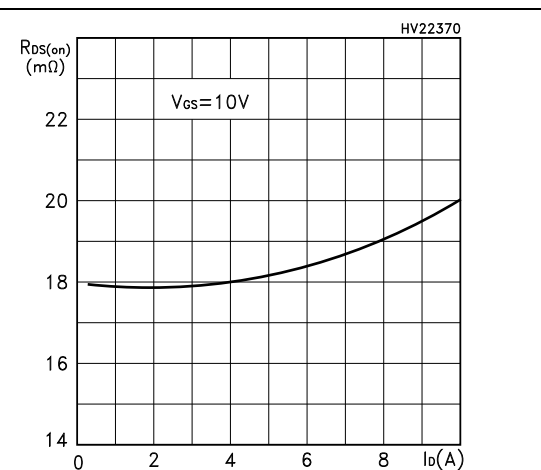


Figure 8. Gate charge vs. gate-source voltage  
n-ch

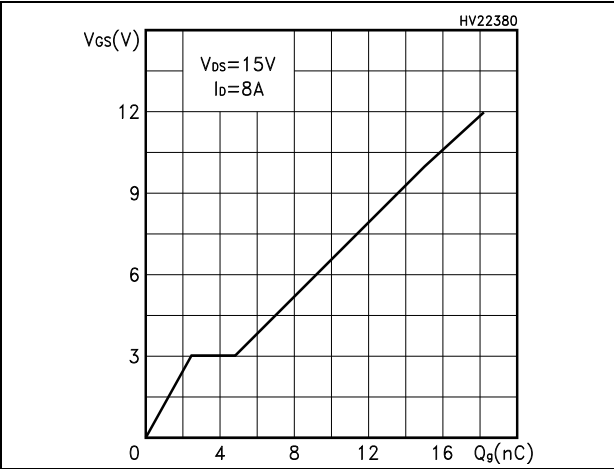


Figure 9. Capacitance variations n-ch

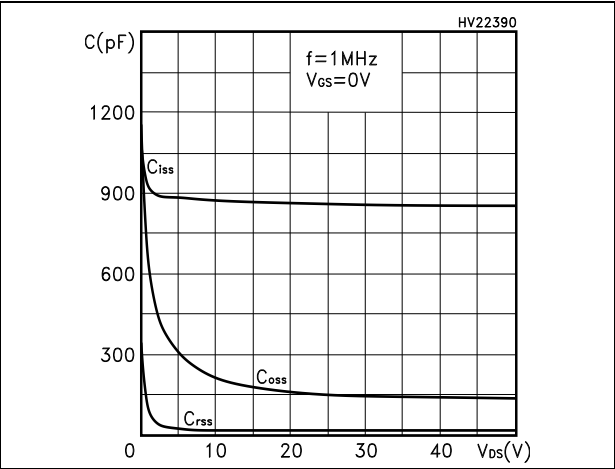


Figure 10. Normalized gate threshold voltage  
vs. temperature n-ch

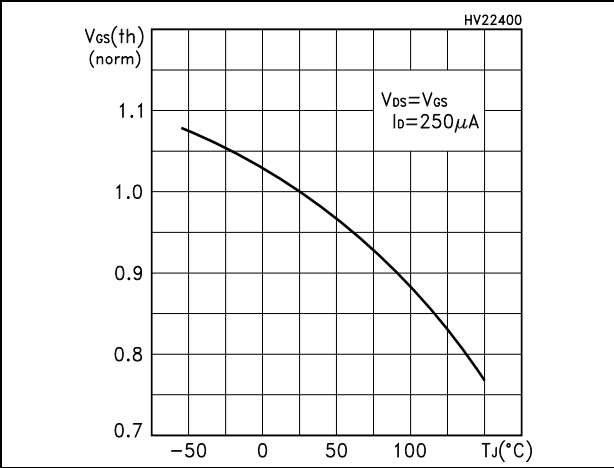


Figure 11. Normalized on resistance vs.  
temperature n-ch

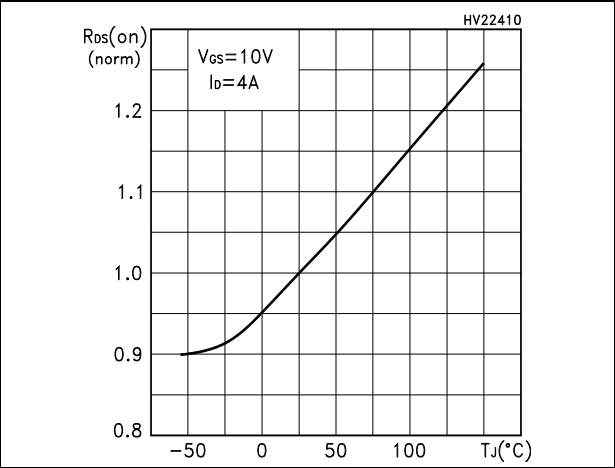


Figure 12. Source-drain diode forward  
characteristics n-ch

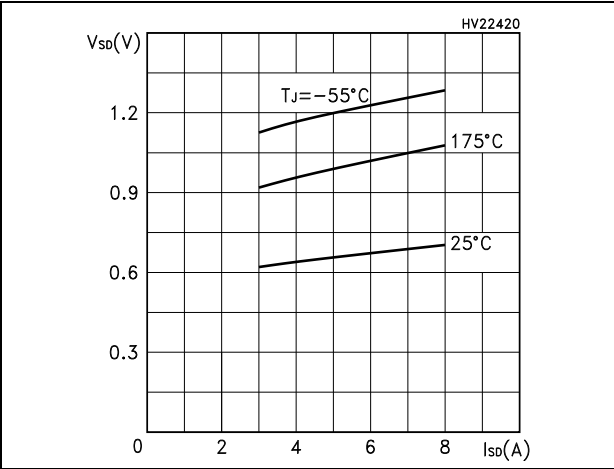


Figure 13. Normalized breakdown voltage vs.  
temperature n-ch

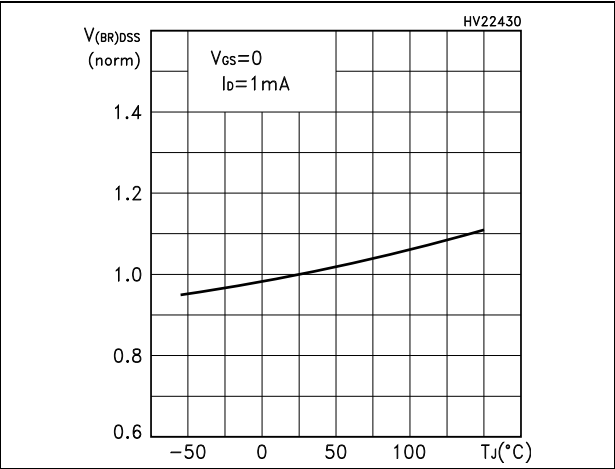




Figure 14. Safe operating area p-ch

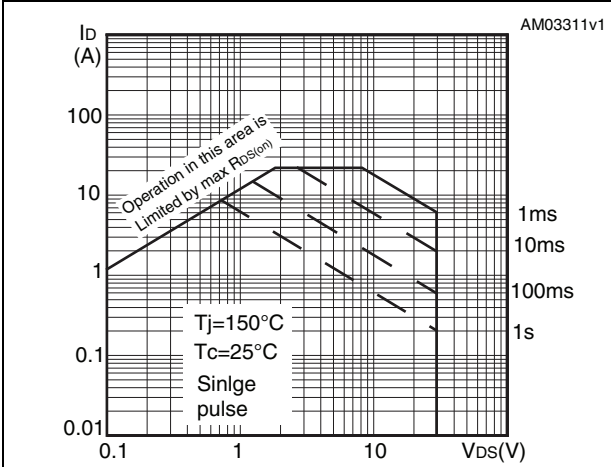


Figure 15. Thermal impedance p-ch

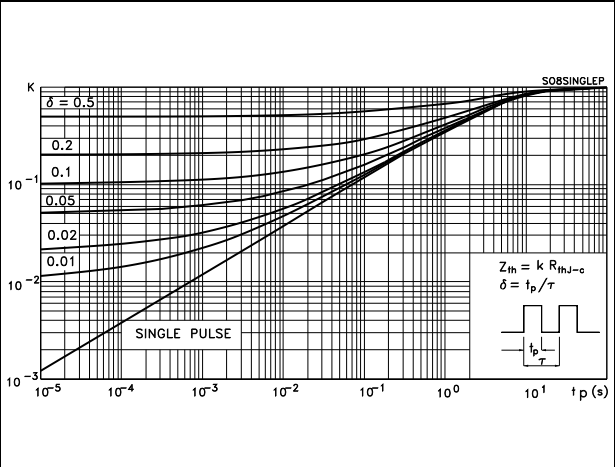


Figure 16. Output characteristics p-ch

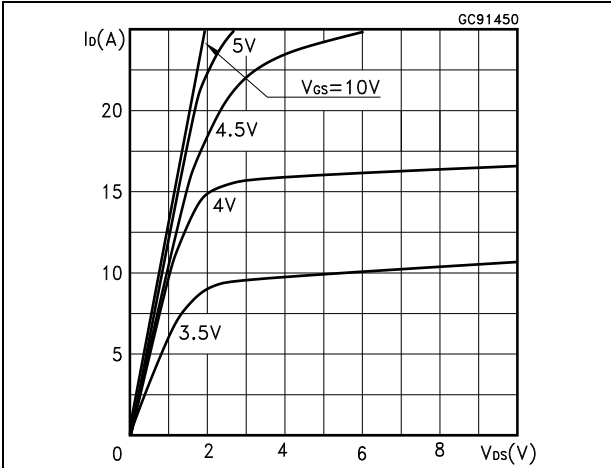


Figure 17. Transfer characteristics p-ch

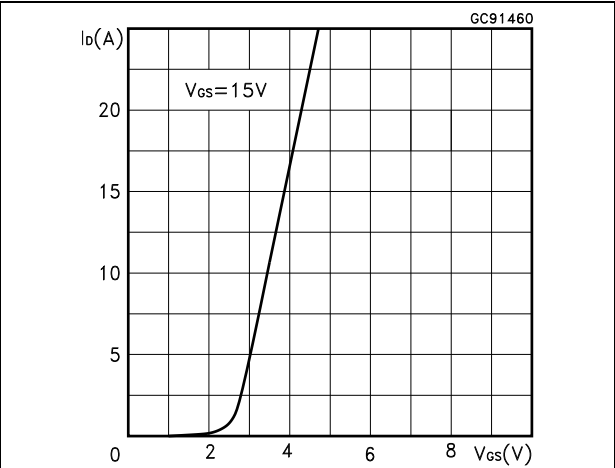


Figure 18. Transconductance p-ch

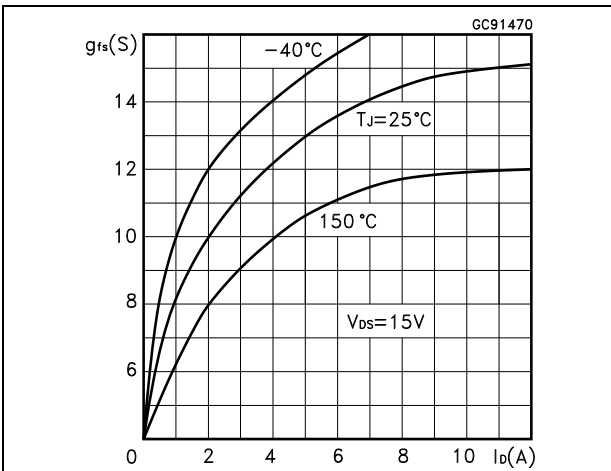


Figure 19. Static drain-source on resistance p-ch

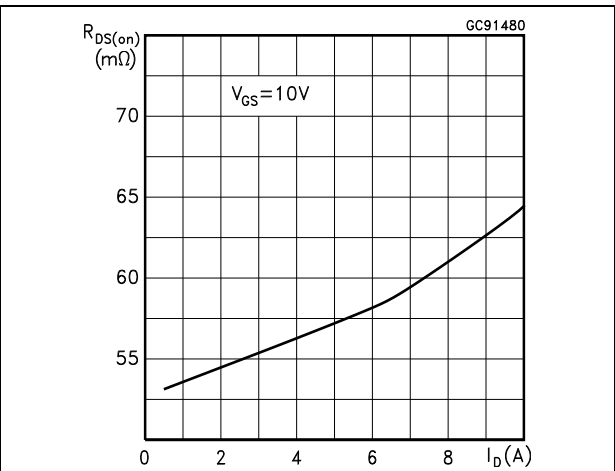


Figure 20. Gate charge vs. gate-source voltage  
p-ch

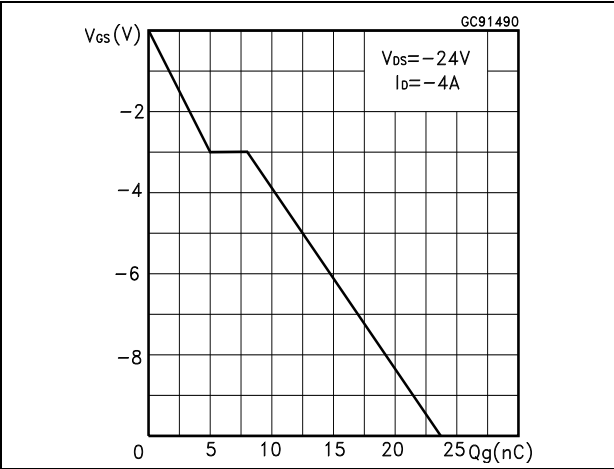


Figure 21. Capacitance variations p-ch

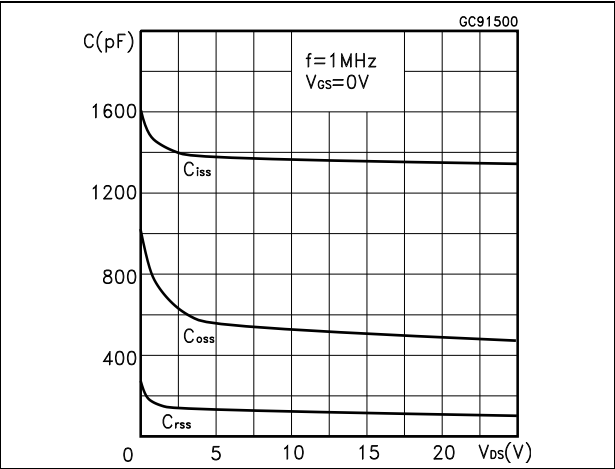


Figure 22. Normalized gate threshold voltage  
vs. temperature p-ch

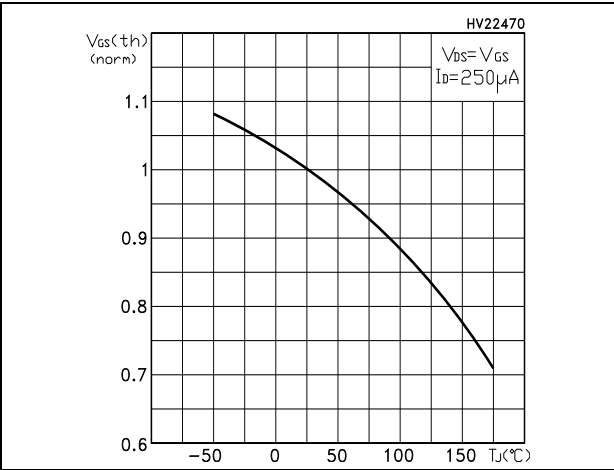


Figure 23. Normalized on resistance vs.  
temperature p-ch

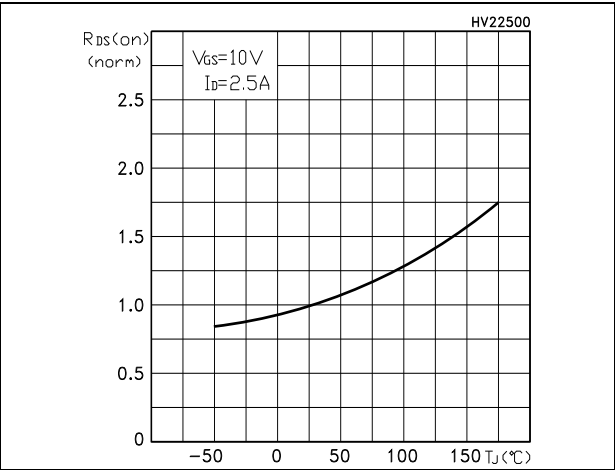


Figure 24. Source-drain diode forward  
characteristics p-ch

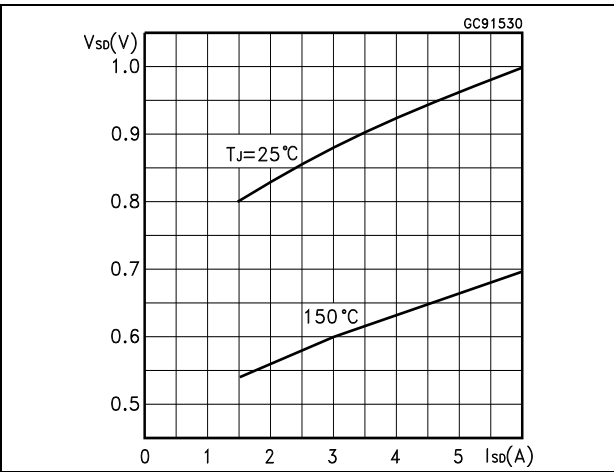
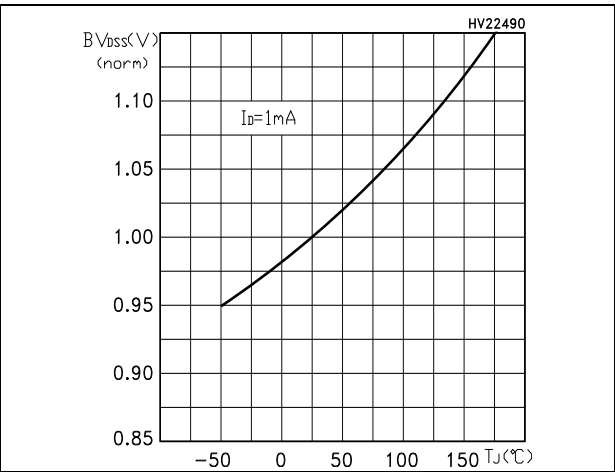
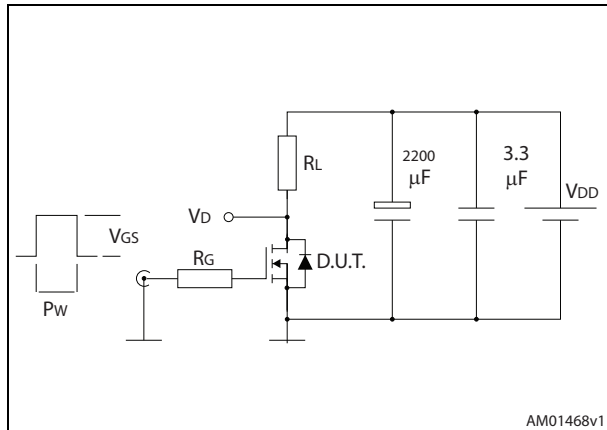


Figure 25. Normalized breakdown voltage vs.  
temperature p-ch

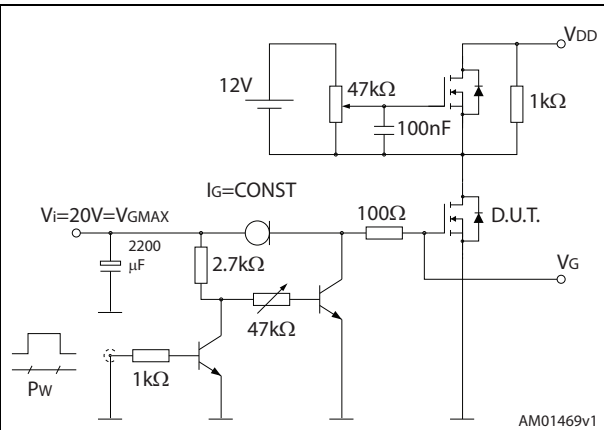


### 3 Test circuits

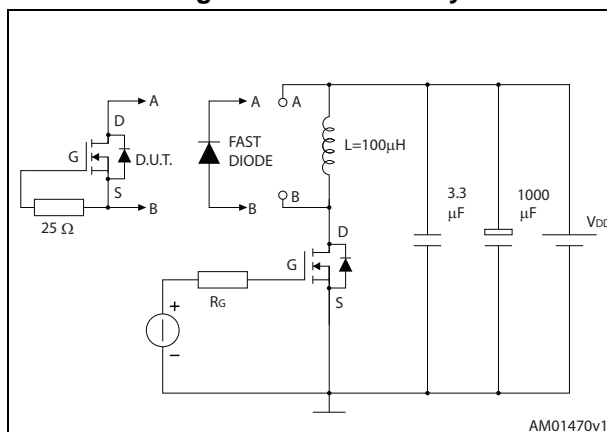
**Figure 26. Switching times test circuit for resistive load**



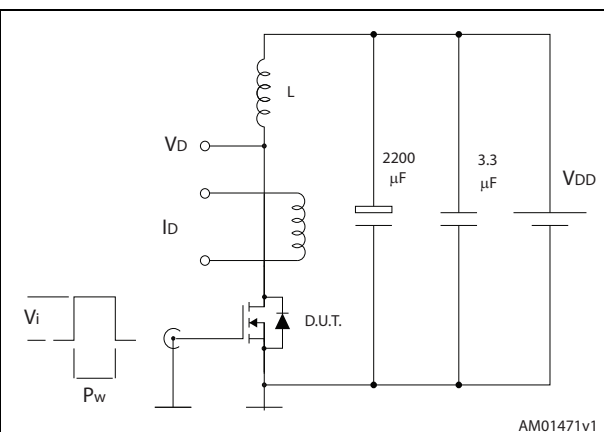
**Figure 27. Gate charge test circuit**



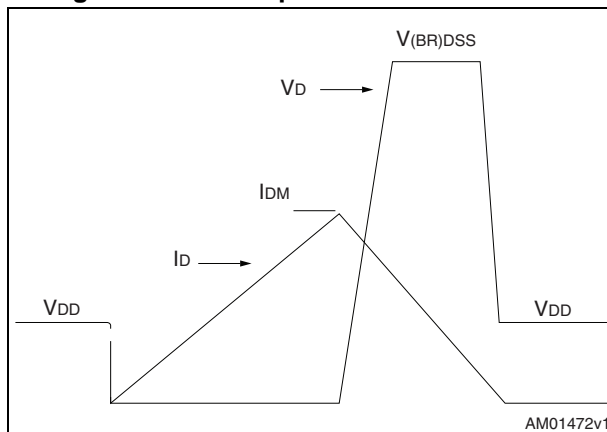
**Figure 28. Test circuit for inductive load switching and diode recovery times**



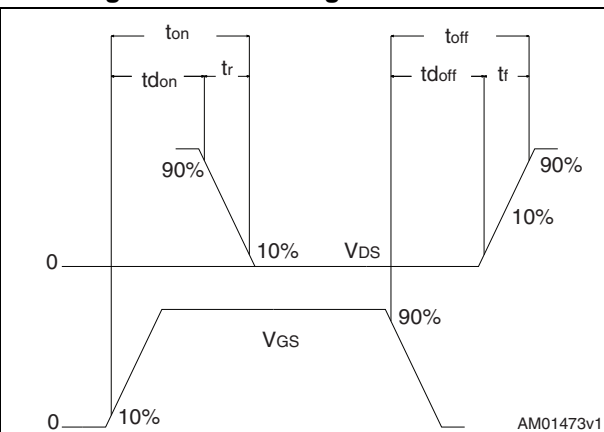
**Figure 29. Unclamped inductive load test circuit**



**Figure 30. Unclamped inductive waveform**



**Figure 31. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 32. SO-8 drawing

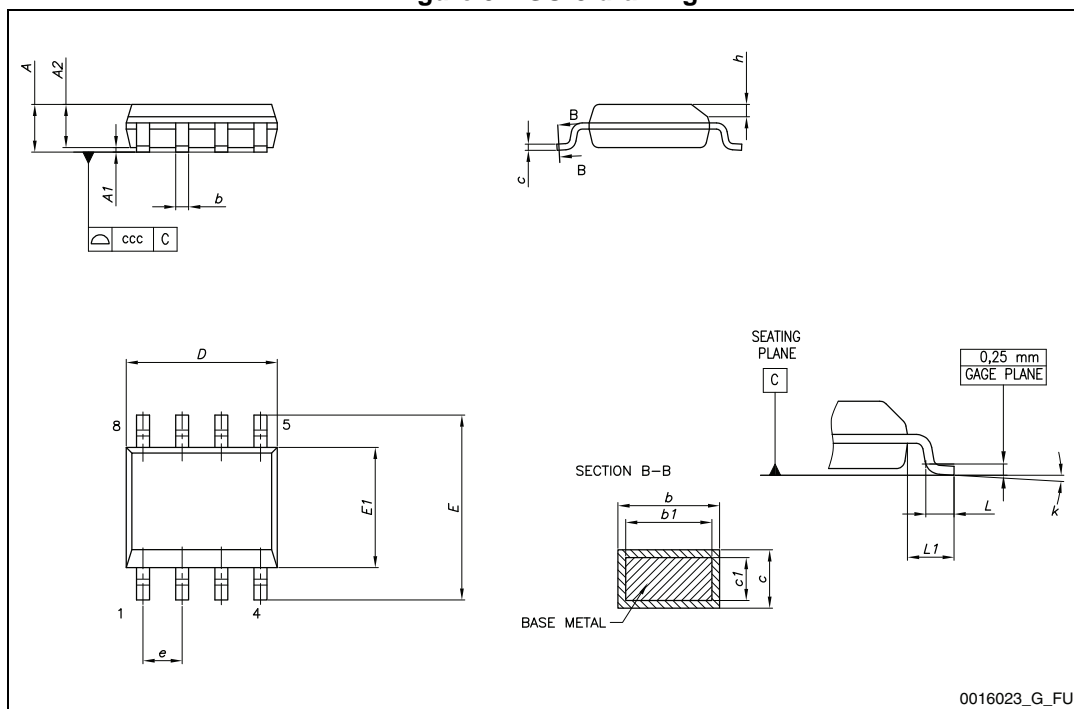
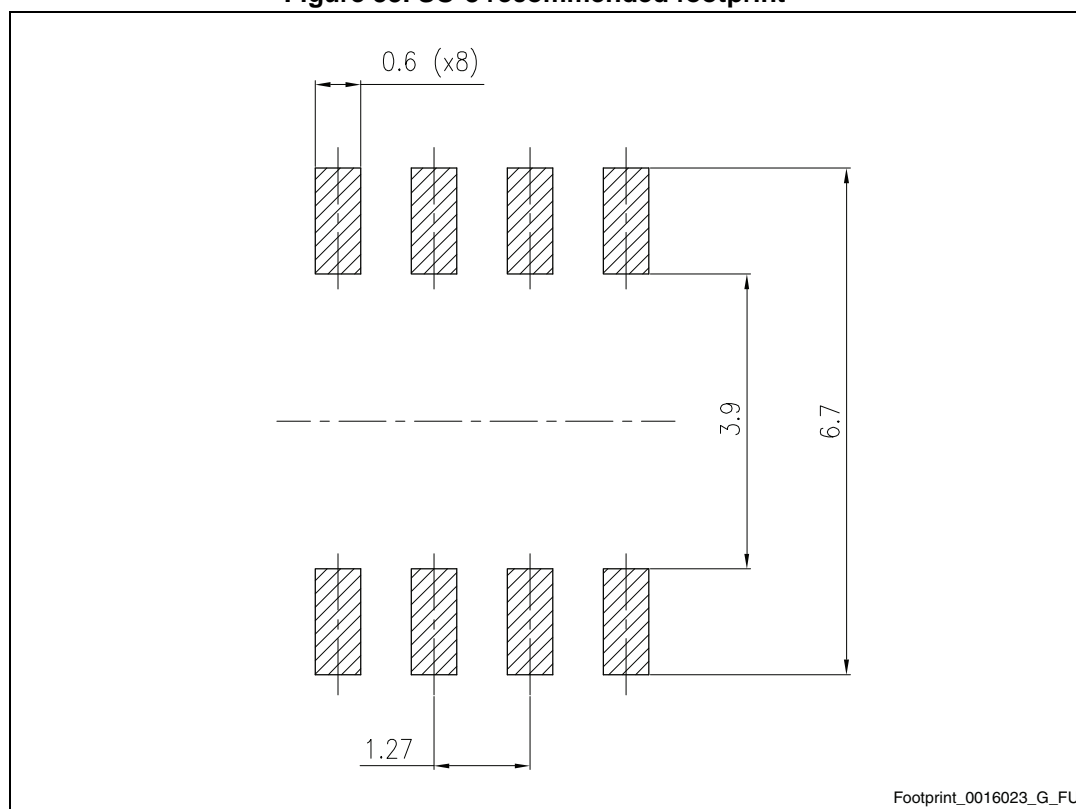


Table 8. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

**Figure 33. SO-8 recommended footprint<sup>(a)</sup>**

a. All dimensions are in millimeters.

## 5 Packaging mechanical data

Figure 34. SO-8 tape and reel dimensions

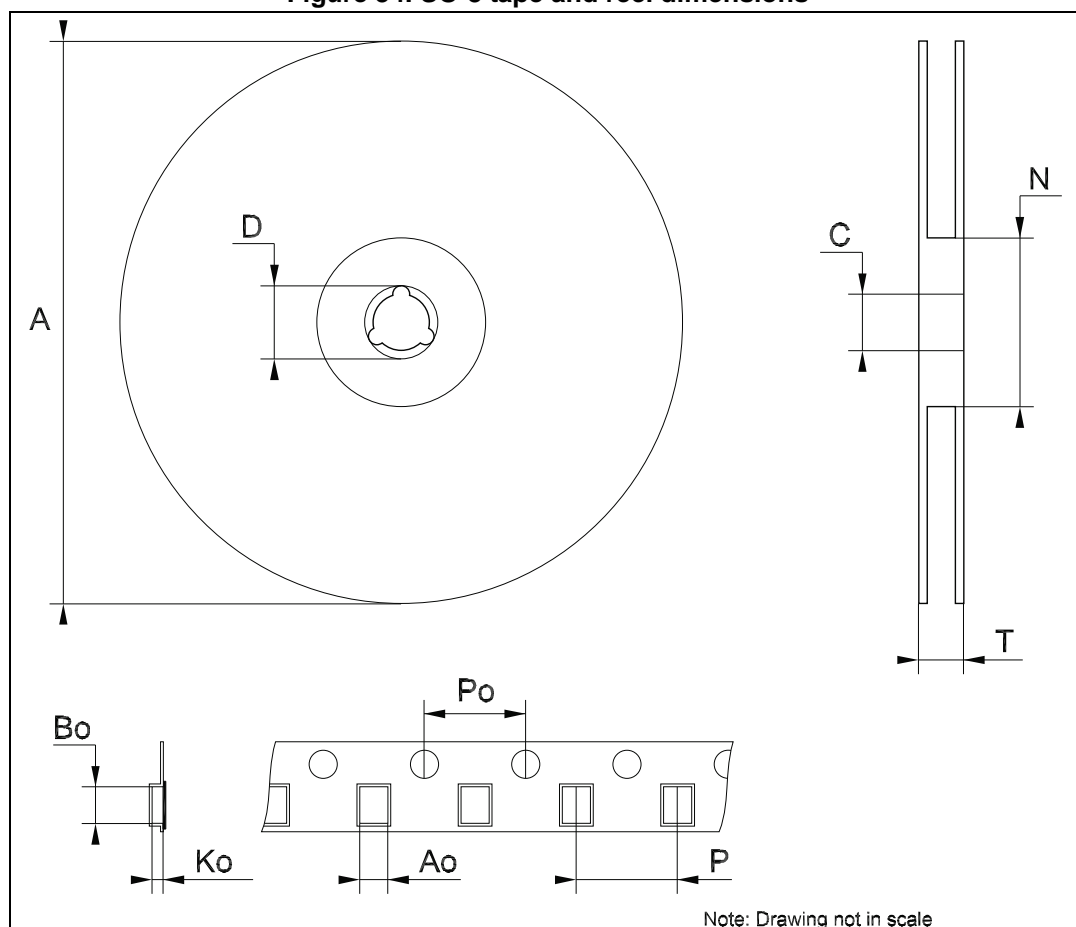


Table 9. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	8.1	-	8.5
Bo	5.5	-	5.9
Ko	2.1	-	2.3
Po	3.9	-	4.1
P	7.9	-	8.1



## 6 Revision history

Table 10. Revision history

Date	Revision	Changes
17-Sep-2004	1	First revision.
31-Oct-2006	2	The document has been reformatted.
30-Jan-2007	3	typo mistake on <a href="#">Table 2</a> .
23-Jul-2007	4	<a href="#">Figure 14</a> has been updated.
23-Feb-2009	5	<a href="#">Figure 2</a> , <a href="#">Figure 3</a> , <a href="#">Figure 14</a> and <a href="#">Figure 15</a> have been changed.
10-Jun-2010	6	Updated $V_{GS(th)}$ in <a href="#">Table 4: On/off states</a> .
13-Jun-2014	7	<ul style="list-style-type: none"><li>– Modified: title</li><li>– Modified: <a href="#">Description</a></li><li>– Modified: marking in <a href="#">Table 1</a></li><li>– Updated: <a href="#">Section 4: Package mechanical data</a></li><li>– Minor text changes</li></ul>

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