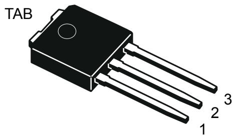
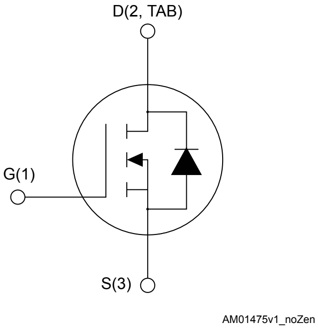
STU10NM60N

Datasheet

N-channel 600 V, 530 mΩ typ., 10 A MDmesh II Power MOSFET in an IPAK package



IPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STU10NM60N	600 V	550 mΩ	10 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh technology. This revolutionary Power MOSFET associates a vertical structure to the company’s strip layout to yield one of the world’s lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Product status link
STU10NM60N

Product summary	
Order code	STU10NM60N
Marking	10NM60N
Package	IPAK
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	10	A
	Drain current (continuous) at T_C = 100 °C	5	
I_{DM} (1)	Drain current (pulsed)	32	A
P_{TOT}	Total power dissipation at T_C = 25 °C	70	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	200	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width limited by safe operating area.*
2. *$I_{SD} \leq 10$ A, di/dt ≤ 400 A/μs, V_{DS} (peak) ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.79	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	100	°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. **On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate body leakage current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		530	550	mΩ

1. *Specified by design, not tested in production.*

Table 4. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz,V_{GS} = 0 V	-	540	-	pF
C_{oss}	Output capacitance		-	44	-	pF
C_{rss}	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	110	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 0 to 10 V (see Figure 12. Test circuit for gate charge behavior)	-	19	-	nC
Q_{gs}	Gate-source charge		-	3	-	nC
Q_{gd}	Gate-drain charge		-	10	-	nC

1. *$C_{oss\ eq.}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 5. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	10	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	15	-	ns

Table 6. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM} (1)	Source-drain current (pulsed)		-		32	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	250		ns
Q_{rr}	Reverse recovery charge		-	2.12		µC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	315		ns
Q_{rr}	Reverse recovery charge		-	2.6		µC
I_{RRM}	Reverse recovery current		-	16.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

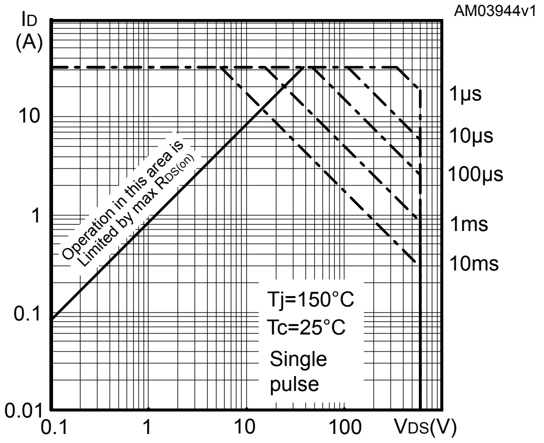


Figure 2. Normalized transient thermal impedance

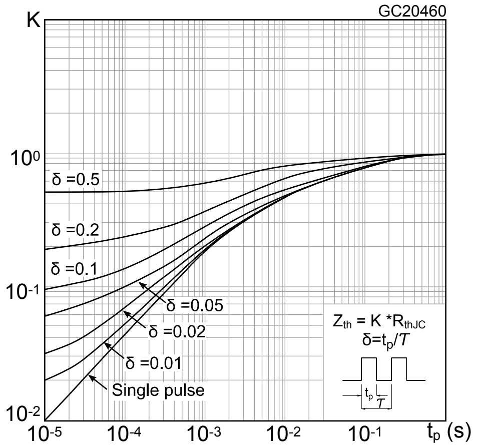


Figure 3. Typical output characteristics

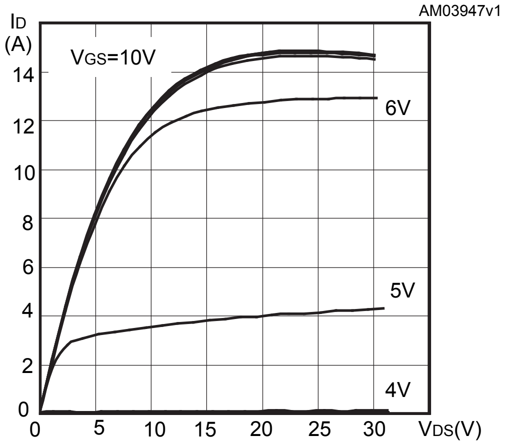


Figure 4. Typical transfer characteristics

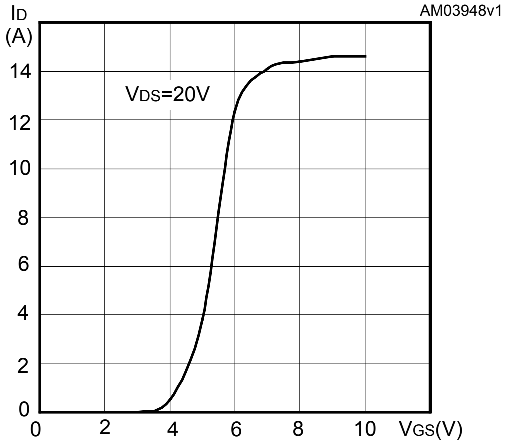


Figure 5. Typical gate charge characteristics

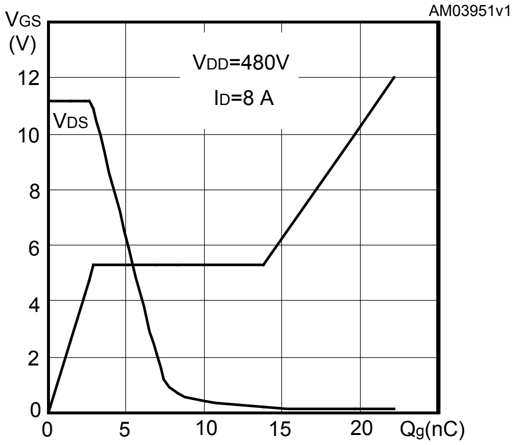


Figure 6. Typical capacitance characteristics

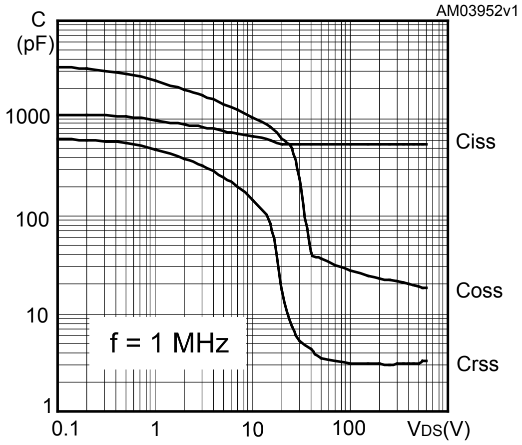


Figure 7. Typical drain-source on-resistance

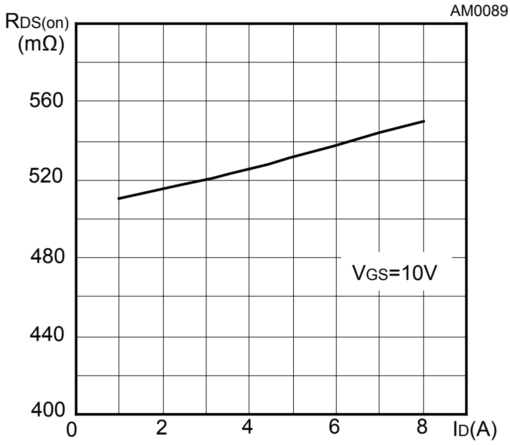


Figure 8. Normalized breakdown voltage vs temperature

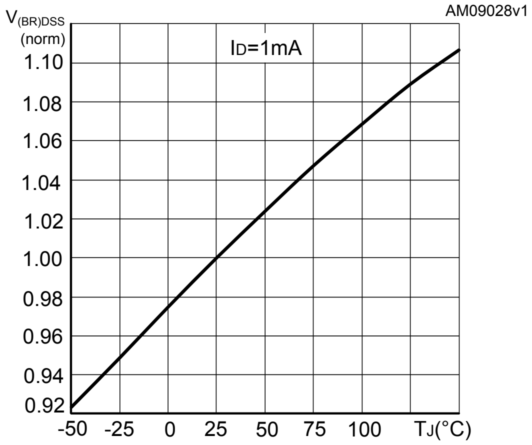


Figure 9. Normalized gate threshold vs temperature

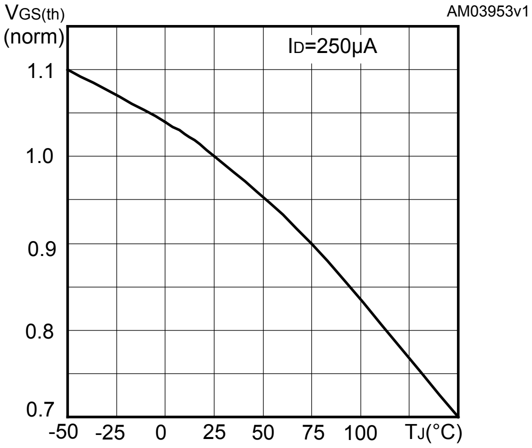
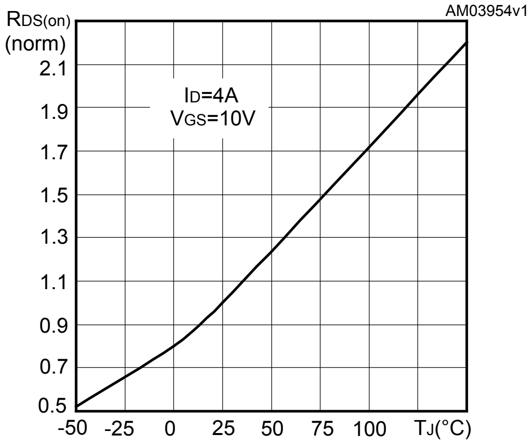


Figure 10. Normalized on-resistance vs temperature



3 Test circuits

Figure 11. Test circuit for resistive load switching times

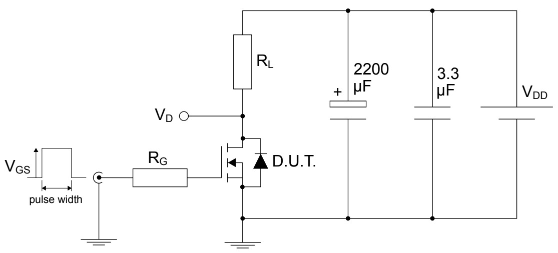


Figure 12. Test circuit for gate charge behavior

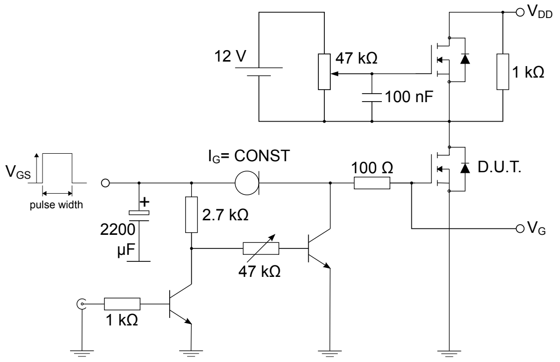


Figure 13. Test circuit for inductive load switching and diode recovery times

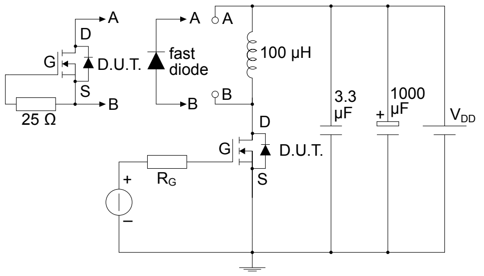


Figure 14. Unclamped inductive load test circuit

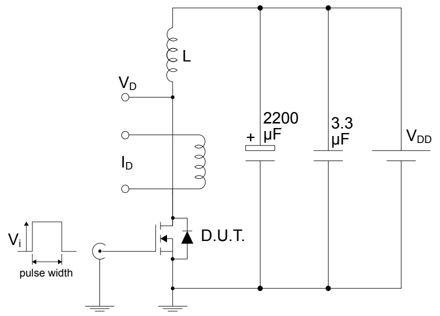


Figure 15. Unclamped inductive waveform

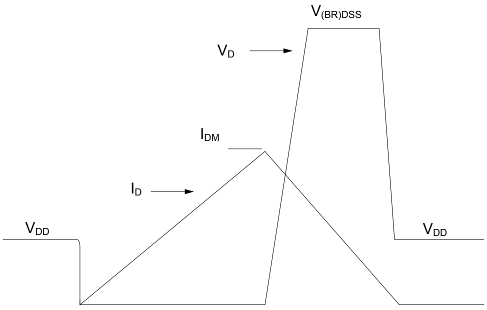
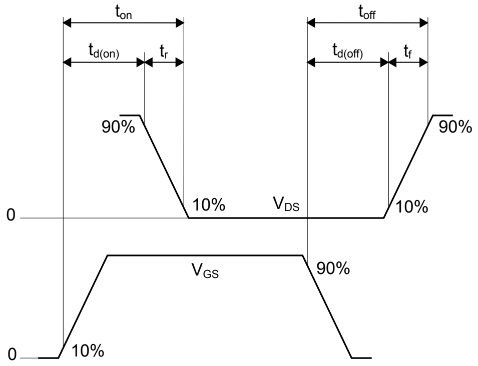


Figure 16. Switching time waveform

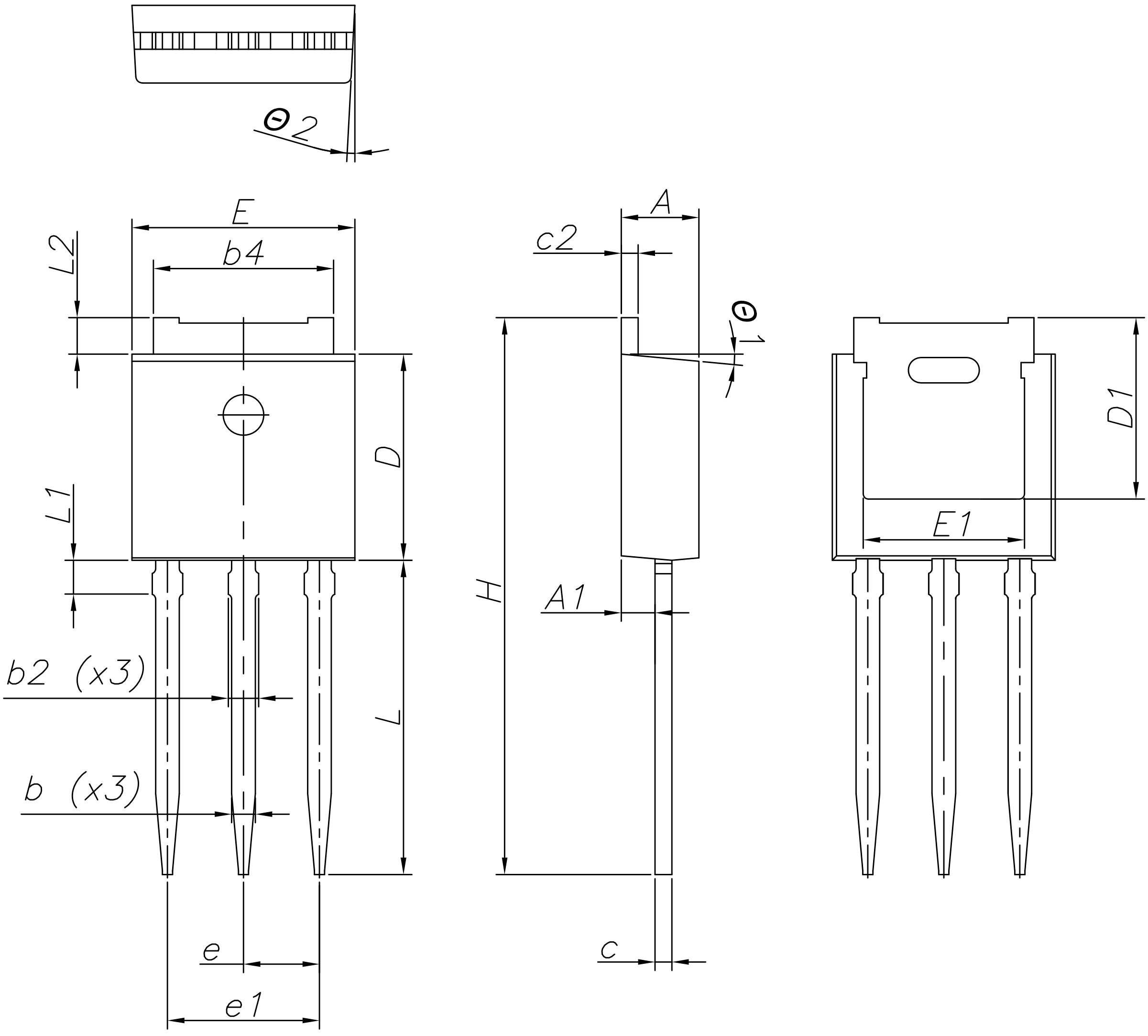


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 IPAK (TO-251) type C package information

Figure 17. **IPAK (TO-251) type C package outline**



0068771_IK_typeC_rev16

Table 7. **IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
07-Nov-2023	1	First release. Part number STU10NM60N previously included in datasheet DS11416.

Contents

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