



# STD12N65M5, STF12N65M5, STI12N65M5 STP12N65M5, STU12N65M5

N-channel 650 V, 0.39  $\Omega$ , 8.5 A MDmesh™ V Power MOSFET  
DPAK, I<sup>2</sup>PAK, TO-220FP, TO-220, IPAK

## Features

Type	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STD12N65M5	710 V	< 0.43 $\Omega$	8.5 A	70 W
STF12N65M5			8.5 A <sup>(1)</sup>	25 W
STI12N65M5			8.5 A	70 W
STP12N65M5			8.5 A	70 W
STU12N65M5			8.5 A	70 W

1. Limited only by maximum temperature allowed.

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating and high dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

## Applications

Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

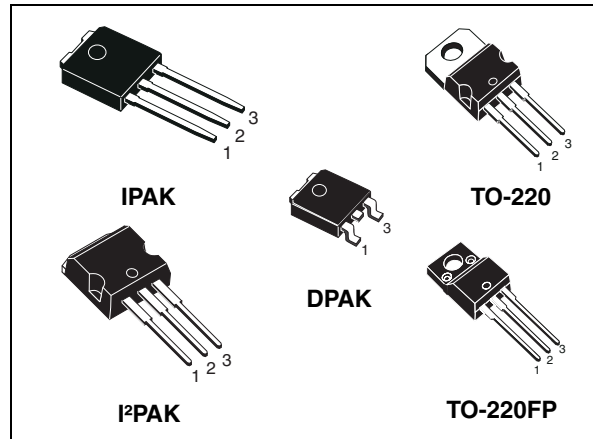


Figure 1. Internal schematic diagram

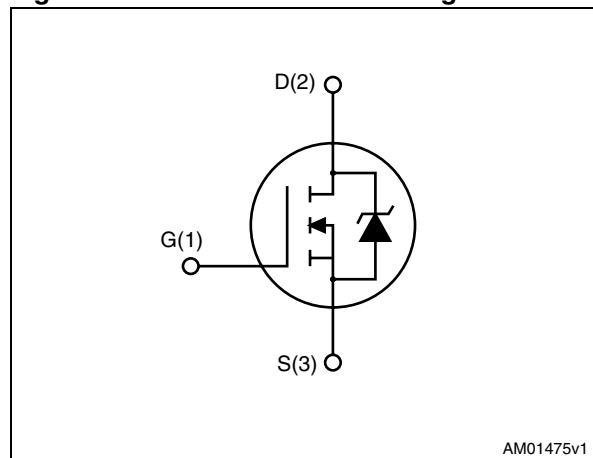


Table 1. Device summary

Order codes	Marking	Packages	Packaging
STD12N65M5	12N65M5	DPAK	Tape and reel
STF12N65M5		TO-220FP	Tube
STI12N65M5		I <sup>2</sup> PAK	Tube
STP12N65M5		TO-220	Tube
STU12N65M5		IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, IPAK, DPAK, I <sup>2</sup> PAK	TO-220FP	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	650		V
V <sub>GS</sub>	Gate-source voltage	25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	8.5	8.5 <sup>(1)</sup>	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	5.4	5.4 <sup>(1)</sup>	A
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	34	34 <sup>(1)</sup>	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	70	25	W
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by T <sub>j</sub> max)	2.5		A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	150		mJ
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T <sub>C</sub> = 25 °C)		2500	V
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		°C

1. Limited only by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. I<sub>SD</sub> ≤ 8.5 A, di/dt ≤ 400 A/μs; V<sub>Peak</sub> < V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 400 V

**Table 3. Thermal data**

Symbol	Parameter	Value					Unit
		DPAK	IPAK	I <sup>2</sup> PAK	TO-220	TO-220FP	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.79			5	°C/W	
R <sub>thj-amb</sub>	Thermal resistance junction-ambient max		100	62.5		°C/W	
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	50				°C/W	
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300				°C	

1. When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.3\text{ A}$		0.39	0.43	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	900	-	pF
$C_{oss}$	Output capacitance			22		pF
$C_{rss}$	Reverse transfer capacitance			2		pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0$	-	64	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			21		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	2.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 4.25\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )	-	20	-	nC
$Q_{gs}$	Gate-source charge			4.8		nC
$Q_{gd}$	Gate-drain charge			8.3		nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (v)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 5$ A,		22.6		ns
$t_r$ (v)	Voltage rise time	$R_G = 4.7$ $\Omega$ , $V_{GS} = 10$ V		17.6		ns
$t_f$ (i)	Current fall time	(see <a href="#">Figure 21</a> and		15.6		ns
$t_c$ (off)	Crossing time	<a href="#">Figure 24</a> )		23.4		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				8.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				34	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8.5$ A, $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 8.5$ A, $di/dt = 100$ A/ $\mu$ s		230		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V (see <a href="#">Figure 24</a> )		2.2		$\mu$ C
$I_{RRM}$	Reverse recovery current			19		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 8.5$ A, $di/dt = 100$ A/ $\mu$ s		280		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C		2.7		$\mu$ C
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 24</a> )		19		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 and I<sup>2</sup>PAK

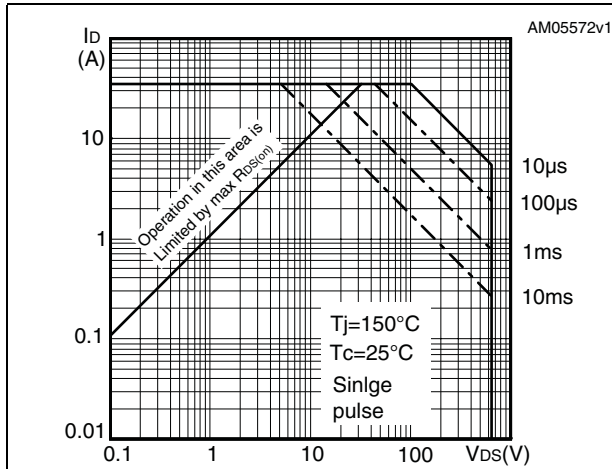


Figure 3. Thermal impedance for TO-220 and I<sup>2</sup>PAK

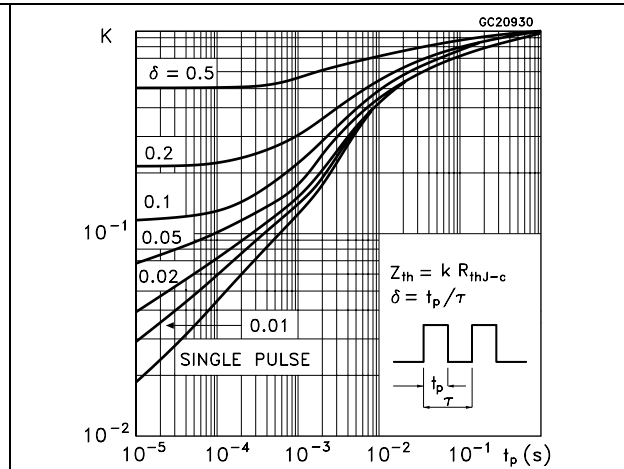


Figure 4. Safe operating area for TO-220FP

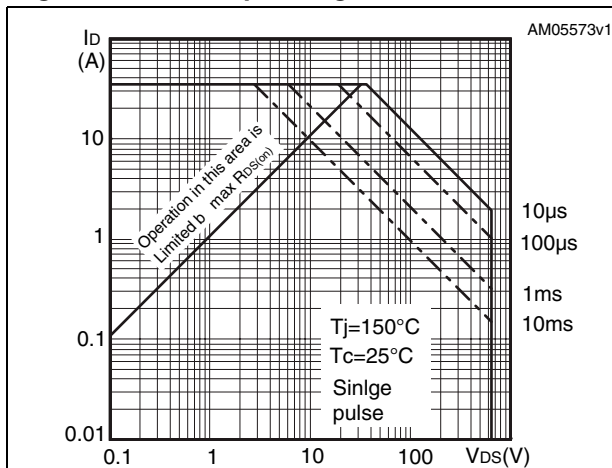


Figure 5. Thermal impedance for TO-220FP

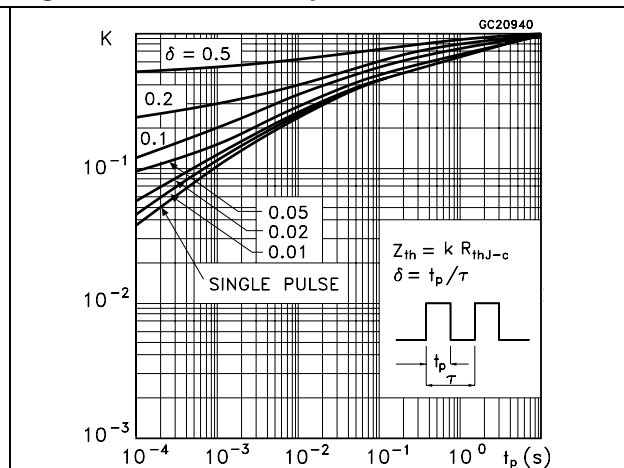


Figure 6. Safe operating area for DPAK, IPAK

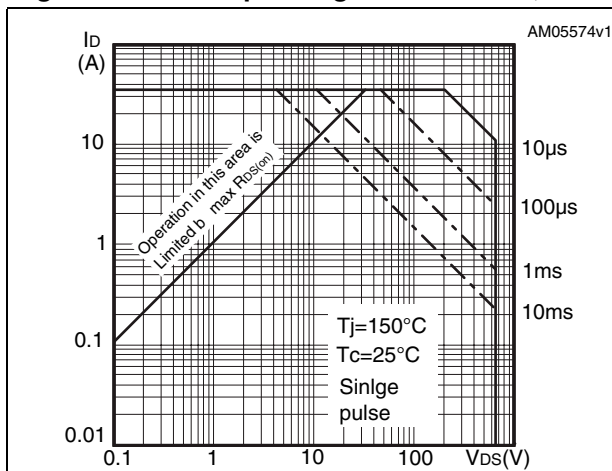


Figure 7. Thermal impedance for DPAK, IPAK

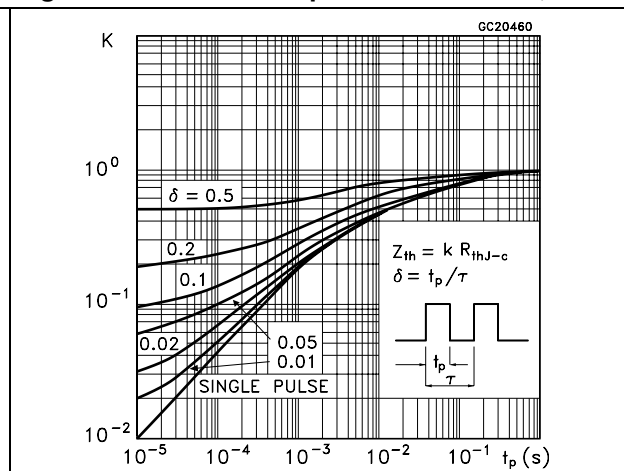


Figure 8. Output characteristics

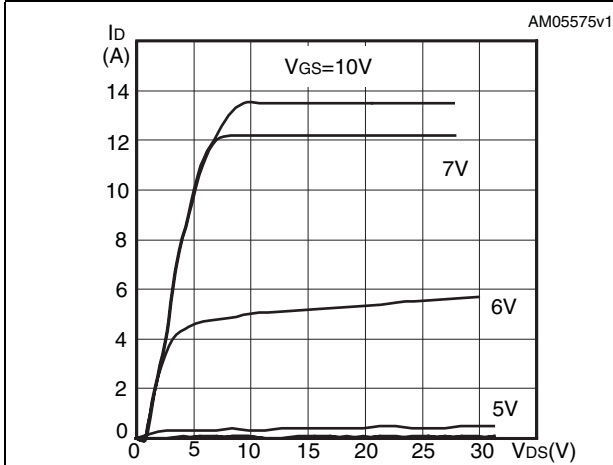


Figure 9. Transfer characteristics

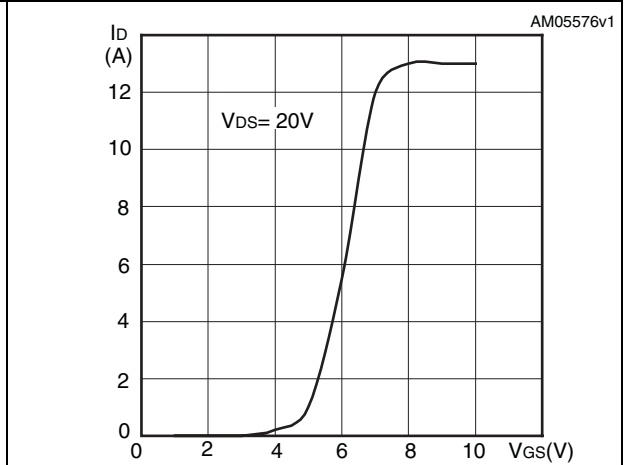


Figure 10. Gate charge vs gate-source voltage

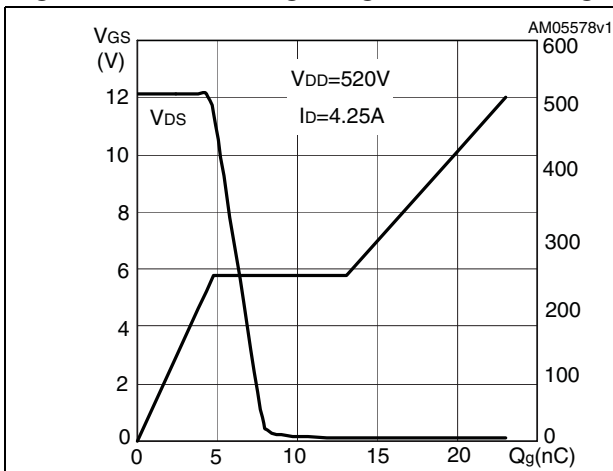


Figure 11. Static drain-source on resistance

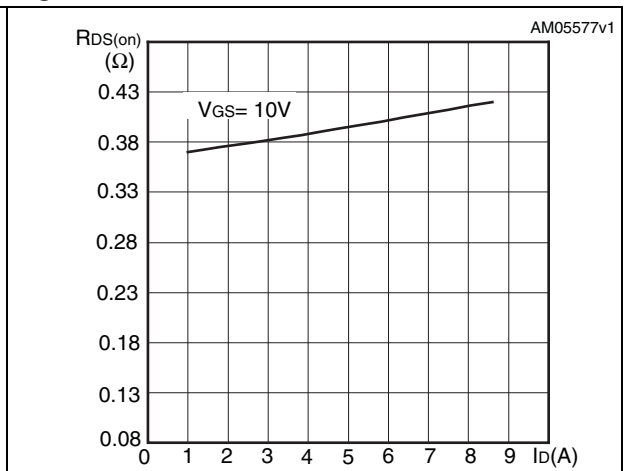


Figure 12. Capacitance variations

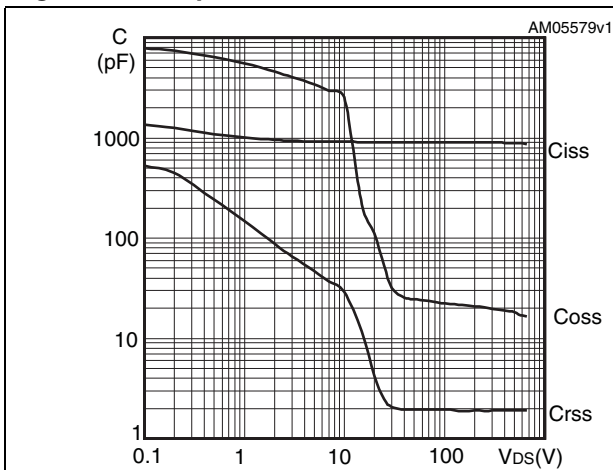


Figure 13. Output capacitance stored energy

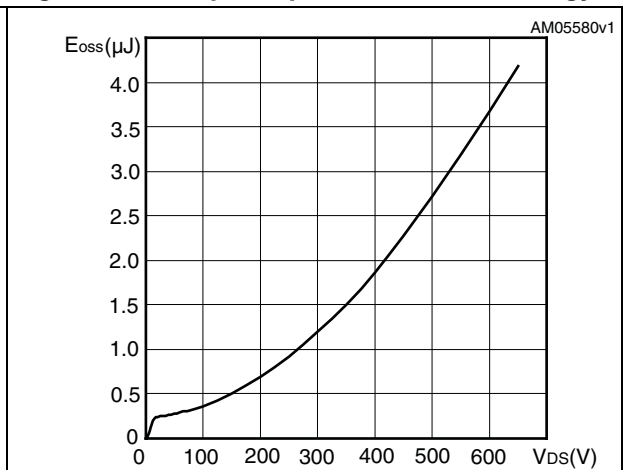


Figure 14. Normalized gate threshold voltage vs temperature

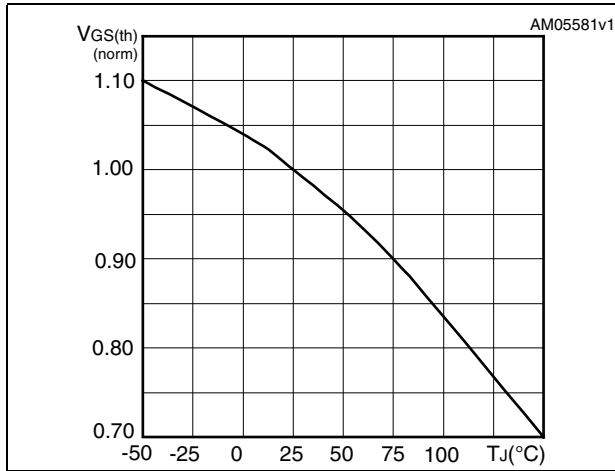


Figure 15. Normalized on resistance vs temperature

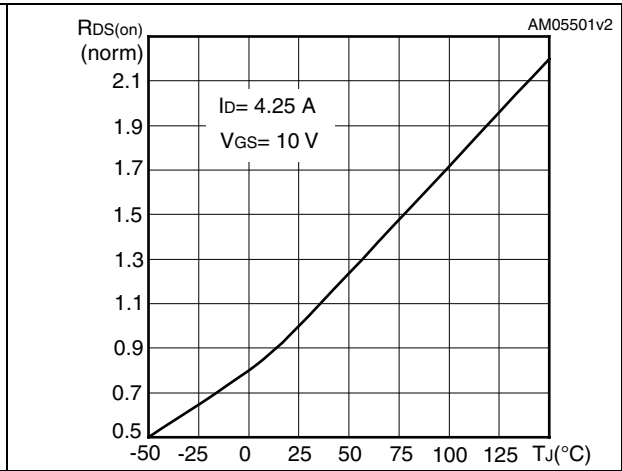


Figure 16. Source-drain diode forward characteristics

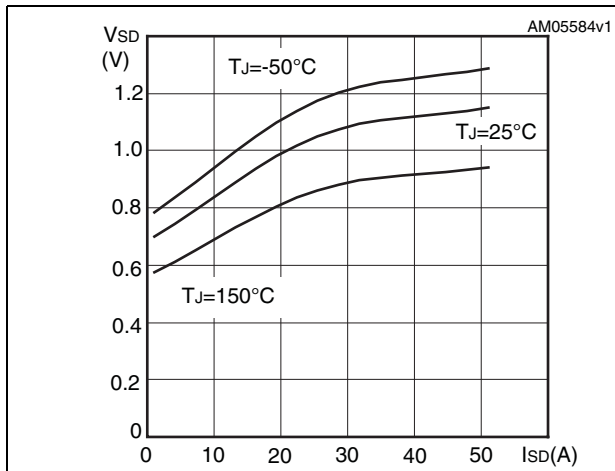


Figure 17. Normalized BV<sub>DSS</sub> @ 1 mA vs temperature

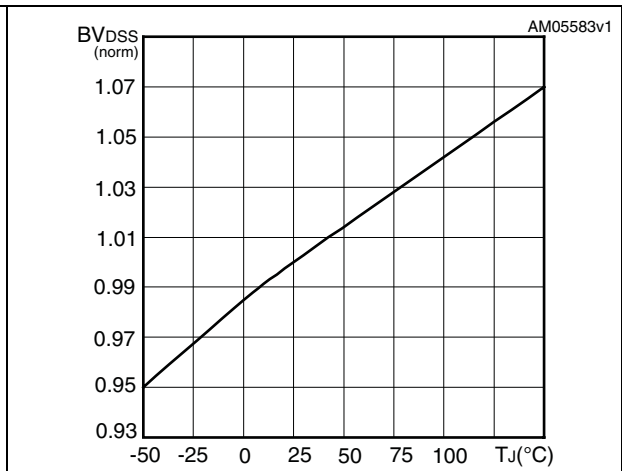
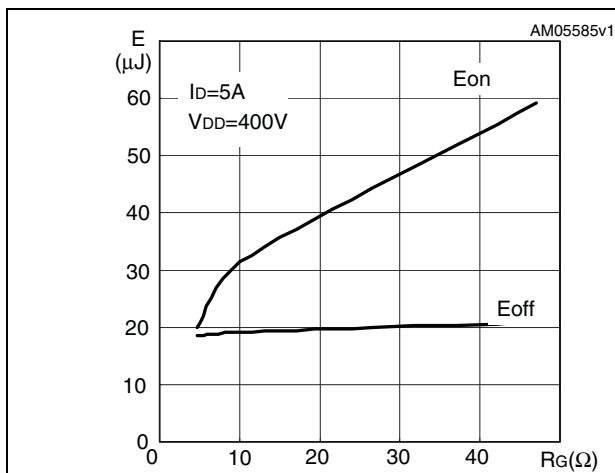


Figure 18. Switching losses vs gate resistance (1)

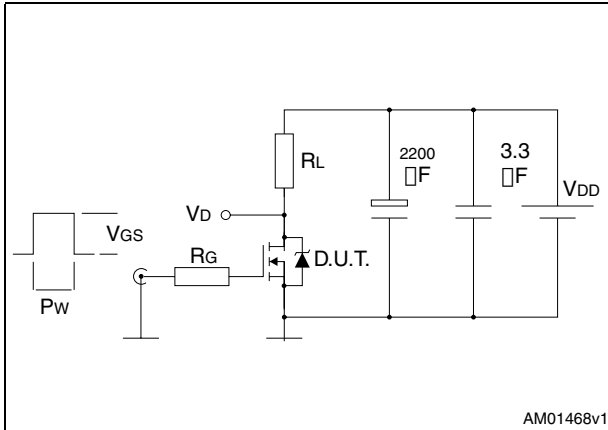


1. Eon including reverse recovery of a SiC diode

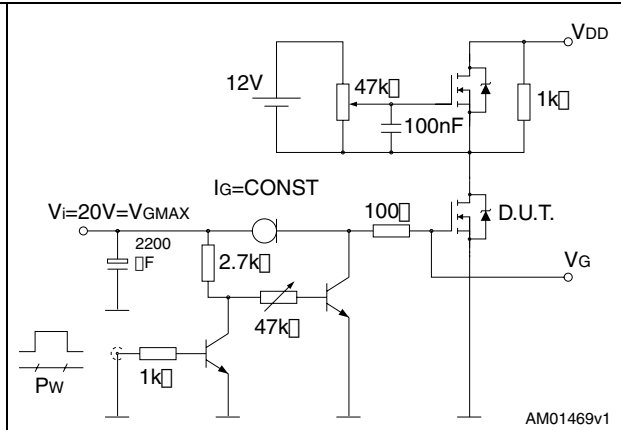


### 3 Test circuits

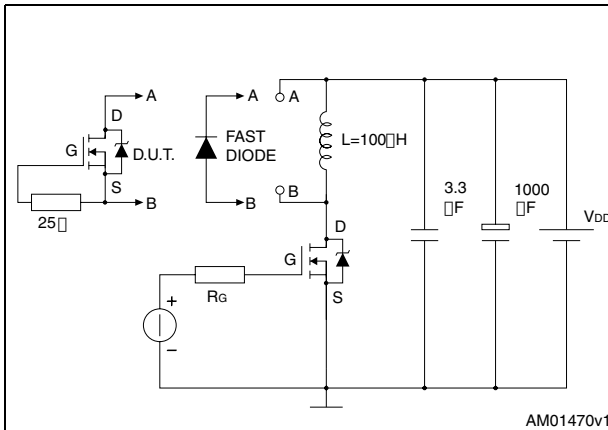
**Figure 19. Switching times test circuit for resistive load**



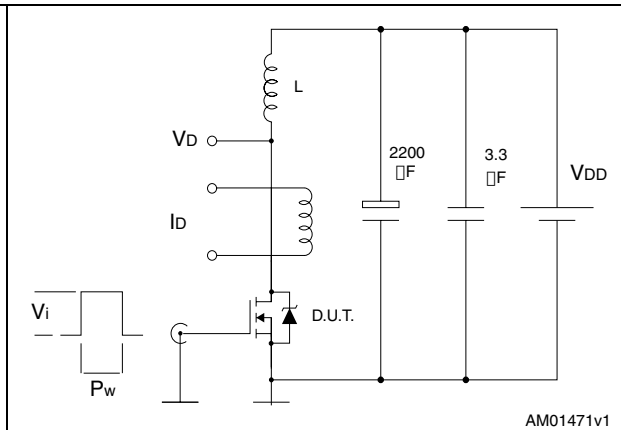
**Figure 20. Gate charge test circuit**



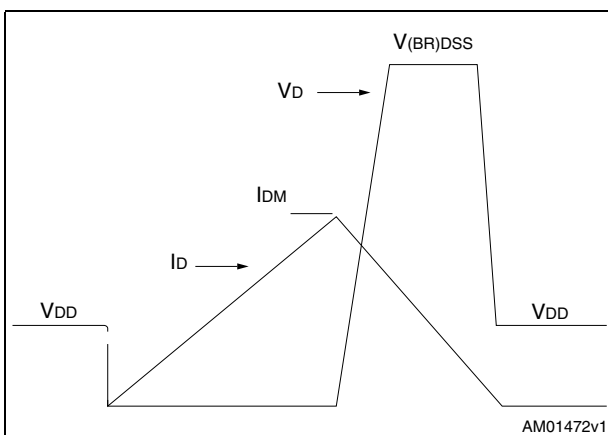
**Figure 21. Test circuit for inductive load switching and diode recovery times**



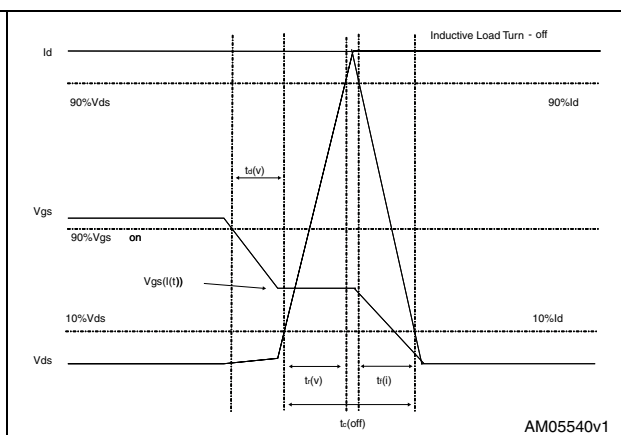
**Figure 22. Unclamped inductive load test circuit**



**Figure 23. Unclamped inductive waveform**



**Figure 24. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

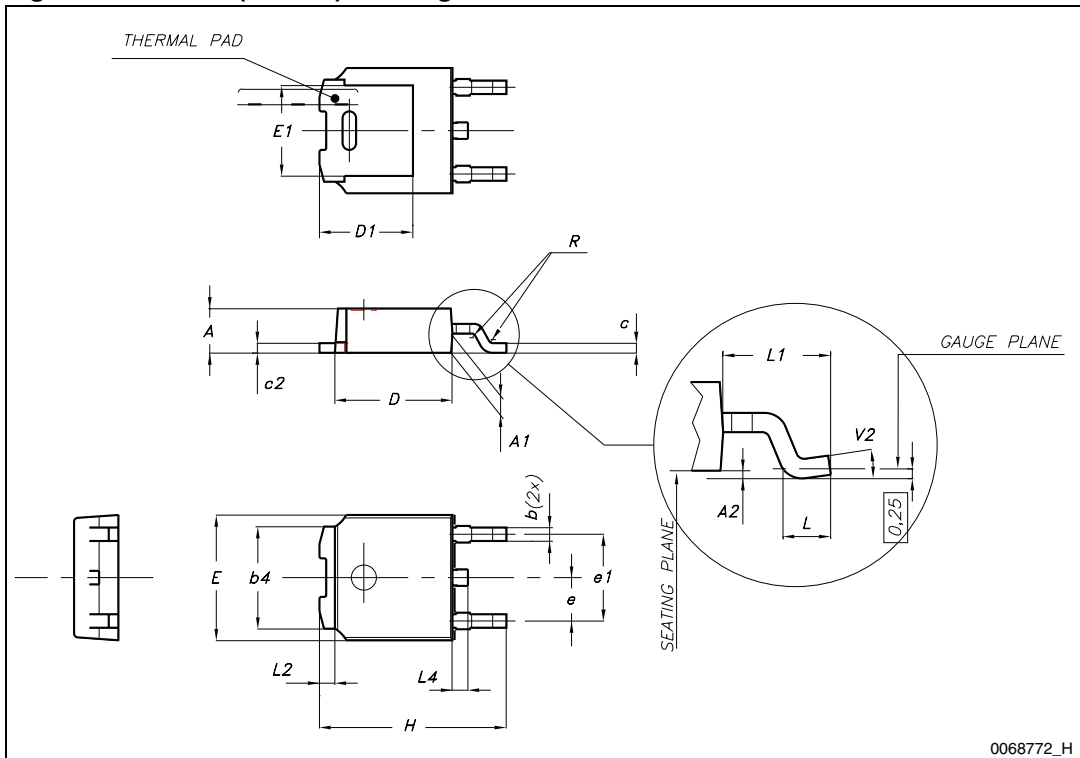
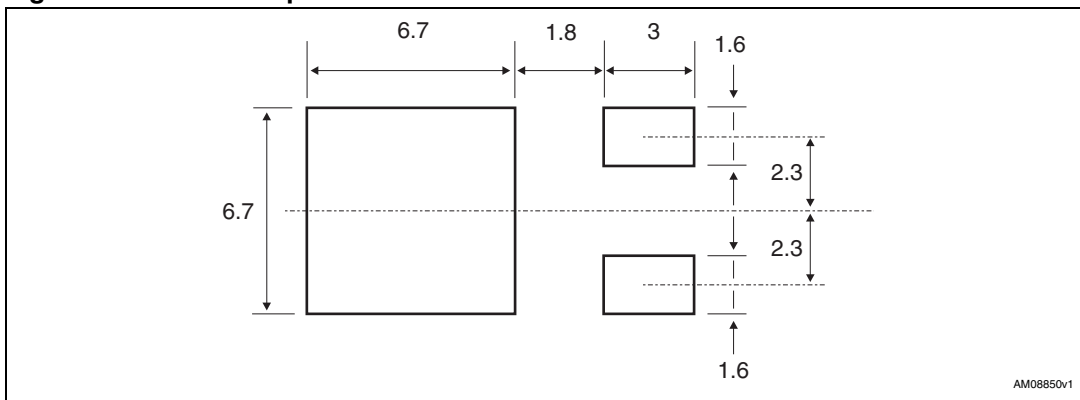


Figure 26. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

Table 9. IPAK (TO-251) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 27. IPAK (TO-251) drawing

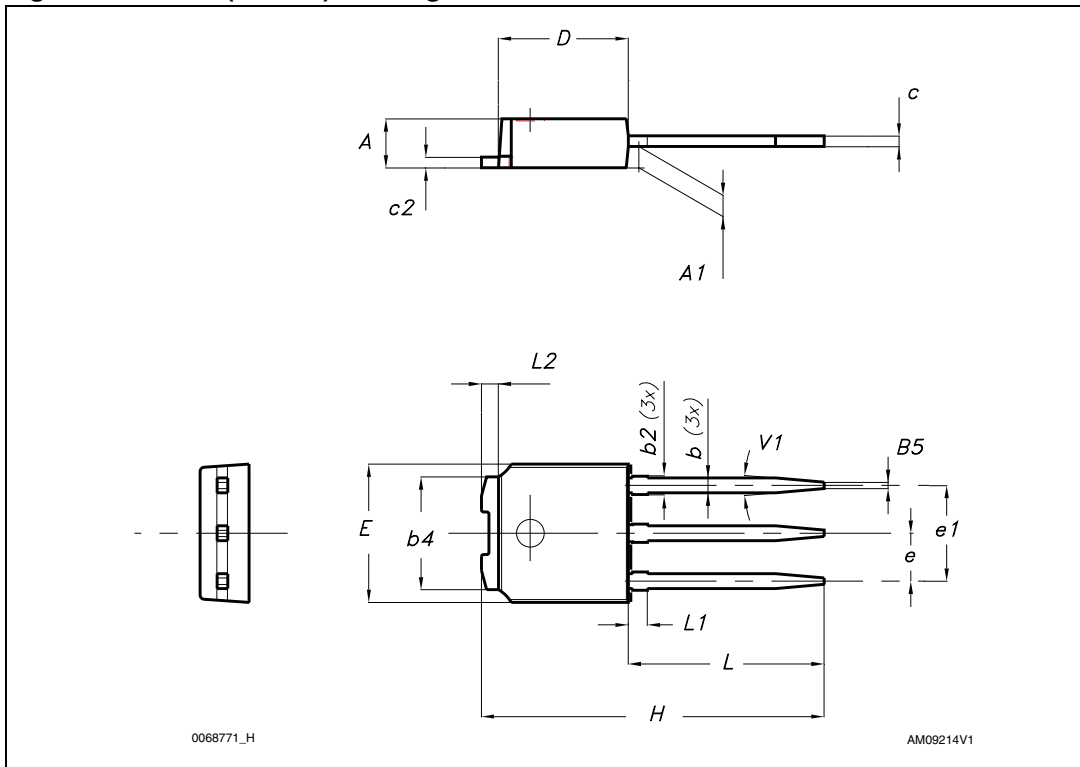


Table 10. I<sup>2</sup>PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 28. I<sup>2</sup>PAK (TO-262) drawing

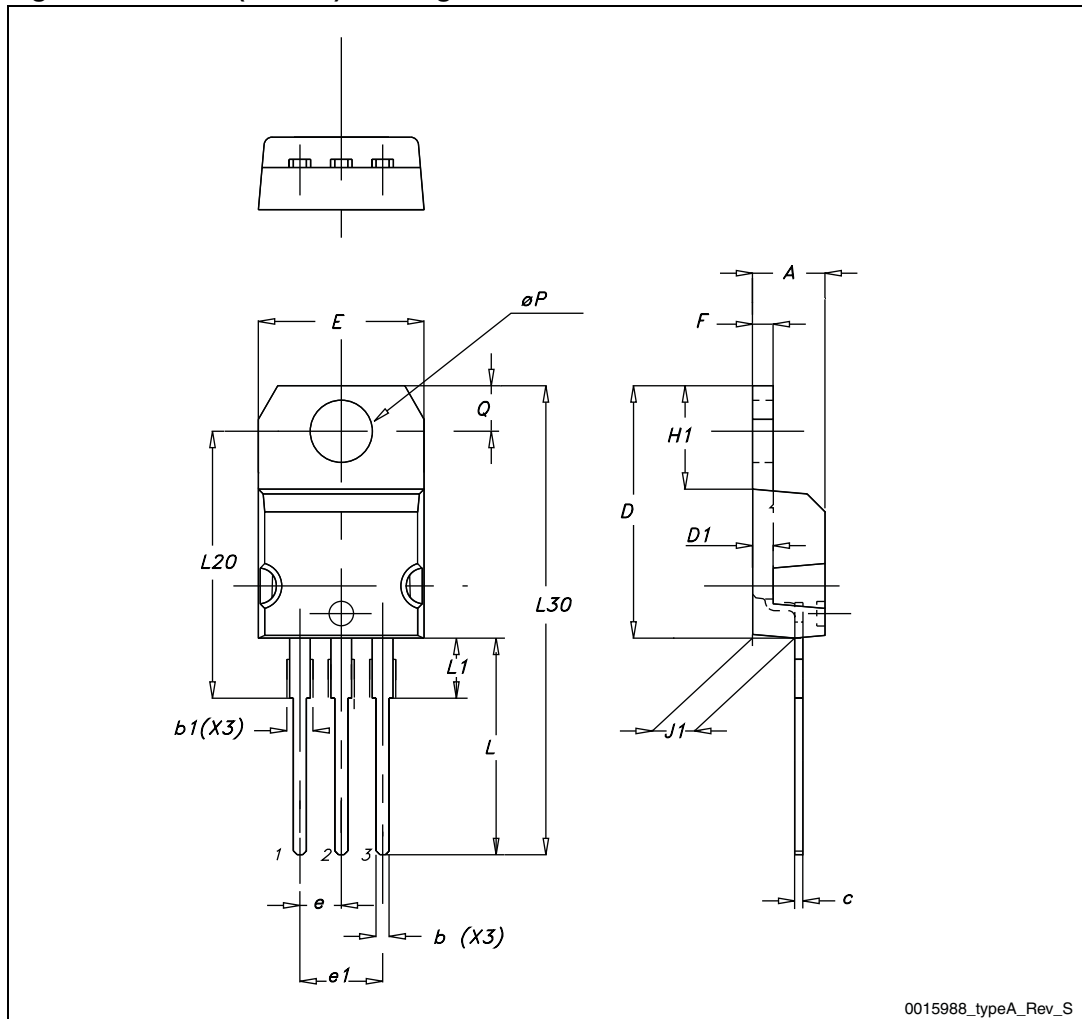
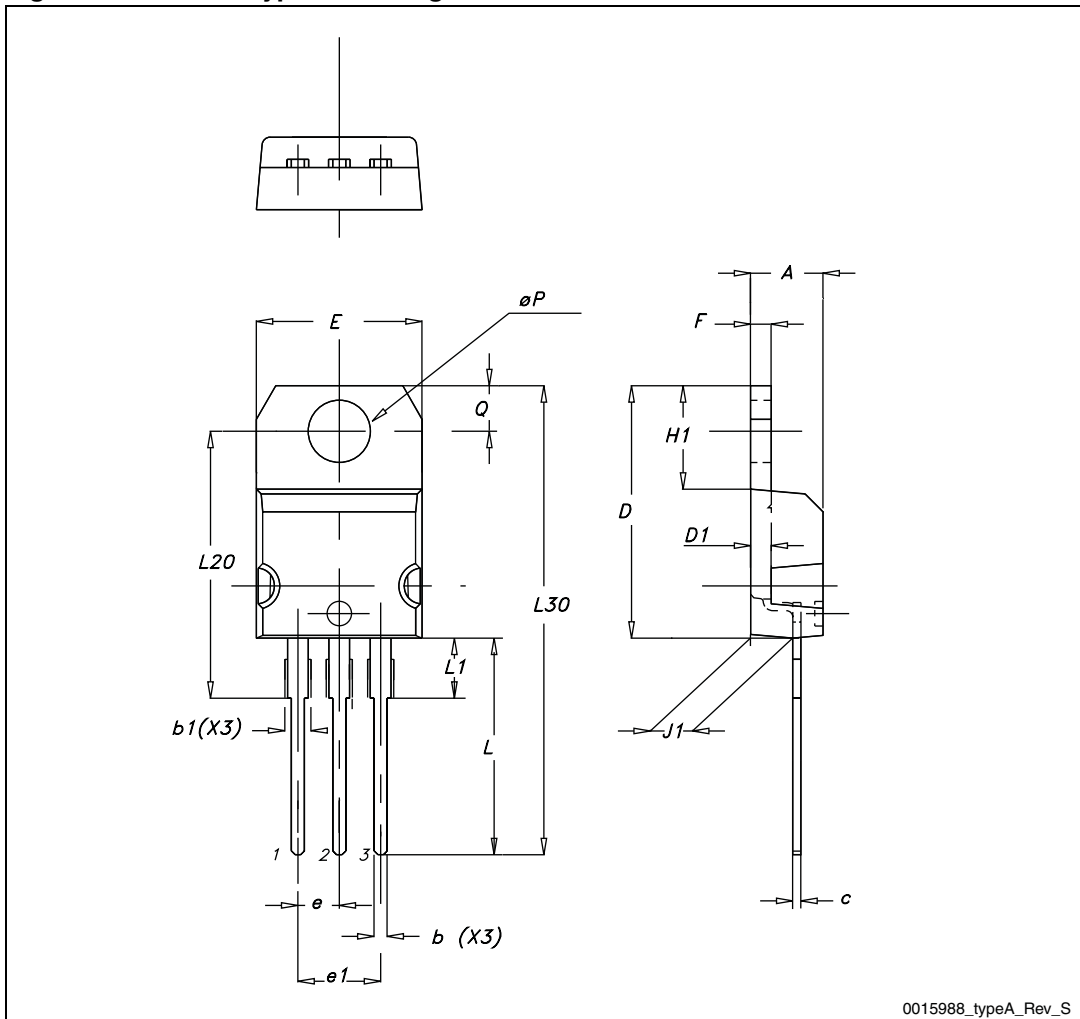




Table 11. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

Figure 29. TO-220 type A drawing

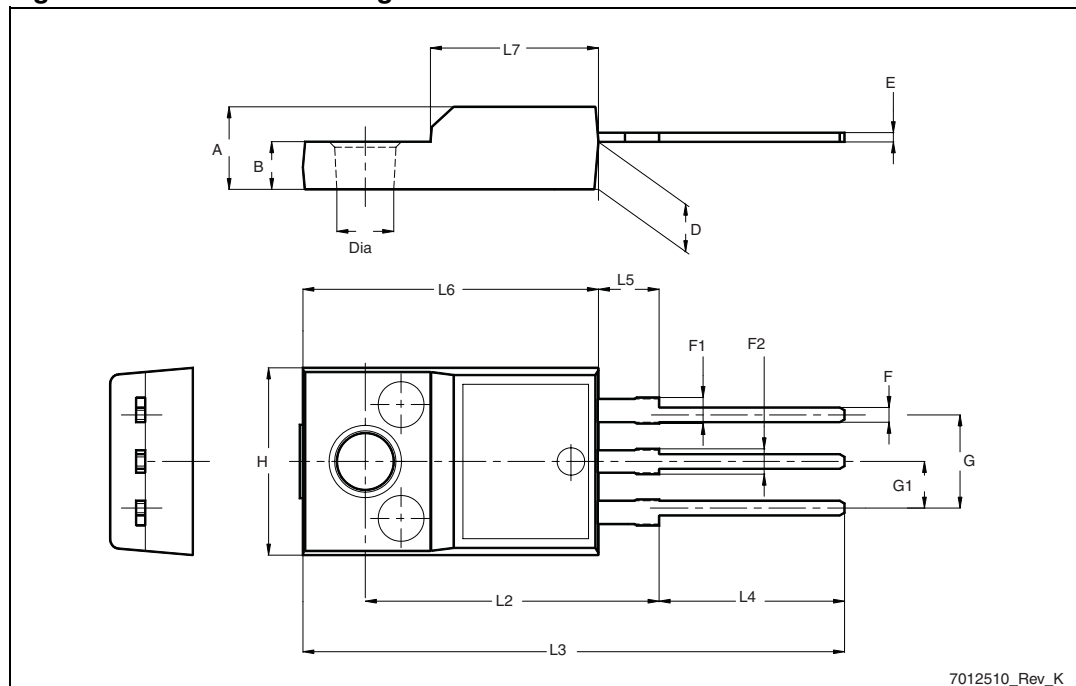


0015988\_typeA\_Rev\_S

Table 12. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 30. TO-220FP drawing

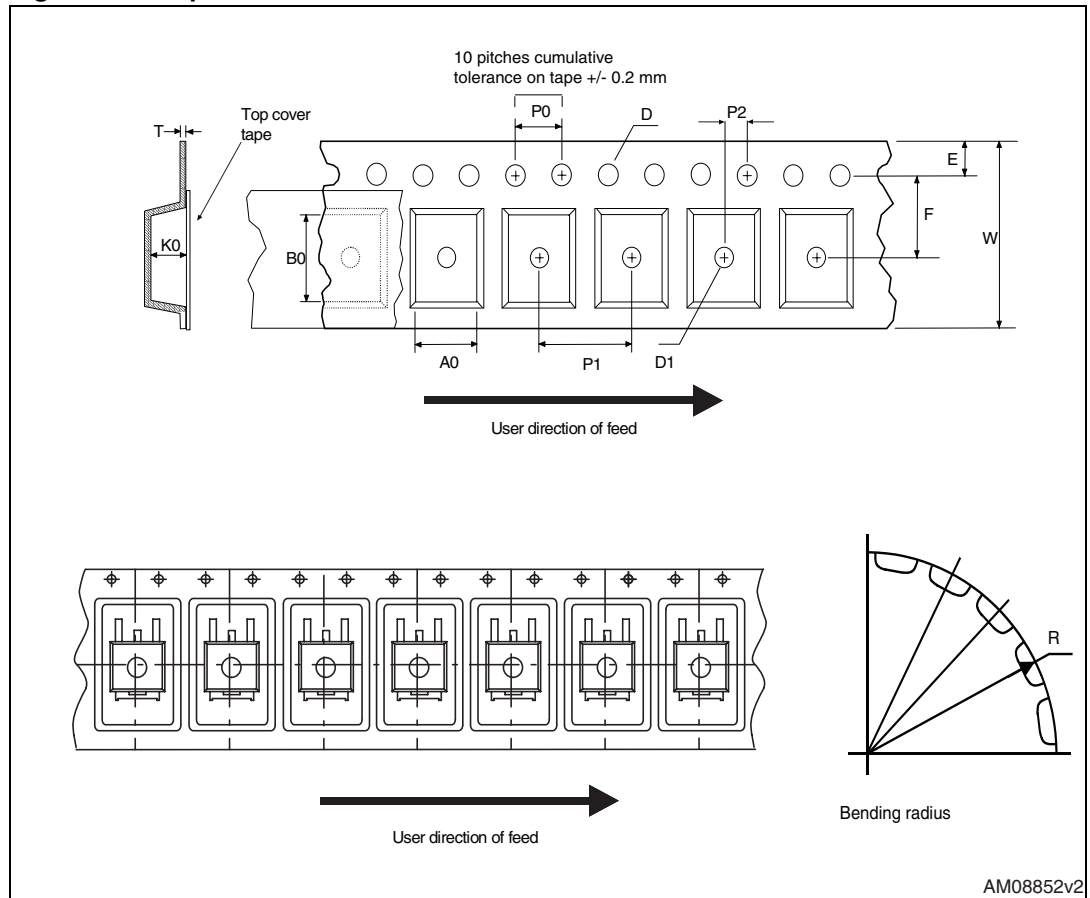


## 5 Packaging mechanical data

Table 13. DPAK (TO-252) tape and reel mechanical data

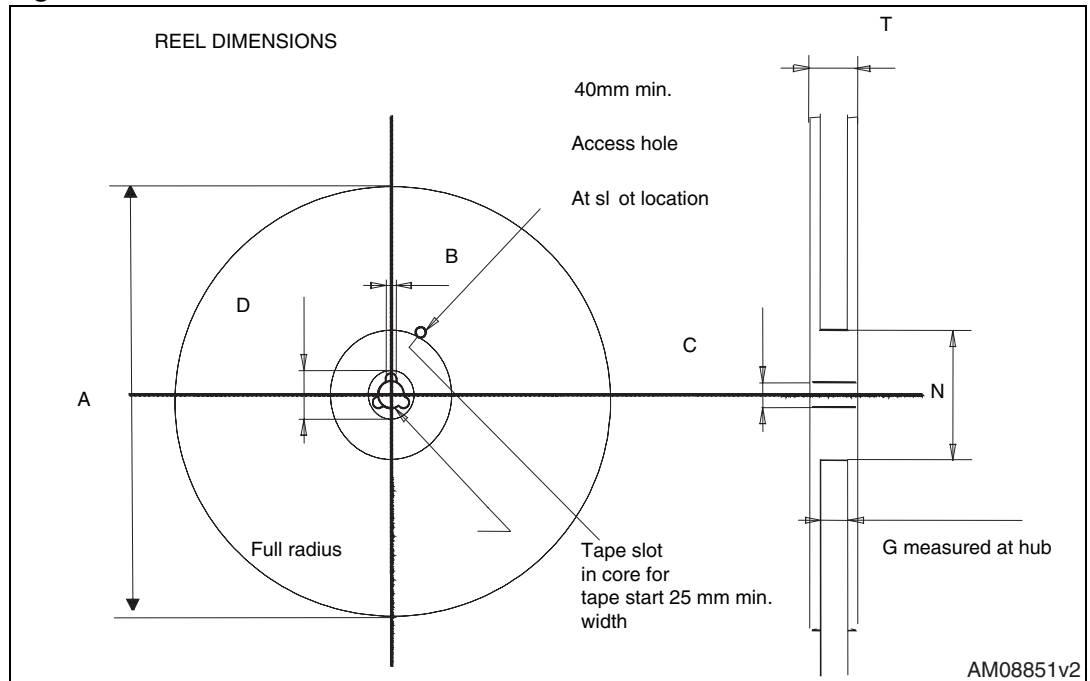
Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 31. Tape



AM08852v2

Figure 32. Reel



AM08851v2

## 6 Revision history

**Table 14. Document revision history**

Date	Revision	Changes
24-Feb-2009	1	First release
27-Feb-2009	2	Corrected package information on first page
21-Jan-2010	3	Document status promoted from preliminary data to datasheet
29-Jun-2010	4	<ul style="list-style-type: none"><li>– <i>Figure 15: Normalized on resistance vs temperature</i> has been updated</li><li>– <math>V_{GS}</math> vale in <i>Table 4</i> has been corrected</li></ul>
22-Jun-2011	5	Updated <i>Figure 18</i> and <i>Figure 20</i> . Updated gate charge in <i>Table 5</i> and switching time in <i>Table 6</i> .

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