STV0913

Multi-standard advanced demodulator for satellite digital TV broadcast set-top boxes

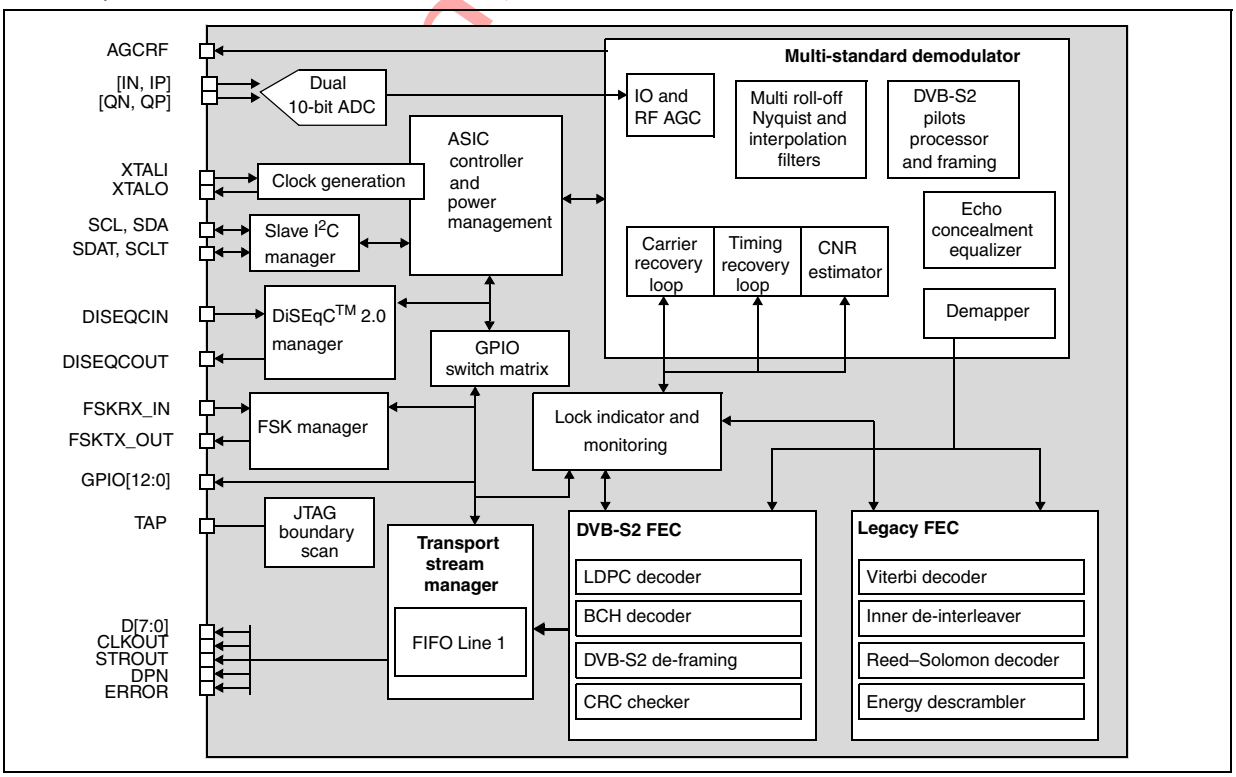
Datasheet – preliminary data

Features

- Multi-standard demodulation
  - DVB-S2 QPSK and 8PSK
  - Legacy DVB-S and DirecTV™ QPSK
  - Multi-tap equalizer for RF reflection removal
  - Wide range carrier frequency tracking loop for offset recovery
- Multi-standard decoding
  - DVB-S2 FEC and framing
  - Up to 135 Mbit/s channel bit rate
  - DVB-S or DirecTV™ legacy
- Interfaces
  - Data to MPEG decoder
  - DVB common interface compliant
  - I^2C serial bus interface, including private repeater for tuner
  - JTAG interface for boundary scan
  - DiSEqC 2.x 22-kHz interface
  - FSK interface
  - Flexible GPIOs and interrupts
  - Bit error rate monitoring and reporting
- Technology
  - Multi supply: 1.1-V core, 2.5-V analog, 3.3-V digital interfaces
  - Fine grained power management
  - LFBGA-77 8x8 mm^2 package, RoHS

Description

The STV0913 is a cost-effective, high-performance demodulator-decoder for advanced DVB satellite reception. The device supports DVB-S2 in QPSK and 8PSK as well as DVB-S and DirecTV™ legacy transmission standards.



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1 Overview

The STV0913 features a high-speed DVB-S2 forward error corrector (FEC) which is designed to handle up to 135 channel-Mbits/s at its input. To feed the FEC the STV0913 implements a demodulator, capable of handling QPSK legacy, DVB-S2 constant coding and modulation for satellite broadcast services.

The STV0913 integrates all the features needed to provide a low-cost broadcast satellite receiver solution including: integrated crystal oscillator, DiSEqC controller, tuner I^2C repeater, FSK modem, ancillary DACs and ADCs and many unattributed general purpose input output ports for peripheral control.

A number of state machines and algorithms have been implemented to allow standard functions to be accessed easily and with a minimum of code overhead. Blind scan is implemented allowing an entire band to be searched automatically once a minimum of parameters have been provided. Cold and warm start acquisition and re-acquisition procedures are provided.

Advanced power saving features have been implemented, the LDPC stops once the solution is sufficiently converged and the various blocks of the IC (demodulator, LDPC, Legacy FEC, and so on) may be completely shut down if not required.

Full error monitoring facilities are available and signal statistic are provided via I^2C. For example, antenna pointing may be assisted via the carrier to noise ratio metric or the electrical installation may be judged according to received RF level and equalizer tap readings (reflection intensity).

1.1 Key features for broadcast applications

- Single-channel DVB-S / DVB-S2 demodulator/decoder
- Demodulator:
  - dual 10-bit ADCs
  - one ΣΔ digital RF AGC
  - QPSK, 8PSK
  - CCM
  - automatic detection and configuration of:
    - modulation type
    - filter roll-off
    - symbol rate
    - pilot presence (on/off)
    - long frames only
  - cold or warm start
  - blind recovery of symbol and carrier frequency
- Forward error correction:
  - Viterbi and Reed–Solomon dual decoder (DVB-S)
  - LDPC + BCH dual decoder (DVB-S2)
  - error monitoring
- Transport stream interface:
  - parallel or serial TS interface
  - transport bit rate automatic regulation corresponding to transport clock
  - DVB common interface compliant
- DiSEqC 2.0 interface
- FSK interface
- I^2C repeater
- JTAG interface

The STV0913 has been extensively validated for the broadcast operating range of 1 to 45 Msymb/s in DVB-S2 (QPSK and 8PSK) and 1 to 62 Msymb/s in DVB-S (and DTV legacy). Full test results, reference designs and supporting software are provided.

The maximum DVB-S rate (hard limit) is 67.5 MHz.

Table 1. Maximum symbol rate limitations in DVB-S2 CCM

Modulation	Msymbols/s		
	Demod	LDPC	Single
QPSK	67.5	135	67.5
8PSK	67.5	67.5	67.5

Table 2. DVB-S2 profile implemented and supported for the broadcast market

System configuration	Case	Supported
QPSK	1/4, 1/3, 2/5	No
	1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10	Yes
8PSK	3/5, 2/3, 3/4, 5/6, 8/9, 9/10	Yes
16APSK	2/3, 3/4, 4/5, 5/6, 8/9, 9/10	No
32APSK	3/4, 4/5, 5/6, 8/9, 9/10	No
CCM	-	Yes
VCM(1)	-	Yes
ACM	-	No
FECFRAME(normal)	64800 (bits)	Yes
FECFRAME(short)	16200 (bits)	No
Single Transport Stream	-	Yes
Multiple Transport Stream	-	Yes
Single Generic Stream	-	Yes
Multiple Generic Stream	-	Yes
Combined Single Generic & Single TS	-	Yes
Roll-Off	0,35 0,25 0,20	Yes
ISSYI (input stream synchronizer)	-	Yes
Null Packet Deletion	-	Yes
Dummy Frame insertion	-	Yes
RCS Specific	-	-
SOF & NCR synchronization	-	No

1. VCM is supported in that any MODCODS including dummyPL frames are supported in the carrier but only one MODCOD can output to the transport stream.

Note: The above table refers to broadcast applications. For professional and two-way satellite markets more functionality is available in the Advanced version. Please contact STMicroelectronics for further details.

2 BGA footprint

The ball grid array (BGA) diagram gives the allocation of balls to the package, shown from the top looking down using the PCB footprint.

Table 3. Key to BGA diagrams

Function	Type	Key
Transport	SIG	
Power (DVDD1V1)	VDD	
Power (AVDD1V1)	VDD	
Power (AVDD2V5)	VDD	
Power (DVDD3V3)	VDD	
Ground	GND	
GPIO	SIG	
No connection(1)	NC	NC
No ball		

1. There is no internal connection. Routing is allowed over these balls.

Figure 1. Ball map

	1	2	3	4	5	6	7	8	9	
A	NC	XTALI	AVDD2V5	GND	DVDD3V3	DISEQCOUT	SDA	CLKOUT	NC	A
B	FSKRXIN	XTALO	VREG_2V5O	GND	DVDD3V3	FSKTXOUT	SCL	DPN	ERROR	B
C	GND	GND	DISEQCIN	GND		DVDD3V3	GPIO3_STDBY	D7	STROUT	C
D	QP	QN	GPIO1_DIRCLK	GND	GND	GND	VDD1V1	D5	D6	D
E	IN	IP		GND	GND	GND		D3	D4	E
F	SDAT	SCLT	TDI	GND	GND	GND	VDD1V1	D1	D2	F
G	AGCRF	GPIO5	TCK	GND		VDD1V1	GPIO8	GPIO11	D0	G
H	TDO	GPIO6	TRSTN	GPIO7	VDD1V1	GPIO4_CS0	GPIO9	GPIO12	CLKOUT30	H
J	NC	GPIO0_CLKI	TMS	AVDD1V1	VDD1V1	GPIO2_CS1	GPIO10	RESETB	NC	J
	1	2	3	4	5	6	7	8	9	

Table 4. Ball list arranged by ball number

Ball number	Ball name	Description
A1	NC	Not connected
A2	XTALI	Oscillator in
A3	AVDD2V5	Analog 2V5 supply
A4	GND	Ground
A5	DVDD3V3	Digital 3V3 supply
A6	DISEQCOUT	DISEQC
A7	SDA	I2C serial data
A8	CLKOUT	Clock
A9	NC	Not connected
B1	FSKRXIN	FSK receiver input
B2	XTALO	Oscillator out
B3	VREG_2V5O	2.5V-V regulator
B4	GND	Ground
B5	DVDD3V3	Digital 3V3 supply
B6	FSKTXOUT	FSK transmitter output
B7	SCL	I2C serial clock
B8	DPN	Transport stream data parity
B9	ERROR	Transport stream error
C1	GND	Ground
C2	GND	Ground
C3	DISEQCIN	DISEQC
C4	GND	Ground
C5	NO BALL	No package pin
C6	DVDD3V3	Digital 3V3 supply
C7	GPIO3_STDBY	General purpose Input/Output - standby
C8	D7	Transport stream data
C9	STROUT	Transport stream sync
D1	QP	ADC quadrature phase signal
D2	QN	ADC quadrature phase signal
D3	GPIO1_DIRCLK	General purpose Input/Output - clock dierction
D4	GND	Ground
D5	GND	Ground
D6	GND	Ground
D7	VDD1V1	1.1 V power supply
D8	D5	Transport stream data

Table 4. Ball list arranged by ball number (continued)

Ball number	Ball name	Description
D9	D6	Transport stream data
E1	IN	ADC in phase signal
E2	IP	ADC in phase signal
E3	NO BALL	No package pin
E4	GND	Ground
E5	GND	Ground
E6	GND	Ground
E7	NO BALL	No package pin
E8	D3	Transport stream data
E9	D4	Transport stream data
F1	SDAT	Tuner dedicated SDA signal
F2	SCLT	Tuner dedicated SCL signal
F3	TDI	JTAG test data in
F4	GND	Ground
F5	GND	Ground
F6	GND	Ground
F7	VDD1V1	1.1 V power supply
F8	D1	Transport stream data
F9	D2	Transport stream data
G1	AGCRF	Control Signal for external AGC
G2	GPIO5	General purpose Input/Output
G3	TCK	JTAG test clock
G4	GND	Ground
G5	NO BALL	No package pin
G6	VDD1V1	1.1 V power supply
G7	GPIO8	General purpose Input/Output
G8	GPIO11	General purpose Input/Output
G9	D0	Transport stream data
H1	TDO	JTAG test data out
H2	GPIO6	General purpose Input/Output
H3	TRSTN	JTAG test reset
H4	GPIO7	General purpose Input/Output
H5	VDD1V1	1.1 V power supply
H6	GPIO4_CS0	General purpose Input/Output - CS0
H7	GPIO9	General purpose Input/Output

Table 4. Ball list arranged by ball number (continued)

Ball number	Ball name	Description
H8	GPIO12	General purpose Input/Output
H9	CLKOUT30	Clock
J1	NC	Not connected
J2	GPIO0_CLKI	General purpose Input/Output - clock
J3	TMS	JTAG test mode
J4	AVDD1V1	Analog 1V1 supply
J5	VDD1V1	1.1 V power supply
J6	GPIO2_CS1	General purpose Input/Output - CS1
J7	GPIO10	General purpose Input/Output
J8	RESETB	Chip reset
J9	NC	Not connected

Table 5. Ball list grouped in functions

Ball number	Ball name	Description
G1	AGCRF	Control Signal for external AGC
J4	AVDD1V1	Analog 1V1 supply
A3	AVDD2V5	Analog 2V5 supply
A8	CLKOUT	Clock
H9	CLKOUT30	Clock
G9	D0	Transport stream data
F8	D1	Transport stream data
F9	D2	Transport stream data
E8	D3	Transport stream data
E9	D4	Transport stream data
D8	D5	Transport stream data
D9	D6	Transport stream data
C8	D7	Transport stream data
C3	DISEQCIN	DISEQC
A6	DISEQCOUT	DISEQC
B8	DPN	Transport stream data parity
A5	DVDD3V3	Digital 3V3 supply
B5	DVDD3V3	Digital 3V3 supply
C6	DVDD3V3	Digital 3V3 supply
B9	ERROR	Transport stream error
B1	FSKRXIN	FSK receiver input

Table 5. Ball list grouped in functions (continued)

Ball number	Ball name	Description
B6	FSKTXOUT	FSK transmitter output
A4	GND	Ground
B4	GND	Ground
C1	GND	Ground
C2	GND	Ground
C4	GND	Ground
D4	GND	Ground
D5	GND	Ground
D6	GND	Ground
E4	GND	Ground
E5	GND	Ground
E6	GND	Ground
F4	GND	Ground
F5	GND	Ground
F6	GND	Ground
G4	GND	Ground
J2	GPIO0_CLKI	General purpose Input/Output - clock
D3	GPIO1_DIRCLK	General purpose Input/Output - clock dierction
J7	GPIO10	General purpose Input/Output
G8	GPIO11	General purpose Input/Output
H8	GPIO12	General purpose Input/Output
J6	GPIO2_CS1	General purpose Input/Output - CS1
C7	GPIO3_STDBY	General purpose Input/Output - standby
H6	GPIO4_CS0	General purpose Input/Output - CS0
G2	GPIO5	General purpose Input/Output
H2	GPIO6	General purpose Input/Output
H4	GPIO7	General purpose Input/Output
G7	GPIO8	General purpose Input/Output
H7	GPIO9	General purpose Input/Output
E1	IN	ADC in phase signal
E2	IP	ADC in phase signal
A1	NC	Not connected
A9	NC	Not connected
J1	NC	Not connected
J9	NC	Not connected

Table 5. Ball list grouped in functions (continued)

Ball number	Ball name	Description
C5	NO BALL	No package pin
E3	NO BALL	No package pin
E7	NO BALL	No package pin
G5	NO BALL	No package pin
D2	QN	ADC quadrature phase signal
D1	QP	ADC quadrature phase signal
J8	RESETB	Chip reset
B7	SCL	I2C serial clock
F2	SCLT	Tuner dedicated SCL signal
A7	SDA	I2C serial data
F1	SDAT	Tuner dedicated SDA signal
C9	STROUT	Transport stream sync
G3	TCK	JTAG test clock
F3	TDI	JTAG test data in
H1	TDO	JTAG test data out
J3	TMS	JTAG test mode
H3	TRSTN	JTAG test reset
D7	VDD1V1	1.1 V power supply
F7	VDD1V1	1.1 V power supply
G6	VDD1V1	1.1 V power supply
H5	VDD1V1	1.1 V power supply
J5	VDD1V1	1.1 V power supply
B3	VREG_2V5O	2.5V-V regulator
A2	XTALI	Oscillator in
B2	XTALO	Oscillator out

3 I²C interface

3.1 Introduction

The I²C implementation in the STV0913 follows the *I²C bus specification, version 2.1, January 2000* as edited by Philips Semiconductors.

The STV0913 internal registers have widths of 8 to 64 bits which are accessed using a device master address of 8 bits combined with an internal address of 16 bits.

3.2 I²C chip addresses

The four I²C (device master) addresses are chosen as shown in *Table 6*.

CS0 and CS1 refer to the logic levels applied to the pins CS0 and CS1 at power up or after recovering from a reset.

Table 6. I²C addresses

Access mode	CS1 / CS0			
	0/0	0/1	1/0	1/1
Write	D0	D2	D4	D6
Read	D1	D3	D5	D7

3.3 Identification register

The identification register (*MID*) allows the release version of the IC to be established through the I²C bus:

- an IC with release 1.0 would return a value of 0x10
- an IC with release 2.1 would return a value of 0x21

3.4 Register access

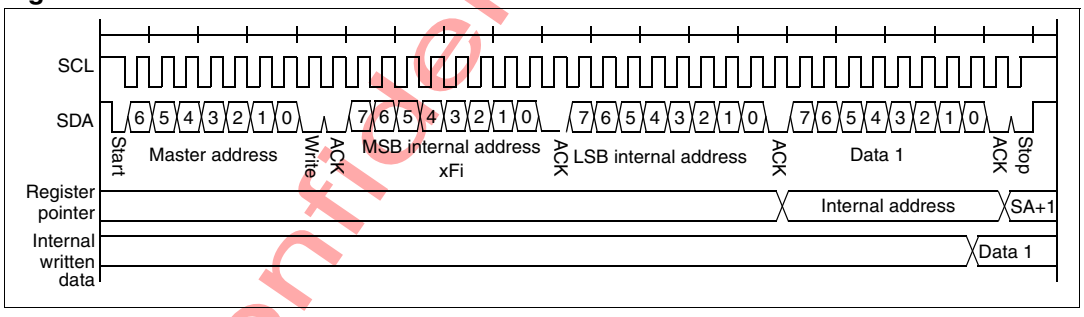
The internal address is passed on a 2-byte field of 16 bits.

3.4.1 Write operation

The byte sequence is:

1. The first byte gives the device master address plus the direction bit (RW = 0).
2. The second byte contains the most significant part of the internal address of the first register to be accessed.
3. The third byte contains the least significant part of the internal address of the first register to be accessed.
4. The next byte is written in the internal register. Following bytes (if any) are written in successive internal registers.
5. The transfer lasts until stop conditions are encountered (SDA and SCL high).
6. The STV0913 acknowledges every byte transfer. The I²C controller puts the SDA line into high impedance after each byte transmitted and the STV0913 drives the line low to acknowledge reception.

Figure 2. 16-bit address write access



3.4.2 Read operation

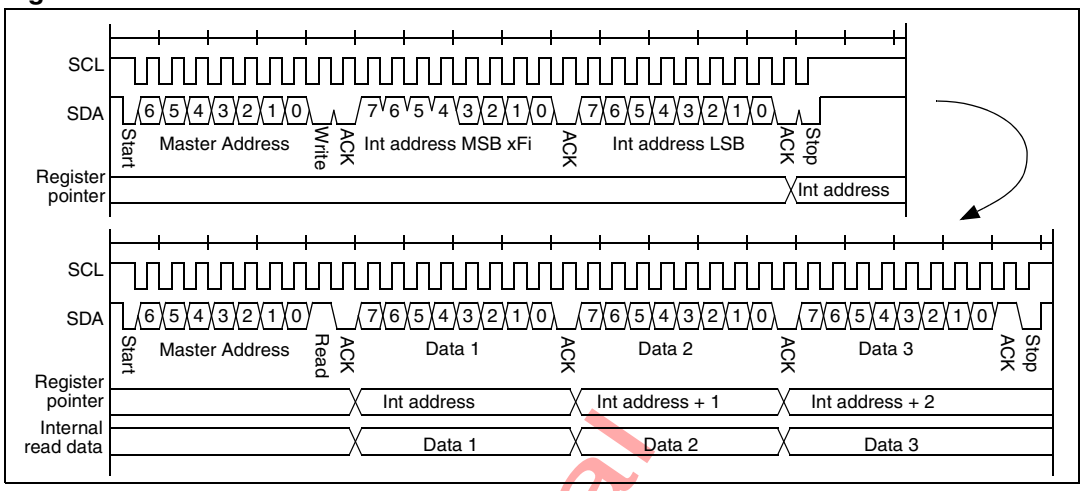
The address of the first register to be read is programmed in a write operation without data. This positions the internal pointer:

1. The first byte gives the device master address plus the direction bit (RW = 0).
2. The second byte contains the most significant part of the internal address of the first register to be accessed.
3. The third byte contains the least significant part of the internal address of the first register to be accessed.
4. A STOP is then sent.

A new start is then followed by the device master address and RW = 1. All following bytes are now data read at successive positions starting from the last write internal address.

5. The first byte gives the device master address plus the direction bit (RW = 1).
6. The second byte is the first byte of data read out (The I²C controller is in high impedance state and the STV0913 drives the SDA line).
7. Subsequent bytes are then read out until a STOP is reached.

Figure 3. 16-bit address read access



3.4.3 Example

Object: to write to device D0, registers F300 to F303 with AA, BB, CC, DD.

CS0 and CS1 are held low, which, from *Table 6*, dictates a write address of D0 and a read address of D1.

Figure 4. Example of normal mode read and write operation

Write registers F300 to F303 with AA, BB, CC, DD and I²C chip address 0xD0

Start	Device addr D0	ACK	Reg addr F3	ACK	Reg addr 00	ACK	Data 0xAA	ACK	Data 0xBB	ACK	Data 0xCC	ACK	Data 0xDD	ACK	Stop

Read registers F302 and F303

Start	Device address, write 0xD0	ACK	Register addr 0xF3	ACK	Register addr 0x02	ACK	Stop
Start	Device address, read 0xD1	ACK	Data read 0xCC	ACK	Data read 0xDD	ACK	Stop

3.4.4 Advanced modes

The I²C bus transactions (clock and data) are oversampled to ascertain their true logic values in a robust manner. The oversampling rate may be varied depending on design goals (rapidity vs. robustness). The fast mode is selected when register bit *I2CCFG*.I2C_FASTMODE is set to high, in this mode a bit is detected using an average of 16 samples. When I2C_FASTMODE is low, averaging is over 41 samples. The sample rate is mclk (default 135 MHz)

The transactions given in the examples above were made using the address pointer increment set to +1. This is useful for reading or writing to banks of consecutive registers. For DiSEqC FIFO and other similar transactions it may be useful to set the increment to zero thereby accessing the same register each read or write cycle. Bit *I2CCFG*.I2CADDR_INC controls this function.

3.5 Standby mode

In standby modes, the I²C bus stays active and the chip can still be awakened by I²C write in the *SYNTCTRL*.STANDBY register field (see *Section 4.3.2: Standby*).

3.6 I²C bus repeater

The STV0913 integrates an I²C bus repeater that, by default, uses pins SDAT and SCLT though any of the GPIO pins configured for the function. See *Chapter 11: General purpose I/O (GPIO)*.

In some applications, signal pollution generated by the SDA/SCL lines of the I²C bus may significantly degrade tuner performance. To avoid this problem, the STV0913 offers an I²C bus repeater for the tuner so the SDAT-SCLT are activated only when necessary and muted otherwise. The repeater is configurable by the register *I2CRPT*.

The SDAT and SCLT pins are set to high impedance at reset. When the microprocessor writes 1 into register bit *I2CRPT*.I2CT_ON, the next I²C message on SDA and SCL is repeated on the SDAT and SCLT pins respectively. There are two options for controlling I²C bus transactions (selectable through *I2CRPT*.STOP_ENABLE). The first (STOP_ENABLE high) causes the I²C repeater to turn off automatically as soon as the next stop bit is encountered. Any size of byte transfer is allowed, regardless of the address, until the stop conditions are detected. If STOP_ENABLE is low the exchanges on the main I²C bus continue to be forwarded on to the I²C repeater bus until the I2CT_ON bit is set low.

To write to the tuner, the external microprocessor must perform the following sequence for each tuner message:

1. Program 1 in *I2CRPT*.I2CT_ON to enable messages to be carried from main I²C bus to the repeater.
2. Send the message to the tuner.
3. If STOP_ENABLE was set high then I2CT_ON will automatically be set to zero on the first stop signal encountered (turning off the I²C repeater); no further action is necessary. If I2CT_ON was low then I2CT_ON must be programmed to zero to disable the repeater line.

Transfers are fully bidirectional. The *I2CRPT*.STOP_SDAT2SDA bit allows return messages from the tuner to be blocked from propagating to the main I²C bus.

The I²C bus repeater is a bidirectional bus. As such the conditions for oscillation on the SDAT line exist. In order to overcome this a sophisticated circuit requiring some tuning has been implemented to allow fast I²C bus transactions without oscillation.

The stability of the I²C repeater depends strongly on residual capacitance and thus on the board layout and may vary from tuner to tuner. Consult tuner datasheet for maximum allowable rise times on I²C bus lines. R, C values may need to be adjusted accordingly.

Stability is obtained by adjusting a the sampling period (and hence delay) in the SDA line. The same sampling period (and delay) may also be introduced in the SCL line if necessary (though not for reasons of stability).

The sampling period is controlled via register *I2CRPT* fields ENARPT_LEVEL and SCLT_DELAY. ENARPT_LEVEL sets the division ratio which controls the delay inserted on the SDAT line. SCLT_DELAY activates the same delay on the SCLT line; this makes the delay equal on both SDAT and SCLT but implements the delay with respect to the main I²C bus.

It is advised to vary empirically the ENARPT_LEVEL around the recommended value to ensure stability in the final application. If further support is required please contact STMicroelectronics field application engineers.

The START, ACK and STOP conditions must be respected.

START condition:

SDA must fall a half clock period prior to SCL falling.

Data: 8-bit data are presented on SCL falling edge and read in (to the tuner) on SCL rising edge.

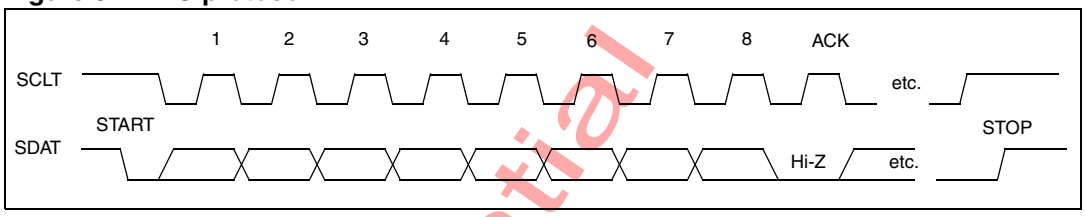
ACK condition:

A ninth SCL pulse with SDA set high-Z is sent. The master then reads that the line has been pulled low by the tuner to complete the acknowledge.

STOP condition:

SCL must rise a half clock period prior to SDA rising.

Figure 5. I²C protocol



If for any reason the master detects the SDA rising whilst SCL is high the transaction will be aborted.

If not used for the I²C repeater, both SDAT and SCLT can be used as general-purpose input/output ports. See *Chapter 11: General purpose I/O (GPIO)*.

4 Clock generation

4.1 Frequency synthesis

The internal clocks are generated by a PLL. The PLL is based on a charge pump, phase detector and VCO which takes its reference from either the XTALI pin of the internal oscillator or the CLKI pin. The CLKI pin is an ancillary clock input (not advised in normal applications).

The default reference frequency is 30 MHz; all electrical characteristics in the specification are validated at this frequency.

The XTALI pins can be driven in two ways—either by using the internal crystal oscillator or by using an external source such as a tuner. The internal oscillator is designed to be used in the frequency range from 27 MHz to 30 MHz. The external clock may be applied from 4 MHz to 30 MHz. It is recommended to use a low phase noise source such as one of STMicroelectronics's tuners.

The PLL operating frequency is given by the following equation:

$$f_{PII} = f_{xtal} \times 2 \times [NDIV / IDF]$$

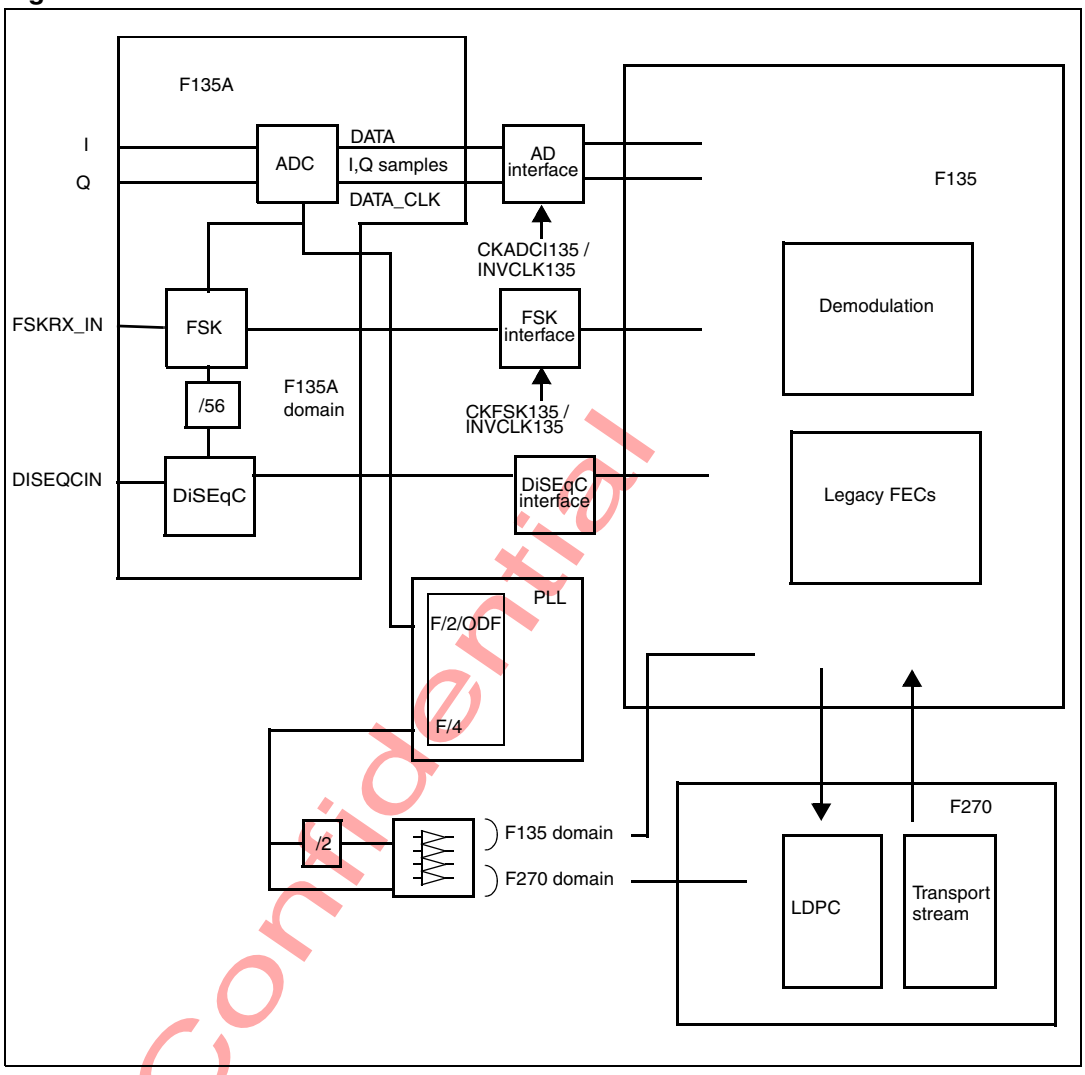
Where f_{xtal} is the crystal oscillator frequency and NDIV is the bitfield of the *NCOARSE1* register and IDF the bitfield of the NCOARSE register.

Clock domains

There are two main clock domains in the STV0913:

- F270/F135 (270/135 MHz) is used by all the digital processing, that is, the transport stream, the LDPC decoder and its interfaces, the demodulation, the legacy forward error correction and the I^2C register control.
- F135A (135 MHz) is used in the clocked analog blocks (ADCs, FSK and DiSEqC). This clock stays in the analog part of the chip to ensure better noise immunity.

Figure 6. Clock domains



Power management

Separating the clock tree into several distinct blocks allows advanced power management features to be used. Through the *STOPCLK1* and *STOPCLK2* registers, clock domains can be activated or shut down as required.

4.2 Starting PLL, power up sequence

Following steps are followed:

1. Configure the pins.
   – DIRCLK = 0: clock is taken from XTALI.
   – STANDBY = 1: put chip in standby mode but I^2C interface active. The I^2C operates with a sample clock frequency of f = f(XTALI).
2. RESETB should transit from low to high (at least 3 ms after last power supply has stabilized).
3. The clock registers, such as NCOARSE should be configured and the demodulator should be disabled in software.
   An appropriate start up sequence is given in the low-level application drivers.
4. Set STANDBY = 0. This starts the PLL. Then switches on the clocks by writing 0 to SYNTCTRL.BYPASSPLLCORE. The preprogrammed register values take effect.
   The I^2C sample rate is now governed by Mclk.

4.3 Clock sources

4.3.1 DIRCLK

When setting the DIRCLK pin, one of two clock paths are chosen. DIRCLK is sampled when recovering from a reset. A reset must be generated after power-up.

- When sampled as 0, the oscillator is active, the PLL is active and the clock is sourced from XTALI. It is the advised functional path.
- When sampled as 1, the PLL is turned off, the oscillator is turned off, the PLL is bypassed and the clock is taken from the CLKI as a PLL bypass application mode (not advised in normal applications).

4.3.2 Standby

The standby mode permits enhanced power saving.

A device enters standby mode when:

- the device powers up and the STDBY pin is tied to VDD
- the device recovers after a reset and the STDBY pin is tied to VDD
- the STANDBY bit in the *SYNTCTRL* register is set using the I^2C bus

In the standby mode all the main functions are stopped except for the reference clock (see CLKOUT30) and the I^2C bus which remains active awaiting new commands. When the standby mode is invoked all internal clocks are turned off except the I^2C clock and the reference clock path. All pads retain their last programmed configuration. This means that any pin configured as push pull will continue to drain current. It is recommended to put the GPIOs in high-impedance state during standby.

4.3.3 Summary

The *Table 7* summarizes the clock control registers.

Table 7. Clock generation registers

Function	Register	Field
Stops all clocks except I^2C	*SYNTCTRL*	STANDBY
Allows external clocks to access digital clock tree		BYPASSPLLCORE
Turns off PLL and VCO		STOPPLL
Oscillator pad enable		OSCI_E
Sets PLL division ratio	*NCOARSE*	MDIV
	NCOARSE1	NDIV
	NCOARSE2	PDIV
		KDIV
Stop individual clock trees	*STOPCLK1*	See register description
Stop individual clock trees	*STOPCLK2*	See register description
Goes high if PLL is locked	*PLLSTAT*	PLLLOCKED

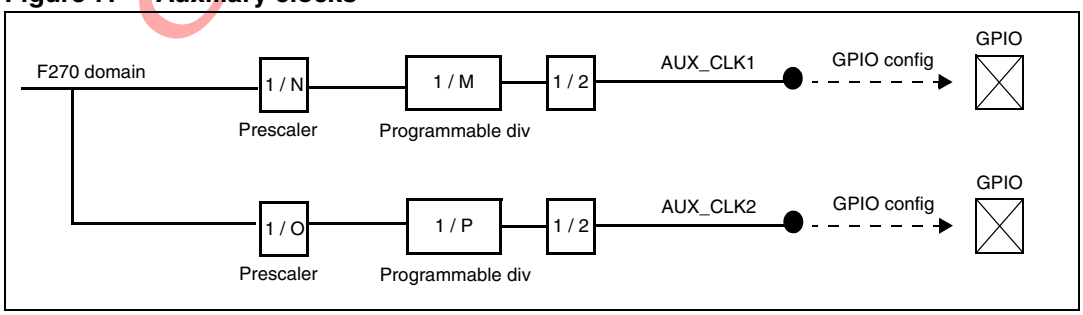
4.4 CLKOUT30

The CLKOUT30 is a pin which replicates the clock generated or re-generated through XTALI.

The output is designed to minimize phase noise degradation and is compatible with driving MPEG decoder ICs. This pin is active as soon as power is applied and is unaffected by a hardware (or software) reset. In this way the system is protected from entering a deadlock state and may safely be used to drive the backend decoder.

4.5 AUX_CLK

Figure 7. Auxiliary clocks



There are two programmable auxiliary clocks. The source frequency is taken from the F135 domain then prescaled, divided and gated before being output though any of the programmable GPIO pins. The prescaler register *ACRPRESC* controls both prescalers.

Programmable divider

Table 8. Prescaler ratios

Prescaler code (ACR_PRESC)	Division ratio (presc_div_ratio)
000	Reserved
001	2
010	16
011	128
100	1024
101	8192
110	65536
111	524288

Table 9. Divider ratios

Divider code (ACR_DIV)	Main divider (main_div_ratio)
0x00	256
0x01	1
0x02	2
...	...
0xFC	252
0xFD	253
0xFE	254
0xFF	255

Register *ACRDIV* field 7:0 are used respectively for AUX_CLK1, AUX_CLK2.

f_{aux} = F135 / (*presc_div_ratio * main_div_ratio*)

Frequencies in the range from 1 kHz to 135 MHz are achievable.

5 Demodulation

The demodulator block performs QPSK and 8PSK demodulation according to DVB-S, legacy DirecTV^{TM} and DVB-S2 specifications.

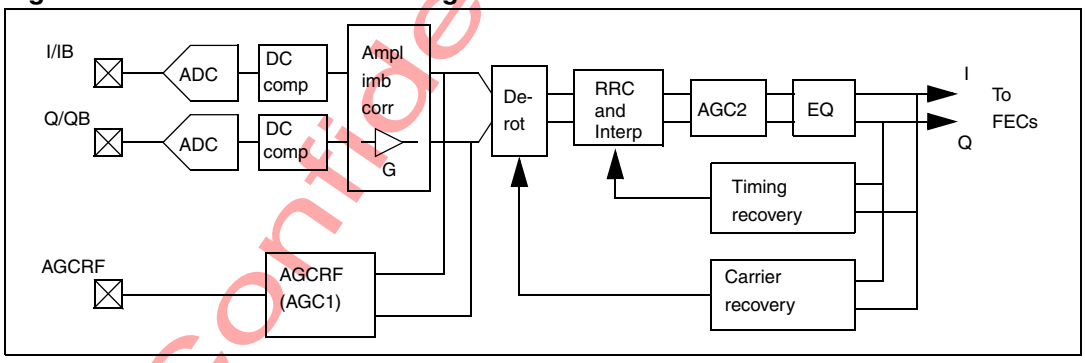
The input signal from the tuner is A-to-D converted on 10 bits. The DC offset, amplitude mismatch and quadrature error are corrected and the AGC signal level to the tuner is calculated. The carrier frequency offset is corrected. Then the signal is subsampled and Nyquist root filtered. The signal amplitude is controlled through the second stage (AGC2) block.

The pilots, when present, are used to help phase lock to the symbol stream. The signal is equalized, descrambled, and passed to the FEC.

An internal state machine controls the automatic acquisition of a channel with various entry points, including warm start (known symbol frequency, small carrier offset), cold start (known symbol frequency and large carrier frequency offset), and blind search (all parameters unknown).

It is possible to observe the internal IQ signal constellation with *ISYMB* and *QSYMB* controlled by *IQCONST*.IQSYMB_SEL.

Figure 8. Demodulator block diagram



5.1 ADCs

Each channel is digitally converted with a 10-bit dual ADC, working at least twice the symbol frequency, typically at 135 MHz.

The input is typically 1 V p-p differential for STB6100, STV6110A or STV6111 tuner.

5.2 DC offset compensation, IQ mismatch and quadrature error correction

The applied DC offset correction may be read in register bits *IDCCOMP*.IAVERAGE_ADJ and *QDCCOMP*.QAVERAGE_ADJ. The maximum correction range is ±63 LSBs.

The bitfield *AGC1AMM*.AMM_VALUE represents the value of the amplitude mismatch, and *AGC1QUAD*.QUAD_VALUE quadrature error angle.

The amplitude correction capability is ±3.5 dB, and the angle correction capability is ± 14 degrees. The amplitude correction applied is Q = I * (1 - alpha) where -0.5 < alpha < +0.5. Alpha corresponds to the signed value of AMM_VALUE. The corrections are applied to the RMS average.

These correction functions may be controlled through the register *AGC1CFG*:

- DC compensation: bits DC_FROZEN and DC_CORRECT
- amplitude compensation: bits AMM_FROZEN and AMM_CORRECT
- quadrature compensation: bits QUAD_FROZEN and QUAD_CORRECT

For each function, there are 3 possible modes:

- no correction
- frozen (parameter updating stopped but correction still applied)
- running (normal mode, reset default state)

5.3 AGC1 tuner level control

The tuner AGC reference value is set via *AGC1REF*.AGCIQ_REF. This field represents the magnitude of the signal on 8 unsigned bits.

AGCIQ_REF = sqrt((I^2 + Q^2)/2)

The AGC time constant is set via *AGC1CN*.AGCIQ_BETA, legal values are 1 (slowest) to 7 (fastest); 0 freezes the operation of the loop, that is, stops the AGC value from being updated (useful during debug).

The gain may be read in registers *AGCIQINx* (16 bits).

The AGC polarity may be inverted through the two bits *PADCFG.AGCRF1_XOR (in SYS registers)*.

The output is pulse density modulated, and must be externally filtered with an appropriate low-pass filter before driving the tuner AGC input.

5.4 Spectrum inversion

In order to facilitate hardware design, the IQ spectrum may be inverted at the input of the IC. This is useful for correcting IQ signal inversions between the tuner and STV0913. For example:

- *TNRCFG2*.TUNER_IQSWAP = 1 (inversion)
- *TNRCFG2*.TUNER_IQSWAP = 0 (no inversion)

When demodulating DVB-S2 signals, spectrum inversion is automatically managed by the control state machine. The state of the spectrum inversion may be interrogated via *PLHMODCOD*.SPECINV_DEMOD.

When demodulating DVB-S1/DirecTV signals the spectrum inversion is managed by the FEC state machine. The state of the spectrum inversion can be found by interrogating *FECM*.IQINV.

Spectrum inversion can be manually forced with *DEMOD*.SPECINV_CONTROL.

5.5 Roll-off factor

The roll-off factor may be configured automatically or programmed manually. This selection is made via *DEMOD*.MANUALSX_ROLLOFF (1 bit) for DVB-S1 and DTV and *DEMOD*.MANUALS2_ROLLOFF for DVB-S2

If manual mode is selected the roll-off factor selected in ROLLOFF_CONTROL is used.

If automatic mode is chosen the following happens. The roll-off is selected in ROLLOFF_CONTROL[1:0] and used during the acquisition of the signal. Once the modulation type has been resolved the Nyquist filter is automatically switched according to:

- DVB-S2, the roll-off factor is read from the MAtype field of the BBHeader and may be observed in registers *MATSTRx* and *TMGOBS.ROLLOFF_STATUS* (this is the definitive indicator)
- DVB-S, the roll-off factor is set to 35%
- DIRECTV legacy, the roll-off factor is set to 20%

5.6 AGC2 signal amplitude control

The AGC2 reference value is set via *AGC2REF*.AGC2_REF. This field represents the magnitude of the signal on 8 unsigned bits.

AGCIQ_REF = sqrt(I^2 + Q^2)

The AGC2 time constant is set via *AGC2O*.AGC2_COEF, legal values are 1 (slowest) to 7 (fastest); 0 freezes the operation of the loop, that is, stops the AGC value from being updated.

The gain may be read in bit AGC2_INTEGRATOR of registers *AGC2Ix*.

5.7 Timing loop

The timing loop core is a second order PLL controlled by two parameters, alpha and beta.

The timing loop has three states: coarse acquisition, fine acquisition and tracking. The execution through these modes when acquiring is controlled via a powerful state-machine described in *Section 5.13*.

- Coarse acquisition: The coarse (and fine) search range may be specified in absolute frequency (manual mode) as defined in *SFRUPx*, (upper bound) and *SFRLOWx* (lower bound). Alternatively, SFRUP and SFRLOW may be calculated (automatic mode) from *SFRINITx*, *SFRUPRATIO* and *SFRLOWRATIO*. The scan mode (automatic/manual) is set in bit 7 of *SFRUP1* and *SFRLOW1*. The boundary conditions depend on the algorithm chosen, see *Section 5.13: Algorithmic entry points (AEP)*. When a border is reached, the scanning is inverted or stopped; an interrupt may be raised when this occurs.
- Fine acquisition: a scanning range is defined automatically as a result of the coarse search. The fineness or speed of the scanning is controlled by parameter *SFRSTEP*.SFR_SCANSTEP. During the initial search the DVB-S alpha and beta parameters are used.
- Tracking: once the modulation type has been identified the state-machine enters tracking mode loading the appropriate loop parameters. For tracking performance reasons separate alphas and betas are required for DVB-S and DVB-S2. They are bits TMGALPHA_EXP and TMGBETA_EXP in registers *RTC* for DVB-S/DirecTV and bits TMGALPHAS2_EXP and TMGBETAS2_EXP in registers *RTCS2* for DVB-S2.

When the state-machine has achieved lock the timing offset may be found in registers *TMGREGx*.

A further function allows the timing offset to be cancelled, that is, the value in registers *TMGREGx* is set to zero and that in registers *SFRx* is adjusted accordingly.

5.8 Timing lock detector

The timing lock indicator (register *DSTATUS*) is a value which is maximized when the timing is locked. Once locked, it is a function of the C/N ratio and the roll-off factor of the transmitted signal, thus the timing lock thresholds need adjusting to optimize lock stability.

The timing lock indicator is filtered with a programmable time constant (register bit *TMGCFG*.TMGLOCK_BETA) and is compared to two thresholds, *TMGTHRISE*.TMGLOCK_THRISE and *TMGTHFALL*.TMGLOCK_THFALL, in order to issue TMGLOCK_QUALITY[1:0], a 2-bit lock indicator with hysteresis (registers *DSTATUS*).

Lock is achieved when TMGLOCK > TMGLOCK_THRISE (MSBs of TMGLOCK_QUALITY), lock loss is declared when TMGLOCK falls below TTMGLOCK_THFALL (LSBs of TMGLOCK_QUALITY).

5.9 Carrier loop

The carrier frequency and phase are corrected by a second order PLL when in tracking mode. During acquisition frequency detection is used:

The carrier loop has three states (same states as the timing loop): coarse acquisition, fine acquisition and tracking. The execution through these modes when acquiring is controlled via a powerful state-machine described in *Section 5.13: Algorithmic entry points (AEP)*.

- Coarse acquisition: a coarse frequency offset is identified. The speed and precision of the search is controlled via register *CARFREQ*. The limits of the coarse frequency search are defined in *CFRUPx* and *CFRLOWx*. The search step is set in *CFRINCx*.
- Fine acquisition: the fine frequency offset is determined using a frequency offset detector. The timer constant of the frequency offset detector is defined in *CARFREQ*.BETA_FREQ. Once the frequency has been determined a phase tracking loop is engaged. The loop parameters are *ACLC* and *BCLC*. If a DVB-S signal is not resolved, a reading of the DVB-S2 header is conducted. The state machine then goes on to fine tune the DVB-S2 acquisition by averaging the frequency offset over many headers. The register *CARHDR*.K_FREQ_HDR controls this process.
- Tracking: for tracking performance reasons separate alphas and betas are required for DVB-S and DVB-S2.
  - DVB-S and DirecTV: loop coefficients are alpha on register *ACLC* and beta on register *BCLC*.
  - DVB-S2: loop coefficients are alpha and beta in registers *ACLC2S2Q* and *ACLC2S28*, respectively, for QPSK (data, pilots and PLHeader symbols) and 8PSK data symbols.

5.10 Carrier lock detector (DVB-S/DirecTV only)

A lock indicator is provided for DVB-S and DirecTV modes only. The lock indicator is based on an accumulator which is maximized when locked to a QPSK signal. The accumulator value may be found in registers *LDI*. This level depends on the current CNR as well as the lock state. Thus, settings adapted for specific code-rates may be required. This value is permanently compared to a programmable threshold set in registers *LDT* (the lock acquired threshold) and *LDT2* (the lock lost threshold). The result is given in *DSTATUS*.CAR_LOCK flag.

When the CAR_LOCK flag is set, the frequency detector is automatically disabled and the demodulator starts phase tracking.

5.11 Equalizer

An equalizer allows for the compensation of echoes on the cable, and/or imperfect channel filtering.

The equalizer converges and tracks (updates) automatically. No operator intervention is required. The equalizer is divided into two parts DFE and FFE.

The update speed of the DFE part is determined in register *Px_EQUALCFG*.MU_EQUALDFE. The equalizer may be switched on or off with bit EQUAL_ON, or may be frozen with bitfield MU_EQUALDFE = 0.

The update speed of the FFE part is determined in register *FFECFG*.MU_EQUALFFE. The equalizer may be switched on or off with bit EQUALFFE_ON, or may be frozen with bitfield MU_EQUALFFE = 0.

5.12 Tuner control

The favoured method of tuner operation is via external driver; STMicroelectronics supplied low level ‘application (LLA) drivers or STTUNER software are available on request.

The I^2C repeater bus must be configured as described in *Section 3.6: I2C bus repeater*.

5.13 Algorithmic entry points (AEP)

The demodulator is managed by a powerful but flexible state machine. The basic method of usage is to initialize the necessary parameters and then start the state machine at the appropriate point. These starting points are known as the algorithmic entry points (AEPs).

Register field *DMDISTATE*.I2C_DEMOD_MODE is used to set the AEP which determines the type of search to be used, the material to be involved and hence the parameters that have to be initialized. Most of the initial parameters will be retained after the completion of an acquisition cycle and need only be set once. Refer to *Section 5.7: Timing loop* and *Section 5.9: Carrier loop* for setting the loop coefficients and search boundaries.

When using the state-machine the two most important parameters are:

- *CFRINITx*: initial carrier offset
- *SFRINITx*: initial symbol rate

Once these parameters are set up, the acquisition may be launched by writing the appropriate AEP value to *DMDISTATE*.I2C_DEMOD_MODE.

The symbol rate search limits may be set either automatically or defined manually.

The automatic mode is invoked by default after a reset.

In automatic mode the symbol rate boundaries are expressed as a percentage of the initial symbol rate (+/- 25% at reset). The symbol rate range boundaries may be finely adjusted by programming SFRUPRATIO(0xF455) and SFRLOWRATIO(0xF456).

In manual mode the boundaries are expressed as absolute symbol rate values. Manual symbol rate search is invoked by setting *SFRUP1*:AUTO_GUP(0xF460[7])=0 and *SFRLOW1*:AUTO_GLOW(0xF462[7])=0

The hard symbol rate boundaries may then be programmed in

SFRUPx:SFRUP(0xF460,0xF461[14:0]) and

*SFRLOW*x:SFRLOW(0xF462,0xF463[14:0]).

The AEP (I2C_DEMOD_MODE) values:

1. **Blind Scan** (symbol rate, carrier offset and modulation unknown; demodulator will lock to the nearest channel).

- 0x00: Zero offset start.
  a) Required values: *CFRINC*x (if in manual mode) and SFRINITx. SFRINITx is given as approximate start value.
  b) *CFRINCx* is the carrier frequency step size used in the carrier frequency search algorithm. *CFRINITx* is automatically set to zero offset at the start of the search.
  c) The demodulator will then attempt to find the symbol rate, carrier offset, modulation type (DVB-S2, DVB-S or DirecTV) and code rate.
  d) If the demodulator does not find a signal at that frequency the state-machine re-starts with a new value of *CFRINITx* and expands, with step given by register *CFRINCx*, from the initial frequency using a zig-zag algorithm until a signal is found or the boundaries reached. The value of *CFRINCx* must be small to capture narrow channels.
- 0x01: best guess start.
  – Same as 0x00 except *CFRINITx* and *SFRINITx* are given as approximate start values.

2. **Cold start**: (carrier offset unknown, symbol rate known).

- 0x15: Zero offset start.
  – Program *SFRINITx*.
- 0x05: best guess start.
  – Same as 0x15 but requires *CFRINITx*.

3. **Warm start** (carrier offset known, symbol rate known).

- 0x18: Zero offset start.
  – SFR and CFR are used as start point. *CFRINITx* and *SFRINITx* required to set limits.

4. **Others**

- 0xA: As per 0x18 but for DVB-S1/ legacy DIRECTV only.
- 0xB: As per 0x18 but for DVB-S2 only.
- 0x1C: demod stop.
- 0x1F: reset demod state-machine.
- 0x14: next channel.
  – Nothing to program before launching.
  – The demodulator finds the next channel (or preceding channel according to selected search direction). The search is linear (not zig-zag). Direction of search is given by *CFRICFG*.NEG_CFRSTEP.
- 0x11: bandwidth scan.
  – The analogue tuner bandwidth is searched for channels (useful for low symbol rates).

5.14 Results FIFO

It is possible to observe final and intermediate working results in the demodulator. After each channel is acquired, results are stacked in a FIFO (accessed by registers *DMDRESDATAx*). These registers contain all of the important data found by the demodulator:

- symbol rate
- carrier offset
- tuner frequency
- modulation type / code (DVB-S2, DVB-S or DirecTV with their roll-off, mapping, puncture rate and spectrum inversion) or tag “Undecodable Channel” (giving important data to correct any problem)

“Undecodable Channel” tag indicates that there is clearly something at this position but the demodulator could not determine its code (too much noise or unknown code). For instance, analog channels are tagged “Undecodable Channel”.

The FIFO is used by the auto-scan AEP (0x11 and 0x1B, see below) to stack its results.

There are up to 15 results (current number given by *DMDRESADR*.DMDRES_RESNBR) so, the stacked results must be regularly de-stacked.

A facility exists to pause the demodulator when the stack becomes full.

5.15 Interrupt controller

The demodulator can generate interrupt signals for the host processor for the following events:

- AGC1, AGC2, carrier offset and/or symbol rate overflow -> no signal
- no signal after coarse search (blind search)
- undecodable channel (timing lock but impossible to determine if it is a DVB-S2, DVB-S or DirecTV signal)
- undecodable channel (no timing lock)
- DVB-S2 lock
- DVB-S2 delock
- DVB-S/DirecTV lock
- DVB-S/DirecTV delock
- autoscan done
- threshold indicators 1 and 2
- rain fade indicator
- carrier offset is out of *CFRUPx* to *CFRLOWx* limit and/or symbol rate is out of *SFRUPx* and *SFRLOWx* limit
- results FIFO is full
- results FIFO is almost full

The cause of the last interrupt is given on field *DMDFLYW*.I2C_IRQVAL. Previous interrupt events are overwritten.

5.16 Noise indicators

Two methods of measuring noise are available:

- Data: measures the absolute noise on all data symbols (but not on pilots, PLHeader or DummyPL frames). This is the only relevant measurement for a DVB-S/DirecTV signal. The value of the indicator is a monotonic function of the noise, and must be corrected by look-up table in the host. This method is compatible with STMicroelectronics legacy demodulators.
- Header: measures the noise on the pilot/header and DummyPL frames (if any). The measurement needs to be averaged over a large number of blocs to be precise. The value is directly proportional to the noise power. This method is more accurate when measuring DVB-S2 signals.

A number of methods of reading the noise value are provided. They include the raw noise magnitude, the noise power, noise normalized to the signal level and a quadratic value where the square of the noise level is ratioed with the signal power (equivalent to CNR). The measurements may be found in the following registers:

- *NOSDATATx*: absolute raw noise level measured on data only
- *NNOSRADx*: normalized linear radial noise level measured on pilots or imaginary pilots
- *NNOSFRAMEx*: normalized square of the noise level (raw computed value divided by agc2_ref) measured on data only and by frame
- *NNOSDATATx*: normalized noise level (raw computed value divided by agc2_ref) measured on data only
- *NNOSDATAx*: normalized square of the raw noise level (noise power divided by $agc2\_ref^2$) measured on data only (CNR)
- *NNOSPLHTx*: normalized noise level (raw computed value divided by agc2_ref) measured on headers only
- *NNOSPLHx*: normalized square of the raw noise level (noise power divided by $agc2\_ref^2$) measured on headers only (CNR)

5.17 C/N estimator

Coupled with the noise indicators described above, a table has been implemented to give a C/N estimation directly in dB.

It is made of 128 lines of a triplet NNOSPLHT-NNOSDATAT-C/N. Based on the real-time value of NNOSPLHT (DVB-S2) or NNOSDATAT (DVB-S1-DTV), an estimate of the current C/N is made by interpolation. It can be read on registers *NOSRAMPOS*/*NOSRAMVAL*, field NOSRAM_CNRVAL.

The CNRVAL is in 1/10th of dB with a maximum value of 51.1 dB, for example, NOSRAM_CNRVAL as a maximum value of 511 (or 0x1FF).

The table is loaded as booting time by means of registers *NOSRAMCFG*, *NOSRAMPOS* and *NOSRAMVAL*.

To load the table in standard mode, please follow this operating mode:

1. Write 0x00 then 0x18 to *NOSRAMCFG*
2. Write 0x00 to *NOSRAMPOS*
3. Write 0x99 to *I2CCFG* to enable I2C address auto increment and be able to write the data in long I2C writes
4. for each table line, Write 6 bytes to *NOSRAMVAL*. The message is structured as 16 bits NNOSPLHT then 16 bits NNOSDATA then 10 bits CNR padded with 6 bits of zeros
5. Write a last line as 0x 00 00 00 00 7F C0
6. Write 0x88 to *I2CCFG* to return to normal I2C mode
7. Write 0x28 to *NOSRAMCFG* to start the C/N estimator

5.18 Other indicators

5.18.1 Threshold indicators

There are two threshold indicators going to '1' or raising the IRQ when the C/N level is equal or less than a programmed value.

These indicators, DSTATUS4/NOSTHRES1_FAIL and DSTATUS4/NOSTHRES2_FAIL, have their threshold programmed in registers NOSTHRESx by two methods depending on RAINFADE/NOSTHRES_UNITS:

- When 0, the unit of the registers is the normalized noise level divided by 64, for example, NNOSPLHT/64 when DVB-S2 and NNOSDATAT/64 when DVB-S1/Legacy DTV. The threshold indicators are raised when the noise level is upper than the programmed thresholds.
- When 1, the unit of the registers is the C/N in dB (the C/N estimator must be enabled). The threshold indicators are raised when the C/N level is lower than the programmed thresholds.

Also a margin indicator is available, NOSDIFF1, measuring the margin above the threshold indicator 1 there is. The unit are the same as NOSTHRESx.

5.18.2 Rain fade indicator

A rain fade indicator is available in DSTATUS4/RAINFADE_DETECT. It indicates when a C/N dB drop over a sliding time window occurs. The dB drop value is set by RAINFADE/RAINFADE_CNLIMIT from 1 to 6 dB and the time window is set by RAINFADE/RAINFADE_TIMEOUT from 1 to 7 minutes.

6 DVB-S forward error correction

6.1 FEC modes, status and error reporting

By default the appropriate FEC (DVB-S1 or DVB-S2) is automatically selected by the demodulator (observable and controllable by register bits *DMDCFGMD*.DVBS1_ENABLE) depending on the mode discovered during acquisition.

The viterbi decoder is configured through register *FECM*. By default it automatically switches between DVB-S and legacy DirecTV™ modes (result observed with bit DSS_DVB). This automatic feature may be disabled if bit DSS_SRCH is reset, DSS_DVB becoming the control bit. As an option (only for special uses), the sync byte search can be de-activated (with SYNCVIT) and IQ swap can be enforced (register bit *DEMOD*.SPECINV_CONTROL).

The read-only register *VSTATUSVIT* reports the viterbi status (active, locked, sporadic delock events). Register bitfield *VITCURPUN*.VIT_CURPUN reports the puncture rate found. The modulation scheme is always QPSK.

Register bitfield *VERROR*.REGERR_VIT reports a ratio of the average number of bit errors the viterbi decoder has found and corrected over a predefined interval. The number of bits used for averaging can be programmed through the *VAVSRVIT*.SNVIT field. A maximum mode (*VITSCALE*.VERROR_MAXMODE set) reports the maximum REGERR_VIT (register *VERROR)* value (the peak) encountered.

When decoding DirecTV legacy signals which are highly loaded by null packets (more than around 50%), a feedback from the Reed–Solomon decoder is invoked. This feedback may be disabled through *VITSCALE*.DIS_DTV67_FLOCK.

For information, viterbi decoder mode results (puncture rate, DVB-S/DirecTV, IQ swap status) are stacked in the results FIFO of the demodulator.

6.2 Viterbi decoder

The convolution codes are generated by the polynomial G_x = 171 bytes and G_y = 133 bytes in both DVB-S and legacy DirecTV modes.

The viterbi decoder computes the metrics of the four possible paths for each symbol, proportional to the square of the euclidian distance between the received I and Q and the theoretical symbol value.

The following puncture rates have been implemented in both DVB-S and legacy DirecTV modes:

- 1/2
- 2/3
- 3/4
- 5/6
- 6/7
- 7/8

To optimize search time the allowed rates can be enabled or disabled by programming register *PRVIT*.

Note: To minimize the viterbi search time, the puncture rates 3/4, 5/6, 7/8 can be disabled in legacy DirecTV *mode. In DVB-S mode, the puncture rate 6/7 can be disabled.*

A search algorithm acquires the puncture rate and phase, the resulting signal path error rate is compared to a programmable threshold. If it is greater than this threshold, another phase (or another rate) is tried until an acceptable error rate is obtained. Therefore the search algorithm steps through phases and puncture rates until an error rate below the threshold is found. The error threshold can be set for each puncture rate (registers *VTH12*, *VTH23*, *VTH34*, *VTH56*, *VTH67*, *VTH78*).

The viterbi software decision processing can be scaled through registers *KDIV12*, *KDIV23*, *KDIV34*, *KDIV56*, *KDIV67*, *KDIV78*. It is recommended to use the reset values unless STMicroelectronics recommends other values.

6.3 Synchronization

The DVB packet length, after inner decoding, is 204 bytes. The sync word is the first byte of each packet. Its value is 0x47, but this value is complemented (inverted) every eight packets. In the legacy DirecTV system, the packet length is 147 bytes and the sync word a constant, 0x1D.

When the puncture rate and its phase have been found, a sync word search is started. An up/down sync counter counts whenever a sync word is recognized with the correct timing, and counts down during each missing sync word. This counter is bounded by a programmable maximum (register bitfield *VAVSRVIT*.HYPVIT). When this value is reached, bit *VSTATUSVIT*.LOCKEDVIT is set. When the event counter counts down to 0, this flag is reset.

The time-out period for this sync word search is selectable through register bitfield *VAVSRVIT*.TOVVIT.

This lock definitively locks the demodulator.

6.4 Convolutive de-interleaver

In DVB-S mode, the convolutive de-interleaver is 17 x 12. The period of 204 bytes per sync byte is retained. In the legacy DirecTV system the convolutive de-interleaver is 146 x 13, and also a period of 147 bytes per sync byte. The de-interleaver can be bypassed (see register bit *TSSTATEM*.TSDIL_ON).

6.5 Reed–Solomon decoder and descrambler

The input blocks are 204 bytes long with 16 parity bytes in DVB mode. The sync byte is the first byte of the block. Up to eight byte errors can be fixed.

The code generator polynomial is:

$$g(x) = (x - \omega^0)(x - \omega^1)...(x - \omega^{15})$$

over the galois field generated by:

$$x^8 + x^4 + x^3 + x^2 + 1 = 0$$

Energy dispersal descrambler (DVB-S only) and output energy dispersal descrambler generator:

$$x^{15} + x^{14} + 1$$

The polynomial is initialized every eight packets with the sequence 100 1010 1000 0000. The sync words are unscrambled. The descrambler activity is controlled by register bit *TSSTATEM*.TSDESCRAMB_ON. Descrambler is activated (or de-activated) only if the regular presence of an inverted sync word each 8 packets is detected.

The Reed–Solomon decoder correction is controlled through bit *TSSTATEM*.TSRS_ON.

Finally the demodulated and decoded data is presented to the transport stream manager.

7 DVB-S2 forward error correction

7.1 Introduction

This block includes three main functions:

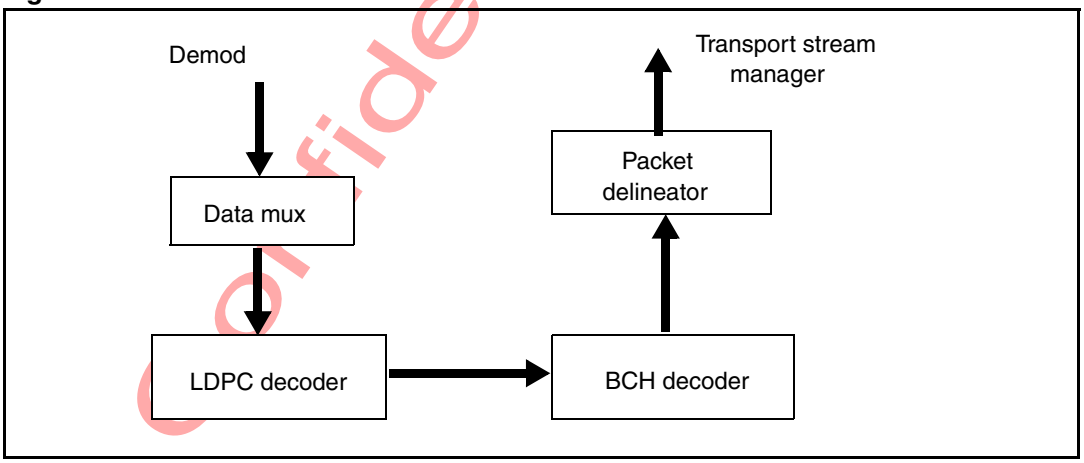
- an LDPC decoder
- a BCH decoder
- a packet delineator

The DVB-S2 LDPC/BCH decoder has an input interface and a single output interface. The data coming from the demodulator is multiplexed and decoded by the same engine. After decoding, a packet delineator do the demultiplexing and DVB-S2 de-framing before sending data to the output transport stream manager.

For a 270-MHz clock we may have a maximum data rate of 135 Mbit/s at the input to the FEC decoder.

7.2 Architecture

Figure 9. DVB-S2 FEC architecture



7.3 Features summary

- LDPC decoder

  The LDPC decoder can decode normal frames (64800 bits), and 8 code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9 and 9/10).
- BCH decoder

  In addition the BCH decoder is able to correct up to 12 bits for code rates where more than 192 redundancy bits are available. As such, correction is only possible up to 10 bits for 2/3 and 5/6 code rates, and only up to 8 bits for 8/9 and 9/10 code rates.
- Packet delineator

  The packet delineator is used for descrambling, checking the integrity of BBFrame headers, processing the cache and data fields and providing a lock indicator.

7.3.1 Single input functional description

- Normal FEC frame with 8 code rates
- De-interleaving on 8PSK with inversion for 3/5
- Bit rate up to 135 Mbit/s, on only one input buffer

7.4 LDPC/BCH decoder

This FEC is capable of decoding DVB-S2 CCM/VCM signals. It performs:

- bit de-interleaving
- inner code decoding (LDPC)
- outer code decoding (BCH)

For ACM functional description, see STV0913 Advanced Annex.

7.4.1 Supported MODCODs

The LDPC decoder supports 14 MODCODs in Normal FEC Frame (64800 bits).

Table 10. MODCOD encoding

Mode	MOD COD	Mode	MOD COD	Mode	MOD COD	Mode	MOD COD
		QPSK 5/6	9_D	8PSK 9/10	17_D		
		QPSK 8/9	10_D				
		QPSK 9/10	11_D				
QPSK 1/2	4_D	8PSK 3/5	12_D				
QPSK 3/5	5_D	8PSK 2/3	13_D				
QPSK 2/3	6_D	8PSK ¾	14_D				
QPSK 3/4	7_D	8PSK 5/6	15_D				
QPSK 4/5	8_D	8PSK 8/9	16_D				

7.4.2 Iteration control

The number of iterations carried out by the LDPC can be scaled up or down to optimize throughput, decoder performance, and power dissipation for a given application, depending on the operating frequency.

The number of iterations are programmed by the 14 registers for each stream x Px_NBITER_NFn for normal FEC frames. The trailing number of the register name is the MODCOD number (see *Table 10*).

7.4.3 Input gain

For each frame, for each modulation (QPSK, 8PSK), for each code rate (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10), it is possible to change the input gain applied on the input software decision values of the LDPC. This is programmable by the *GAINLLR_NFx* registers. Reset values correspond to a gain equal to 1. The 7-bit register value allows a gain between 0 and 4 (that is, from 0 to 127 / 32).

7.5 Packet delineator

This block manages the interface between the DVB-S2 channels and the transport stream outputs.

The control and monitoring registers of this block are in the address range 0xF550-0xF56F. The control registers are *PDELCTRL1*-2 and the block status can be monitored with registers *PDELSTATUS1*-2.

The main functions of the packet delineator are listed as below.

- Descrambling: recovery of BBFRAME.
- Base band frame header (BBH) integrity checking: cyclic redundancy checksum (CRC 8 bits) validation.
- Lock monitoring: consecutive valid blocks are detected and compared with threshold registers with lock hysteresis.
- Header processing and transport stream filtering: BBH fields are stored and communicated to the transport stream block.
- Data field processing: this process extracts and generates standard user packets. Payload CRC computation and sync byte insertion are made on the fly.
- SYNCD estimation: in the case of corrupted BBHEADER the SYNCD is calculated.

7.5.1 Descrambling

The complete DVB-S2 BBFRAME received from the FEC decoder is de-scrambled. The descrambling sequence is synchronous with the BBFRAME, starting from the MSB and ending after Kbch bits.

The (de) scrambling sequence is generated by the feed-back shift register. The polynomial for the pseudorandom binary sequence (PRBS) generator is:

$$1 + X14 + X15$$

Loading of the sequence (100 1010 1000 0000) into the PRBS register, is initiated at the start of every BBFRAME.

7.5.2 Baseband frames header (BBH) integrity checking

The useful part of the incoming stream (excluding the sync byte) is processed by a systematic 8-bit CRC encoder. The generator polynomial is:

$$g(X)= (X5 + X4 + X3 + X2 + 1)(X2 + X + 1)(X + 1) = X8 + X7 + X6 + X4 + X2 + 1$$

The CRC encoder output is computed as: CRC = remainder [X8 u(X): g(X)] where u(X) is the input sequence (data, 8 bits) to be systematically encoded.

The number of erroneous frames is available in *BBFCRCKOx*.

7.5.3 Lock monitoring

This block uses the BBHEADER CRC check result to drive an up/down counter. The counter counts up whenever a CRC check is correct, and counts down if not correct. If this counter is above *HYSTTHRESH*.DELIN_LOCK_THRESHOLD, *PDELSTATUS1*.PKTDELIN_LOCK is set. If it goes below *HYSTTHRESH*.UNLOCK_THRESHOLD, it is reset.

The *PDELSTATUS1*.FIRST_LOCK register is simpler. Once its value has been reached it is set and indicates that the packet delineator has started to treat frames.

7.5.4 Header processing and transport stream filtering

A dedicated mechanism identifies the incoming streams based on the MATYPE information. A fixed length base-band header (BBHEADER) of 10 bytes is inserted in front of the data field, describing its format. The MATYPE can be found in the read-only register *MATSTRx*.

MATYPE (2 bytes) describes the input stream format, the type of mode adaptation and the transmission roll-off factor. All the stream information fields are stored in registers *MATSTRx*, *UPLSTRx*, *DFLSTRx*, *SYNCSTR* and *SYNCDSTRx*.

SIS/MIS (1 bit) describes whether there is a single input stream or multiple input streams. If SIS/MIS = multiple input stream, then the second byte is the input stream identifier (ISI), otherwise the second byte is reserved.

In the case of multiple input streams, ISI filtering can be activated. In this case only BBFRAMES with the correct ISI will be forwarded to the transport stream.

7.5.5 Data field processing

The packets are assembled into groups of the appropriate byte length (including sync bytes). For example, MPEG packets are assembled into groups of 188 bytes.

A CRC is computed for each packet which provides the ERROR signal on the transport stream output.

7.5.6 SYNCD estimator

In case of failure of BBHEADER CRC check it is assumed the BBHEADER is corrupted. This means the SYNCD value must be considered as potentially wrong. In this case SYNCD is estimated. The object being to ensure the integrity of the shared packet between the previous BBFRAME and current (corrupted) BBFRAME.

7.5.7 BCH check

A final frame verification, based on the BCH check result, has been implemented. If one single error occurs anywhere in the frame the entire frame will be rejected. This service was made available because occasionally errors may occur in the BB header that fool the relatively weak CRC check.

For BCH check on: PDELCTRL2[bit 0]=1, PDELCTRL3[bit 5]=1.

For BCH check off: PDELCTRL2[bit 0]=0, PDELCTRL3[bit 5]=0.

8 Transport stream interface

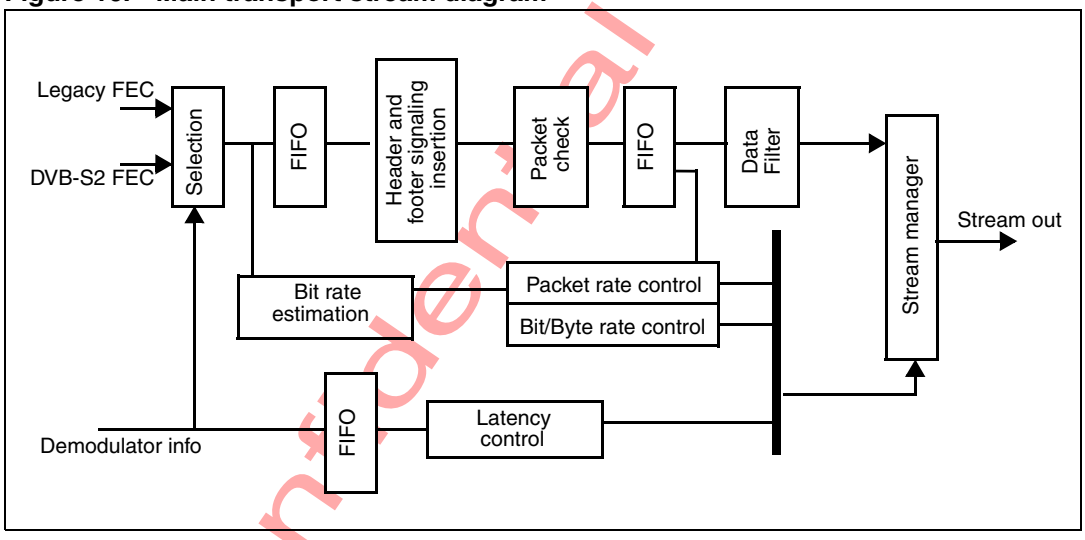
The transport stream (TS) interface takes data from the DVB-S2 or legacy Reed–Solomon forward error correctors and formats the data for transmission to the back-end decoder.

TS can be configured in serial or parallel mode.

8.1 Transport stream overview

The block diagrams of the TS block are shown in *Figure 10* below.

Figure 10. Main transport stream diagram



8.2 Transport stream output processing

The stream may be formatted with or without sync bytes or header bytes and the output rate may be controlled manually or adjusted automatically.

The register *TSINSDELH* allows the sync and header bytes in an MPEG packet to be removed. This is useful when using external bit error rate test equipment.

Each TS line is programmed respectively by *TSCFGH/M/L* registers.

The TS interface is DVB-CI compliant but also supports some extended behavior.

8.2.1 General

The transport bus is made of the following pins: CLKOUT, STROUT, DPN, ERROR and D7 to D0 in parallel mode or only D7 in serial mode.

After a hardware reset, the transport bus is set to high impedance (disabled) and must be configured to low impedance (enabled) by programming register *OUTCFG*. TS can be serial or parallel. For TS, there are two control bits to configure the pins; one for the serial part (control signals + data 7) and one for the data bits 6:0.

The transport stream is activated when one of the FEC decoders outputs valid data. The transport stream remains active until lock loss is detected.

The DPN (data valid / parity negated) pin is high when payload data is being output from the FEC. The DPN signal is low when redundant data is present (redundant data can be the parity data or rate regulation stuffing bits).

Data is regulated by both CLKOUT and DPN. There are two regulation modes known as ‘data valid’ and ‘envelope’. The data valid mode uses a continuous clock and selects valid data on DPN. The envelope mode indicates the periods of valid data on DPN and then uses a punctured clock for rate regulation. The regulation mode is selected by register bit *TSCFGH*. TSFIFO_DVBCI (1 for a data valid mode, 0 for the envelope mode)

The polarity of CLKOUT signal is selected with bit XOR. The change can be done with bit TS1_CLKOUT_XOR of the register *OUTCFG2*.CLKOUT_XOR = 0 the output signals are valid on the rising edge of the CLKOUT signal (on the falling edge if CLKOUT_XOR = 1).

8.2.2 Data rate control

The TS interface controls the output data rate. Padding bits are generated automatically according to the instantaneous bit rate and actual output data rate. The configuration is set in field TSFIFO_MANSPEED. Four modes are provided, three of them are fully automatic and the fourth allows manual control of the regulation. The fully automatic mode is recommended, see *Table 11*.

Table 11. TSFIFO_MANSPEED configuration

TS Rate Control Mode	TSFIFO_MANSPEED
Manual	11
Fully automatic	00
Conservative automatic	01
Dynamic automatic	10

For all configurations, the output data rate is:

- serial interface, data rate = bit rate = mclk * 32 / TSFIFO_OUTSPEED
- parallel interface, data rate = byte rate = mclk * 4 / TSFIFO_OUTSPEED

Where mclk = 135 MHz, and TSFIFO_OUTSPEED is the field of the register *TSSPEED*. The speeds allowed are summarized in *Table 14*. If the value of TSFIFO_OUTSPEED is less than allowed, it will be clipped to the minimum allowed value.

Table 12. TS allowed speeds

TS mode	Min rate	Max rate
Serial	17 MHz TSFIFO_OUTSPEED = 0xFF	135 MHz TSFIFO_OUTSPEED = 0x20
Parallel	4.25 MHz TSFIFO_OUTSPEED = 0xFF	67.5 MHz TSFIFO_OUTSPEED = 0x08

Some TSFIFO_OUTSPEED values can create a clock with a duty cycle not equal to 50%. To ensure a clock duty cycle of 50%, the bit TSFIFO_DUTY50 of the register *TSCFGH* can be set. It will constrain TSFIFO_OUTSPEED to be:

- a multiple of 32 in serial mode
- a multiple of 4 in parallel mode

Automatic mode (recommended)

In this case, the chip computes TSFIFO_OUTSPEED from these data:

- packet rate
- header and footer (if any) signaling rate
- Reed–Solomon parity (if any) rate

The packet rate equations are

DVB-S1, packet rate = SR * mapping * PR / UPL

DVB-S2, packet rate = SR * DFL * (NPDav + 1) / (PLFL * UPL)

Where:

SR = symbol rate

Mapping = 2 for QPSK, 3 for 8PSK, etc.

PR = puncture rate

UPL = packet length in bit (for example, 204x8 in DVB-S1)

DFL = datafield length

PLFL = PLFrame length

NPDav = mean value of NPD byte if MATYPE/NPD = 1 or 0 if MATYPE/NPD = 0

In automatic mode the chip recomputes TSFIFO_OUTSPEED after any change in one parameter involved in the equations.

Other automatic modes

- Not recommended

Manual mode

In manual mode, the user sets the desired speed with by programming the TSFIFO_OUTSPEED register. Should the required data rate exceed the capacity, the start of the next packet will overwrite the end of the current packet.

8.2.3 Latency control

In the STV0913 the total latency from the signal entering the pins IQ to the output on one of the transport stream bus is controlled, fixed and known, see *Table 13*.

Table 13. Chip total latency

Mode	Total latency(1)
Legacy DVB-S1	58404 symbols
Legacy DTV	22848 symbols
DVB-S2	71680 symbols

1. these values might change slightly.

8.3 Serial output modes

In serial mode the data is output MSB first. The serial mode supports both rate regulation modes in the following way.

- Serial output mode with pin DPN used as data valid signal for discriminating between wanted data and "*don't care*" bits, *Figure 12* and *Figure 14*.

  In this mode, the CLKOUT clock signal is continuous. The desired rate is obtained by skipping the unwanted data using the DPN signal. The 'holes' in DPN signal are automatically inserted with regards to both the actual data payload rate (including the parity bits when present) and the CLKOUT frequency.

- Serial output mode uses the DPN signal as an envelope for the valid data section of the transport stream; the CLKOUT signal is then interrupted ('punctured' in order to skip the unwanted data *Figure 13* and *Figure 15*.

  In this mode, the DPN data valid signal is used as an envelop to the useful data, excluding the parity bits. The CLKOUT signal is used to reach the actual payload rate: holes are automatically inserted in the regular periodic clock signal to adjust the mean frequency to the desired payload rate.

The STROUT pin is high during the first bit of the packet payload.

The rate compensation mode (TSCFGH:TSFIFO_DVBCI bit) is set as in *Table 14*.

Table 14. Rate compensation mode settings

	Serial1 mode = data valid	Serial2 mode = envelope
TSFIFO_DVBCI	1	0

Figure 11. Serial output interface (CLKOUT_XOR = 1), data valid

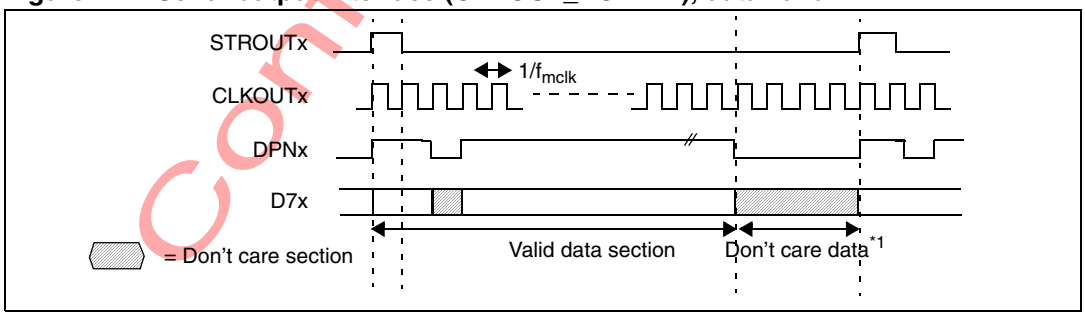


Figure 12. Serial mode options in valid data section (CLKOUT_XOR = 0), data valid

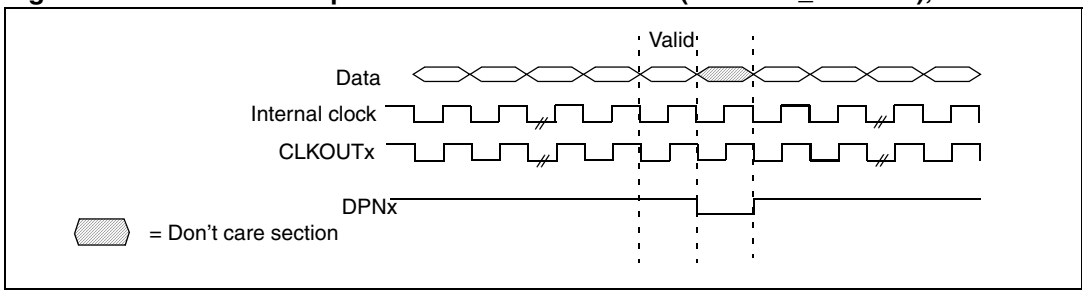


Figure 13. Serial output interface (CLKOUT_XOR = 1), envelope

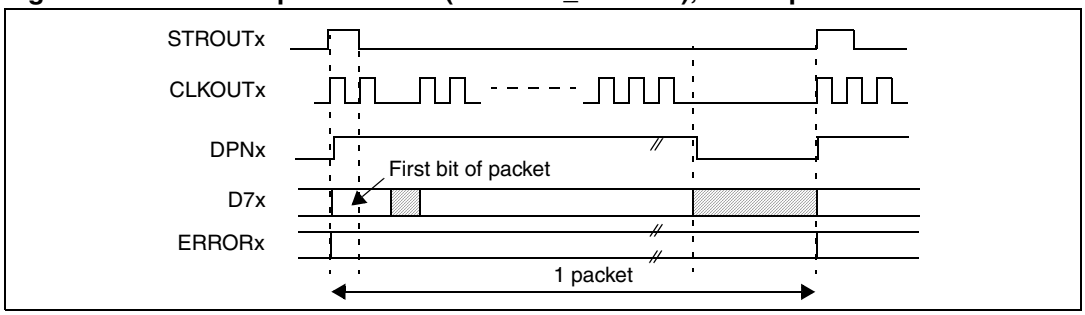
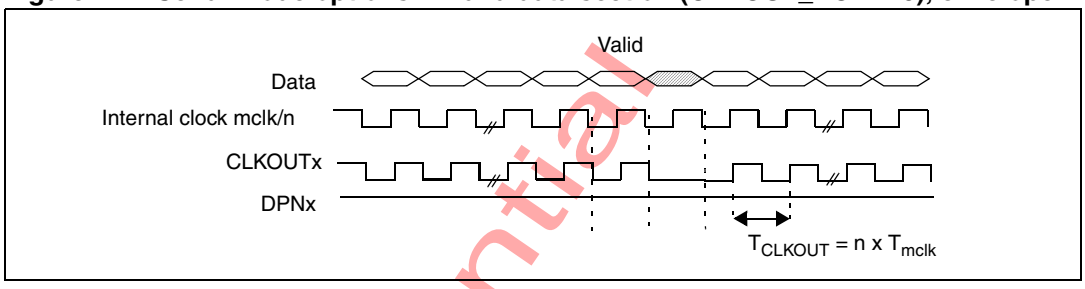


Figure 14. Serial mode options in valid data section (CLKOUT_XOR = 0), envelope



8.4 Parallel output modes

The STV0913 features two different parallel output modes.

- ST back-end (recommended mode). CLKOUT is held high or low (depending on register bit *TSCFGH*.TSFIFO_DVBCI) for unknown data sections, see *Figure 15* and *Figure 17*.
- DVB-CI. Where DPN is held high or low (depending on register bit *OUTCFG2*.CLKOUT_XOR) for unknown data sections, see *Figure 16* and *Figure 18*.

In both parallel output modes, the STROUT pin is high during the first byte of the packet.

The rate compensation mode (*TSCFGH*.TSFIFO_DVBCI bit) is set as in *Table 15*.

Table 15. Rate compensation mode settings

	DVB-CI	ST Back-end
TSFIFO_DVBCI	1	0

Figure 15. ST back-end output interface (CLKOUT_XOR = 0)

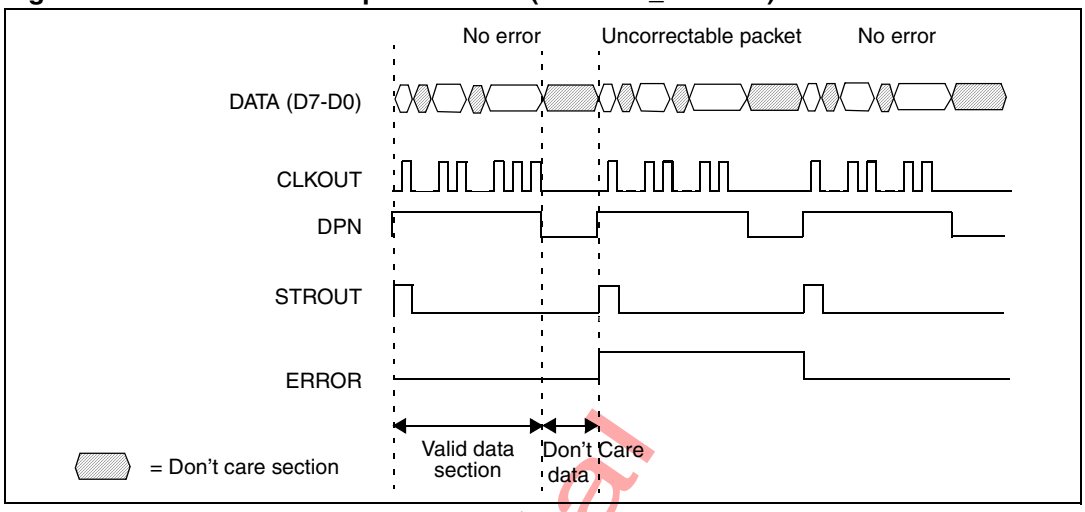


Figure 16. DVB-CI output interface (CLKOUT_XOR = 0)

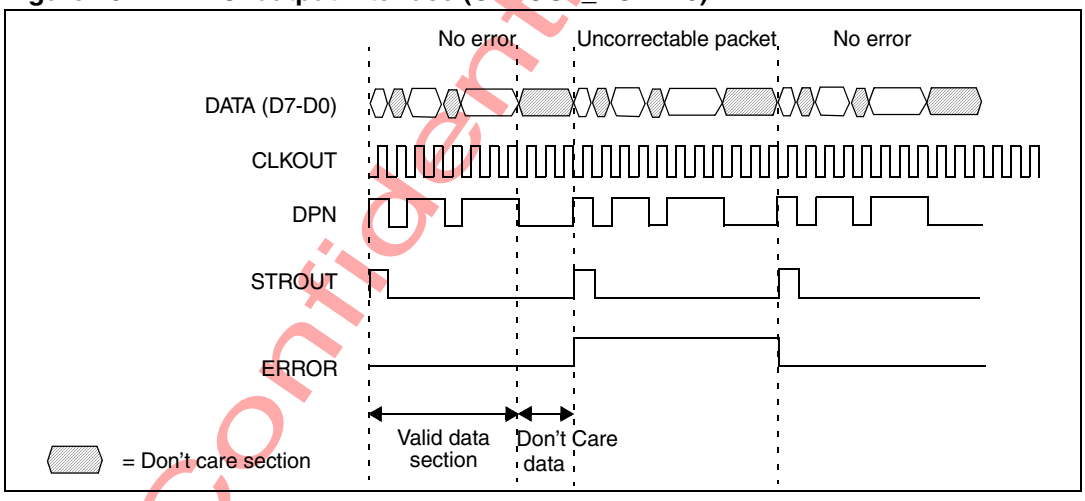


Figure 17. ST back-end in valid data section (CLKOUT_XOR = 0 example)

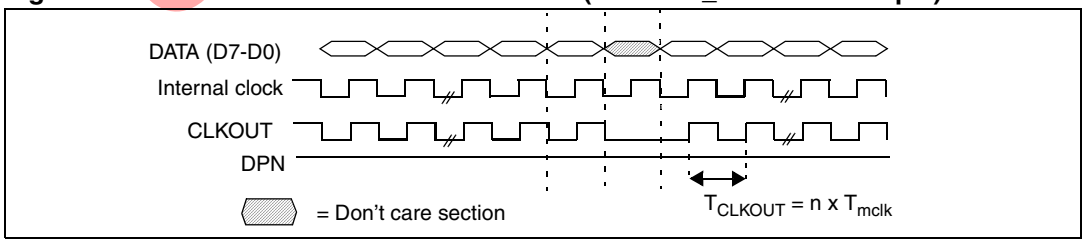
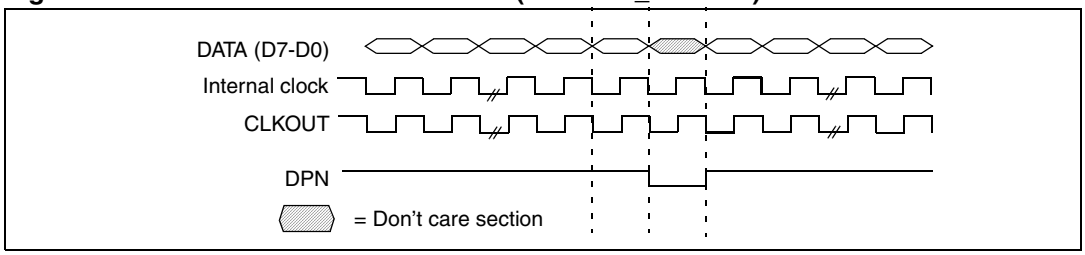


Figure 18. DVB-CI in valid data section (CLKOUT_XOR = 0)



9 DiSEqC 2.x interface

9.1 Introduction

The STV0913 integrates one DiSEqC 2.x interface to communicate with an LNB. This interface is designed to fulfill the Echostar requirement as described and referenced in the document 159239 (December 2007) section 7.19.

9.2 DiSEqC receiver

The RX block implements the receiver section of the DiSEqC specification.

The following steps describe the implementation of the receiver section:

1. The reception is done by sampling the external signal by a 10-bit AD at 1 MHz (approximately).
2. After DC removal, the signal is filtered at 22 kHz (approximately).
3. After envelope detection, the duty cycle is computed.
4. After data retrieval, the data is supplied into a FIFO to be read externally by the I^2C interface.

The demodulation can tolerate high variations on the DiSEqC signal through the use of a powerful auto-adaptative receiver:

- ± 20% on modulation frequency
- ± 20% on bit duration
- ± 50% on AC level

It also offers a strong protection against interference near the 22 kHz band.

During the DC removal, the DC value is measured and can be read in the Px_DISRXDC1/0 registers (Px_DC_VALUE bitfield) of the I^2C interface. This DC value is used to estimate the LNB voltage, provided appropriate filtering between the line and the ADC input.

9.2.1 Typical message reception

The DiSEqC analog signal is sampled by a 10-bit AD at a frequency in the range from 100 kHz to 2 MHz.

The bits are extracted, then assembled into bytes, checked for parity and stacked in the 16 byte FIFO.

The following two conditions can signal to the external microprocessor to get the acquired data (by IRQ or Px_DISRXSTAT1 register polling):

- RXEND: the end of a message is detected. The transaction is done and the data must be read in the FIFO.
- 8BFIFOREADY: 8 bytes are in the FIFO. The microprocessor must read the data before the arrival of the next 8 bytes to avoid the FIFO overflow.

In case of the RXEND condition, the number of bytes remaining in the FIFO can be read in the *DISRXBYTES* register.

9.2.2 LNB voltage measurement

To measure the LNB voltage, the LNB voltage can be added to the DiSEqC signal and read as the DC component of the sampled signals in the DISRXDC1 and DISRXDC0 registers.

9.2.3 Status

The received bytes are stacked in the receiver FIFO (*DISRXFIFO* register). The status registers (DISRXSTATx) provide the following information concerning the state of the receiver:

- reception ended
- receiver active
- continuous tone detected
- 8 bytes ready for reading
- FIFO empty
- reception failed
- parity error detected
- wrong number of bits to make a byte detected
- FIFO overflow
- number of bytes in FIFO

In addition to the above mentioned status registers there are interrupt flags (in the *DISRXCFG* register) to:

- generate an interrupt at the end of a received block
- generate an interrupt if there are eight or more bytes in the FIFO ready for reading

9.2.4 External envelope

An external envelope can also be used as a DiSEqC signal. The signal is input by a digital pad and is used directly in the bit decision finite state machine (fsm), bypassing all the envelope detection.

This mode is triggered by the *DISRXCFG*.EXTENVELOP bitfield. This pin used to input the digital signal is configured by the *DISRXCFG*.PINSELECT bitfield.

9.2.5 Parity check

In a DiSEqC message, all bytes have a parity bit. A global check can be observed in the DISRXSTAT0.FIFOPFAIL register bitfield. If at least one byte in the FIFO has a parity fail, the DISRXSTAT0.FIFOPFAIL register bitfield is set to '1'. All the 16 parities for the 16 bytes in the FIFO can be read in *DISRXPARITYx* registers.

10 FSK interface

10.1 Introduction

The integrates a flexible FSK modem for on-cable communication. A wide range of carrier, deviation and modulation frequencies are supported.

The design has been optimized with respect to the bill of materials to allow an economical implementation of the FSK function.

The transmitter consists of a digital oscillator which is modulated by a digitally generated deviation frequency. The output is then shaped by a single-bit sigma-delta DAC. The system has been designed to meet spectral suppression requirements in conjunction with a simple external filter.

The receiver is also implemented using a sigma-delta converter, allowing efficient linear filtering whilst minimizing the external bill of materials. Thus, the IC can support relatively high adjacent channel impairments.

The associated registers are detailed in *Section 17.3: FSK register descriptions*.

10.2 FSK activation

Some GPIOs must be reprogrammed to output the FSK control signals:

- FSKTX_OUT, FSK transmitter output
- FSKTX_IN, FSK transmitter in
- FSKTX_EN, FSK transmitter enable
- FSKRX_DETECT, FSK receiver detect flag
- FSKRX_OUT, FSK receiver out

See *Chapter 11: General purpose I/O (GPIO)* on how to configure the GPIOs.

10.3 FSK transmitter

The transmitter (modulator) outputs an instantaneous frequency depending on the digital value (one or zero) on pin FSKTX_IN. The modulator output is on pin FSKTX_OUT and has three states:

- off: high impedance, one or zero
- low frequency: the carrier frequency (fc) minus the deviation frequency (Δf)
- high frequency: the carrier frequency (fc) plus the deviation frequency (Δf)

The transmitter may be activated by a hardware pin (FSKTX_EN) or by register control in register bit *FSKTCTRL*.FSKT_MOD_EN.

Both transmitter control pins (FSKTX_EN and FSKTX_IN) may have their sense inverted through the appropriate bits in register *FSKTCTRL*.

The input bit rate (the rate at which pin FSKTX_IN is toggled) is unknown to the modulator and is not limited.

All frequency values are derived from the master clock f_{MCLK}. The carrier frequency is programmable from 0 to f_{MCLK} / 4 in steps of f_{MCLK} / 2^{20}.

The RF output is implemented using a standard digital pin with three possible signal conversion schemes.

- 1-bit sigma-delta converter with second order loop: this gives the best signal to noise ratio around the carrier frequency. It needs an external low pass filter to remove high frequency components.
- 1-bit sigma-delta converter with first order loop: the signal to noise ratio is worse but the amplitude of the wanted signal may be higher.
- 1-bit converter: the output is the modulated carrier quantized in two frequencies, fc+Δf and fc-Δf. The amplitude is at its maximum, but the signal spectrum contains lots of spurious frequencies. This scheme may be used for low carrier frequencies (below 1 MHz).

When using the delta-sigma schemes, the amplitude may be controlled by register bitfield *FSKTCTRL*.FSKT_KMOD according to the *Table 16* below.

Table 16. Modulator gain values

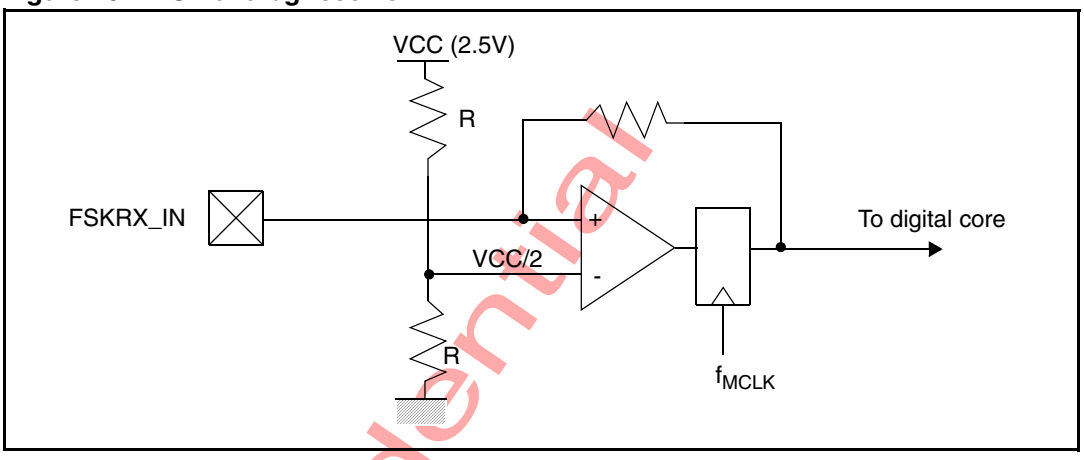
Modulator	Max gain value FSKT_KMOD	Max pk to pk level (after LPF)	Typical CNR at 0.04 * f_{MCLK}
Delta-sigma 2nd order	32 (TBC)	0.22 VCC (TBC)	35 dB (TBC)
Delta-sigma 1st order	63 (TBC)	0.44 VCC (TBC)	30 dB (TBC)
1-bit DAC	NA	1.4 VCC (TBC)	14 dB (TBC)

10.4 FSK receiver

The input RF input is applied to the input pin FSKRX_IN via an external RC integrator. The average input voltage (on pin FSKRX_IN) is maintained constant by internal feedback (a resistor switched to ground or VCC). This RC configuration with feedback implements a 1^{st}-order sigma-delta converter.

As per the transmitter, the receiver (demodulator) centre frequency is programmable from 0 to f_{MCLK} / 4 in steps of f_{MCLK} / 2^{20}.

Figure 19. FSK analog receiver



The input RF signal range is from 2 mV to VCC.

After conversion, the signal is filtered by a 2^{nd}-order filter centered on the carrier with programmable bandwidth defined by k1 and k2:

$k1 = 2^{20} * 8 * \pi * BW / f_{MCLK}$

$k2 = 2^{20} * (8 * \pi * BW / f_{MCLK})^2$

Where BW is the single sided bandwidth of the external filter, typically equal to the expected frequency deviation plus half the baud rate, and k1 and k2 are defined by pseudo floating point values in registers FSKRK1 and FSKRK2:

$k1 = fskr\_k1\_mant * 2^{8+fskr\_k1\_exp}$

where fskr_k1_mant = 1 to 31 and fskr_k1_exp = 0 to 5

$k2 = fskr\_k2\_mant * 2^{fskr\_k2\_exp}$

where fskr_k2_mant = 1 to 31, fskr_k2_exp = 0 to 7

A signal AGC maintains the output level to the programmed reference level in register bit *FSKRAGCR*.FSKR_AGC_REF with six possible time constants in powers of 2. Value 0 corresponds to the longest time constant. The AGC accumulator may be read in register *FSKRAGC*, its content is an image of the in-band signal amplitude, this may serve as an FSK received strength indicator.

The instantaneous frequency deviation is then extracted by a PLL, compared with a threshold and the result made available on the output pin FSKRX_OUT. The output only changes if the absolute value of the deviation is above a programmable threshold FSKR_PLL_THRESH, thus providing some protection against noise. The unit of the threshold is f_{MCLK} / 2^{20}.

The PLL is a second order loop, with damping factor (ξ) and natural frequency (*fnat*) depending on parameters α and β:

$$fnat = 7\times10^{-6} \cdot fo \cdot \sqrt{\beta \cdot FSKR\_AGC\_REF}$$

$$\xi = 88\times10^{-6} \cdot \alpha \cdot \sqrt{\frac{FSKR\_AGC\_REF}{\beta}}$$

where:

α = 256 * (4 + fskr_alpha_m) * $2^{fskr\_alpha\_exp}$

β = 2^{fskr_beta}

The recommended settings correspond to a damping factor close to 0.8 to 1 and a natural frequency up to 100% above the baud rate.

The presence of an FSK signal is detected by register bitfield FSKR_CARDET_ACCU (made up of two registers *FSKRDETx*). This indicates a value representative of the average absolute value of the frequency deviation. It is compared to two thresholds to declare the lock state or the lost state of the PLL (FSKR_CARDET_THRESH, FSKR_CARLOSS_THRESH). The unit is $f_{MCLK} / 2^{20}$.

The recommended values (TBC) are:

fskr_cardet_thresh = 3/4 Δf

fskr_carloss_thresh = 1/4 Δf

where Δf is the frequency deviation.

The carrier detection depends on a statistical analysis controlled by FSKR_STEP_PLUS and FSKR_STEP_MINUS.

The parameters step_plus and step_minus defined in pseudo floating point by:

step_plus = fskr_step_plus[4:0] * $2^{fskr\_step\_plus[7:5]}$

step_minus = fskr_step_minus[4:0] * $2^{fskr\_step\_minus[7:5]}$

As a first approximation it is recommended to set these values to:

step_plus = 80000 * $\Delta f / f_{MCLK}$

step_minus = 4 * step_plus

The result of the carrier detection can be routed on any GPIO pin configured as FSKRX_DETECT (see *Chapter 11: General purpose I/O (GPIO)*). The sign of this output is also programmable in register *FSKTCTRL*, bit FSKT_EN_SGN.

11 General purpose I/O (GPIO)

11.1 Overview

The flexible GPIO implementation allows simple, in-depth debug and allows digital signals to be routed to the most convenient pin (facilitating board layout and test).

The syntax for programming all the GPIO registers is shown in the following bitfield.

7	6	5	4	3	2	1	0
Open drain	Configuration value						XOR

Bit[7] is for open drain. When high it configures the pin in open-drain (current sink, high impedance or input); when low it configures the pin as a classical push-pull (output).

Bits [6:1] configure the value.

Bit[0] selects XOR to invert the signal selected (by applying an XOR operation with the value of bit[7]).

The 13 GPIO pins are configured by default to 0x82 which implies they are set to open drain, logic 1 (that is, high impedance).

Refer to the *GPIOxCFG* registers to configure these pins for application-specific requirements.

Table 17. GPIO configuration

Config value	Definition	Description
0	0	Forces output to logical 0
1	1	Forces output to logical 1
2	STREAM_STATUS1	Stream Status 1
3	STREAM_STATUS2	Stream Status 2
4	STREAM_STATUS3	Stream Status 3
5	STREAM_STATUS4	Stream Status 4
6	STREAM_STATUS5	Stream Status 5
7	STREAM_STATUS6	Stream Status 6
8	DEMOD_AGCIQ_OUT	Demodulator I or IQ control output of AGC
10	DISEQCOUT	DiSEqC1 2.0 output
12	FSKTX_OUT	FSK transmitter output
13	FSKRX_DETECT	FSK receiver detect flag
14	FSKTX_IN	FSK transmitter input
15	FSKTX_EN	FSK transmitter enable
16	FSKRX_OUT	FSK receiver output
17	OUT_BIT1	Output test out bit 1
18	OUT_BIT2	Output test out bit 2

Table 17. GPIO configuration (continued)

Config value	Definition	Description
19	DAC_OUT	DAC is output
20	IRQ	Interrupt request flag
21	VALID_SIM	FEC spy valid simulation flag
24	SDAT	Tuner dedicated SDA signal
25	SCLT	Tuner dedicated SCL signal
28	I2C_MAP0	Out register bit 1
29	I2C_MAP1	Out register bit 2
30	SDA2_OUT	SDA auxiliary output
31	SCL2_OUT	SCL auxiliary output
32	DPN	Transport stream dp/n
33	STROUT	Transport stream strout
34	ERROR	Transport stream error
35	CLKOUT	Transport stream clockout
36	D7	Transport stream serial data
47	SDD_SOF	Stream serial data description start of frame
48	SDD_ENA	Stream serial data description clock enable
49	SDD_DATA	Stream serial data description data
53	SIGNALLING_1	Signaling stream bit 1
54	SIGNALLING_2	Signaling stream bit 2
59	AUX_CLK1	Auxiliary clock 1
60	AUX_CLK2	Auxiliary clock 2
61	CLK270	Clock 270 MHz
62	CLK135	Clock 135 MHz
63	XTAL_IN	Clock crystal

The Stream Status signals can be configured by the 3 registers STRSTATUS1..3 to route these signals to a GPIO.

Table 18. STREAM_STATUS1..6 configuration

Config value	Definition	Description
0	DEMOD_SYMIQ	Demodulator detected an IQ symmetry
1	DEMOD_LOCKED	Demodulator locked flag
2	DEMOD_FAIL	Demodulator failed flag
3	PKTDEL_LOCKED	Packet Delineator locked flag
4	PKTDEL_ERROR	Packet Delineator error flag

Table 18. STREAM_STATUS1..6 configuration (continued)

Config value	Definition	Description
5	VITERBI_PRF	DVB-S1 Viterbi puncture rate found flag
12	STREAM_LOCKED	Stream (return channel) locked flag (up to transport)

12 Interrupt request (IRQ)

12.1 Overview

Interrupts can be generated by the STV0913.

The interrupt lines can be routed on a GPIO pin by using the GPIO configuration registers (see *Chapter 11: General purpose I/O (GPIO) on page 58*).

Each IRQ source can be masked via one of the registers *IRQMASKx* and the status on the source of the IRQ can be read on the corresponding register *IRQSTATUSx*.

12.2 IRQ configuration

Table 19. List of IRQs

IRQ name	IRQ #	Description
DiSEqC IRQ RE	0	DiSEqC IRQ rising edge
DiSEqC IRQ RE	1	Unused
RESERVED	2	Reserved
RESERVED	3	Reserved
BCH block incorrectable IRQ	4	The BCH decoder detected an unreliable BCH block.
DEMOD IRQ RE	5	Rising edge of demod IRQ. A Status is available to indicate what is the interrupt source
DEMOD LOCKED RE	6	Rising edge of demod locked
DEMOD LOCKED FE	7	Falling edge of demod locked
RESERVED	8	Reserved
RESERVED	9	Reserved
RESERVED	10	Reserved
EXT PIN 1 RE	11	Rising edge on external input port
EXT PIN 1 FE	12	Falling edge on external input port
EXT PIN 2 RE	13	Rising edge on external input port
EXT PIN 2 FE	14	Falling edge on external input port
PKTDEL LOCK RE	15	Rising edge on packet delineator lock
PKTDEL LOCK FE	16	Falling edge on packet delineator lock
PKTDEL ERROR RE	17	Rising edge on packet delineator error
RESERVED	18	Reserved
RESERVED	19	Reserved
RESERVED	20	Reserved
FECSPY ENDSIM	21	FECSPY end of simulation rising edge
RESERVED	22	Reserved
RESERVED	23	Reserved
VITERBI PRF RE	24	Puncture rate found rising edge
RESERVED	25	Reserved
STREAM LOCK RE	26	Stream lock rising edge
RESERVED	27	Reserved
RESERVED	28	Reserved
PLL LOCK RE	29	PLL lock rising edge

13 JTAG interface

The JTAG is compliant with the JTAG IEEE1149.1 standard, also called the boundary scan standard.

JTAG allows a control state-machine to be accessed through its test access port (TAP) to manage production boundary scan tests.

The STV0913 cut 1.0 JTAG identifier is 0x0D438041.

The following mandatory IEEE instructions are available:

- bypass
- extest
- sample/preload

Also, IDcode (and private register) is an additional recommended instruction.

Table 20. TAP control signals

Test signal names	Active	Description
TRSTN	L	Asynchronous TAP reset
TCK	H	Positive edge clock for TAP
TMS	-	Input TAP state-machine control
TDI	-	Scan input for instruction or data
TDO	-	Scan output for instruction or data: negative edge of TCK

Caution: Pin TRSTN must be tied low during normal operation. Allowing this pin to float or be pulled high causes the JTAG state machine to operate, causing anomalous behavior of the IC.

14 Electrical specifications

14.1 Absolute maximum ratings

Table 21. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd_1v1}	DC supply voltage	-0.5	-	1.5	V
V_{dd_2v5}	DC supply voltage	-0.5	-	3.9	V
V_{dd_3v3}	DC supply voltage	-0.5	-	3.9	V
V_{in}	Voltage on input pins	-0.3	-	$V_{dd\_3.3}$ + 0.3	V
V_{ESD_HBM}	Electrostatic discharge voltage (HBM) JESD22-A114 - Class TBD (1)	-	-	-	-
V_{ESD_RCDM}	Electrostatic discharge voltage (RCDM) JESD22-C101- Class TBD (1)	-	-	-	-
T_{stg}	Storage temperature	-40	-	150	°C

1. For a definition of the ESD classes, see the relevant JEDEC standards, or contact STMicroelectronics customer support.

Note: These AMR values are applicable to all pins powered to the given voltage. These are maximum limits. Exceeding them may result in permanent damage to the device. Operation at these limits is not intended.

14.2 Operating conditions

Table 22. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{dd_1V1}	Digital core supply voltage	1.05	-	1.20	V
V_{dd_2V5}	Digital supply voltage	2.25	-	2.75	V
V_{dd_3v3}	Digital pads supply voltage	3.0	3.3	3.6	V
T_{oper}	Operating ambient temperature	0	-	70	°C
$T_{junction}$	Junction temperature	-40	-	125(1)	°C

1. This is the maximum limit allowed to guarantee the performance and reliability of the device.

14.3 Thermal data

Table 23. Thermal data

Symbol	Parameter	Maximum value	Unit
$r_{th(j-a)}$	Thermal resistance (junction-ambient)(1)	TBD(2) TBD (3)	°C/W °C/W
$r_{th(j-c)}$	Thermal resistance (junction-case)	TBD	°C/W

1. The Rth(j-a) has been measured using an FR4 board without heatsink. The value must be considered only as an indication. The thermal performance of the electronic package can vary significantly depending on board design, size, thickness, material and other physical factors.
2. Four-layer PCB
3. Two-layer PCB

14.4 DC electrical specifications

Table 24. DC electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{il} V_{ih}	Input logic low Input logic high	-0.3 2.0	-	0.8 3.6	V V
V_{ol} V_{oh}	Output logic low Output logic high	- 2.6	-	0.4 -	V V
I_{lk}	Input leakage current (v_{in} = 0 V to 3.3 V)	-	7.5	-	µA
I_{ol}	Output sink current	-	-	4	mA

Note: The 3.3-V digital I/Os comply to the JEDEC standard JESD8b.

Note: No constraint is placed on power supply power up sequence. However, pin RESETB, the chip reset, must remain active (low) until at least 3 ms after the last power supply has stabilized (to 90% of its final value).

14.5 AC electrical specifications

The AC electrical specifications have to be detailed (TBD) later.

Table 25. AC electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	External clock frequency applied to XTALI	4	-	30	MHz
f_{xtal_int}	Internal crystal oscillator frequency range	27	-	30	MHz
$I_{dd\_1v0\_rsta}$	Digital core supply current when reset pin active	-	-	-	mA
$I_{dd\_1v0\_rst}$	Digital core supply current after reset	-	-	-	mA
$I_{dd\_1v0\_stb}$	Digital core supply current when in standby	-	-	-	mA
$I_{dd\_1v0\_1s1}$	Digital core supply current, one DVB-S active	-	-	-	A
$I_{dd\_1v0\_2s1}$	Digital core supply current, two DVB-S active	-	-	-	A
$I_{dd\_1v0\_1s2}$	Digital core supply current, one DVB-S2 active	-	-	-	A
$I_{dd\_1v0\_2s2}$	Digital core supply current, two DVB-S2 active	-	-	-	A
$I_{dd\_1v0\_pk}$	Digital core supply current, peak	-	-	-	A
I_{dd_3v3}	Digital pads supply current	-	-	-	mA
I_{dda_1v0}	Analog supply current	-	-	-	mA
I_{dda_2v5}	Analog supply current	-	-	-	mA
P_{max}	Power consumption	-	-	-	W
Vclk_i	CLK_I input amplitude	-	-	-	Vpp
Vxtal_i	XTAL_I input amplitude	-	-	-	Vpp

14.6 Dual 10-bit ADC specifications

Table 26. ADC specifications

Symbol	Parameter	Min	Typ	Max	Unit
-	Resolution	-	-	-	bits
DC specifications					
dle	Differential linearity error	-	-	-	LSB
ilepp	Integral linearity error, peak to peak	-	-	-	LSB
-	Gain error	-	-	-	%FSR
Analog input					
-	Differential input voltage mode 2 Vpp	-	-	-	Vpp
-	Differential input voltage mode 1 Vpp	-	-	-	Vpp
-	Input common mode voltage	-	-	-	V
-	ADC differential input impedance (internal) Required external termination load	-	-	-	kΩ kΩ
-	Input capacitance	-	-	-	pF
-	Analog bandwidth	-	-	-	MHz
Switching performance					
-	Maximum conversion rate	-	-	-	MHz
-	Aperture uncertainty	-	-	-	ps RMS
-	Duty cycle sampling clock	-	-	-	%
Dynamic performance					
enob	Effective number of bits	-	-	-	bits
sinad	Signal-to-noise ratio with distortion	-	-	-	dB

14.7 Transport stream timing specifications

Table 27. Transport stream timing specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	CLK_IN or XTAL frequency (dispersion including thermal drift and aging)	-100 ppm	27	+100 ppm	MHz
Parallel output D[7:0], D/PN, CLKOUT, STROUT, ERROR output characteristics					
Bit CLKPOL = 0. Refer to *Figure 20*.					
t_{cksu}	Outputs stable before CLKOUT rising edge	5.0	-	-	ns
t_{ckh}	Outputs stable after CLKOUT rising edge	5.0	-	-	ns
Bit CLKPOL = 1. Refer to *Figure 20*.					
t_{cksu}	Outputs stable before CLKOUT falling edge	5.0	-	-	ns
t_{ckh}	Outputs stable after CLKOUT falling edge	5.0	-	-	ns
Serial output D[7] or D[0], D/PN, CLKOUT, STROUT, ERROR output characteristics					
Bit CLKPOL = 0 Refer to *Figure 21*.					
t_{cksu}	Outputs stable before CLKOUT rising edge	3.0	-	-	ns
t_{ckh}	Outputs stable after CLKOUT rising edge	3.0	-	-	ns
Bit CLKPOL = 1. Refer to *Figure 21*.					
t_{cksu}	Outputs stable before CLKOUT falling edge	3.0	-	-	ns
t_{ckh}	Outputs stable after CLKOUT falling edge	3.0	-	-	ns

Figure 20. Parallel output timing diagram

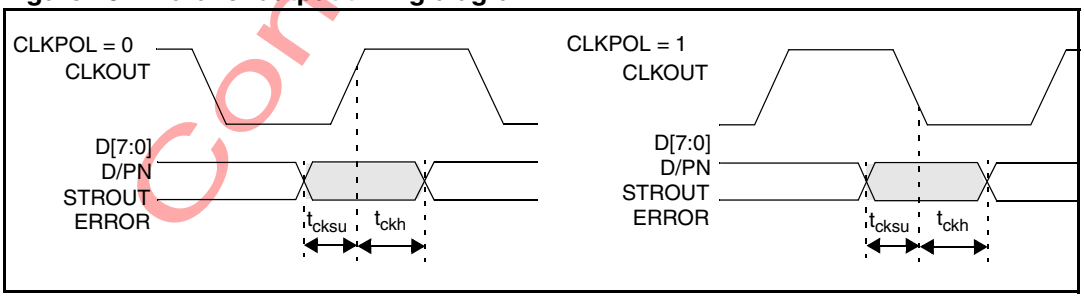
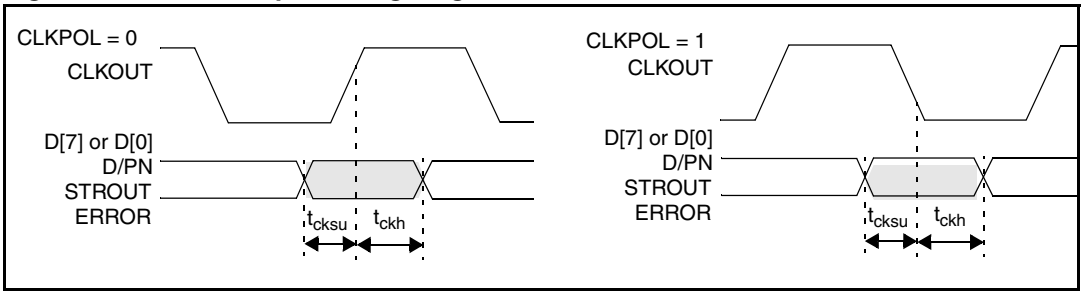


Figure 21. Serial output timing diagram

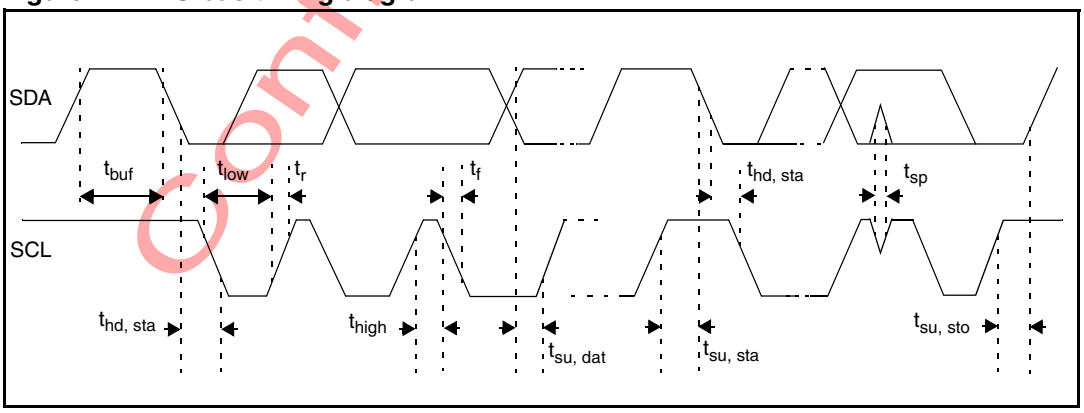


14.8 I²C bus specifications

Table 28. I²C bus specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{scl}	SCL clock frequency	Normal mode	0	-	400	kHz
t_{buf}	Bus free time between a stop and start condition	-	1.3	-	-	µs
$t_{hd, sta}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	-	0.6	-	-	µs
t_{low} t_{high}	Low period of the SCL clock High period of the SCL clock	-	1.3 0.6	-	-	µs µs
t_r	Rise time for SDA and SCL signals	Fast mode	-	-	300	ns
t_f	Fall time for SDA and SCL signals	Fast mode	-	-	300	ns
$t_{su, sta}$	Setup time for a repeated start condition	-	0.6	-	-	µs
$t_{su, sto}$	Setup time for stop condition	-	0.6	-	-	µs
$t_{su, dat}$	Data setup time	-	100	-	-	ns
t_{sp}	Pulse width of spikes to be suppressed by input filter	Fast mode	0	-	50	ns

Figure 22. I²C bus timing diagram



14.9 Crystal oscillator specifications

Table 29. Crystal oscillator specifications

Parameter	Min	Typ	Max	Unit
Oscillation mode				
Startup time(1)	-	-	2	ms
Oscillation frequency	27	-	30	MHz
Duty cycle at ZI and ZI2V5	40	-	60	%
Amplitude of oscillation at ZO (Pk-Pk)	0.7	-	2.2	V
Output load at ZI and ZI2V5	-	-	100	fF
Functional bypass mode				
Input frequency (single-ended input clock of 0-VDDA CMOS levels)	-	-	30	MHz
Traise/Tfall [10% to 90%] at PAD A	-	-	3	nSec
Output load at ZI and ZI2V5	-	-	100	fF
Input clock duty cycle(2)	45	50	55	%
Test bypass mode				
Input frequency (single-ended input clock of 0-VDDA CMOS levels)	-	-	60	MHz
Traise/Tfall [10% to 90%] at PAD A	-	-	2	nSec
Output load at ZI and ZI2V5	-	-	100	fF
Input clock duty cycle(2)	45	50	55	%

1. The startup time is defined as the time difference between initiation of the Oscillation mode and the oscillation amplitudes at ZO reaching 90% of the final stable value. This parameter is strongly dependent on board parasitics.
2. Input duty at A is assumed to be 50%. If input duty cycle is different, there can be +/-5% spread over the input clock duty cycle.

Phase noise at ZI/ZI2V5

Table 30. Phase noise (With worst case crystal model as given in *Table 31*)

Offset from carrier	SSB (dBc/Hz)
1k	-90
10k	-130
100k	-145
1M	-150

Figure 23. Crystal oscillator equivalent model

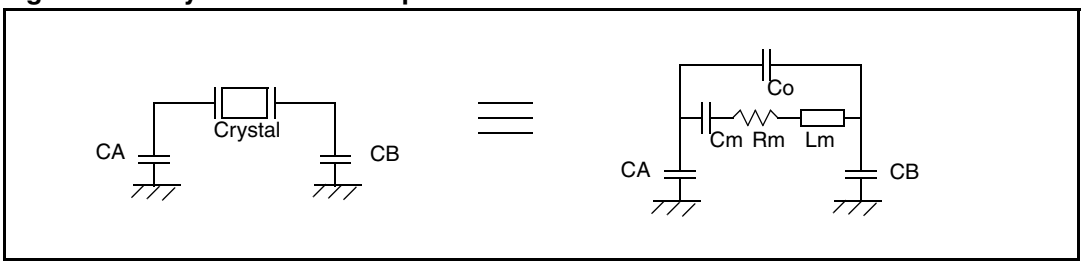


Table 31. Quartz and worst case model

Crystal model	Frequency (MHz)	Lm (mH)	Rm (Ω)	Cm (fF)	CO (pF)	Q (K)	CA = CB (pF)
30 MHz crystal parameters	30.000	2.6075 (typ)	50 (max)	10.8 (typ)	7(1) (max)	9.83	30

1. Co (tot) = Cs + CO, should not exceed 9pF, otherwise it may cause start-up failure of the oscillator.

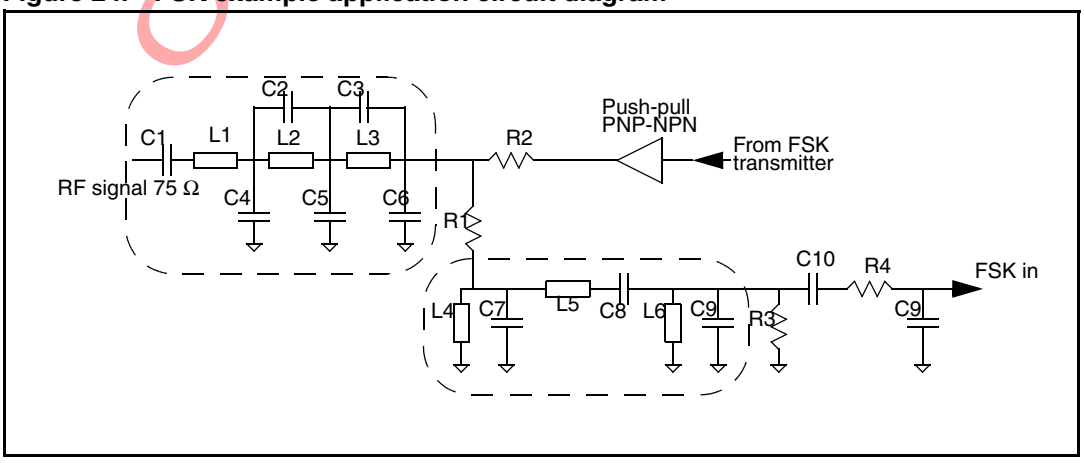
*Note: Crystal Load= CA*CB/(CA+CB) + Co(tot)*

14.10 FSK receiver, transmitter specifications

Table 32. FSK specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f_{o_fsk}	Carrier frequency	-	1	-	7	MHz
Δf_fsk	Deviation frequency	-	8	-	250	kHz
Rx_{p_fsk}	Receive power	75 Ω	10	-	48	dBmV
Rx_{p_fsk}	Transmit power	-	-	-	-	dBmV

Figure 24. FSK example application circuit diagram



15 Package mechanical data

The the device is housed in a 77-pin LFBGA 8x8x1.7 2R9x9 pitch 0.8 ball 0.4 package. The package code is A0JL.

Table 33 gives the values of the dimensions indicated in *Figure 25*.

Figure 25. Package diagram

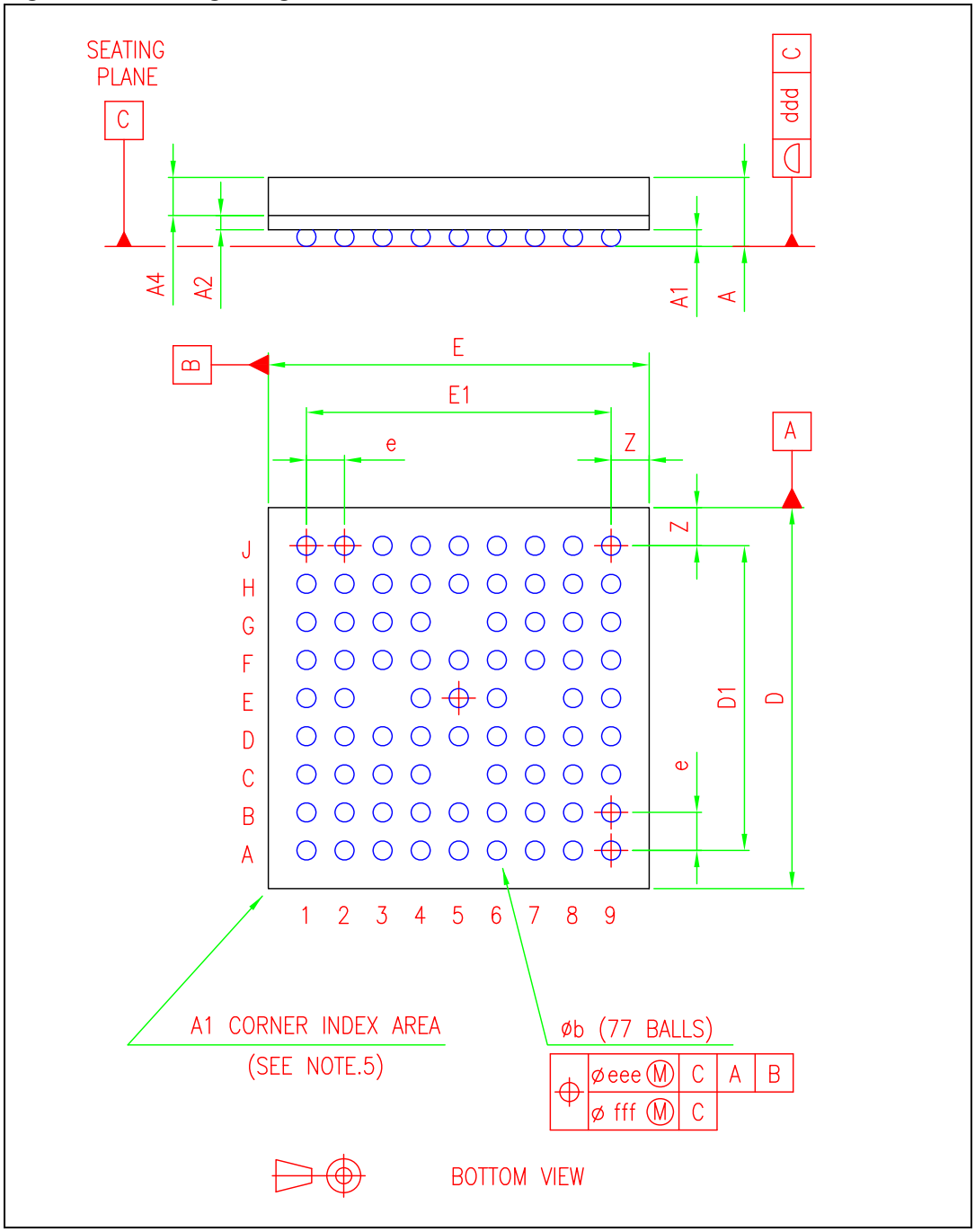


Table 33. JEDEC standard package dimensions

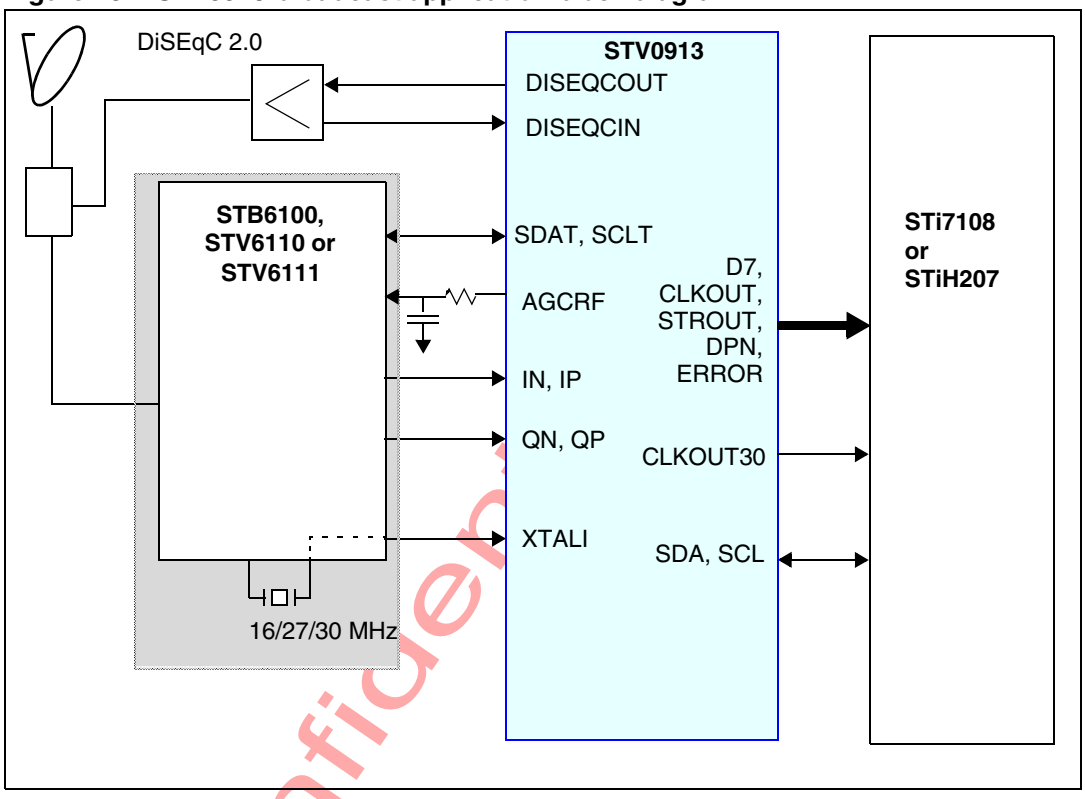
Dimensions	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.70	-	-	0.067
A1	0.21	-	-	0.008	-	-
A2	-	0.30	-	-	0.012	-
A4	-	-	0.80	-	-	0.031
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.85	8.00	8.15	0.309	0.315	0.321
D1	-	6.40	-	-	0.252	-
E	7.85	8.00	8.15	0.309	0.315	0.321
E1	-	6.40	-	-	0.252	-
e	-	0.80	-	-	0.031	-
Z	-	0.80	-	-	0.031	-
ddd	-	-	0.10	-	-	0.004
eee	-	-	0.15	-	-	0.006
fff	-	-	0.08	-	-	0.003

15.1 Environmentally friendly packaging

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

16 Applications block diagram

Figure 26. STV0913 broadcast application block diagram



Possible broadcast configurations are:

- DVB-S or DIRECTV legacy decoding with serial or parallel TS output
- DVB-S2 decoding with serial or parallel TS output
- DVB-S or DirecTV legacy and DVB-S2 decoding with serial or parallel TS output

17 Registers

17.1 Register summary

Table 34. SYS register list

Address	Register name	Description	Page
0xF100	MID	Chip identification	page 85
0xF101	DID	Device Identification	page 85
0xF113	DACR1	DAC control	page 85
0xF114	DACR2	DAC control	page 86
0xF11A	PADCFG	Dedicated Pads Configuration	page 86
0xF11B	OUTCFG2	Transport stream output configuration 2	page 86
0xF11C	OUTCFG	Transport stream output configuration	page 87
0xF120:0xF123 (0x1)	IRQSTATUSx	Interrupt request status	page 88
0xF124:0xF127 (0x1)	IRQMASKx	Interrupt request mask	page 90
0xF129	I2CCFG	I2C bus configuration	page 91
0xF12A	I2CRPT	I2C bus repeater control	page 91
0xF140:0xF14C (0x1)	GPIOxCFG	General purpose IO control	page 92
0xF16A:0xF16C (0x1)	STRSTATUSx	Stream status	page 94
0xF1B3	NCOARSE	Analog PLL divider control	page 94
0xF1B4:0xF1B5 (0x1)	NCOARSEx	Analog PLL divider control	page 95
0xF1B6	SYNTCTRL	Frequency synthesis control	page 96
0xF1B7	FILTCTRL	Filter control	page 96
0xF1B8	PLLSTAT	PLL Status	page 97
0xF1C2:0xF1C3 (0x1)	STOPCLKx	Stop clock control x	page 97
0xF1C8	PREGCTL	Power Regulator Control	page 98
0xF1DF	TSTTNR0	FSK analog cell test and configuration	page 98
0xF1E0	TSTTNR1	ADC 1 test and configuration	page 98
0xF1E1	TSTTNR2	DiSEqC 1 test and configuration	page 99

Table 35. FSK register list

Address	Register name	Description	Page
0xF170	FSKTFC2	FSK Transmitter gain and carrier frequency	page 100
0xF171	FSKTFC1	FSK transmitter gain and carrier frequency	page 100
0xF172	FSKTFC0	FSK transmitter gain and carrier frequency	page 100
0xF173:0xF174 (0x1)	FSKTDELTAFx	FSK transmitter frequency deviation	page 101
0xF175	FSKTCTRL	FSK transmitter control	page 101
0xF176:0xF178 (0x1)	FSKRFCx	FSK receiver carrier frequency	page 102
0xF179:0xF17A (0x1)	FSKRKx	FSK receiver Kx	page 103
0xF17B	FSKRAGCR	FSK receiver AGC reference	page 103
0xF17C	FSKRAGC	FSK receiver AGC status	page 103
0xF17D	FSKRALPHA	FSK receiver alpha coefficient	page 104
0xF17E:0xF17F (0x1)	FSKRPLTHx	FSK receiver beta coefficient and PLL threshold	page 104
0xF180:0xF181 (0x1)	FSKRDFx	FSK receiver frequency deviation	page 104
0xF182	FSKRSTEPP	FSK receiver positive step	page 105
0xF183	FSKRSTEPM	FSK receiver negative step	page 105
0xF184:0xF185 (0x1)	FSKRDETx	FSK receiver detection status	page 105
0xF186:0xF187 (0x1)	FSKRDTHx	FSK receiver carrier detection and loss threshold	page 106
0xF188	FSKRLOSS	FSK receiver carrier loss threshold	page 106

Table 36. DMD register list

Address	Register name	Description	Page
0xF400	IQCONST	Constellation editor configuration	page 107
0xF401	NOSCFG	Configuration of noise indicators	page 107
0xF402	ISYMB	Constellation editor I track	page 108
0xF403	QSYMB	Constellation editor Q track	page 108
0xF404	AGC1CFG	IQ mismatch control	page 109
0xF406	AGC1CN	AGC1 control	page 109
0xF407	AGC1REF	AGC1 reference	page 110
0xF408	IDCCOMP	DC compensation on I	page 110
0xF409	QDCCOMP	DC compensation on Q	page 111
0xF40A	POWERI	Power measured on I	page 111
0xF40B	POWERQ	Power measured on Q	page 111

Table 36. DMD register list (continued)

Address	Register name	Description	Page
0xF40C	AGC1AMM	Amplitude compensation of Q with respect to I	page 111
0xF40D	AGC1QUAD	Quadrature compensation of Q with respect to I	page 112
0xF40E:0xF40F (0x1)	AGCIQINx	AGC1 accumulator	page 112
0xF410	DEMOD	General register for demodulator main functions	page 112
0xF411	DMDMODCOD	Override register for MODCOD&TYPE	page 113
0xF412	DSTATUS	Demodulator status 1	page 114
0xF413	DSTATUS2	Demodulator status 2	page 115
0xF414	DMDCFGMD	Demodulator configuration 1	page 115
0xF415	DMDCFG2	Demodulator configuration 2	page 116
0xF416	DMDISTATE	AEP launch register	page 117
0xF417	DMDT0M	Coarse carrier & symbol time constant	page 117
0xF41B	DMDSTATE	Step currently in progress in the demodulator general state machine	page 117
0xF41C	DMDFLYW	Demodulator status	page 118
0xF41D	DSTATUS3	Demodulator status 3	page 118
0xF41E	DMDCFG3	Demodulator configuration 3	page 119
0xF41F	DMDCFG4	Demodulator configuration 4	page 119
0xF420	CORRELMANT	Differential correlator limit mantissa	page 120
0xF421	CORRELABS	Absolute correlator limit mantissa	page 120
0xF422	CORRELEXP	Relative and absolute correlation limit exponents	page 120
0xF424	PLHMODCOD	Current MODCOD&TYPE, only DVB-S2	page 122
0xF425	DMDREG	Various special cases	page 122
0xF42C	AGC2O	AGC2 configuration	page 122
0xF42D	AGC2REF	Demodulator general reference	page 123
0xF42E	AGC1ADJ	AGC1 loop set point	page 123
0xF436:0xF437 (0x1)	AGC2Ix	AGC2 accumulator	page 123
0xF438	CARCFG	Carrier 1 configuration	page 124
0xF439	ACLC	Alpha DVB-S1/legacy DTV	page 124
0xF43A	BCLC	Beta DVB-S1/legacy DTV	page 124
0xF43D	CARFREQ	Loop carrier 1 coefficients	page 125
0xF43E	CARHDR	PLHeader delta F coefficient in DVB-S2	page 125
0xF43F	LDT	Positive edge of carrier lock detector	page 125
0xF440	LDT2	Negative edge of carrier lock detector	page 126
0xF441	CFRICFG	CFRINIT management configuration	page 126

Table 36. DMD register list (continued)

Address	Register name	Description	Page
0xF442:0xF443 (0x1)	CFRUPx	Upper limit of carrier offset	page 126
0xF446:0xF447 (0x1)	CFRLOWx	Lower limit of carrier offset	page 127
0xF448:0xF449 (0x1)	CFRINITx	Carrier offset init value	page 127
0xF44A:0xF44B (0x1)	CFRINCx	Carrier offset increment	page 127
0xF44C	CFR2	Current carrier offset (unit: samples)	page 128
0xF44D	CFR1	Current carrier offset (unit: samples)	page 128
0xF44E	CFR0	Current carrier offset (unit: samples)	page 128
0xF44F	LDI	Carrier lock indicator accumulator	page 129
0xF450	TMGCFG	Timing loop configuration	page 129
0xF451	RTC	Timing loop DVB-S1/legacy DTV	page 130
0xF452	RTCS2	Timing loop specific to DVB-S2	page 130
0xF453	TMGTHRISE	Positive edge of timing lock detector	page 130
0xF454	TMGTHFALL	Negative edge of timing lock detector	page 131
0xF455	SFRUPRATIO	Ratio to calculate SFRUP	page 131
0xF456	SFRLOWRATIO	Ratio to calculate SFRLOW	page 131
0xF458	KREFTMG	Reference level for the symbol rate part of the coarse steps	page 131
0xF459	SFRSTEP	Scan and centering increment steps	page 132
0xF45A	TMGCFG2	Timing loop additional configuration	page 132
0xF45B	KREFTMG2	Coarse symbol rate reference frequency	page 133
0xF45D	TMGCFG3	Additional configuration of the timing loop	page 133
0xF45E:0xF45F (0x1)	SFRINITx	Symbol rate init value	page 133
0xF460:0xF461 (0x1)	SFRUPx	Symbol rate upper limit	page 134
0xF462:0xF463 (0x1)	SFRLOWx	Symbol rate lower limit	page 134
0xF464:0xF467 (0x1)	SFRx	Current symbol rate	page 134
0xF468:0xF46A (0x1)	TMGREGx	Timing recovery accumulator	page 135
0xF46B:0xF46C (0x1)	TMGLOCKx	Timing lock indicator accumulator	page 135
0xF46D	TMGOBS	Observation of the timing loop	page 135
0xF46F	EQUALCFG	DFE equalizer configuration	page 136

Table 36. DMD register list (continued)

Address	Register name	Description	Page
0xF470:0xF47E (0x2)	EQUAIx	DFE Equalizer observation	page 136
0xF471:0xF47F (0x2)	EQUAQx	DFE Equalizer observation	page 137
0xF480:0xF481 (0x1)	NNOSDATATx	Linear noise normalized on the data	page 137
0xF482:0xF483 (0x1)	NNOSDATAx	Quadratic noise normalized on the data	page 137
0xF484:0xF485 (0x1)	NNOSPLHTx	Linear noise normalized on the structures	page 138
0xF486:0xF487 (0x1)	NNOSPLHx	Quadratic noise normalized on the structures	page 138
0xF488:0xF489 (0x1)	NOSDATATx	Absolute linear noise on the data	page 139
0xF48A:0xF48B (0x1)	NNOSFRAMEx	Quadratic noise normalized on the data and by frame	page 139
0xF48C	NNOSRAD1	Quadratic noise normalized radial	page 140
0xF48D	NNOSRAD0	Quadratic noise normalized radial	page 140
0xF48E	NOSCFGF1	Configuration of the noise indicators	page 141
0xF490	CAR2CFG	Carrier loop 2 configuration	page 141
0xF491	CFR2CFR1	Carrier offset transfer control	page 142
0xF493	CFR22	Current carrier offset 2 (unit: symbols)	page 142
0xF494	CFR21	Current carrier offset 2 (unit: symbols)	page 143
0xF495	CFR20	Current carrier offset 2 (unit: symbols)	page 143
0xF497	ACLC2S2Q	Alpha specific DVB-S2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)	page 143
0xF498	ACLC2S28	Alpha specific DVB-S2 data 8PSK	page 144
0xF49C	BCLC2S2Q	Beta specific DVB-S2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)	page 144
0xF49D	BCLC2S28	Beta specific DVB-S2 data 8PSK	page 144
0xF4AC:0xF4AE (0x1)	PLROOTx	Gold code description	page 145
0xF4B7:0xF4B9 (0x1)	MODCODLSTx	List of prohibited MODCOD	page 145
0xF4BA	MODCODLSTA	List of prohibited MODCOD	page 146
0xF4BB	MODCODLSTB	List of prohibited MODCOD	page 147
0xF4BC	MODCODLSTC	List of prohibited MODCOD	page 147
0xF4BD	MODCODLSTD	List of prohibited MODCOD	page 147
0xF4C0	GAUSSR0	Gaussien phase detector radius, R0	page 148

Table 36. DMD register list (continued)

Address	Register name	Description	Page
0xF4C1	CCIR0	CCI phase detector radius, R0	page 148
0xF4C2	CCIQUANT	CCI detector quantifier	page 149
0xF4C3	CCITHRES	CCI threshold detector level	page 149
0xF4C4	CCIACC	CCI detector accumulator	page 149
0xF4C5	DSTATUS4	Demodulator Status	page 150
0xF4C6	DMDRESCFG	FIFO results configuration	page 150
0xF4C7	DMDRESADR	FIFO results status	page 151
0xF4C8:0xF4CF (0x1)	DMDRESDATAx	FIFO results	page 151
0xF4D0:0xF4D6 (0x2)	FFEIx	FFE Equalizer coefficients	page 152
0xF4D1:0xF4D7 (0x2)	FFEQx	FFE Equalizer coefficients	page 153
0xF4D8	FFECFG	FFE equalizer configuration	page 153
0xF500	SMAPCOEF7	LLR gain in DVB-S2 QPSK	page 154
0xF501:0xF502 (0x1)	SMAPCOEFx	LLR gain in DVB-S2 8PSK	page 154
0xF509:0xF50A (0x1)	NOSTHRESx	Noise level Threshold x	page 154
0xF50B	NOSDIFF1	Margin Indicator	page 155
0xF50C	RAINFADE	Rain fading Indicator	page 155
0xF50D	NOSRAMCFG	C/N estimator control	page 156
0xF50E	NOSRAMPOS	C/N estimator Position	page 157
0xF50F	NOSRAMVAL	C/N estimator Value	page 157
0xF520	DMDPLHSTAT	PLHeaders failure rate	page 157
0xF522:0xF525 (0x1)	LOCKTIMEx	Demodulator locking time	page 158

Table 37. TUN register list

Address	Register name	Description	Page
0xF4E1	TNRCFG2	Tuner & input IQ control	page 159

Table 38. DVB1 register list

Address	Register name	Description	Page
0xF532	VITSCALE	Additional configuration of Viterbi decoder	page 160
0xF533	FECM	Viterbi decoder configuration	page 160
0xF534	VTH12	Error threshold for puncture rate 1/2	page 161
0xF535	VTH23	Error threshold for puncture rate 2/3	page 161

Table 38. DVB1 register list

Address	Register name	Description	Page
0xF536	VTH34	Error threshold for puncture rate 3/4	page 161
0xF537	VTH56	Error threshold for puncture rate 5/6	page 162
0xF538	VTH67	Error threshold for puncture rate 6/7	page 162
0xF539	VTH78	Error threshold for puncture rate 7/8	page 162
0xF53A	VITCURPUN	Current puncture rate on the Viterbi decoder	page 162
0xF53B	VERROR	Current error rate	page 163
0xF53C	PRVIT	List of authorized puncture rates	page 163
0xF53D	VAVSRVIT	Viterbi decoder search speeds	page 164
0xF53E	VSTATUSVIT	Viterbi decoder status	page 164
0xF53F	VTHINUSE	Viterbi threshold currently in use	page 165
0xF540	KDIV12	Gain (k_divider) of puncture rate 1/2	page 165
0xF541	KDIV23	Gain (k_divider) of puncture rate 2/3	page 165
0xF542	KDIV34	Gain (k_divider) of puncture rate 3/4	page 166
0xF543	KDIV56	Gain (k_divider) of puncture rate 5/6	page 166
0xF544	KDIV67	Gain (k_divider) of puncture rate 6/7	page 166
0xF545	KDIV78	Gain (k_divider) of puncture rate 7/8	page 167

Table 39. DVB2 register list

Address	Register name	Description	Page
0xF550	PDELCTRL1	Packet delineator configuration	page 168
0xF551	PDELCTRL2	Packet delineator additional configuration	page 168
0xF55E	ISIENTRY	MIS mode selection filter	page 168
0xF55F	ISIBITENA	MIS mode selection mask	page 169
0xF560:0xF561 (0x1)	MATSTRx	MATYPE of the current frame	page 169
0xF562:0xF563 (0x1)	UPLSTRx	UPL of the current frame	page 169
0xF564:0xF565 (0x1)	DFLSTRx	DFL of the current frame	page 170
0xF566	SYNCSTR	SYNC of the current frame	page 170
0xF567:0xF568 (0x1)	SYNCDSTRx	SYNCD of the current frame	page 170
0xF569	PDELSTATUS1	Packet delineator status	page 171
0xF56A	PDELSTATUS2	Additional status for packet delineator	page 171
0xF56B:0xF56C (0x1)	BBFCRCKOx	BBHeader KO counter	page 172

Table 39. DVB2 register list (continued)

Address	Register name	Description	Page
0xF56D:0xF56E (0x1)	UPCRCKOx	Packet KO counter	page 172
0xFA03:0xFA10 (0x1)	NBITER_NFx	Number of LDPC decoding iterations	page 173
0xFA43:0xFA50 (0x1)	GAINLLR_NFx	LDPC input LLR gain	page 174
0xFA86	GENCFG	General Configuration	page 175
0xFA96:0xFA97 (0x1)	LDPCERRx	LDPC error counter	page 175
0xFA98	BCHERR	BCH error	page 175
0xFAB1	MAXEXTRAITER	LDPC Extra-iteration value	page 176
0xFABC	STATUSITER	LDPC iteration number performed	page 176
0xFABD	STATUSMAXITER	LDPC maximum iteration number performed	page 176

Table 40. TS register list

Address	Register name	Description	Page
0xF570	TSSTATEM	Configuration of merger-hardware stream line 1	page 177
0xF572	TSCFGH	Configuration of merger-hardware stream line 1	page 178
0xF573	TSCFGM	Configuration of merger-hardware stream line 1	page 179
0xF574	TSCFGL	Configuration of merger-hardware stream line 1	page 179
0xF576	TSINSDELH	Insertion/deletion mask of output packet parts	page 181
0xF579	TSDIVN	Output frequency control	page 181
0xF57A	TSCFG4	Stream merger line 1 hardware configuration	page 182
0xF580	TSSPEED	CLKOUT frequency	page 182
0xF581	TSSTATUS	Merger-hardware stream status	page 183
0xF582	TSSTATUS2	Additional status of merger-hardware stream	page 184
0xF583:0xF584 (0x1)	TSBITRATEx	Observation of raw bit rate	page 184
0xF598:0xF59C (0x4)	ERRCTRLx	Configuration of error counter x	page 185
0xF599:0xF59B (0x1)	ERRCNTx	Result of error counter 2	page 187
0xF59D	ERRCNT22	Result of error counter 2	page 187
0xF59E	ERRCNT21	Result of error counter 2	page 188
0xF59F	ERRCNT20	Result of error counter 2	page 188
0xF5A0	FECSPY	FEC spy configuration	page 188
0xF5A1	FSPYCFG	FEC spy configuration	page 189
0xF5A2	FSPYDATA	Tested packet contents	page 190

Table 40. TS register list (continued)

Address	Register name	Description	Page
0xF5A3	FSPYOUT	FEC spy miscellaneous configuration	page 192
0xF5A4	FSTATUS	FEC spy status	page 192
0xF5A8:0xF5AC (0x1)	FBERCPTx	BER/PER meter byte counter	page 193
0xF5AD:0xF5AF (0x1)	FBERERRx	BER/PER meter error bit counter	page 193
0xF5B2	FSPYBER	BER/PER meter configuration	page 194
0xF630	TSGENERAL	General configuration of the stream merger hardware	page 195

Table 41. SFEC register list

Address	Register name	Description	Page
0xF5C3	SFECSTATUS	Viterbi Super FEC Status	page 196
0xF5C4	SFKDIV12	Super FEC K divider 12	page 196
0xF5C5	SFKDIV23	Super FEC K divider 23	page 197
0xF5C6	SFKDIV34	Super FEC K divider 34	page 197
0xF5C7	SFKDIV56	Super FEC K divider 56	page 197
0xF5C8	SFKDIV67	Super FEC K divider 67	page 198
0xF5C9	SFKDIV78	Super FEC K divider 78	page 198
0xF5CC	SFSTATUS	Super FEC status (delay line)	page 198
0xF5D8	SFERRCTRL	Configuration of the Super FEC error counter	page 199
0xF5D9:0xF5DB (0x1)	SFERRCNTx	Super FEC error counter value	page 199

Table 42. DISEQC register list

Address	Register name	Description	Page
0xF700	DISIRQCFG	DiSEqC interrupt enable register	page 201
0xF701	DISIRQSTAT	DiSEqC interrupt status register	page 201
0xF702	DISTXCFG	DiSEqC Transmitter Control	page 202
0xF703	DISTXSTATUS	DiSEqC Transmitter Status	page 202
0xF704	DISTXBYTES	DiSEqC Tx Number of bytes in FIFO	page 203
0xF705	DISTXFIFO	DiSEqC Transmitter FIFO	page 203
0xF706	DISTXF22	DiSEqC 22 kHz Transmitter Frequency Tone Control	page 203
0xF708	DISTIMEOCFG	DiSEqC Interrupt Timer Configuration	page 204
0xF709	DISTIMEOUT	DiSEqC Interrupt Timer	page 204
0xF70A	DISRXCFG	DiSEqC Receiver Control	page 204
0xF70B:0xF70C (0x1)	DISRXSTATx	DiSEqC Receiver Status	page 205

Table 42. DISEQC register list (continued)

Address	Register name	Description	Page
0xF70D	DISRXBYTES	DiSEqC Rx Number of bytes in FIFO	page 206
0xF70E:0xF70F (0x1)	DISRXPARITYx	DiSEqC Receiver Parity Bytes	page 206
0xF710	DISRXFIFO	DiSEqC Receiver FIFO	page 206
0xF711:0xF712 (0x1)	DISRXDCx	DiSEqC Rx DC Value observation	page 207
0xF714	DISRXF221	DiSEqC 22 kHz Receiver Frequency Tone Control	page 207
0xF715	DISRXF220	DiSEqC 22 kHz Receiver Frequency Tone Control	page 207
0xF716	DISRXF100	DiSEqC Rx 100 kHz Frequency Control	page 208
0xF71C	DISRXSHORT22K	DiSEqC Rx Short22k length	page 208
0xF71E	ACRPRESC	Auxiliary clock control	page 208
0xF71F	ACRDIV	Auxiliary clock division control	page 209

Table 43. TST register list

Address	Register name	Description	Page
0xFF48	TCTL4	Test of demodulator Carrier loop	page 210

17.2 SYS register descriptions

MID — Chip identification

7	6	5	4	3	2	1	0
MCHIP_IDENT				MRELEASE			
R				R			

Address: 0xF100

Type: R

Reset: 0x50

Description: This represents the ID and release number. For example, a 2.3 release would be read 0x23.

[7:4] **MCHIP_IDENT**: Base layer version (unsigned)

[3:0] **MRELEASE**: Metal fix version (unsigned)

DID — Device Identification

7	6	5	4	3	2	1	0
DEVICE_ID							
R							

Address: 0xF101

Type: R

Reset: 0x20

Description: Device Identification

[7:0] **DEVICE_ID**: Device ID (unsigned)

DACR1 — DAC control

7	6	5	4	3	2	1	0
DAC_MODE			RESERVED	DAC_VALUE[11:8]			
R/W			R	R/W			

Address: 0xF113

Type: R/W

Reset: 0x0

Description: DACR1 and DACR2 generate a sigma-delta digital signal to be output to any of the GPIOs

[7:5] **DAC_MODE**: Controls the clock frequency used to generate DAC_VALUE
110: mclk/4
101: mclk/8
100: mclk/32 (unsigned)

[3:0] **DAC_VALUE**: DAC value (unsigned)

DACR2 DAC control

7	6	5	4	3	2	1	0
DAC_VALUE[7:0]							
R/W							

Address: 0xF114

Type: R/W

Reset: 0x0

Description: DAC control

[7:0] **DAC_VALUE**: DAC value (unsigned)

PADCFG Dedicated Pads Configuration

7	6	5	4	3	2	1	0
RESERVED						AGCRF1_OPD	AGCRF1_XOR
R						R/W	R/W

Address: 0xF11A

Type: R/W

Reset: 0x5

Description: Dedicated Pads Configuration

[1] **AGCRF1_OPD**: open-drain configuration of AGCRF1 pin
0: push-pull
1: open drain (unsigned)

[0] **AGCRF1_XOR**: 1: inverts AGCRF1 signal polarity (unsigned)

OUTCFG2 Transport stream output configuration 2

7	6	5	4	3	2	1	0
RESERVED				TS1_ERROR_XOR	TS1_DPN_XOR	TS1_STROUT_XOR	TS1_CLOCKOUT_XOR
R				R/W	R/W	R/W	R/W

Address: 0xF11B

Type: R/W

Reset: 0x0

Description: Transport stream (TS) output configuration 2

[3] **TS1_ERROR_XOR**: 1: inverts Transport Stream 1 ERROR signal polarity (unsigned)

[2] **TS1_DPN_XOR**: 1: inverts Transport Stream 1 DP/N signal polarity (unsigned)

[1] **TS1_STROUT_XOR**: 1: inverts Transport Stream 1 STR_OUT signal polarity (unsigned)

[0] **TS1_CLOCKOUT_XOR**: 1: inverts Transport Stream 1 CLK_OUT signal polarity (unsigned)

OUTCFG Transport stream output configuration

7	6	5	4	3	2	1	0
RESERVED			TS1_OUTSER_HZ	RESERVED	TS1_OUTPAR_HZ	TS_SERDATA0	RESERVED
R			R/W	R	R/W	R/W	R

Address: 0xF11C

Type: R/W

Reset: 0x7E

Description: Transport stream (TS) output configuration

[4] **TS1_OUTSER_HZ**: 1: sets Transport Stream 1 Serial pins to high impedance
0: sets Transport Stream 1 Serial pins to push-pull (unsigned)

[2] **TS1_OUTPAR_HZ**: 1: sets Transport Stream 1 Parallel pins to high impedance
0: sets Transport Stream 1 Parallel pins to push-pull (unsigned)

[1] **TS_SERDATA0**: 1: Serial data output is DATA0
0: Serial data output is DATA7 (unsigned)

IRQSTATUSx Interrupt request status

	7	6	5	4	3	2	1	0
IRQSTATUS3	RESERVED		SPLL_LOCK	SSTREAM_LCK_1	RESERVED			SDVBS1_PRF_1
	R		R	R	R			R

	7	6	5	4	3	2	1	0
IRQSTATUS2	SSPY_ENDSIM_1	RESERVED					SPKTDEL_ERROR_1	SPKTDEL_LOCKB_1
	R	R					R	R

	7	6	5	4	3	2	1	0
IRQSTATUS1	SPKTDEL_LOCK_1	RESERVED		SFEC_LOCKB_1	SFEC_LOCK_1	RESERVED		
	R	R		R	R	R		

	7	6	5	4	3	2	1	0
IRQSTATUS0	SDEMOD_LOCKB_1	SDEMOD_LOCK_1	SDEMOD_IRQ_1	SBCH_ERRFLAG	RESERVED			SDISEQC1_IRQ
	R	R	R	R	R			R

Address: 0xF123 - x * 0x1 (x=0 to 3)

Type: RH

Reset: Undefined

Description: Status register block giving the list of currently pending interrupt request occurrences.
0: no interrupt request detected since last erase of this bit.
1: an interrupt request has been detected since last erase of this bit. The bits of these registers are reset to 0 when the register is read from or written to.

IRQSTATUS3: [5] **SPLL_LOCK**: 1: PLL is locked (read put to 0 on a read,unsigned)

IRQSTATUS3: [4] **SSTREAM_LCK_1**: 1: transport stream 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS3: [0] **SDVBS1_PRF_1**: 1: dvb-s1 block 1 has found the puncture rate (read put to 0 on a read,unsigned)

IRQSTATUS2: [7] **SSPY_ENDSIM_1**: 1: fec spy 1 has finished (read put to 0 on a read,unsigned)

IRQSTATUS2: [1] **SPKTDEL_ERROR_1**: 1: dvb-s2 packet delineator 1 error (read put to 0 on a read,unsigned)

IRQSTATUS2: [0] **SPKTDEL_LOCKB_1**: 1: dvb-s2 packet delineator 1 is unlocked (read put to 0 on a read,unsigned)

IRQSTATUS1: [7] **SPKTDEL_LOCK_1**: 1: dvb-s2 packet delineator 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS1: [4] **SFEC_LOCKB_1**: 1: fec 1 (dvb-s1 or dvb-s2) 1 is unlocked (read put to 0 on a read,unsigned)

IRQSTATUS1: [3] **SFEC_LOCK_1**: 1: fec 1 (dvb-s1 or dvb-s2) 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS0: [7] **SDEMOD_LOCKB_1**: 1: demod block 1 is unlocked (read put to 0 on a read,unsigned)

IRQSTATUS0: [6] **SDEMOD_LOCK_1**: 1: demod block 1 is locked (read put to 0 on a read,unsigned)

IRQSTATUS0: [5] **SDEMOD_IRQ_1**: demod block 1 irq value (read put to 0 on a read,unsigned)

IRQSTATUS0: [4] **SBCH_ERRFLAG**: 1: dvb-s2 bch has an error (read put to 0 on a read,unsigned)

IRQSTATUS0: [0] **SDISEQC1_IRQ**: diseqc block 1 irq value (read put to 0 on a read,unsigned)

IRQMASKx Interrupt request mask

	7	6	5	4	3	2	1	0
IRQMASK3	RESERVED		MPLL_LOCK	MSTREAM_LCK_1	RESERVED			MDVBS1_PRF_1
	R		R/W	R/W	R			R/W

	7	6	5	4	3	2	1	0
IRQMASK2	MSPY_ENDSIM_1	RESERVED					MPKTDEL_ERROR_1	MPKTDEL_LOCKB_1
	R/W	R					R/W	R/W

	7	6	5	4	3	2	1	0
IRQMASK1	MPKTDEL_LOCK_1	RESERVED		MFEC_LOCKB_1	MFEC_LOCK_1	RESERVED		
	R/W	R		R	R	R		

	7	6	5	4	3	2	1	0
IRQMASK0	MDEMOD_LOCKB_1	MDEMOD_LOCK_1	MDEMOD_IRQ_1	MBCH_ERRFLAG	RESERVED			MDISEQC1_IRQ
	R/W	R/W	R/W	R/W	R			R/W

Address: 0xF127 - x * 0x1 (x=0 to 3)

Type: R/W

Reset: 0x0

Description: Enable interrupt mask. These registers give the list of interrupt request occurrences which are enabled to generate the IRQ signal.
1: interrupt request enabled to generate IRQ signal.
0: interrupt request not enabled to generate IRQ signal.

IRQMASK3: [5] **MPLL_LOCK**: (unsigned)

IRQMASK3: [4] **MSTREAM_LCK_1**: (unsigned)

IRQMASK3: [0] **MDVBS1_PRF_1**: (unsigned)

IRQMASK2: [7] **MSPY_ENDSIM_1**: (unsigned)

IRQMASK2: [1] **MPKTDEL_ERROR_1**: (unsigned)

IRQMASK2: [0] **MPKTDEL_LOCKB_1**: (unsigned)

IRQMASK1: [7] **MPKTDEL_LOCK_1**: (unsigned)

IRQMASK1: [4] **MFEC_LOCKB_1**: (read put to 0 on a read,unsigned)

IRQMASK1: [3] **MFEC_LOCK_1**: (read put to 0 on a read,unsigned)

IRQMASK0: [7] **MDEMOD_LOCKB_1**: (unsigned)

IRQMASK0: [6] **MDEMOD_LOCK_1**: (unsigned)

IRQMASK0: [5] **MDEMOD_IRQ_1**: (unsigned)

IRQMASK0: [4] **MBCH_ERRFLAG**: (unsigned)

IRQMASK0: [0] **MDISEQC1_IRQ**: (unsigned)

I2CCFG I2C bus configuration

7	6	5	4	3	2	1	0
RESERVED				I2C_FASTMODE	RESERVED	I2CADDR_INC	
R				R/W	R	R/W	

Address: 0xF129

Type: R/W

Reset: 0x88

Description: I2C bus configuration

[3] **I2C_FASTMODE**: 1: I2C bus is in fast mode (default recommended mode). The oversampling ratio of the I2C bus rate is 1/16 of the master clock.
0: I2C bus oversampling ratio 1/41 of the master clock. (unsigned)

[1:0] **I2CADDR_INC**: controls the auto-increment value for burst access modes.
00: default, +1 increment.
01: stop increment mode, automatic increment is frozen.
10: reserved
11: reserved. (unsigned)

I2CRPT I2C bus repeater control

7	6	5	4	3	2	1	0
I2CT_ON	ENARPT_LEVEL			SCLT_DELAY	STOP_ENABLE	STOP_SDAT2SDA	RESERVED
R/W	R/W			R/W	R/W	R/W	R

Address: 0xF12A

Type: R/W

Reset: 0xB2

Description: I2C bus repeater control

[7] **I2CT_ON**: 1: repeater is turned on.
This bit is automatically set to 0 when STOP_ENABLE = 1 by a stop event on the SDA line. (unsigned)

[6:4] **ENARPT_LEVEL**: the speed of the I2C repeater obtained by dividing the internal chip frequency (that is, 135 MHz).
000: divide by 256 (slow)
001: divide by 128
010: divide by 64
011: divide by 32
100: divide by 16
101: divide by 8
110: divide by 4
111: divide by 2 (very fast) (unsigned)

[3] **SCLT_DELAY**: SCL to SCLT signal transmission mode (SCLT2, for P2).
0: SCLT line is not delayed (default).
1: SCLT line is delayed with the same enarpt_level delay as SDAT. (unsigned)

[2] **STOP_ENABLE**: I2C repetition end mode.
0: manual: end of repetition when I2CT_ON is set to 0 by software, so several I2C accesses can be transmitted.
1: automatic: end of repetition on the next stop event on SDA line. (unsigned)

[1] **STOP_SDAT2SDA**: stop propagation from SDAT to SDA (SDAT2 for P2) line.
0: bidirectional mode: data is transferred from SDAT to SDA and SDA to SDAT.
1: monodirectional mode: data is never transferred from SDAT to SDA. (unsigned)

GPIOxCFG — General purpose IO control

	7	6	5	4	3	2	1	0
GPIO0CFG	GPIO0_OPD			GPIO0_CONFIG				GPIO0_XOR
GPIO1CFG	GPIO1_OPD			GPIO1_CONFIG				GPIO1_XOR
GPIO2CFG	GPIO2_OPD			GPIO2_CONFIG				GPIO2_XOR
GPIO3CFG	GPIO3_OPD			GPIO3_CONFIG				GPIO3_XOR
GPIO4CFG	GPIO4_OPD			GPIO4_CONFIG				GPIO4_XOR
GPIO5CFG	GPIO5_OPD			GPIO5_CONFIG				GPIO5_XOR
GPIO6CFG	GPIO6_OPD			GPIO6_CONFIG				GPIO6_XOR
GPIO7CFG	GPIO7_OPD			GPIO7_CONFIG				GPIO7_XOR
GPIO8CFG	GPIO8_OPD			GPIO8_CONFIG				GPIO8_XOR
GPIO9CFG	GPIO9_OPD			GPIO9_CONFIG				GPIO9_XOR
GPIO10CFG	GPIO10_OPD			GPIO10_CONFIG				GPIO10_XOR
GPIO11CFG	GPIO11_OPD			GPIO11_CONFIG				GPIO11_XOR
GPIO12CFG	GPIO12_OPD			GPIO12_CONFIG				GPIO12_XOR
	R/W			R/W				R/W

Address: 0xF140 + x * 0x1 (x=0 to 12)

Type: R/W

Reset: 0x82

Description: Control for configurations of pins GPIOx.

GPIO0CFG: [7] **GPIO0_OPD**: open-drain configuration of GPIO pin
0: push-pull
1: open drain (unsigned)

GPIO0CFG: [6:1] **GPIO0_CONFIG**: general purpose input and output configuration. (unsigned)

GPIO0CFG: [0] **GPIO0_XOR**: XOR the result of GPIOCFG configuration.
0: no change
1: invert the logical value. (unsigned)

GPIO1CFG: [7] **GPIO1_OPD**: (unsigned)

GPIO1CFG: [6:1] **GPIO1_CONFIG**: (unsigned)

GPIO1CFG: [0] **GPIO1_XOR**: (unsigned)

GPIO2CFG: [7] **GPIO2_OPD**: (unsigned)

GPIO2CFG: [6:1] **GPIO2_CONFIG**: (unsigned)

GPIO2CFG: [0] **GPIO2_XOR**: (unsigned)

GPIO3CFG: [7] **GPIO3_OPD**: (unsigned)

GPIO3CFG: [6:1] **GPIO3_CONFIG**: (unsigned)

GPIO3CFG: [0] **GPIO3_XOR**: (unsigned)

GPIO4CFG: [7] **GPIO4_OPD**: (unsigned)

GPIO4CFG: [6:1] **GPIO4_CONFIG**: (unsigned)

GPIO4CFG: [0] **GPIO4_XOR**: (unsigned)

GPIO5CFG: [7] **GPIO5_OPD**: (unsigned)

GPIO5CFG: [6:1] **GPIO5_CONFIG**: (unsigned)

GPIO5CFG: [0] **GPIO5_XOR**: (unsigned)

GPIO6CFG: [7] **GPIO6_OPD**: (unsigned)

GPIO6CFG: [6:1] **GPIO6_CONFIG**: (unsigned)

GPIO6CFG: [0] **GPIO6_XOR**: (unsigned)

GPIO7CFG: [7] **GPIO7_OPD**: (unsigned)

GPIO7CFG: [6:1] **GPIO7_CONFIG**: (unsigned)

GPIO7CFG: [0] **GPIO7_XOR**: (unsigned)

GPIO8CFG: [7] **GPIO8_OPD**: (unsigned)

GPIO8CFG: [6:1] **GPIO8_CONFIG**: (unsigned)

GPIO8CFG: [0] **GPIO8_XOR**: (unsigned)

GPIO9CFG: [7] **GPIO9_OPD**: (unsigned)

GPIO9CFG: [6:1] **GPIO9_CONFIG**: (unsigned)

GPIO9CFG: [0] **GPIO9_XOR**: (unsigned)

GPIO10CFG: [7] **GPIO10_OPD**: (unsigned)

GPIO10CFG: [6:1] **GPIO10_CONFIG**: (unsigned)

GPIO10CFG: [0] **GPIO10_XOR**: (unsigned)

GPIO11CFG: [7] **GPIO11_OPD**: (unsigned)

GPIO11CFG: [6:1] **GPIO11_CONFIG**: (unsigned)

GPIO11CFG: [0] **GPIO11_XOR**: (unsigned)

GPIO12CFG: [7] **GPIO12_OPD**: (unsigned)

GPIO12CFG: [6:1] **GPIO12_CONFIG**: (unsigned)

GPIO12CFG: [0] **GPIO12_XOR**: (unsigned)

STRSTATUSx — Stream status

	7	6	5	4	3	2	1	0
STRSTATUS1	STRSTATUS_SEL2				STRSTATUS_SEL1			
STRSTATUS2	STRSTATUS_SEL4				STRSTATUS_SEL3			
STRSTATUS3	STRSTATUS_SEL6				STRSTATUS_SEL5			
	R/W				R/W			

Address: 0xF16A + (x-1) * 0x1 (x=1 to 3)

Type: R/W

Reset: 0x60, 0x71, 0x82

Description: Configure what information will be available when selecting streamstatus1..6 GPIO functions :

0: DEMOD_SYMIQ - Demodulator detected an IQ inversion
1: DEMOD_LOCKED - Demodulator locked flag
2: DEMOD_FAIL - Demodulator failed flag
3: PKTDEL_LOCKED - Packet delineator locked flag
4: PKTDEL_ERROR - Packet delineator error flag
5: VITERBI_PRF - DVB-S1 Viterbi puncture rate found flag
6: DEMOD_SYMIQ2 - Reserved
7: DEMOD_LOCKED2 - Reserved
8: DEMOD_FAIL2 - Reserved
9: PKTDEL_LOCKED2 - Reserved
10: PKTDEL_ERROR2 - Reserved
11: VITERBI_PRF2 - Reserved
12: STREAM_LOCKED1 - Stream 1 locked flag (up to transport)
13: STREAM_LOCKED2 - Stream 2 locked flag (up to transport)
14: Reserved
15: Reserved

STRSTATUS1: [7:0] **STRSTATUS_SEL[2:1]**: (unsigned)

STRSTATUS2: [7:0] **STRSTATUS_SEL[4:3]**: (unsigned)

STRSTATUS3: [7:0] **STRSTATUS_SEL[6:5]**: (unsigned)

NCOARSE — Analog PLL divider control

7	6	5	4	3	2	1	0
CP					IDF		
R/W					R/W		

Address: 0xF1B3

Type: R/W

Reset: 0x39

Description: Analog PLL divider control

[7:3] **CP**: Charge Pump Setting
It is linked to NDIV
The recommended setting are
NDIV = 8 - 71 -> CP = 7
NDIV = 72 - 79 -> CP = 8
NDIV = 80 - 87 -> CP = 9
NDIV = 88 - 95 -> CP = 10
NDIV = 96 - 103 -> CP = 11
NDIV = 104 - 111 -> CP = 12
NDIV = 112 - 119 -> CP = 13
NDIV = 120 - 127 -> CP = 14
NDIV = 128 - 135 -> CP = 15
NDIV = 136 - 143 -> CP = 16
NDIV = 144 - 151 -> CP = 17
NDIV = 152 - 159 -> CP = 18
NDIV = 160 - 167 -> CP = 19
NDIV = 168 - 175 -> CP = 20
NDIV = 176 - 183 -> CP = 21
NDIV = 184 - 191 -> CP = 22
NDIV = 192 - 199 -> CP = 23
NDIV = 200 - 207 -> CP = 24
NDIV = 208 - 215 -> CP = 25
NDIV = 216 - 223 -> CP = 26
NDIV = 224 - 225 -> CP = 27 (unsigned)

[2:0] **IDF**: Input Division Factor
Fmclk2 = Fref x NDIV / IDF / 2
For Fref = 30MHz, the reset values program a Fmclk2 = 270MHz
IDF = 1 when bitfield is at 0, same value as bitfield otherwise (unsigned)

NCOARSEx — Analog PLL divider control

	7	6	5	4	3	2	1	0
NCOARSE1	N_DIV							
	R/W							

	7	6	5	4	3	2	1	0
NCOARSE2	RESERVED		ODF					
	R		R/W					

Address: 0xF1B4 + (x-1) * 0x1 (x=1 to 2)

Type: R/W

Reset: 0x12, 0x4

Description: Analog PLL divider control

NCOARSE1: [7:0] **N_DIV**: PLL Divider
Fmclk2 = Fref x N_DIV / IDF / 2
For Fref = 30MHz, the reset values program a Fmclk2 = 270MHz
NDIV must be between 8 ad 225 inclusive
Forbidden : NDIV < 8 and NDIV > 225 (unsigned)

NCOARSE2: [5:0] **ODF**: Output Division Factor
Fana = Fref x NDIV / IDF / ODF
For Fref = 30MHz, the reset values program a Fana = 135MHz
ODF = 1 when bitfield is at 0, same value as bitfield otherwise (unsigned)

SYNTCTRL — Frequency synthesis control

7	6	5	4	3	2	1	0
STANDBY	BYPASSPLLCORE	RESERVED		STOP_PLL	RESERVED	OSCI_E	RESERVED
R/W	R/W	R		R/W	R	R/W	R

Address: 0xF1B6

Type: R/W

Reset: 0x42

Description: Frequency synthesis control

[7] **STANDBY**: stop all clocks except I2C clock.
0: device active
1: device in standby (unsigned)

[6] **BYPASSPLLCORE**: controls the digital clocks
1: PLL is bypassed (external clocks)
0: digital clocks from PLL (unsigned)

[3] **STOP_PLL**: 1: the analog PLL is stopped (unsigned)

[1] **OSCI_E**: 1: the OSCI pad is enabled (unsigned)

FILTCTRL — Filter control

7	6	5	4	3	2	1	0
RESERVED						INV_CLKFSK	BYPASS_APPLI
R						R/W	R/W

Address: 0xF1B7

Type: R/W

Reset: 0x1

Description: Filter control

[1] **INV_CLKFSK**: 1: inverts the FSK clock (unsigned)

[0] **BYPASS_APPLI**: control external clocks
1: when PLL is bypassed, the clocks are derived from one external clock on pin CLKI which should be at a frequency = Fmclk * 2
0: when PLL is bypassed, two clocks are provided on pins CLKI and CLKI2 (CLKI = Fmclk * 2, CLKI2 = Fmclk) (unsigned)

PLLSTAT PLL Status

7	6	5	4	3	2	1	0
RESERVED							PLLLOCK
R							R

Address: 0xF1B8

Type: R

Reset: Undefined

Description: PLL Status

[0] **PLLLOCK**: 1: the PLL is locked
0: the PLL is unlocked (unsigned)

STOPCLKx Stop clock control x

	7	6	5	4	3	2	1	0
STOPCLK1	RESERVED							INV_CLKADCI1
	R							R/W

	7	6	5	4	3	2	1	0
STOPCLK2	RESERVED			STOP_DVBS2FEC	RESERVED	STOP_DVBS1FEC	RESERVED	STOP_DEMOD
	R			R/W	R	R/W	R	R/W

Address: 0xF1C2 + (x-1) * 0x1 (x=1 to 2)

Type: R/W

Reset: 0x0

Description: Stop clock control x

STOPCLK1: [0] **INV_CLKADCI1**: 1: inverts the ADC interface 1 clock (unsigned)

STOPCLK2: [4] **STOP_DVBS2FEC**: 1: stops the dvb-s2 fec path 1 clock (unsigned)

STOPCLK2: [2] **STOP_DVBS1FEC**: 1: stops the dvb-s1 fec path 1 clock (unsigned)

STOPCLK2: [0] **STOP_DEMOD**: 1: stops the demodulator 1 clock (unsigned)

PREGCTL Power Regulator Control

7	6	5	4	3	2	1	0
REG3V3TO2V5_POFF	RESERVED						
R/W	R						

Address: 0xF1C8

Type: R/W

Reset: 0x0

Description: Power Regulator Control

[7] **REG3V3TO2V5_POFF**: 1: DC-DC Linear Regulator 3v3 -> 2v5 Power Off (unsigned)

TSTTNR0 FSK analog cell test and configuration

7	6	5	4	3	2	1	0
RESERVED					FSK_PON	RESERVED	
R					R/W	R	

Address: 0xF1DF

Type: R/W

Reset: 0x4

Description: FSK analog cell test and configuration

[2] **FSK_PON**: 1: fsk analog cell power on
0: FSK analog cell power off (unsigned)

TSTTNR1 ADC 1 test and configuration

7	6	5	4	3	2	1	0
RESERVED						ADC1_PON	RESERVED
R						R/W	R

Address: 0xF1E0

Type: R/W

Reset: 0x26

Description: ADC 1 test and configuration

[1] **ADC1_PON**: 1: ADC 1 power on
0: ADC 1 power off (unsigned)

TSTTNR2 DiSEqC 1 test and configuration

7	6	5	4	3	2	1	0
RESERVED		I2C_DISEQC_PON	RESERVED	DISEQC_CLKDIV			
R		R/W	R	R/W			

Address: 0xF1E1

Type: R/W

Reset: 0x6B

Description: DiSEqC 1 test and configuration

[5] **I2C_DISEQC_PON**: 1: DiSEqC ADC 1 power on
0: DiSEqC ADC 1 power off (unsigned)

[3:0] **DISEQC_CLKDIV**: Fdiseqc = F135 / 2x(dig_diseqc_clkdiv+17) (unsigned)

17.3 FSK register descriptions

FSKTFC2 FSK Transmitter gain and carrier frequency

7	6	5	4	3	2	1	0
FSKT_KMOD						FSKT_CAR[17:16]	
R/W						R/W	

Address: 0xF170

Type: R/W

Reset: 0x8C

Description: FSK Transmitter gain and carrier frequency

[7:2] **FSKT_KMOD**: gain of the FSK modulator (unsigned)

[1:0] **FSKT_CAR**: FSK modulator carrier frequency (unsigned)

FSKTFC1 FSK transmitter gain and carrier frequency

7	6	5	4	3	2	1	0
FSKT_CAR[15:8]							
R/W							

Address: 0xF171

Type: R/W

Reset: 0x45

Description: FSK transmitter gain and carrier frequency

[7:0] **FSKT_CAR**: FSK modulator carrier frequency (unsigned)

FSKTFC0 FSK transmitter gain and carrier frequency

7	6	5	4	3	2	1	0
FSKT_CAR[7:0]							
R/W							

Address: 0xF172

Type: R/W

Reset: 0xC9

Description: FSK transmitter gain and carrier frequency

[7:0] **FSKT_CAR**: FSK modulator carrier frequency (unsigned)

FSKTDELTAFx FSK transmitter frequency deviation

	7	6	5	4	3	2	1	0
FSKTDELTAF1	RESERVED				FSKT_DELTAF[11:8]			
	R				R/W			

	7	6	5	4	3	2	1	0
FSKTDELTAF0	FSKT_DELTAF[7:0]							
	R/W							

Address: 0xF174 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x1, 0x37

Description: FSK transmitter frequency deviation

FSKTDELTAF1: [3:0]
FSKTDELTAF0: [7:0]

FSKT_DELTAF: FSK modulator frequency deviation (unsigned)

FSKTCTRL FSK transmitter control

7	6	5	4	3	2	1	0
FSKT_PINSEL	FSKT_EN_SGN	FSKT_MOD_SGN	FSKT_MOD_EN			FSKT_DACMODE	
R/W	R/W	R/W	R/W			R/W	

Address: 0xF175

Type: R/W

Reset: 0x8

Description: FSK transmitter control

[7] **FSKT_PINSEL**: 0: reserved
1: use UART routed from GPIOs (unsigned)

[6] **FSKT_EN_SGN**: sign of FSKTX_EN
0: modulator is on when FSKTX_EN = 1, off when FSKTX_EN = 0
1: modulator is off when FSKTX_EN = 1, on when FSKTX_EN = 0 (unsigned)

[5] **FSKT_MOD_SGN**: sign of the modulator output frequency
0: FSKTX_OUT = Fc-df when FSKTX_IN = 0, FSKTX_OUT = Fc+df when FSKTX_IN = 1
1: FSKTX_OUT = Fc+df when FSKTX_IN = 0, FSKTX_OUT = Fc-df when FSKTX_IN = 1
(unsigned)

[4:2] **FSKT_MOD_EN**: modulator control bus
000: modulator off
001: modulator on
010: modulator enabled by FSKTX_EN input
011: FSK carrier (no deviation)
100: modulator output is Fc-df
101: modulator output is Fc+df (unsigned)

[1:0] **FSKT_DACMODE**: control of the FSK modulator output
00: second order sigma-delta converter
01: first order sigma-delta converter
10: no sigma-delta conversion (unsigned)

FSKRFCx FSK receiver carrier frequency

	7	6	5	4	3	2	1	0
FSKRFC2	RESERVED	FSKR_DETSGN	FSKR_OUTSGN	FSKR_KAGC			FSKR_CAR[17:16]	
	R	R/W	R/W	R/W			R/W	

	7	6	5	4	3	2	1	0
FSKRFC1	FSKR_CAR[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
FSKRFC0	FSKR_CAR[7:0]							
	R/W							

Address: 0xF178 - x * 0x1 (x=0 to 2)

Type: R/W

Reset: 0x10, 0x45, 0xC9

Description: FSK receiver carrier frequency

FSKRFC2: [6] **FSKR_DETSGN**: sign of demod detect output (FSKRX_DETECT)
0: FSKRX_DETECT = 1 when a frequency deviation is detected, else 0
0: FSKRX_DETECT = 0 when a frequency deviation is detected, else 1 (unsigned)

FSKRFC2: [5] **FSKR_OUTSGN**: sign of demod output (FSKRX_OUT) (unsigned)

FSKRFC2: [4:2] **FSKR_KAGC**: FSK demodulator AGC time constant (unsigned)

FSKRFC2: [1:0]
FSKRFC1: [7:0]
FSKRFC0: [7:0]
FSKR_CAR: FSK demod carrier frequency
fskr_carrier = 2^20 * Fc / FMCLK, Fc = carrier freq., FMCLK = master clock freq. (unsigned)

FSKRKx FSK receiver Kx

	7	6	5	4	3	2	1	0
FSKRK1	FSKR_K1_EXP			FSKR_K1_MANT				
FSKRK2	FSKR_K2_EXP			FSKR_K2_MANT				
	R/W			R/W				

Address: 0xF179 + (x-1) * 0x1 (x=1 to 2)

Type: R/W

Reset: 0x38, 0x71

Description: FSK receiver Kx

FSKRK1: [7:5] **FSKR_K1_EXP**: K1 coefficient exponent (unsigned)

FSKRK1: [4:0] **FSKR_K1_MANT**: K1 coefficient mantissa K1 = fskr_k1_mant * 2^(8 + fskr_k1_exp), fskr_k1_exp = 0 to 5 (unsigned)

FSKRK2: [7:5] **FSKR_K2_EXP**: K2 coefficient exponent (unsigned)

FSKRK2: [4:0] **FSKR_K2_MANT**: K2 coefficient mantissa K2 = fskr_k2_mant * 2^fskr_k2_exp, fskr_k2_exp = 0 to 7 (unsigned)

FSKRAGCR FSK receiver AGC reference

7	6	5	4	3	2	1	0
FSKR_OUTCTL		FSKR_AGC_REF					
R/W		R/W					

Address: 0xF17B

Type: R/W

Reset: 0x28

Description: FSK receiver AGC reference

[7:6] **FSKR_OUTCTL**: demod output control bus
00: normal mode
01: FSKRX_OUT stuck at last value
10: FSKRX_OUT stuck at 0
11: FSKRX_OUT stuck at 1 (unsigned)

[5:0] **FSKR_AGC_REF**: demod AGC reference (unsigned)

FSKRAGC FSK receiver AGC status

7	6	5	4	3	2	1	0
FSKR_AGC_ACCU							
R							

Address: 0xF17C

Type: R

Reset: Undefined

Description: FSK receiver AGC status

[7:0] **FSKR_AGC_ACCU**: demod AGC value (unsigned)

FSKRALPHA FSK receiver alpha coefficient

7	6	5	4	3	2	1	0
RESERVED			FSKR_ALPHA_EXP			FSKR_ALPHA_M	
R			R/W			R/W	

Address: 0xF17D

Type: R/W

Reset: 0x13

Description: FSK receiver alpha coefficient

[4:2] **FSKR_ALPHA_EXP**: alpha coefficient exponent (unsigned)

[1:0] **FSKR_ALPHA_M**: alpha coefficient mantissa
alpha = 256 * (4 + fskr_alpha_m) * 2^fskr_alpha_exp (unsigned)

FSKRPLTHx FSK receiver beta coefficient and PLL threshold

	7	6	5	4	3	2	1	0
FSKRPLTH1	FSKR_BETA				FSKR_PLL_TRESH[11:8]			
	R/W				R/W			

	7	6	5	4	3	2	1	0
FSKRPLTH0	FSKR_PLL_TRESH[7:0]							
	R/W							

Address: 0xF17F - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x90, 0xBE

Description: FSK receiver beta coefficient and PLL threshold

FSKRPLTH1: [7:4] **FSKR_BETA**: beta coefficient = 2^fskr_beta (unsigned)

FSKRPLTH1: [3:0]
FSKRPLTH0: [7:0] **FSKR_PLL_TRESH**: PLL threshold frequency (unsigned)

FSKRDFx FSK receiver frequency deviation

	7	6	5	4	3	2	1	0
FSKRDF1	FSKR_OUT	RESERVED			FSKR_DELTAF[12:8]			
	R	R			R			

	7	6	5	4	3	2	1	0
FSKRDF0	FSKR_DELTAF[7:0]							
	R							

Address: 0xF181 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: FSK receiver frequency deviation

FSKRDF1: [7] **FSKR_OUT**: value of FSKRX_OUT (unsigned)

FSKRDF1: [4:0]
FSKRDF0: [7:0] **FSKR_DELTAF**: demod dynamic frequency deviation value (unsigned)

FSKRSTEPP FSK receiver positive step

7	6	5	4	3	2	1	0
FSKR_STEP_PLUS							
R/W							

Address: 0xF182

Type: R/W

Reset: 0x58

Description: FSK receiver positive step

[7:0] **FSKR_STEP_PLUS**: signal detection positive step
step_plus = fskr_step_plus[4:0] * 2^fskr_step_plus[7:5] (unsigned)

FSKRSTEPM FSK receiver negative step

7	6	5	4	3	2	1	0
FSKR_STEP_MINUS							
R/W							

Address: 0xF183

Type: R/W

Reset: 0x6F

Description: FSK receiver negative step

[7:0] **FSKR_STEP_MINUS**: signal detection negative step
step_minus = fskr_step_minus[4:0] * 2^fskr_step_minus[7:5] (unsigned)

FSKRDETx FSK receiver detection status

	7	6	5	4	3	2	1	0
FSKRDET1	FSKR_DETECT	RESERVED			FSKR_CARDET_ACCU[11:8]			
	R	R			R			

	7	6	5	4	3	2	1	0
FSKRDET0	FSKR_CARDET_ACCU[7:0]							
	R							

Address: 0xF185 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: FSK receiver detection status

FSKRDET1: [7] **FSKR_DETECT**: value of FSKRX_DETECT (unsigned)

FSKRDET1: [3:0]
FSKRDET0: [7:0] **FSKR_CARDET_ACCU**: demod average absolute frequency deviation (unsigned)

FSKRDTHx FSK receiver carrier detection and loss threshold

	7	6	5	4	3	2	1	0
FSKRDTH1	FSKR_CARLOSS_THRESH[11:8]				FSKR_CARDET_THRESH[11:8]			
	R/W				R/W			

	7	6	5	4	3	2	1	0
FSKRDTH0	FSKR_CARDET_THRESH[7:0]							
	R/W							

Address: 0xF187 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x0, 0xE9

Description: FSK receiver carrier detection and loss threshold

FSKRDTH1: [7:4] **FSKR_CARLOSS_THRESH**: signal lost frequency threshold (unsigned)

FSKRDTH1: [3:0]
FSKRDTH0: [7:0] **FSKR_CARDET_THRESH**: signal detected frequency threshold (unsigned)

FSKRLOSS FSK receiver carrier loss threshold

7	6	5	4	3	2	1	0
FSKR_CARLOSS_THRESH[7:0]							
R/W							

Address: 0xF188

Type: R/W

Reset: 0x4D

Description: FSK receiver carrier loss threshold

[7:0] **FSKR_CARLOSS_THRESH**: signal lost frequency threshold (unsigned)

17.4 DMD register descriptions

IQCONST Constellation editor configuration

7	6	5	4	3	2	1	0
RESERVED	CONSTEL_SELECT		IQSYMB_SEL				
R	R/W		R/W				

Address: 0xF400

Type: R/W

Reset: 0x0

Description: Constellation editor configuration

[6:5] **CONSTEL_SELECT**: observation mode for ISYMB & QSYMB.
00: normal mode, observe the selection iqsymb_sel[4:0]
01: inverse mode, observe the selection TCTL1/tst_iqsymbsel[4:0]
10: superpose mode: observe iqsymb_sel[4:0] and TCTL1/tst_iqsymbsel[4:0]
11: staggered superpose mode: observe the selection iqsymb_sel[4:0] and the selection TCTL1/tst_iqsymbsel[4:0] divided by 2 (this will help distinguish the 2 figures). (unsigned)

[4:0] **IQSYMB_SEL**: selection of measuring point
Measuring Points in data flow:
0x00: demodulator IQ output
0x01: equalizer output
0x02: derotator 2 output (signal divided by 2)
0x03: symbols+inter symbols output (superimposed)
0x04: symbols output
0x05: inter symbols output
0x06: derotator 1 output (samples, divided by 2)
0x07: IQ mismatches output (amplitude, angle, DC)
0x08: demodulation input

NOSCFG Configuration of noise indicators

7	6	5	4	3	2	1	0
RESERVED		DUMMYPL_NOSDATA	NOSPLH_BETA		NOSDATA_BETA		
R		R/W	R/W		R/W		

Address: 0xF401

Type: R/W

Reset: 0x14

Description: Forcing (internally) nosplh_beta = 11 and nosdata_beta = 111 while the demodulator is unlocked will set the registers to globally correct values (correct order of magnitude) as quickly as possible.

[5] **DUMMYPL_NOSDATA**: Method of accounting for Dummy PLFrames in DVB-S2:
0: consider them when calculating xNOSPLHx
1: consider them when calculating xNOSDATAx (unsigned)

[4:3] **NOSPLH_BETA**: error collection speed for structure symbols (DVB-S2 only):
11: fastest, 2^0
10: 2^-8
01: 2^-10, standard value
00: slowest (unsigned)

[2:0] **NOSDATA_BETA**: error collection speed for usable load (DVB-S2 or DVB-S1/Legacy DTV):
111: fastest, 2^0
110: 2^-8
101: 2^-10
100: 2^-12, standard value
011: 2^-14
010: 2^-16
001: 2^-18
000: slowest, 2^-20 (unsigned)

ISYMB — Constellation editor I track

7	6	5	4	3	2	1	0
I_SYMBOL							
R							

Address: 0xF402

Type: R

Reset: Undefined

Description: Constellation editor I track

[7:0] **I_SYMBOL**: (signed)

QSYMB — Constellation editor Q track

7	6	5	4	3	2	1	0
Q_SYMBOL							
R							

Address: 0xF403

Type: R

Reset: Undefined

Description: Constellation editor Q track

[7:0] **Q_SYMBOL**: time consistent with ISYMB.i_symbol. (signed)

AGC1CFG IQ mismatch control

7	6	5	4	3	2	1	0
DC_FROZEN	DC_CORRECT	AMM_FROZEN	AMM_CORRECT	QUAD_FROZEN	QUAD_CORRECT	RESERVED	
R/W	R/W	R/W	R/W	R/W	R/W	R	

Address: 0xF404

Type: R/W

Reset: 0x54

Description: IQ mismatch control

[7] **DC_FROZEN**: compensation freeze (unsigned)

[6] **DC_CORRECT**: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

[5] **AMM_FROZEN**: compensation freeze (unsigned)

[4] **AMM_CORRECT**: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

[3] **QUAD_FROZEN**: compensation freeze (unsigned)

[2] **QUAD_CORRECT**: compensation authorization
01: DC compensation active
11: DC compensation active but fixed
10: more compensation with conservation of the last measure
00: more compensation, the measure is becoming abnormal (unsigned)

AGC1CN AGC1 control

7	6	5	4	3	2	1	0
AGC1_LOCKED	RESERVED		AGC1_MINPOWER	AGCOUT_FAST	AGCIQ_BETA		
R	R		R/W	R/W	R/W		

Address: 0xF406

Type: R/W

Reset: 0x19

Description: AGC1 control

[7] **AGC1_LOCKED**: AGC1 stability indicator
1: AGC1 has stabilized. (read put to 0 on a read,unsigned)

[4] **AGC1_MINPOWER**: limit selection for POWERI+POWERQ (see above). (unsigned)

[3] **AGCOUT_FAST**: PWM signal speed output from AGC1:
0: 1/64 Mclk
1: 1/4 Mclk
Operation latitude is required to compensate for a loss on the RC network connected to the pin of AGC1. (unsigned)

[2:0] **AGCIQ_BETA**: AGC1 loop speed:
As soon as the demodulator is in the process of locking (demod_tracked=1), subtract 1.5 from agciq_beta internally (division of this speed by 8).
000: stop
001: slowest
..
111: fastest (unsigned)

AGC1REF — AGC1 reference

7	6	5	4	3	2	1	0
AGCIQ_REF							
R/W							

Address: 0xF407

Type: R/W

Reset: 0x58

Description: AGC1 reference

[7:0] **AGCIQ_REF**: AGC1 reference module.
Unit = ADCI or Q / sqrt(2)
Consign AGC1 = I^2 + Q^2 - 2 * (agciq_ref^2) (unsigned)

IDCCOMP — DC compensation on I

7	6	5	4	3	2	1	0
IAVERAGE_ADJ							
R							

Address: 0xF408

Type: R

Reset: Undefined

Description: DC compensation on I

[7:0] **IAVERAGE_ADJ**: Unit = in 1/2 of ADCI
0x80: error of +0x40 on ADCI
0x00: no correction necessary
0x7F: error of -0x3F on ADCI (signed)

QDCCOMP DC compensation on Q

7	6	5	4	3	2	1	0
QAVERAGE_ADJ							
R							

Address: 0xF409

Type: R

Reset: Undefined

Description: DC compensation on Q

[7:0] **QAVERAGE_ADJ**: Unit = in 1/2 of ADCQ
0x80: error of +0x40 on ADCQ
0x00: no correction necessary
0x7F: error of -0x3F on ADCQ (signed)

POWERI Power measured on I

7	6	5	4	3	2	1	0
POWER_I							
R							

Address: 0xF40A

Type: R

Reset: Undefined

Description: Power measured on I

[7:0] **POWER_I**: Unit: in 1/4 of ADCI. (unsigned)

POWERQ Power measured on Q

7	6	5	4	3	2	1	0
POWER_Q							
R							

Address: 0xF40B

Type: R

Reset: Undefined

Description: Power measured on Q

[7:0] **POWER_Q**: Unit: in 1/4 of ADCQ. (unsigned)

AGC1AMM Amplitude compensation of Q with respect to I

7	6	5	4	3	2	1	0
AMM_VALUE							
R/W							

Address: 0xF40C

Type: R/W

Reset: Undefined

Description: Amplitude compensation of Q with respect to I

[7:0] **AMM_VALUE**: < 0x80: Q attenuated
= 0x80: no correction necessary
> 0x80: Q amplified
Compensation = amm_value / 0x80 (unsigned)

AGC1QUAD Quadrature compensation of Q with respect to I

7	6	5	4	3	2	1	0
QUAD_VALUE							
R/W							

Address: 0xF40D

Type: R/W

Reset: Undefined

Description: Quadrature compensation of Q with respect to I

[7:0] **QUAD_VALUE**: < 0x00: a little of I taken from Q
0x00: no correction necessary
> 0x00: a little of I added to Q (signed)

AGCIQINx AGC1 accumulator

	7	6	5	4	3	2	1	0
AGCIQIN1	AGCIQ_VALUE[15:8]							
AGCIQIN0	AGCIQ_VALUE[7:0]							
	R/W							

Address: 0xF40F - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: AGC1 accumulator

[7:0] **AGCIQ_VALUE**: 0x0000: maximum amplification (signal too weak)
0x8000: middle value
0xFFFF: minimum amplification (signal too strong) (unsigned)

DEMOD General register for demodulator main functions

7	6	5	4	3	2	1	0
MANUALS2_ROLLOFF	RESERVED	SPECINV_CONTROL		RESERVED	MANUALSX_ROLLOFF	ROLLOFF_CONTROL	
R/W	R	R/W		R	R/W	R/W	

Address: 0xF410

Type: R/W

Reset: 0x0

Description: General register for demodulator main functions

[7] **MANUALS2_ROLLOFF**: Roll-Off filter control mode (DVB-S2 only):
0: automatic mode. Start with value in rolloff_control (described below) then set value read in MATYPE/RO[1:0].
1: manual mode, use value set in rolloff_control (full stop). (unsigned)

[5:4] **SPECINV_CONTROL**: local spectral inversion control
00: automatic
01: automatic, with reset to 0 when a new search is launched
10: manual set to 0
11: manual set to 1 (unsigned)

[2] **MANUALSX_ROLLOFF**: Roll-Off control of Nyquist filters in DVB-S1/Legacy DTV (for DVB-S2, see manuals2_rolloff above):
0:automatic mode,
DVB-S1: initialization with rolloff_control (above). Then after lock force a value of 35%.
Legacy DTV:initialization with rolloff_control (above). Then after lock force a value of 20%.
1: manual mode, use rolloff_control whatever the situation. (unsigned)

[1:0] **ROLLOFF_CONTROL**: roll off at init or in manual mode
00:35% 01:25% 10:20% (11:15%)
(The same table as the DVB-S2 specification)
See TMGOBS/rolloff_status to observe the chosen roll-off. (unsigned)

DMDMODCOD Override register for MODCOD&TYPE

7	6	5	4	3	2	1	0
MANUAL_MODCOD	DEMOD_MODCOD					DEMOD_TYPE	
R/W	R/W					R/W	

Address: 0xF411

Type: R/W

Reset: Undefined

Description: Override register for MODCOD&TYPE

[7] **MANUAL_MODCOD**: manual override of MODCOD & TYPE (DVB-S2 only)
1: MODCOD & TYPE are set by the fields demod_modcod and demod_type as below.
0: they are inactive. (unsigned)

[6:2] **DEMOD_MODCOD**: DVB-S2:
0: DummyPL 8: QPSK 4/5 16: 8PSK 8/9 24: 32APSK 3/4
1: QPSK 1/4 9: QPSK 5/6 17: 8PSK 9/10 25: 32APSK 4/5
2: QPSK 1/3 10: QPSK 8/9 18: 16APSK 2/3 26: 32APSK 5/6
3: QPSK 2/5 11: QPSK 9/10 19: 16APSK 3/4 27: 32APSK 8/9
4: QPSK 1/2 12: 8PSK 3/5 20: 16APSK 4/5 28: 32APSK 9/10
5: QPSK 3/5 13: 8PSK 2/3 21: 16APSK 5/6 29: --
6: QPSK 2/3 14: 8PSK 3/4 22: 16APSK 8/9 30: --
7: QPSK 3/4 15: 8PSK 5/6 23: 16APSK 9/10 31: RQ
DVB-S1/Legacy DTV convention:
4: QPSK 1/2
5: QPSK 3/5
6: QPSK 2/3
7: QPSK 3/4
9: QPSK 5/6
10: QPSK 6/7 (DVB-S2 QPSK 8/9)
11: QPSK 7/8 (DVB-S2 QPSK 9/10)
The others have no meaning (unsigned)

[1:0] **DEMOD_TYPE**: DVB-S2 only
bit 1: Short frame mode
bit 0: Pilots present (unsigned)

DSTATUS — Demodulator status 1

7	6	5	4	3	2	1	0
CAR_LOCK	TMGLOCK_QUALITY		RESERVED	LOCK_DEFINITIF	RESERVED		OVADC_DETECT
R	R		R	R	R		R

Address: 0xF412

Type: R

Reset: Undefined

Description: General status

[7] **CAR_LOCK**: carrier lock (unsigned)

[6:5] **TMGLOCK_QUALITY**: timing lock quality
00: timing not locked
01: timing in process of being locked
1x: timing locked (unsigned)

[3] **LOCK_DEFINITIF**: demodulator locked
The official locking indicator. (unsigned)

[0] **OVADC_DETECT**: Persistent ADC overflow detected; on more than 1/16th of all samples from the input ADCs (i.e. >6%) . (unsigned)

DSTATUS2 Demodulator status 2

7	6	5	4	3	2	1	0
DEMOD_DELOCK	RESERVED			AGC1_NOSIGNALACK	AGC2_OVERFLOW	CFR_OVERFLOW	GAMMA_OVERUNDER
R/W	R			R	R	R	R

Address: 0xF413

Type: R

Reset: Undefined

Description: Failure observation.
The [6:0] bits are automatically reset at the start of a new AEP.

[7] **DEMOD_DELOCK**: Detection of a zero passage in DSTATUS/LOCK_DEFINITIF. Useful for debug. Reset to zero by an I2C write. (read put to 0 on a write,unsigned)

[3] **AGC1_NOSIGNALACK**: diagnostic “Tuner no signal“. No signal at the ADC entries. (read put to 0 on a read,unsigned)

[2] **AGC2_OVERFLOW**: AGC2 saturation at maximum amplification (no signal after Nyquist filtering). (read put to 0 on a read,unsigned)

[1] **CFR_OVERFLOW**: CFR has reached the limit of CFRUP, CFRLOW or +-tuner max range. (read put to 0 on a read,unsigned)

[0] **GAMMA_OVERUNDER**: SFR has reached the limit of SFRmin (symbol rate min range) or SFRmax (tuner max range). (read put to 0 on a read,unsigned)

DMDCFGMD Demodulator configuration 1

7	6	5	4	3	2	1	0
DVBS2_ENABLE	DVBS1_ENABLE	RESERVED	SCAN_ENABLE	CFR_AUTOSCAN	RESERVED	TUN_RNG	
R	R	R	R	R	R	R	

Address: 0xF414

Type: R

Reset: 0xC9

Description: Main modes. Value recommended: 0xF8+tuner_range[1:0]
Certain bits of this register are independently set to 1 or 0 (internally) depending upon the AEP selected and upon the step currently in progress in the state machine.

[7] **DVBS2_ENABLE**: 1: authorize a DVB-S2 search. (unsigned)

[6] **DVBS1_ENABLE**: 1: authorize a DVB-S1/Legacy DTV search. (unsigned)

[4] **SCAN_ENABLE**: 1: authorize symbol rate scanning. (unsigned)

[3] **CFR_AUTOSCAN**: 1: authorize CFRINIT as a variable. (unsigned)

[1:0] **TUN_RNG**: tuner bandwidth range:
tuner_range: 0 1 2 3
SFRxx max: 1/2 1/2 1/4 1/8 MCLK
CFRxx max: +-1/2 +-1/4 +-1/8 +-1/16 MCLK
@135 MHz 67.5 67.5 33.7 16.9 MSymb/s
+-67.5 +-33.7 +-16.9 +-8.4 MHz
Usual range: 1 (unsigned)

DMDCFG2 Demodulator configuration 2

7	6	5	4	3	2	1	0
RESERVED	S1S2_SEQUENTIAL	RESERVED	INFINITE_RELOCK	RESERVED			
R	R/W	R	R/W	R			

Address: 0xF415

Type: R/W

Reset: 0x3B

Description: State machine internal behavior. Value recommended in general: 0xFB
Certain bits of this register are independently set to 1 or 0 (internally) in “demod relock“ and “tuner centering“ modes.

[6] **S1S2_SEQUENTIAL**: 1: sequential search DVB-S2 and DVB-S1/Legacy DTV (if DMDCFGMD.dvbs2_enable AND DMDMDCFG.dvbs1_enable are at 1).
0: parallel search.
For broadcast QPSK and 8PSK,parallel search (Pn_S1S2_SEQUENTIAL = 0) is recommended
For 16APSK and 32APSK (advanced version only) sequential search (Pn_S1S2_SEQUENTIAL = 1) is recommended (unsigned)

[4] **INFINITE_RELOCK**: timeout mode during relock:
1: try to relock infinitely.
0: time out after 64 trials. (unsigned)

DMDISTATE — AEP launch register

7	6	5	4	3	2	1	0
RESERVED			I2C_DEMOD_MODE				
R			R/W				

Address: 0xF416

Type: R/W

Reset: 0x1C

Description: AEP launch register

[4:0] **I2C_DEMOD_MODE**: See Chapter 5.13 Algorithmic Entry Points. (unsigned)

DMDT0M — Coarse carrier & symbol time constant

7	6	5	4	3	2	1	0
DMDT0_MIN							
R/W							

Address: 0xF417

Type: R/W

Reset: 0x40

Description: Coarse carrier & symbol time constant

[7:0] **DMDT0_MIN**: minimum wait time (in samples) in coarse carrier search.
0xFF: no step 2
0x01..0xFE: dmdt0_min*2^14 samples exactly.
0x00: infinite step 2 (debug mode to observe coarse step).
timebase at 135MHz : 121 microseconds/unit (0x10=1.9 millisecond). (unsigned)

DMDSTATE — Step currently in progress in the demodulator general state machine

7	6	5	4	3	2	1	0
RESERVED	HEADER_MODE		RESERVED				
R	R		R				

Address: 0xF41B

Type: R

Reset: Undefined

Description: Attention: If bit 7 is set to ‘0‘ then any I2C write to this register will cause the AEP to be re-launched.

[6:5] **HEADER_MODE**: locking status
00: searching
01: 1st DVB-S2 PLHeader detected, searching for residual offset symbol.
10: DVB-S2 mode
11: DVB-S1/Legacy DTV mode (unsigned)

DMDFLYW Demodulator status

7	6	5	4	3	2	1	0
I2C_IRQVAL				FLYWHEEL_CPT			
R				R			

Address: 0xF41C

Type: R

Reset: 0x0

Description: Demodulator status

[7:4] **I2C_IRQVAL**: IRQ (Interrupt ReQuest) sent by the demodulator. Also serves as a final diagnostic for the demodulator. This info is supplied at the same time as the impulse demod_irq to the circuit interrupt manager. The host processor must therefore read this field to get details on the interruption received:
0x0: --
0x1: AGC1/AGC2/CFR1/SFR overflow -> no signal
0x2: limits of CFRUP<->CFRLOW and/or SFRUP<->SFRLOW exceeded
If the demodulator is locked, a simple indication
Otherwise, a timeout (followed by demod_fail)
0x3: timeout steps 3,6 -> no signal
0x4: fail after 8 (or 64 in force relock mode) looped
0x5: timeout step 9 -> undecodable
0x6: lock DVB-S2
0x7: unlock DVB-S2
0x8: lock DVB-S1/Legacy DTV
0x9: unlock DVB-S1/Legacy DTV
0xA: --
0xB: --
0xC: FIFO results full
Final demand to empty
0xD: BandWidth FullScan done
Scan finished (end of AEP 0x11 or 0x1B)
0xE: FIFO results have passed the mark of 8 results
Urgent demand to empty results register
0xF: --
A write to this register erases the value in i2c_irqval (unsigned)

[3:0] **FLYWHEEL_CPT**: PLHeader correct counter detected. When this counter becomes 0xF the demodulator is defined as locked (DVB-S2 only). A little before (from 3), the internal signal demod_tracked becomes 1 (visible on the SD Data, see chapter “SDD - Serial Data Description“). (unsigned)

DSTATUS3 Demodulator status 3

7	6	5	4	3	2	1	0
RESERVED	DEMOD_CFGMODE		RESERVED				
R	R		R				

Address: 0xF41D

Type: R

Reset: Undefined

Description: Status of certain operation steps

[6:5] **DEMOD_CFGMODE**: Demodulator functional mode:
00: demodulation
01: Scanning pass band (no tuner control)
10: Scanning tuner range
11: Calibration (of tuner) (unsigned)

DMDCFG3 Demodulator configuration 3

7	6	5	4	3	2	1	0
RESERVED				NOSTOP_FIFOFULL	RESERVED		
R				R/W	R		

Address: 0xF41E

Type: R/W

Reset: 0x8

Description: Demodulator configuration 3

[3] **NOSTOP_FIFOFULL**: behavior when FIFO results full
0: wait for emptying before continuing. Can lead to hang situations (that can be baffling) if no emptying procedure is in action for that FIFO.
1: do not hang the system (the data may be lost). (unsigned)

DMDCFG4 Demodulator configuration 4

7	6	5	4	3	2	1	0
RESERVED				TUNER_NRELAUNCH	RESERVED		
R				R/W	R		

Address: 0xF41F

Type: R/W

Reset: 0x0

Description: Demodulator configuration 4

[3] **TUNER_NRELAUNCH**: A method of reprogramming the tuner in the case of failure due to tuner I2C error or tuner lock criteria.
1: soft increment tuner. Hypothesis: the problem may have been related to a 'frequency hole' thus it is better to move along a bit.
0: AEP Stop. Stop the state machine for manual intervention. (unsigned)

CORRELMANT Differential correlator limit mantissa

7	6	5	4	3	2	1	0
CORREL_MANT							
R/W							

Address: 0xF420

Type: R/W

Reset: 0x78

Description: Differential correlator limit mantissa

[7:0] **CORREL_MANT**: see CORRELEXP.correl_exp (unsigned)

CORRELABS Absolute correlator limit mantissa

7	6	5	4	3	2	1	0
CORREL_ABS							
R/W							

Address: 0xF421

Type: R/W

Reset: 0x8C

Description: Absolute correlator limit mantissa

[7:0] **CORREL_ABS**: see CORRELEXP.correl_absexp (unsigned)

CORRELEXP Relative and absolute correlation limit exponents

7	6	5	4	3	2	1	0
CORREL_ABSEXP				CORREL_EXP			
R/W				R/W			

Address: 0xF422

Type: R/W

Reset: 0xAA

Description: Relative and absolute correlation limit exponents

[7:4] **CORREL_ABSEXP**: calculation mode of absolute limit (“Fast Hadamar“)
Values referenced on simple AGC2REF.agc2_ref:
0000: limit = correl_abs*agc2_ref/32
0001: limit = correl_abs*agc2_ref/16
0010: limit = correl_abs*agc2_ref/8
0011: limit = correl_abs*agc2_ref/4
Manual values:
0100: limit = correl_abs*8
0101: limit = correl_abs*16
0110: limit = correl_abs*32
0111: limit = correl_abs*64
Values referenced on adaptive agc2_ref (3/4=0.75):
1000: init limit = correl_abs*agc2_ref/32
1001: init limit = correl_abs*agc2_ref/16
1010: init limit = correl_abs*agc2_ref/8 <-Recommended
1011: init limit = correl_abs*agc2_ref/4
Special case reference values:
0100: --
0101: limit = 640
0110: --
0111: limit = 0xFFFF
correl_abs: CORRELABS register field. (unsigned)

[3:0] **CORREL_EXP**: calculation mode of relative limit (“Real Time Correlator“)
Values referenced on simple AGC2REF.agc2_ref:
0000: limit = (correl_mant*agc2_ref)^2/4
0001: limit = (correl_mant*agc2_ref)^2/2
0010: limit = (correl_mant*agc2_ref)^2
0011: limit = (correl_mant*agc2_ref)^2*2
Manual values:
0100: limit = correl_mant*32
0101: limit = correl_mant*64
0110: limit = correl_mant*128
0111: limit = correl_mant*256
Values referenced on adaptive agc2_ref (3/4):
1000: init limit = (correl_mant*agc2_ref)^2/4
1001: init limit = (correl_mant*agc2_ref)^2/2
1010: init limit = (correl_mant*agc2_ref)^2 <-Recommended
1011: init limit = (correl_mant*agc2_ref)^2*2
Values referenced on adaptive agc2_ref (1/2):
1100: init limit = (correl_mant*agc2_ref)^2/4
1101: init limit = (correl_mant*agc2_ref)^2/2
1110: init limit = (correl_mant*agc2_ref)^2
1111: init limit = (correl_mant*agc2_ref)^2*2
agc2_ref: see AGC2REF register
correl_mant: CORRELMANT register field. (unsigned)

PLHMODCOD — Current MODCOD&TYPE, only DVB-S2

7	6	5	4	3	2	1	0
SPECINV_DEMOD	PLH_MODCOD					PLH_TYPE	
R	R					R	

Address: 0xF424

Type: R

Reset: Undefined

Description: Current MODCOD&TYPE, only DVB-S2

[7] **SPECINV_DEMOD**: local spectral inversion detected by the demodulator in DVB-S2 mode. (unsigned)

[6:2] **PLH_MODCOD**: Current MODCOD (value not stable). Use register DMDMODCOD. (unsigned)

[1:0] **PLH_TYPE**: current TYPE (value not stable). Use register DMDMODCOD. (unsigned)

DMDREG — Various special cases

7	6	5	4	3	2	1	0
RESERVED						HIER_SHORTFRAME	RESERVED
R						R/W	R

Address: 0xF425

Type: R/W

Reset: 0x1

Description: Various special cases

[1] **HIER_SHORTFRAME**: 1: eliminate 1 frame in 2 if noise is too high to be able to decode the data.
This can prevent the IC from overheating in rain fade conditions. (unsigned)

AGC2O — AGC2 configuration

7	6	5	4	3	2	1	0
RESERVED						AGC2_COEF	
R						R/W	

Address: 0xF42C

Type: R/W

Reset: 0x5B

Description: AGC2 configuration

[2:0] **AGC2_COEF**: 000: open loop, AGC2I1/0 manual
001: slowest
...
111: fastest (unsigned)

AGC2REF — Demodulator general reference

7	6	5	4	3	2	1	0
AGC2_REF							
R/W							

Address: 0xF42D

Type: R/W

Reset: 0x38

Description: Demodulator general reference

[7:0] **AGC2_REF**: reference module for the whole demodulator (applies much further than AGC2). Same units as the IQ coming from the ADC. (unsigned)

AGC1ADJ — AGC1 loop set point

7	6	5	4	3	2	1	0
RESERVED	AGC1_ADJUSTED						
R	R/W						

Address: 0xF42E

Type: R/W

Reset: 0x58

Description: AGC1 loop set point

[6:0] **AGC1_ADJUSTED**: Set point value applied to AGC1 loop. Normally constant. However, if this value moves then the machine is receiving 16 or 32 APSK in constant envelope mode. (unsigned)

AGC2Ix — AGC2 accumulator

	7	6	5	4	3	2	1	0
AGC2I1	AGC2_INTEGRATOR[15:8]							
AGC2I0	AGC2_INTEGRATOR[7:0]							
	R/W							

Address: 0xF437 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: AGC2 accumulator

[7:0] **AGC2_INTEGRATOR**: 0x0000: minimum amplification
0xFFFF: maximum amplification (unsigned)

CARCFG Carrier 1 configuration

7	6	5	4	3	2	1	0
RESERVED					ROTAON	PH_DET_ALGO	
R					R/W	R/W	

Address: 0xF438

Type: R/W

Reset: 0x46

Description: Carrier 1 configuration

[2] **ROTAON**: 1: carrier 1 derotator in action
0: carrier 1 loop open (unsigned)

[1:0] **PH_DET_ALGO**: algorithm used to calculate the phase error on the QPSK symbols:
00: costas
01: citroen 1
10: citroen 2
11: -- (unsigned)

ACLC Alpha DVB-S1/legacy DTV

7	6	5	4	3	2	1	0
RESERVED		CAR_ALPHA_MANT		CAR_ALPHA_EXP			
R		R/W		R/W			

Address: 0xF439

Type: R/W

Reset: 0x2B

Description: This register is used primarily for DVB-S1/legacy DTV.

[5:4] **CAR_ALPHA_MANT**: (unsigned)

[3:0] **CAR_ALPHA_EXP**: 0000: feedback loop is frozen in its last accumulated state
0001: slowest
1111: fastest (unsigned)

BCLC Beta DVB-S1/legacy DTV

7	6	5	4	3	2	1	0
RESERVED		CAR_BETA_MANT		CAR_BETA_EXP			
R		R/W		R/W			

Address: 0xF43A

Type: R/W

Reset: 0x1A

Description: This register is used primarily for DVB-S1/legacy DTV.

[5:4] **CAR_BETA_MANT**: (unsigned)

[3:0] **CAR_BETA_EXP**: 0000: feedback loop is frozen in its last accumulated state
0001: slowest
1111: fastest (unsigned)

CARFREQ — Loop carrier 1 coefficients

7	6	5	4	3	2	1	0
KC_COARSE_EXP				BETA_FREQ			
R/W				R/W			

Address: 0xF43D

Type: R/W

Reset: 0x79

Description: Loop carrier 1 coefficients

[7:4] **KC_COARSE_EXP**: exponent of coarse carrier loop coefficient: multcoef_kccoarse = (4 + kc_coarse_mant) * 2^(1 + 2 * kc_coarse_exp)
0000: stop coarse carrier.
0001: slowest
1111: fastest (unsigned)

[3:0] **BETA_FREQ**: Frequency Detector, DVB-S1 only
0000: stop coarse carrier corrections
0001: minimum coefficient
1111: maximum coefficient (unsigned)

CARHDR — PLHeader delta F coefficient in DVB-S2

7	6	5	4	3	2	1	0
K_FREQ_HDR							
R/W							

Address: 0xF43E

Type: R/W

Reset: 0x20

Description: PLHeader delta F coefficient in DVB-S2

[7:0] **K_FREQ_HDR**: carrier offset coefficient detected by the PLHeader in stable conditions
0x00: no more correction
0x40: coefficient 1.00 at start up and 1/32 in steady state conditions (unsigned)

LDT — Positive edge of carrier lock detector

7	6	5	4	3	2	1	0
CARLOCK_THRES							
R/W							

Address: 0xF43F

Type: R/W

Reset: 0xD0

Description: Positive edge of carrier lock detector

[7:0] **CARLOCK_THRES**: (signed)

LDT2 Negative edge of carrier lock detector

7	6	5	4	3	2	1	0
CARLOCK_THRES2							
R/W							

Address: 0xF440

Type: R/W

Reset: 0xB8

Description: Negative edge of carrier lock detector

[7:0] **CARLOCK_THRES2**: (signed)

CFRICFG CFRINIT management configuration

7	6	5	4	3	2	1	0
RESERVED							NEG_CFRSTEP
R							R/W

Address: 0xF441

Type: R/W

Reset: 0xF8

Description:

Note: previous channel = channel captured during previous locking process.

[0] **NEG_CFRSTEP**: 1: negative increment mode for CFRINIT (also valid for RF frequency increments).
0: positive increment mode for CFRINIT (also valid for RF frequency increments). (unsigned)

CFRUPx Upper limit of carrier offset

	7	6	5	4	3	2	1	0
CFRUP1	CFR_UP[15:8]							
CFRUP0	CFR_UP[7:0]							
	R/W							

Address: 0xF443 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] **CFR_UP**: Upper limit of carrier offset.
Unit : depends on ADC clock (ckadc = Mclk = 135MHz in standard mode).
cfr_up in MHz = ckadc * cfr_up / 2^16 (signed)

CFRLOWx Lower limit of carrier offset

	7	6	5	4	3	2	1	0
CFRLOW1	CFR_LOW[15:8]							
CFRLOW0	CFR_LOW[7:0]							
	R/W							

Address: 0xF447 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: Used internally if CARCFG/cfruplow_test=1. Read-only if CARCFG/cfruplow_auto=1

[7:0] **CFR_LOW**: Lower limit of carrier offset.
Unit : depends on ADC clock (ckadc = Mclk = 135MHz in standard mode).
cfr_low in MHz = ckadc * cfr_low / 2^16 (signed)

CFRINITx Carrier offset init value

	7	6	5	4	3	2	1	0
CFRINIT1	CFR_INIT[15:8]							
CFRINIT0	CFR_INIT[7:0]							
	R/W							

Address: 0xF449 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: Carrier offset init value

[7:0] **CFR_INIT**: Carrier offset init value.
Unit : depends on ADC clock (ckadc = Mclk = 135MHz in standard mode).
cfr_init in MHz = ckadc * cfr_init / 2^16 (signed)

CFRINCx Carrier offset increment

	7	6	5	4	3	2	1	0
CFRINC1	MANUAL_CFRINC	RESERVED	CFR_INC[13:8]					
	R/W	R	R/W					

	7	6	5	4	3	2	1	0
CFRINC0	CFR_INC[7:0]							
	R/W							

Address: 0xF44B - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x0, 0x20

Description: Carrier offset increment

CFRINC1: [7] **MANUAL_CFRINC**: Method of calculating cfr_inc (the step increment used in carrier searches):
0: automatic mode, see cfrinc_mode[1:0] below.
1: manual mode. Value set in cfr_inc[13:3]. (unsigned)

CFRINC1: [5:0] **CFR_INC**: Carrier search step size.
CFRINC0: [7:0] Increment in MHz = Mclk * CFR_INC / 2^13 (unsigned)

CFR2 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[23:16]							
R/W							

Address: 0xF44C

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] **CAR_FREQ**: (signed)

CFR1 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[15:8]							
R/W							

Address: 0xF44D

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] **CAR_FREQ**: (signed)

CFR0 Current carrier offset (unit: samples)

7	6	5	4	3	2	1	0
CAR_FREQ[7:0]							
R/W							

Address: 0xF44E

Type: R/W

Reset: Undefined

Description: carrier_frequency in MHz = mclk * carrier_frequency / 2^24

[7:0] **CAR_FREQ**: (signed)

LDI Carrier lock indicator accumulator

7	6	5	4	3	2	1	0
LOCK_DET_INTEGR							
R							

Address: 0xF44F

Type: R

Reset: Undefined

Description: Especially useful in DVB-S1/legacy DTV. not in DVB-S2. The diagnostic on this digital value is provided by DSTATUS/car_lock.

[7:0] **LOCK_DET_INTEGR**: > LDT.carlock_thres: carrier locked, DSSTATSUS.car_lock=1.
< LDT2.carlock_thres2: carrier unlocked, DSTATSUS.car_lock=0.
car_lock functions by hysteresis. (signed)

TMGCFG Timing loop configuration

7	6	5	4	3	2	1	0
TMGLOCK_BETA		RESERVED	DO_TIMING_CORR	RESERVED		TMG_MINFREQ	
R/W		R	R/W	R		R/W	

Address: 0xF450

Type: R/W

Reset: 0xD3

Description: Timing loop configuration

[7:6] **TMGLOCK_BETA**: Timing Lock Indicator loop speed
00: Minimum speed
01:
10:
11: Maximum speed
Acceleration +1 if DSTATUS3/gamma_lowbaudrate=1 as long as the demodulator is not locked. (unsigned)

[4] **DO_TIMING_CORR**: DVB-S2 only
1: use the symbol rate offset calculated on the 2nd PLHeader (unsigned)

[1:0] **TMG_MINFREQ**: compensate for symbol minimum rate
tmg_minfreq 00 01 10 11
SFRxx min: 1/32 1/128 1/512 1/2048 MCLK
at 135 MHz 4.2 1.06 0.264 0.066 MSymb/s (unsigned)

RTC Timing loop DVB-S1/legacy DTV

7	6	5	4	3	2	1	0
TMGALPHA_EXP				TMGBETA_EXP			
R/W				R/W			

Address: 0xF451

Type: R/W

Reset: 0x68

Description: This register is used primarily for DVB-S1/legacy DTV.

[7:4] **TMGALPHA_EXP**: 0000: alpha stopped
0001: slowest
1111: fastest (unsigned)

[3:0] **TMGBETA_EXP**: 0000: beta stopped
0001: slowest
1111: fastest (unsigned)

RTCS2 Timing loop specific to DVB-S2

7	6	5	4	3	2	1	0
TMGALPHAS2_EXP				TMGBETAS2_EXP			
R/W				R/W			

Address: 0xF452

Type: R/W

Reset: 0x68

Description: This register is used by DVB-S2. Same description as RTC.

[7:4] **TMGALPHAS2_EXP**: (unsigned)

[3:0] **TMGBETAS2_EXP**: (unsigned)

TMGTHRISE Positive edge of timing lock detector

7	6	5	4	3	2	1	0
TMGLOCK_THRISE							
R/W							

Address: 0xF453

Type: R/W

Reset: 0x20

Description: Positive edge of timing lock detector

[7:0] **TMGLOCK_THRISE**: (unsigned)

TMGTHFALL Negative edge of timing lock detector

7	6	5	4	3	2	1	0
TMGLOCK_THFALL							
R/W							

Address: 0xF454

Type: R/W

Reset: 0x8

Description: Negative edge of timing lock detector

[7:0] **TMGLOCK_THFALL**: (unsigned)

SFRUPRATIO Ratio to calculate SFRUP

7	6	5	4	3	2	1	0
SFR_UPRATIO							
R/W							

Address: 0xF455

Type: R/W

Reset: 0x20

Description: Ratio to calculate SFRUP

[7:0] **SFR_UPRATIO**: (unsigned)

SFRLOWRATIO Ratio to calculate SFRLOW

7	6	5	4	3	2	1	0
SFR_LOWRATIO							
R/W							

Address: 0xF456

Type: R/W

Reset: 0xD0

Description: Ratio to calculate SFRLOW

[7:0] **SFR_LOWRATIO**: (unsigned)

KREFTMG Reference level for the symbol rate part of the coarse steps

7	6	5	4	3	2	1	0
KREF_TMG							
R/W							

Address: 0xF458

Type: R/W

Reset: 0x80

Description: Reference level for the symbol rate part of the coarse steps

[7:0] **KREF_TMG**: kref_tmg_absolu = (KREF_TMG + 0x80) * agc2_ref / 2^7
But when TAGC2/nocalc_kreftmg=1, where kref_tmg_absolu = kref_tmg (unsigned)

SFRSTEP — Scan and centering increment steps

7	6	5	4	3	2	1	0
SFR_SCANSTEP				SFR_CENTERSTEP			
R/W				R/W			

Address: 0xF459

Type: R/W

Reset: 0x88

Description: Scan and centering increment steps

[7:4] **SFR_SCANSTEP**: scroll speed between SFRUP and SFRLOW during the symbol rate scan.
0000: stop
0001: slowest
1111: fastest
Subtract 1 in DVB-S1/Legacy DTV if TMGCFG2.notmg_dvbs1derat = 0. (unsigned)

[3:0] **SFR_CENTERSTEP**: TMGREG2/1/0 content transfer speed towards SFR3/2/1 once locking is launched. This speed must be small enough not to disrupt the locking process.
0000: Stop
0001: slowest
1111: fastest (unsigned)

TMGCFG2 — Timing loop additional configuration

7	6	5	4	3	2	1	0
RESERVED							SFRRATIO_FINE
R							R/W

Address: 0xF45A

Type: R/W

Reset: 0x40

Description: Timing loop additional configuration

[0] **SFRRATIO_FINE**: fine mode on SFRUPRATIO and SFRLOWRATIO
1: fine mode (sensitivity multiplied by 64)
SFRUP = SFR(INIT) * (1 + SFRUPRATIO/16384)
SFRLOW = SFR(INIT) * (63/64 + SFRLOWRATIO/16384)
0: normal mode (or coarse)
SFRUP = SFR(INIT) * (1 + SFRUPRATIO/256)
SFRLOW = SFR(INIT) * (0 + SFRLOWRATIO/256) (unsigned)

KREFTMG2 Coarse symbol rate reference frequency

7	6	5	4	3	2	1	0
KREF_TMG2							
R							

Address: 0xF45B

Type: R

Reset: 0x40

Description: Coarse symbol rate reference frequency

[7:0] **KREF_TMG2**: observation register of the current value of the coarse search symbol rate reference
Useful when TMGCFG2/kreftmg2_decmode[1:0]!=00. (unsigned)

TMGCFG3 Additional configuration of the timing loop

7	6	5	4	3	2	1	0
RESERVED					AUTO_GUP	AUTO_GLOW	RESERVED
R					R/W	R/W	R

Address: 0xF45D

Type: R/W

Reset: 0x6

Description: Additional configuration of the timing loop

[2] **AUTO_GUP**: automatic calculation mode
1: automatic calculation based on SFRUPRATIO, symb_freq_up below is read-only.
0: manual mode, symb_freq_up is read/write. (unsigned)

[1] **AUTO_GLOW**: automatic calculation mode
1: automatic calculation based on SFRLOWRATIO, symb_freq_low below is read-only.
0: manual mode, symb_freq_low is read/write. (unsigned)

SFRINITx Symbol rate init value

	7	6	5	4	3	2	1	0
SFRINIT1	SFR_INIT[15:8]							
SFRINIT0	SFR_INIT[7:0]							
	R/W							

Address: 0xF45F - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x1, 0x0

Description: Symbol rate init value

[7:0] **SFR_INIT**: used at launch of certain AEPs.
Unit: depends on the ADC clock frequency (ckadc = Mclk = 135MHz in standard mode):
sfr_init in MHz = ckadc * sfr_init / 2^16 (unsigned)

SFRUPx Symbol rate upper limit

	7	6	5	4	3	2	1	0
SFRUP1	SYMB_FREQ_UP[15:8]							
SFRUP0	SYMB_FREQ_UP[7:0]							
	R/W							

Address: 0xF461 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x80(0 XF0), UNDEFINED

Description: Symbol rate upper limit

[7:0] **SYMB_FREQ_UP**: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 256)
TMGCFG2.sfrratio_fine=1 (fine mode) in automatic mode:
SFRUP = SFR * (1 + SFRUPRATIO / 16384)
Unit: ADC clock frequency ckadc.
symb_freq_up in MHz = ckadc * symb_freq_up / 2^16 (unsigned)

SFRLOWx Symbol rate lower limit

	7	6	5	4	3	2	1	0
SFRLOW1	SYMB_FREQ_LOW[15:8]							
SFRLOW0	SYMB_FREQ_LOW[7:0]							
	R/W							

Address: 0xF463 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: 0x80(0 XF0), UNDEFINED

Description: Symbol rate lower limit

[7:0] **SYMB_FREQ_LOW**: TMGCFG2.sfrratio_fine = 0 (coarse mode) in automatic mode:
SFRLOW = SFR * (0 + SFRLOWRATIO / 256)
TMGCFG2.sfrratio_fine = 1 (fine mode) in automatic mode:
SFRLOW = SFR * (63 / 64 + SFRLOWRATIO / 16384)
Unit: ADC clock frequency ckadc.
symb_freq_low in MHz = ckadc * symb_freq_low / 2^16 (unsigned)

SFRx Current symbol rate

	7	6	5	4	3	2	1	0
SFR3	SYMB_FREQ[31:24]							
SFR2	SYMB_FREQ[23:16]							
SFR1	SYMB_FREQ[15:8]							
SFR0	SYMB_FREQ[7:0]							
	R/W							

Address: 0xF467 - x * 0x1 (x=0 to 3)

Type: R/W, R/W, R/W, R

Reset: 0x1, 0x0, 0x0, 0x0

Description: Current symbol rate

[7:0] **SYMB_FREQ**: Bits 7:0 are read-only.
Unit: depends on ADC clock frequency ckadc.
symb_freq in MHz = ckadc * symb_freq / 2^32 (unsigned)

TMGREGx Timing recovery accumulator

	7	6	5	4	3	2	1	0
TMGREG2	TMGREG[23:16]							
TMGREG1	TMGREG[15:8]							
TMGREG0	TMGREG[7:0]							
	R/W							

Address: 0xF46A - x * 0x1 (x=0 to 2)

Type: R/W

Reset: 0x0

Description: Timing recovery accumulator

[7:0] **TMGREG**: Timing Recovery accumulator, Symbol Rate offset.
Unit: symbol frequency from SFRH/M/L/LL.
tmgreg in MHz = symb_freq in MHz * (tmgreg * 2^-(24+5)) (unsigned)

TMGLOCKx Timing lock indicator accumulator

	7	6	5	4	3	2	1	0
TMGLOCK1	TMGLOCK_LEVEL[15:8]							
TMGLOCK0	TMGLOCK_LEVEL[7:0]							
	R							

Address: 0xF46C - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: The diagnostic on this digital value is provided by the DSTATUS/tmglock_quality field. It uses the TMGTHRISE/tmglock_thrise and TMGTHFALL/tmglock_thfall limits.
tmglock_quality[0] simply indicates that tmglock_level > tmglock_thfall
tmglock_quality[1] functions by hysteresis on tmglock_level with tmglock_thrise and tmglock_thfall.

[7:0] **TMGLOCK_LEVEL**: (signed)

TMGOBS Observation of the timing loop

7	6	5	4	3	2	1	0
ROLLOFF_STATUS		RESERVED					
R		R					

Address: 0xF46D

Type: R

Reset: Undefined

Description: Observation of the timing loop

[7:6] **ROLLOFF_STATUS**: Roll-off in progress (list DVB-S2)
00: 35%
01: 25%
10: 20%
(11: 15%) (unsigned)

EQUALCFG DFE equalizer configuration

7	6	5	4	3	2	1	0
RESERVED	EQUAL_ON	RESERVED			MU_EQUALDFE		
R	R/W	R			R/W		

Address: 0xF46F

Type: R/W

Reset: 0x41

Description: DFE equalizer configuration

[6] **EQUAL_ON**: 1: activate the equalizer
0: stop and reset the equalizer. Disconnection of data flow and coefficient reset. (unsigned)

[2:0] **MU_EQUALDFE**: DFE Equalizer loop speed.
111: Fastest
100: median value
001: Very slow (good for tracking)
000: Coefficients frozen (but equalizer still active). (unsigned)

EQUAIx DFE Equalizer observation

	7	6	5	4	3	2	1	0
EQUAI1	EQUA_ACCI1							
EQUAI2	EQUA_ACCI2							
EQUAI3	EQUA_ACCI3							
EQUAI4	EQUA_ACCI4							
EQUAI5	EQUA_ACCI5							
EQUAI6	EQUA_ACCI6							
EQUAI7	EQUA_ACCI7							
EQUAI8	EQUA_ACCI8							
	R/W							

Address: 0xF470 + (x-1) * 0x2 (x=1 to 8)

Type: R/W

Reset: Undefined

Description: Observation of equalizer behavior:
EQUAI1+EQUAQ1: echo level between 0 and 1 symbols delay.
..
EQUAI8+EQUAQ8: echo level between 7 and 8 symbols delay.

[7:0] **EQUA_ACCIx**: (signed)

EQUAQx DFE Equalizer observation

	7	6	5	4	3	2	1	0
EQUAQ1	EQUA_ACCQ1							
EQUAQ2	EQUA_ACCQ2							
EQUAQ3	EQUA_ACCQ3							
EQUAQ4	EQUA_ACCQ4							
EQUAQ5	EQUA_ACCQ5							
EQUAQ6	EQUA_ACCQ6							
EQUAQ7	EQUA_ACCQ7							
EQUAQ8	EQUA_ACCQ8							
	R/W							

Address: 0xF471 + (x-1) * 0x2 (x=1 to 8)

Type: R/W

Reset: Undefined

Description: Observation of equalizer behavior:
EQUAI1+EQUAQ1: echo level between 0 and 1 symbols delay.
..
EQUAI8+EQUAQ8: echo level between 7 and 8 symbols delay.

[7:0] **EQUA_ACCQx**: (signed)

NNOSDATATx Linear noise normalized on the data

	7	6	5	4	3	2	1	0
NNOSDATAT1	NOSDATAT_NORMED[15:8]							
NNOSDATAT0	NOSDATAT_NORMED[7:0]							
	R/W							

Address: 0xF481 - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: Noise level (in modulus) normalized on the data.

[7:0] **NOSDATAT_NORMED**: nosdatat_normed = 2^6 * nosdatat_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdatat_normed = 0x4000 -> noise as strong as the signal
nosdatat_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSDATAx Quadratic noise normalized on the data

	7	6	5	4	3	2	1	0
NNOSDATA1	NOSDATA_NORMED[15:8]							
NNOSDATA0	NOSDATA_NORMED[7:0]							
	R/W							

Address: 0xF483 - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: Noise level (in squared modulus) normalized on the data.

[7:0] **NOSDATA_NORMED**: nosdata_normed = 2^12 * nosdata_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosdata_normed = 0x4000 -> noise as strong as the signal
nosdata_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLHTx Linear noise normalized on the structures

	7	6	5	4	3	2	1	0
NNOSPLHT1	NOSPLHT_NORMED[15:8]							
NNOSPLHT0	NOSPLHT_NORMED[7:0]							
	R/W							

Address: 0xF485 - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: DVB-S2 only.
Noise level (in modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] **NOSPLHT_NORMED**: nosplht_normed = 2^6 * nosplht_unnormed / agc2_ref
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplht_normed = 0x4000 -> noise as strong as the signal
nosplht_normed = 0x0400 -> noise 16 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSPLHx Quadratic noise normalized on the structures

	7	6	5	4	3	2	1	0
NNOSPLH1	NOSPLH_NORMED[15:8]							
NNOSPLH0	NOSPLH_NORMED[7:0]							
	R/W							

Address: 0xF487 - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: DVB-S2 only.
Noise level (in squared modulus) normalized on PLHeader, pilots (if present) and DummyPL (if present).

[7:0] **NOSPLH_NORMED**: nosplh_normed = 2^12 * nosplh_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosplh_normed = 0x4000 -> noise as strong as the signal
nosplh_normed = 0x0400 -> noise 4 times weaker than the signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSDATATx Absolute linear noise on the data

	7	6	5	4	3	2	1	0
NOSDATAT1	NOSDATAT_UNNORMED[15:8]							
NOSDATAT0	NOSDATAT_UNNORMED[7:0]							
	R/W							

Address: 0xF489 - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: Absolute (non-normalized) noise level (in modulus) on the data.
This register contains the value that is historically compatible with the previous generations of satellite decoders.

[7:0] **NOSDATAT_UNNORMED**: Decimal point between bit 7 and bit 8
nosdatat_unnormed = 0x0200 -> loss of LSB of signal due to noise
nosdatat_unnormed = 0x0400 -> loss of the two LSBs of signal
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSFRAMEx Quadratic noise normalized on the data and by frame

	7	6	5	4	3	2	1	0
NNOSFRAME1	NOSFRAME_NORMED[15:8]							
NNOSFRAME0	NOSFRAME_NORMED[7:0]							
	R/W							

Address: 0xF48B - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: Undefined

Description: Noise level (in squared modulus) normalized on the data.

[7:0] **NOSFRAME_NORMED**: nosframe_normed = 2^12 * nosframe_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosframe_normed = 0x4000 -> noise as strong as the signal
nosframe_normed = 0x0400 -> noise 4 times weaker than the signal
Multiply by 64 the precision (with saturation) if NOSCFGF1/lownoise_mesure=1:
nosframe_normed = 2^18 * nosframe_unnormed / agc2_ref^2
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSRAD1 Quadratic noise normalized radial

7	6	5	4	3	2	1	0
NOSRADIAL_NORMED[15:8]							
R/W							

Address: 0xF48C

Type: R/WH

Reset: Undefined

Description: Noise level (in squared modulus) normalized radial

[7:0] **NOSRADIAL_NORMED**: nosradial_normed = 2^12 * nosradial_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosradial_normed = 0x4000 -> noise as strong as the signal
nosradial_normed = 0x0400 -> noise 4 times weaker than the signal
NOSCFGF1/nosradial_mode indicates if we wants a base result only on the structure symbols (to be compared with NNOSPLHM/L).
NOSCFG/dummypl_nosdata indicates how to use the Data of a Dummy PLFrame.
Sensible on the filtering done by NOSCFGF1/framesel_typesel and NOSCFGF2/framesel_modcodsel only if the Data symbols are used in the computation (defined by NOSCFGF1/nosradial_mode).
In 16APSK, use only of the Data symbols from the big circle R2 (if the Data symbols are used in the computation, see NOSCFGF1/nosradial_mode).
In 32APSK, use only of the Data symbols from the big circle R3 (if the Data symbols are used in the computation, see NOSCFGF1/nosradial_mode).
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NNOSRAD0 Quadratic noise normalized radial

7	6	5	4	3	2	1	0
NOSRADIAL_NORMED[7:0]							
R/W							

Address: 0xF48D

Type: R/WH

Reset: Undefined

Description: Quadratic noise normalized radial

[7:0] **NOSRADIAL_NORMED**: nosradial_normed = 2^12 * nosradial_unnormed / agc2_ref^2
Decimal point between bit 13 and bit 14
for agc2_ref see AGC2REF register
nosradial_normed = 0x4000 -> noise as strong as the signal
nosradial_normed = 0x0400 -> noise 4 times weaker than the signal
NOSCFGF1/nosradial_mode indicates if we wants a base result only on the structure symbols (to be compared with NNOSPLHM/L).
NOSCFG/dummypl_nosdata indicates how to use the Data of a Dummy PLFrame.
Sensible on the filtering done by NOSCFGF1/framesel_typesel and NOSCFGF2/framesel_modcodsel only if the Data symbols are used in the computation (defined by NOSCFGF1/nosradial_mode).
In 16APSK, use only of the Data symbols from the big circle R2 (if the Data symbols are used in the computation, see NOSCFGF1/nosradial_mode).
In 32APSK, use only of the Data symbols from the big circle R3 (if the Data symbols are used in the computation, see NOSCFGF1/nosradial_mode).
reading MSB loads a new value into the register pair and freezes the LSB (read put to 0 on a write,unsigned)

NOSCFGF1 Configuration of the noise indicators

7	6	5	4	3	2	1	0
LOWNOISE_MESURE	RESERVED						
R/W	R						

Address: 0xF48E

Type: R/W

Reset: Undefined

Description: Configuration of the noise indicators

[7] **LOWNOISE_MESURE**: scale factor to the reading of the normalized quadratic noises (NNOSDATA1/0, NNOSPLH1/0 et NNOSFRAME1/0). Not used for non normalized oir linear measures:
0: usual format.
1: amplification by 64 (6 bits) to increase the precision when there is a small noise. The values are saturated when they overflow. (unsigned)

CAR2CFG Carrier loop 2 configuration

7	6	5	4	3	2	1	0
RESERVED					ROTA2ON	PH_DET_ALGO2	
R					R/W	R/W	

Address: 0xF490

Type: R/W

Reset: 0x6

Description: Carrier loop 2 configuration

[2] **ROTA2ON**: 1: carrier 2 derotator in action
0: carrier 2 loop open (unsigned)

[1:0] **PH_DET_ALGO2**: algorithm used to calculate the phase error on the QPSK symbols:
00: Algo 0: For CNR>7dB (Legacy compatibility)
01: Algo 1: For CNR<7dB (Legacy compatibility)
10: Algo 2: 900 native algorithm; recommended.
11: -- (unsigned)

CFR2CFR1 Carrier offset transfer control

7	6	5	4	3	2	1	0
RESERVED		EN_S2CAR2CENTER	RESERVED			CFR2TOCFR1_BETA	
R		R/W	R			R/W	

Address: 0xF491

Type: R/W

Reset: 0x25

Description: Carrier offset transfer control between registers CFR2 to CFR1.

[5] **EN_S2CAR2CENTER**: Re-centering of CFR2 by small increments to CFR1 in DVB-S2 mode when cfr2tocfr1_beta=000
1: transfer of CFR2 into CFR1 once DSTATUS/car_lock=1 by steps of 2^-16 symbols until CFR2 is within 1/1024th of a symbol. (unsigned)

[2:0] **CFR2TOCFR1_BETA**: multiplying coefficient on the carrier 2 offset controlling the speed of transfer to CFR1. Available in DVB-S2(Pilots On or Off). Automatically disconnected in DVB-S1 and Legacy DTV modes:
000: transfer stopped.
001: 1/64
010: 1/32
011: 1/16
100: 1/8
101: 1/4 <---default.
110: 1/2
111: 1/1 (unsigned)

CFR22 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[23:16]							
R/W							

Address: 0xF493

Type: R/W

Reset: Undefined

Description: Normally centered on 0.

[7:0] **CAR2_FREQ**: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

CFR21 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[15:8]							
R/W							

Address: 0xF494

Type: R/W

Reset: Undefined

Description: Current carrier offset 2 (unit: symbols)

[7:0] **CAR2_FREQ**: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

CFR20 Current carrier offset 2 (unit: symbols)

7	6	5	4	3	2	1	0
CAR2_FREQ[7:0]							
R/W							

Address: 0xF495

Type: R/W

Reset: Undefined

Description: Current carrier offset 2 (unit: symbols)

[7:0] **CAR2_FREQ**: carrier2_frequency in MHz = MasterClock * carrier2_frequency / 2^24 (signed)

ACLC2S2Q Alpha specific DVB-S2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)

7	6	5	4	3	2	1	0
ENAB_SPSKSYMB	RESERVED	CAR2S2_Q_ALPH_M		CAR2S2_Q_ALPH_E			
R/W	R	R/W		R/W			

Address: 0xF497

Type: R/W

Reset: 0x4B

Description: This register is used by DVB-S2.

[7] **ENAB_SPSKSYMB**: Stop carrier loop 2 alpha and beta updates during DVB-S2 header, pilot and dummyPL symbols.
1: The structure symbols are never used in the calculation of alpha and beta.
0: The structure symbols contribute to alpha and beta. (unsigned)

[5:4] **CAR2S2_Q_ALPH_M**: (unsigned)

[3:0] **CAR2S2_Q_ALPH_E**: (unsigned)

ACLC2S28 Alpha specific DVB-S2 data 8PSK

7	6	5 4	3 2 1 0
OLDI3Q_MODE	RESERVED	CAR2S2_8_ALPH_M	CAR2S2_8_ALPH_E
R/W	R	R/W	R/W

Address: 0xF498

Type: R/W

Reset: 0x4A

Description: This register is used by DVB-S2.

[7] **OLDI3Q_MODE**: Use the phase detector as implemented in cut 2.0 and prior versions (unsigned)

[5:4] **CAR2S2_8_ALPH_M**: (unsigned)

[3:0] **CAR2S2_8_ALPH_E**: (unsigned)

BCLC2S2Q Beta specific DVB-S2 data QPSK and structure symbols (PLHeader, pilots, DummyPL data)

7 6	5 4	3 2 1 0
RESERVED	CAR2S2_Q_BETA_M	CAR2S2_Q_BETA_E
R	R/W	R/W

Address: 0xF49C

Type: R/W

Reset: 0xC4

Description: This register is used by DVB-S2. Same description as BCLC2.

[5:4] **CAR2S2_Q_BETA_M**: (unsigned)

[3:0] **CAR2S2_Q_BETA_E**: (unsigned)

BCLC2S28 Beta specific DVB-S2 data 8PSK

7 6	5 4	3 2 1 0
RESERVED	CAR2S2_8_BETA_M	CAR2S2_8_BETA_E
R	R/W	R/W

Address: 0xF49D

Type: R/W

Reset: 0xC4

Description: This register is used by DVB-S2. Same description as BCLC2.

[5:4] **CAR2S2_8_BETA_M**: (unsigned)

[3:0] **CAR2S2_8_BETA_E**: (unsigned)

PLROOTx Gold code description

	7	6	5	4	3	2	1	0
PLROOT2	RESERVED						PLSCRAMB_ROOT[17:16]	
	R						R/W	

	7	6	5	4	3	2	1	0
PLROOT1	PLSCRAMB_ROOT[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
PLROOT0	PLSCRAMB_ROOT[7:0]							
	R/W							

Address: 0xF4AE - x * 0x1 (x=0 to 2)

Type: R/W

Reset: 0x0, 0x0, 0x1

Description: Gold code description

PLROOT2: [1:0]

PLROOT1: [7:0] **PLSCRAMB_ROOT**: DVB-S2 Gold Code or root of PRBS X. (unsigned)

PLROOT0: [7:0]

MODCODLSTx List of prohibited MODCOD

	7	6	5	4	3	2	1	0
MODCODLST7	RESERVED		DIS_8PSK_9_10		DIS_8P_8_9			
	R		R/W		R/W			

	7	6	5	4	3	2	1	0
MODCODLST8	DIS_8P_5_6				DIS_8P_3_4			
	R/W				R/W			

	7	6	5	4	3	2	1	0
MODCODLST9	DIS_8P_2_3				DIS_8P_3_5			
	R/W				R/W			

Address: 0xF4B7 + (x-7) * 0x1 (x=7 to 9)

Type: R/W

Reset: 0xC0, 0x0, 0x0

Description: List of prohibited MODCOD

MODCODLST7: **DIS_8PSK_9_10**: disable 8PSK 9/10
[5:4] bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST7: **DIS_8P_8_9**: disable 8PSK 8/9
[3:0] bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST8: **DIS_8P_5_6**: disable 8PSK 5/6
[7:4] bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST8: **DIS_8P_3_4**: disable 8PSK 3/4
[3:0] bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST9: **DIS_8P_2_3**: disable 8PSK 2/3
[7:4] bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLST9: **DIS_8P_3_5**: disable 8PSK 3/5
[3:0] bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTA List of prohibited MODCOD

7	6	5	4	3	2	1	0
RESERVED		DIS_QPSK_9_10		DIS_QP_8_9			
R		R/W		R/W			

Address: 0xF4BA

Type: R/W

Reset: 0xC0

Description: List of prohibited MODCOD

[5:4] **DIS_QPSK_9_10**: disable QPSK 9/10
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] **DIS_QP_8_9**: disable QPSK 8/9
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTB List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_5_6				DIS_QP_4_5			
R/W				R/W			

Address: 0xF4BB

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] **DIS_QP_5_6**: disable QPSK 5/6
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] **DIS_QP_4_5**: disable QPSK 4/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTC List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QP_3_4				DIS_QP_2_3			
R/W				R/W			

Address: 0xF4BC

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] **DIS_QP_3_4**: disable QPSK 3/4
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] **DIS_QP_2_3**: disable QPSK 2/3
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

MODCODLSTD List of prohibited MODCOD

7	6	5	4	3	2	1	0
DIS_QPSK_3_5				DIS_QPSK_1_2			
R/W				R/W			

Address: 0xF4BD

Type: R/W

Reset: 0x0

Description: List of prohibited MODCOD

[7:4] **DIS_QPSK_3_5**: disable QPSK 3/5
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

[3:0] **DIS_QPSK_1_2**: disable QPSK 1/2
bit 3: disable short with pilots
bit 2: disable short without pilots
bit 1: disable long with pilots
bit 0: disable long without pilots (unsigned)

GAUSSR0 Gaussien phase detector radius, R0

7	6	5	4	3	2	1	0
EN_CCIMODE	R0_GAUSSIEN						
R/W	R/W						

Address: 0xF4C0

Type: R/W

Reset: 0x98

Description: Gaussien phase detector radius, R0

[7] **EN_CCIMODE**: 1: switch on this machine (unsigned)

[6:0] **R0_GAUSSIEN**: Reference radius in Gaussian mode. (unsigned)

CCIR0 CCI phase detector radius, R0

7	6	5	4	3	2	1	0
CCIDETECT_PLHONLY	R0_CCI						
R/W	R/W						

Address: 0xF4C1

Type: R/W

Reset: 0x30

Description: CCI phase detector radius, R0

[7] **CCIDETECT_PLHONLY**: 1: allow switching to CCI/Gaussien mode (unsigned)

[6:0] **R0_CCI**: reference radius in CCI mode. (unsigned)

CCIQUANT CCI detector quantifier

7	6	5	4	3	2	1	0
CCI_BETA			CCI_QUANT				
R/W			R/W				

Address: 0xF4C2

Type: R/W

Reset: 0xAC

Description: CCI detector quantifier

[7:5] **CCI_BETA**: CCI detector beta:
000: stop
001: minimum speed
111: maximum speed (unsigned)

[4:0] **CCI_QUANT**: Quantitative estimation on CCI (unsigned)

CCITHRES CCI threshold detector level

7	6	5	4	3	2	1	0
CCI_THRESHOLD							
R/W							

Address: 0xF4C3

Type: R/W

Reset: 0x50

Description: CCI threshold detector level

[7:0] **CCI_THRESHOLD**: To be compared with the value in cci_value. (unsigned)

CCIACC CCI detector accumulator

7	6	5	4	3	2	1	0
CCI_VALUE							
R							

Address: 0xF4C4

Type: R

Reset: Undefined

Description: CCI detector accumulator

[7:0] **CCI_VALUE**: Quantitative estimation of CCI in the signal.
A write to this register causes the CCI state-machine to be reset. (unsigned)

DSTATUS4 Demodulator Status

7	6	5	4	3	2	1	0
RAINFADE_DETECT	NOTHRES2_FAIL	NOTHRES1_FAIL	RESERVED				
R/W	R	R	R				

Address: 0xF4C5

Type: R

Reset: Undefined

Description: Demodulator Status

[7] **RAINFADE_DETECT**: 1: Rain fading detected (read put to 0 on a write,unsigned)

[6] **NOTHRES2_FAIL**: 1: the current noise level is higher than the limit programmed in NOSTHRES2 (read put to 0 on a read,unsigned)

[5] **NOTHRES1_FAIL**: 1: the current noise level is higher than the limit programmed in NOSTHRES1 (read put to 0 on a read,unsigned)

DMDRESCFG FIFO results configuration

7	6	5	4	3	2	1	0
DMDRES_RESET	RESERVED			DMDRES_STRALL	DMDRES_NEWONLY	DMDRES_NOSTORE	RESERVED
R/W	R			R/W	R/W	R/W	R

Address: 0xF4C6

Type: R/W

Reset: 0x29

Description: FIFO results configuration

[7] **DMDRES_RESET**: 1: reset FIFO results (unsigned)

[3] **DMDRES_STRALL**: 1: do not store the undecodables (unsigned)

[2] **DMDRES_NEWONLY**: 1: only store the new channels (unsigned)

[1] **DMDRES_NOSTORE**: 1: only store the tuner information and forget the channel information (both decodables and undecodables). (unsigned)

DMDRESADR FIFO results status

7	6	5	4	3	2	1	0
RESERVED	DMDRES_VALIDCFR	DMDRES_MEMFULL		DMDRES_RESNBR			
R	R	R		R			

Address: 0xF4C7

Type: R

Reset: Undefined

Description: FIFO results status

[6] **DMDRES_VALIDCFR**: 1: channel valid
0: channel undecodable (unsigned)

[5:4] **DMDRES_MEMFULL**: FIFO results load:
00: empty
01: results waiting
10: more than 8 results waiting
11: full, urgently needs to be emptied (unsigned)

[3:0] **DMDRES_RESNBR**: number of results waiting. (unsigned)

DMDRESDATAx FIFO results

	7	6	5	4	3	2	1	0
DMDRESDATA7	DMDRES_DATA[63:56]							
DMDRESDATA6	DMDRES_DATA[55:48]							
DMDRESDATA5	DMDRES_DATA[47:40]							
DMDRESDATA4	DMDRES_DATA[39:32]							
DMDRESDATA3	DMDRES_DATA[31:24]							
DMDRESDATA2	DMDRES_DATA[23:16]							
DMDRESDATA1	DMDRES_DATA[15:8]							
DMDRESDATA0	DMDRES_DATA[7:0]							
	R/W							

Address: 0xF4CF - x * 0x1 (x=0 to 7)

Type: R/WH

Reset: Undefined

Description: The results of one captured channel stored in the FIFO.

Bit 19 indicates whether the results are valid or if the block is empty and should be discarded.
The 64-bit DMDRES_DATA field must be interpreted according to the type of modulation found (DVB-S2/DVB-S/undecoded) which is indicated in bits 7:5.
In order to read the next FIFO result a single write to any of the DMDRES_DATA7..0 registers will flush the present result and index to the next.

The interpretation of the FIFO contents is as follows:
If [7] = 1 then signal = DVB-S2; If [7]=0 & [5] =1 then signal=DVB-S/DSS else invalid.

63..48: SFR[15:0], symbol rate of signal found.
47..32: CFR[15:0], carrier offset 1 of signal found.
31..28: mantissa of AGC2 level of signal found.
27..24: exponent of AGC2 level of signal found. AGC2 ~ AGC2_mantissa * 2^AGC2_exponant.
23..20: noise_exponant, exponent (only) of noise level of signal found. Noise level ~ 2^noise_exponant.
19: valid_result, at 1 if the result is valid (usable). At 0 if the data is not relevant.
18: specinv_demod, local spectral inversion detected by the demodulator (for DVB-S2 only).
17..16: rolloff_control[1:0], Nyquist filter type at the moment of locking (00:35% 01:25% 10:20% 11:15%).
8: Demod locked.

DVB-S2:
7: constant, 1
6..2: MODCOD[4:0], MODCOD of channel found.
1..0: TYPE[1:0], TYPE of channel found.

DVB-S1/Legacy DTV:
7: constant, 0
5: constant, 1
4: local spectral inversion detected by the Viterbi.
3: DVB-S1 or Legacy DTV:
0: DVB-S1
1: Legacy DTV
2..0: puncture rate found. 000:1/2 001:2/3 010:3/4 011:5/6 100:6/7 101:7/8.

Invalid:
7: constant, 0
5: constant, 0

[7:0] **DMDRES_DATA**: (unsigned)

FFEIx — FFE Equalizer coefficients

	7	6	5	4	3	2	1	0
FFEI1	FFE_ACCI1							
FFEI2	FFE_ACCI2							
FFEI3	FFE_ACCI3							
FFEI4	FFE_ACCI4							
	R/W							

Address: 0xF4D0 + (x-1) * 0x2 (x=1 to 4)

Type: R/W

Reset: Undefined

Description: FFE equalizer observation
FFEI1..FFEQ1

.....
FFEI4..FFEQ4

[7:0] **FFE_ACCIx**: (signed)

FFEQx FFE Equalizer coefficients

	7	6	5	4	3	2	1	0
FFEQ1	FFE_ACCQ1							
FFEQ2	FFE_ACCQ2							
FFEQ3	FFE_ACCQ3							
FFEQ4	FFE_ACCQ4							
	R/W							

Address: 0xF4D1 + (x-1) * 0x2 (x=1 to 4)

Type: R/W

Reset: Undefined

Description: FFE equalizer observation
FFEI1..FFEQ1
.....
FFEI4..FFEQ4

[7:0] **FFE_ACCQx**: (signed)

FFECFG FFE equalizer configuration

7	6	5	4	3	2	1	0
RESERVED	EQUALFFE_ON	RESERVED			MU_EQUALFFE		
R	R/W	R			R/W		

Address: 0xF4D8

Type: R/W

Reset: 0x71

Description: FFE equalizer configuration

[6] **EQUALFFE_ON**: 1: activate the FFE equalizer
0: stop and reset the FFE equalizer.
disconnection of the data path and reset of the coefficients>
The FFE equalizer must always be active to compensate for group delay errors. (unsigned)

[2:0] **MU_EQUALFFE**: FFE equalizer update speed.
111: Fastest
100: median value
001: Very slow (good for tracking)
000: Coefficients frozen (but equalizer still active). (unsigned)

SMAPCOEF7 LLR gain in DVB-S2 QPSK

7	6	5	4	3	2	1	0
RESERVED	SMAPCOEF_Q_LLR12						
R	R/W						

Address: 0xF500

Type: R/W

Reset: 0x0

Description: LLR gain in DVB-S2 QPSK

[6:0] **SMAPCOEF_Q_LLR12**: LLR gain in DVB-S2 QPSK (signed)

SMAPCOEFx LLR gain in DVB-S2 8PSK

	7	6	5	4	3	2	1	0
SMAPCOEF6	RESERVED					ADJ_8PSKLLR1	OLD_8PSKLLR1	DIS_AB8PSK
	R					R/W	R/W	R/W

	7	6	5	4	3	2	1	0
SMAPCOEF5	DIS_8SCALE	SMAPCOEF_8P_LLR23						
	R/W	R/W						

Address: 0xF502 - (x-5) * 0x1 (x=5 to 6)

Type: R/W

Reset: 0x0

Description: LLR gain in DVB-S2 8PSK

SMAPCOEF6: [2] **ADJ_8PSKLLR1**: 1: Use STV0900 cut 2.0 or greater method for calculating LLRs. Add adjusting factor. (unsigned)

SMAPCOEF6: [1] **OLD_8PSKLLR1**: 1: The method of calculating LLRs prior to STV0900 cut2.0 is employed. The field SMAPCOEF_32_LLR15[6:0] is used. (unsigned)

SMAPCOEF6: [0] **DIS_AB8PSK**: Disable the addition of the adjusting factor (a+b)(-I) (unsigned)

SMAPCOEF5: [7] **DIS_8SCALE**: disable LLR scaling factor for DVB-S2 8PSK
1: do not use scale factor
0: use scale factor (unsigned)

SMAPCOEF5: [6:0] **SMAPCOEF_8P_LLR23**: (signed)

NOSTHRESx Noise level Threshold x

	7	6	5	4	3	2	1	0
NOSTHRES1	NOS_THRESHOLD1							
NOSTHRES2	NOS_THRESHOLD2							
	R							

Address: 0xF509 + (x-1) * 0x1 (x=1 to 2)

Type: R

Reset: 0x60, 0x69

Description: Noise level Threshold x

[7:0] **NOS_THRESHOLDx**: Noise level threshold x. The measure units are depending on RAINFADE/nosthres_units and NOSRAMPOS/nosram_valid:
If RAINFADE/nosthres_units=1 and NOSRAMPOS/nosram_valid=1 (C/N estimator is on): nos_thresholdx is in same unit as NOSRAMVAL/nosram_cnrval (logarithmic if the table was loaded as is). If nosram_cnrval goes lower than nos_thresholdx, then DSTATUS4/nosthresx_fail goes to 1.
If RAINFADE/nosthres_units=0 or NOSRAMPOS/nosram_valid=0 (C/N estimator is off): nos_thresholdx is the linear unit of NNOSPLHT/64 (DVB-S2) or NNOSDATAT/64 (DVB-S1/Legacy DTV). If NNOSPLHT/64 or NNOSDATAT/64 goes upper than nos_thresholdx, then DSTATUS4/nosthresx_fail goes to 1. (unsigned)

NOSDIFF1 — Margin Indicator

7	6	5	4	3	2	1	0
NOSTHRES1_DIFF							
R							

Address: 0xF50B

Type: R

Reset: Undefined

Description: Margin Indicator

[7:0] **NOSTHRES1_DIFF**: (signed) difference between NOSTHRES1/nos_threshold1 and the current noise. The unit is the same as NOSTHRES1. (unsigned)

RAINFADE — Rain fading Indicator

7	6	5	4	3	2	1	0
NOSTHRES_DATAT	RAINFADE_CNLIMIT			RESERVED	RAINFADE_TIMEOUT		
R	R			R	R		

Address: 0xF50C

Type: R

Reset: 0x35

Description: Rain fading Indicator

[7] **NOSTHRES_DATAT**: measure units for NOSTHRES1, NOSTHRES2 and NOSDIFF1:
0: linear NNOSPLHT/64 or NNOSDATAT/64
1: logarithmic (same as NOSRAMVAL/nosram_cnrval). Be careful, available only if C/N estimator is on (NOSRAMPOS/nosram_valid=1). (unsigned)

[6:4] **RAINFADE_CNLIMIT**: Rain fading C/N drop
000: --
001..110: drop from 1 to 6 dB.
111: -- (unsigned)

[2:0] **RAINFADE_TIMEOUT**: sliding window time to detect rain fading occurrence (unit : 63.63 seconds at 135MHZ of master clock):
000: 1 minute (63.63 seconds, 1 mn and 4 sec),
...
110: 7 minutes (445 seconds, 7 mn and 25 sec),
111: test mode (speed multiplication by 2^20). (unsigned)

NOSRAMCFG C/N estimator control

7	6	5	4	3	2	1	0
RESERVED		NOSRAM_ACTIVATION		NOSRAM_CNRONLY	NOSRAM_LGNCNR[6:4]		
R		R/W		R/W	R/W		

Address: 0xF50D

Type: R/W

Reset: 0x28

Description: C/N estimator control

[5:4] **NOSRAM_ACTIVATION**: C/N estimator control mode
00: stop and reset the table
01: table loading mode
10: C/N estimator on
11: reserved (unsigned)

[3] **NOSRAM_CNRONLY**: The table can be used in two mode (extended or standard)
0: extended mode. For detailed information please ask STMicroelectronics support people.
1: standard mode. Only C/N estimation data are loaded into the table. (unsigned)

[2:0] **NOSRAM_LGNCNR**: Line pointer in the C/N table (unsigned)

NOSRAMPOS C/N estimator Position

7	6	5	4	3	2	1	0
NOSRAM_LGNCNR[3:0]				RESERVED	NOSRAM_VALIDE	NOSRAM_CNRVAL[9:8]	
R/W				R	R/W	R/W	

Address: 0xF50E

Type: R/W

Reset: 0x0

Description: C/N estimator Position

[7:4] **NOSRAM_LGNCNR**: Line pointer in the C/N table (unsigned)

[2] **NOSRAM_VALIDE**: 1: nosram_cnrval is valid
0: nosram_cnrval is invalid (unsigned)

[1:0] **NOSRAM_CNRVAL**: Current C/N estimated from the C/N table (unsigned)

NOSRAMVAL C/N estimator Value

7	6	5	4	3	2	1	0
NOSRAM_CNRVAL[7:0]							
R/W							

Address: 0xF50F

Type: R/W

Reset: 0x0

Description: C/N estimator Value

[7:0] **NOSRAM_CNRVAL**: Current C/N estimated from the C/N table (unsigned)

DMDPLHSTAT PLHeaders failure rate

7	6	5	4	3	2	1	0
PLH_STATISTIC							
R							

Address: 0xF520

Type: R

Reset: Undefined

Description: PLHeaders failure rate

[7:0] **PLH_STATISTIC**: Number of refused PLHeaders. 0 to 255. Rolls over to 0 when 255 reached. (unsigned)

LOCKTIMEx Demodulator locking time

	7	6	5	4	3	2	1	0
LOCKTIME3	DEMOD_LOCKTIME[31:24]							
LOCKTIME2	DEMOD_LOCKTIME[23:16]							
LOCKTIME1	DEMOD_LOCKTIME[15:8]							
LOCKTIME0	DEMOD_LOCKTIME[7:0]							
	R							

Address: 0xF525 - x * 0x1 (x=0 to 3)

Type: R

Reset: Undefined

Description: Demodulator locking time

[7:0] **DEMOD_LOCKTIME**: time taken between writing the AEP and locking. Some options available with DMDCFG3.locktime_mode.

Equation:

locking time = 2^7 * demod_locktime / Master_clock (unsigned)

17.5 TUN register descriptions

TNRCFG2 Tuner & input IQ control

7	6	5	4	3	2	1	0
TUN_IQSWAP	RESERVED						
R/W	R						

Address: 0xF4E1

Type: R/W

Reset: 0x2

Description: Tuner & input IQ control

[7] **TUN_IQSWAP**: Swap IQ paths immediately after ADCs (to correct for external wiring inversion if necessary).
Default for demodulator 1 =1, (unsigned)

17.6 DVB1 register descriptions

VITSCALE Additional configuration of Viterbi decoder

7	6	5	4	3	2	1	0
NVTH_NOSRANGE	VERROR_MAXMODE	RESERVED		NSLOWSN_LOCKED	RESERVED	DIS_RSFLOCK	RESERVED
R/W	R/W	R		R/W	R	R/W	R

Address: 0xF532

Type: R/W

Reset: 0x0

Description: Additional configuration of Viterbi decoder

[7] **NVTH_NOSRANGE**: Automatic calculation of Viterbi threshold as a function of noise. Used during acquisition.
0: The Viterbi threshold is calculated as a function of noise measured by the demodulator
1: No automatic adaptation of Vth. The Vth is taken from the VTHxx registers programmed by I2C. (unsigned)

[6] **VERROR_MAXMODE**: observation mode of VERROR register.
1: VERROR contains the maximum value achieved since its last re-initialization (via I2C write); very useful for adjusting the limits of each puncture rate or to obtain the maximum observed.
0: VERROR contains the instantaneous value of the number of errors. (unsigned)

[3] **NSLOWSN_LOCKED**: Slow the VERROR calculation (for a smoother result)
0: slow down
1: don‘t slow down (unsigned)

[1] **DIS_RSFLOCK**: False lock detection from Reed-Solomon decoder
1: Retrigger Viterbi if false lock detected
0: ignore false lock detection, do nothing. (unsigned)

FECM Viterbi decoder configuration

7	6	5	4	3	2	1	0
DSS_DVB	RESERVED		DSS_SRCH	RESERVED		SYNCVIT	IQINV
R	R		R/W	R		R/W	R

Address: 0xF533

Type: R/W

Reset: 0x10

Description: Viterbi decoder configuration

[7] **DSS_DVB**: standard used
1: Legacy DTV
0: DVB-S1 (read put to 0 on a read,unsigned)

[4] **DSS_SRCH**: norm searching mode
1: automatic DVB-S1/Legacy DTV search
0: manual search, program FECM.dss_dvb. (unsigned)

[1] **SYNCVIT**: 1: freeze the synchro word search mechanism. Very dangerous in case of unlocking: the machine will be incapable of re-hooking. (unsigned)

[0] **IQINV**: observation of the local spectral inversion detected by the Viterbi decoder. In manual mode, i2csym = DEMOD.specinv_control(0). (read put to 0 on a read,unsigned)

VTH12 Error threshold for puncture rate 1/2

7	6	5	4	3	2	1	0
VTH12							
R/W							

Address: 0xF534

Type: R/W

Reset: 0xD7

Description: Error threshold for puncture rate 1/2

[7:0] **VTH12**: (unsigned)

VTH23 Error threshold for puncture rate 2/3

7	6	5	4	3	2	1	0
VTH23							
R/W							

Address: 0xF535

Type: R/W

Reset: 0x85

Description: Error threshold for puncture rate 2/3

[7:0] **VTH23**: (unsigned)

VTH34 Error threshold for puncture rate 3/4

7	6	5	4	3	2	1	0
VTH34							
R/W							

Address: 0xF536

Type: R/W

Reset: 0x58

Description: Error threshold for puncture rate 3/4

[7:0] **VTH34**: (unsigned)

VTH56 Error threshold for puncture rate 5/6

7	6	5	4	3	2	1	0
VTH56							
R/W							

Address: 0xF537

Type: R/W

Reset: 0x3A

Description: Error threshold for puncture rate 5/6

[7:0] **VTH56**: (unsigned)

VTH67 Error threshold for puncture rate 6/7

7	6	5	4	3	2	1	0
VTH67							
R/W							

Address: 0xF538

Type: R/W

Reset: 0x34

Description: Error threshold for puncture rate 6/7

[7:0] **VTH67**: (unsigned)

VTH78 Error threshold for puncture rate 7/8

7	6	5	4	3	2	1	0
VTH78							
R/W							

Address: 0xF539

Type: R/W

Reset: 0x28

Description: Error threshold for puncture rate 7/8

[7:0] **VTH78**: (unsigned)

VITCURPUN Current puncture rate on the Viterbi decoder

7	6	5	4	3	2	1	0
RESERVED			VIT_CURPUN				
R			R				

Address: 0xF53A

Type: R

Reset: Undefined

Description: Current puncture rate on the Viterbi decoder

[4:0] **VIT_CURPUN**: current puncture rate
0x0d:1/2 0x12:2/3 0x15:3/4 0x18:5/6 0x19:6/7 0x1a:7/8 (unsigned)

VERROR Current error rate

7	6	5	4	3	2	1	0
REGERR_VIT							
R/W							

Address: 0xF53B

Type: R/WH

Reset: Undefined

Description: Current error rate

[7:0] **REGERR_VIT**: current error rate or maximum observed by the Viterbi decoder.
Equation:
proportion of errors = regerr_vit / 2048
Examples:
0x00 = no errors, signal perfect
0xFF = 6.23% errors (255 bits corrected out of 2048). (read put to 0 on a write,unsigned)

PRVIT List of authorized puncture rates

7	6	5	4	3	2	1	0
RESERVED	DIS_VTHLOCK	E7_8VIT	E6_7VIT	E5_6VIT	E3_4VIT	E2_3VIT	E1_2VIT
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF53C

Type: R/W

Reset: 0x7F

Description: List of authorized puncture rates

[6] **DIS_VTHLOCK**: Automatic adjustment of VTH as a function of noise after decoder lock.
1: automatic adjustment enabled
0: disabled (unsigned)

[5] **E7_8VIT**: authorization of rate 7/8 (unsigned)

[4] **E6_7VIT**: authorization of rate 6/7 (unsigned)

[3] **E5_6VIT**: authorization of rate 5/6 (unsigned)

[2] **E3_4VIT**: authorization of rate 3/4 (unsigned)

[1] **E2_3VIT**: authorization of rate 2/3 (unsigned)

[0] **E1_2VIT**: authorization of rate 1/2 (unsigned)

VAVSRVIT Viterbi decoder search speeds

7	6	5	4	3	2	1	0
AMVIT	FROZENVIT	SNVIT		TOVVIT		HYPVIT	
R/W	R/W	R/W		R/W		R/W	

Address: 0xF53D

Type: R/W

Reset: 0x0

Description: Viterbi decoder search speeds

[7] **AMVIT**: puncture rate search manual or automatic mode. Used with frozenvit below.
1: manual search. Each positive edge on frozenvit increments the internal puncture rate search mechanism.
0: automatic mode, normal (unsigned)

[6] **FROZENVIT**: freeze the synchronizations
If amvit=0:
1: freeze the puncture rate search mechanism
0: automatic mode, normal
If amvit=1: each positive edge of this bit increments the internal puncture rate search machine. (unsigned)

[5:4] **SNVIT**: measuring time (number of symbols) for evaluating VERROR.regerr_vit
00: 4096 bits
01: 16384 bits
10: 65536 bits
11: 262144 bits (unsigned)

[3:2] **TOVVIT**: synchro word search time-out.
If no synchro word has been found during this time, the internal puncture rate search mechanism switches itself back on.
This time-out counter only starts once a puncture rate has been found (VSTATUSVIT.prfvit goes to 1). 00: 32768 bits or the time for 23 packets DVB+Legacy DTV
01: 65536 bits 46 packets DVB+Legacy DTV
10: 131072 bits 93 packets DVB+Legacy DTV
11: 262144 bits 186 packets DVB+Legacy DTV (unsigned)

[1:0] **HYPVIT**: Viterbi decoder locking validation or devalidation limit
If the specified number of consecutive synchro words are detected, then the Viterbi decoder is locked (VSTATUSVIT.lockedvit goes to 1).
If the specified number of consecutive synchro words are lost, then the Viterbi decoder is unlocked (VSTATUSVIT.lockedvit goes to 0). The puncture rate search mechanism switches itself back on. 00: 16 consecutive synchro words found or lost
01: 32 consecutive synchro words found or lost
10: 64 consecutive synchro words found or lost
11: 128 consecutive synchro words found or lost (unsigned)

VSTATUSVIT Viterbi decoder status

7	6	5	4	3	2	1	0
RESERVED			PRFVIT	LOCKEDVIT	RESERVED		
R			R/W	R/W	R		

Address: 0xF53E

Type: R/WH

Reset: Undefined

Description: Certain bits of this register reset themselves to 0 uniquely via I2C writing (the value of the data written is unimportant, only the action of I2C writing).

[4] **PRFVIT**: Puncture Rate Found
1: puncture rate found
0: searching puncture rate (unsigned)

[3] **LOCKEDVIT**: Viterbi Locked
1: decoder locked
0: searching synchro word (unsigned)

VTHINUSE — Viterbi threshold currently in use

7	6	5	4	3	2	1	0
VIT_INUSE							
R							

Address: 0xF53F

Type: R

Reset: Undefined

Description: Viterbi threshold currently in use

[7:0] **VIT_INUSE**: Actual Viterbi threshold in use (observation).
During acquisition this is controlled by VITSCALE:NVTH_NOSRANGE
After acquisition; PRFVIT:DIS_VTHLOCK (unsigned)

KDIV12 — Gain (k_divider) of puncture rate 1/2

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_12						
R	R/W						

Address: 0xF540

Type: R/W

Reset: 0x27

Description: Gain (k_divider) of puncture rate 1/2

[6:0] **K_DIVIDER_12**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_12 / 256 * II or QI (unsigned)

KDIV23 — Gain (k_divider) of puncture rate 2/3

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_23						
R	R/W						

Address: 0xF541

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 2/3

[6:0] **K_DIVIDER_23**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_23 / 256 * II or QI (unsigned)

KDIV34 Gain (k_divider) of puncture rate 3/4

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_34						
R	R/W						

Address: 0xF542

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 3/4

[6:0] **K_DIVIDER_34**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_34 / 256 * II or QI (unsigned)

KDIV56 Gain (k_divider) of puncture rate 5/6

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_56						
R	R/W						

Address: 0xF543

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 5/6

[6:0] **K_DIVIDER_56**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_56 / 256 * II or QI (unsigned)

KDIV67 Gain (k_divider) of puncture rate 6/7

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_67						
R	R/W						

Address: 0xF544

Type: R/W

Reset: 0x32

Description: Gain (k_divider) of puncture rate 6/7

[6:0] **K_DIVIDER_67**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_67 / 256 * II or QI (unsigned)

KDIV78 Gain (k_divider) of puncture rate 7/8

7	6	5	4	3	2	1	0
RESERVED	K_DIVIDER_78						
R	R/W						

Address: 0xF545

Type: R/W

Reset: 0x50

Description: Gain (k_divider) of puncture rate 7/8

[6:0] **K_DIVIDER_78**: multiplying coefficient applied for the puncture rate. Equation:
Metric = k_divider_78 / 256 * II or QI (unsigned)

17.7 DVB2 register descriptions

PDELCTRL1 Packet delineator configuration

7	6	5	4	3	2	1	0
RESERVED							ALGOSWRST
R							R/W

Address: 0xF550

Type: R/W

Reset: 0x0

Description: Packet delineator configuration

[0] **ALGOSWRST**: 1: Packet Delineator reset (unsigned)

PDELCTRL2 Packet delineator additional configuration

7	6	5	4	3	2	1	0
RESERVED	RESET_UPKO_COUNT	RESERVED					
R	R/W	R					

Address: 0xF551

Type: R/W

Reset: 0x00

Description: Packet delineator additional configuration

[6] **RESET_UPKO_COUNT**: Reset BBFCRCKO and UPCRCKO counters (unsigned)

ISIENTRY MIS mode selection filter

7	6	5	4	3	2	1	0
ISI_ENTRY							
R/W							

Address: 0xF55E

Type: R/W

Reset: 0x0

Description: The multiple input stream filter is available when the BBHeader MATYPE/SISMIS=0 and is activated when register field PDELCTRL1/filter_en=1. A set of masks permit the selection of frames with the correct MATYPE/ISI (the 8 bits LSB of MATYPE at the start of BBheader). The masking equation is the following:
test_MIS = MATYPE/ISI and ISIBITENA/isi_bit_en

The following depends on the polarity of register field PDELCTRL1/inv_mismask:

-inv_mismask=0: the frame is accepted if test_MIS = ISIENTRY/isi_entry

-inv_mismask=1: the frame is accepted if test_MIS /= ISIENTRY/isi_entry

The case MATYPE/ISI=0 could be considered as a special case if PDELCTRL1/en_mis00=1, this frame is always accepted regardless of the configuration of inv_mismask, isi_bit_en and isi_entry.

This frame can then be seen as a system frame which is always accepted, such as the channel descriptors and other telemetry.

[7:0] **ISI_ENTRY**: (unsigned)

ISIBITENA — MIS mode selection mask

7	6	5	4	3	2	1	0
ISI_BIT_EN							
R/W							

Address: 0xF55F

Type: R/W

Reset: 0x0

Description: See ISIENTRY.

[7:0] **ISI_BIT_EN**: (unsigned)

MATSTRx — MATYPE of the current frame

	7	6	5	4	3	2	1	0
MATSTR1	MATYPE_CURRENT[15:8]							
MATSTR0	MATYPE_CURRENT[7:0]							
	R							

Address: 0xF561 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: MATYPE of the current frame

[7:0] **MATYPE_CURRENT**: (unsigned)

UPLSTRx — UPL of the current frame

	7	6	5	4	3	2	1	0
UPLSTR1	UPL_CURRENT[15:8]							
UPLSTR0	UPL_CURRENT[7:0]							
	R							

Address: 0xF563 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: UPL of the current frame

[7:0] **UPL_CURRENT**: (unsigned)

DFLSTRx — DFL of the current frame

	7	6	5	4	3	2	1	0
DFLSTR1	DFL_CURRENT[15:8]							
DFLSTR0	DFL_CURRENT[7:0]							
	R							

Address: 0xF565 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: DFL of the current frame

[7:0] **DFL_CURRENT**: (unsigned)

SYNCSTR — SYNC of the current frame

7	6	5	4	3	2	1	0
SYNC_CURRENT							
R							

Address: 0xF566

Type: R

Reset: Undefined

Description: SYNC of the current frame

[7:0] **SYNC_CURRENT**: (unsigned)

SYNCDSTRx — SYNCD of the current frame

	7	6	5	4	3	2	1	0
SYNCDSTR1	SYNCD_CURRENT[15:8]							
SYNCDSTR0	SYNCD_CURRENT[7:0]							
	R							

Address: 0xF568 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: SYNCD of the current frame

[7:0] **SYNCD_CURRENT**: (unsigned)

PDELSTATUS1 Packet delineator status

7	6	5	4	3	2	1	0
PKTDELIN_DELOCK	SYNCDUPDFL_BADDFL	RESERVED	UNACCEPTED_STREAM	BCH_ERROR_FLAG	RESERVED	PKTDELIN_LOCK	FIRST_LOCK
R/W	R	R	R	R	R	R	R

Address: 0xF569

Type: R

Reset: Undefined

Description: Packet delineator status

[7] **PKTDELIN_DELOCK**: Detection of a 0 event on pktdelin_lock. Useful for debugging the origin of a signal fault
Reset by an I2C write (read put to 0 on a write,unsigned)

[6] **SYNCDUPDFL_BADDFL**: 1: error: DFL > DFL maximum possible for this MODCOD or SYNCD greater than DFL or UPL (and not 0xFFFF)
has happened since last reset
Reset by I2C read (read put to 0 on a read,unsigned)

[4] **UNACCEPTED_STREAM**: 1: current frame refused (due to error or bad ISI) (read put to 0 on a read,unsigned)

[3] **BCH_ERROR_FLAG**: 1: a BCH error occurred in one of the previous frames.
Bit automatically reset to 0 after I2C reading. (read put to 0 on a read,unsigned)

[1] **PKTDELIN_LOCK**: 1: Packet Delineator locked (unsigned)

[0] **FIRST_LOCK**: 1: The Packet Delineator is locked and processing frames (functioning normally) (unsigned)

PDELSTATUS2 Additional status for packet delineator

7	6	5	4	3	2	1	0
RESERVED	FRAME_MODCOD					FRAME_TYPE	
R	R					R	

Address: 0xF56A

Type: R

Reset: Undefined

Description: Additional status for packet delineator

[6:2] **FRAME_MODCOD**: MODCOD of the current frame (unsigned)

[1:0] **FRAME_TYPE**: TYPE of the current frame (unsigned)

BBFCRCKOx BBHeader KO counter

	7	6	5	4	3	2	1	0
BBFCRCKO1	BBHCRC_KOCNT[15:8]							
BBFCRCKO0	BBHCRC_KOCNT[7:0]							
	R/W							

Address: 0xF56C - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: 0x0

Description: BBHeader KO counter

[7:0] **BBHCRC_KOCNT**: number of false frames (CRC8 BBHeader false) since the last re-initialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

UPCRCKOx Packet KO counter

	7	6	5	4	3	2	1	0
UPCRCKO1	PKTCRC_KOCNT[15:8]							
UPCRCKO0	PKTCRC_KOCNT[7:0]							
	R/W							

Address: 0xF56E - x * 0x1 (x=0 to 1)

Type: R/WH

Reset: 0x0

Description: Packet KO counter

[7:0] **PKTCRC_KOCNT**: number of false packets (CRC8 packet false) since the last re-initialization of this register.
Reset to 0 by I2C write. (read put to 0 on a write,unsigned)

NBITER_NFx Number of LDPC decoding iterations

	7	6	5	4	3	2	1	0
NBITER_NF4	NBITER_NF_QPSK_1_2							
NBITER_NF5	NBITER_NF_QPSK_3_5							
NBITER_NF6	NBITER_NF_QPSK_2_3							
NBITER_NF7	NBITER_NF_QPSK_3_4							
NBITER_NF8	NBITER_NF_QPSK_4_5							
NBITER_NF9	NBITER_NF_QPSK_5_6							
NBITER_NF10	NBITER_NF_QPSK_8_9							
NBITER_NF11	NBITER_NF_QPSK_9_10							
NBITER_NF12	NBITER_NF_8PSK_3_5							
NBITER_NF13	NBITER_NF_8PSK_2_3							
NBITER_NF14	NBITER_NF_8PSK_3_4							
NBITER_NF15	NBITER_NF_8PSK_5_6							
NBITER_NF16	NBITER_NF_8PSK_8_9							
NBITER_NF17	NBITER_NF_8PSK_9_10							
	R/W							

Address: 0xFA03 + (x-4) * 0x1 (x=4 to 17)

Type: R/W

Reset: 0x23, 0x1B, 0x24, 0x23, 0x22, 0x21, 0x28, 0x28, 0x1B, 0x24, 0x23, 0x21, 0x28, 0x28

Description: NBITER_NFn -> number of normal frame iterations for MODCOD n.

NBITER_NF4: [7:0] **NBITER_NF_QPSK_1_2**: (unsigned)

NBITER_NF5: [7:0] **NBITER_NF_QPSK_3_5**: (unsigned)

NBITER_NF6: [7:0] **NBITER_NF_QPSK_2_3**: (unsigned)

NBITER_NF7: [7:0] **NBITER_NF_QPSK_3_4**: (unsigned)

NBITER_NF8: [7:0] **NBITER_NF_QPSK_4_5**: (unsigned)

NBITER_NF9: [7:0] **NBITER_NF_QPSK_5_6**: (unsigned)

NBITER_NF10: [7:0] **NBITER_NF_QPSK_8_9**: (unsigned)

NBITER_NF11: [7:0] **NBITER_NF_QPSK_9_10**: (unsigned)

NBITER_NF12: [7:0] **NBITER_NF_8PSK_3_5**: (unsigned)

NBITER_NF13: [7:0] **NBITER_NF_8PSK_2_3**: (unsigned)

NBITER_NF14: [7:0] **NBITER_NF_8PSK_3_4**: (unsigned)

NBITER_NF15: [7:0] **NBITER_NF_8PSK_5_6**: (unsigned)

NBITER_NF16: [7:0] **NBITER_NF_8PSK_8_9**: (unsigned)

NBITER_NF17: [7:0] **NBITER_NF_8PSK_9_10**: (unsigned)

GAINLLR_NFx LDPC input LLR gain

	7	6	5	4	3	2	1	0
GAINLLR_NF4	RESERVED	GAINLLR_NF_QPSK_1_2						
GAINLLR_NF5	RESERVED	GAINLLR_NF_QPSK_3_5						
GAINLLR_NF6	RESERVED	GAINLLR_NF_QPSK_2_3						
GAINLLR_NF7	RESERVED	GAINLLR_NF_QPSK_3_4						
GAINLLR_NF8	RESERVED	GAINLLR_NF_QPSK_4_5						
GAINLLR_NF9	RESERVED	GAINLLR_NF_QPSK_5_6						
GAINLLR_NF10	RESERVED	GAINLLR_NF_QPSK_8_9						
GAINLLR_NF11	RESERVED	GAINLLR_NF_QPSK_9_10						
GAINLLR_NF12	RESERVED	GAINLLR_NF_8PSK_3_5						
GAINLLR_NF13	RESERVED	GAINLLR_NF_8PSK_2_3						
GAINLLR_NF14	RESERVED	GAINLLR_NF_8PSK_3_4						
GAINLLR_NF15	RESERVED	GAINLLR_NF_8PSK_5_6						
GAINLLR_NF16	RESERVED	GAINLLR_NF_8PSK_8_9						
GAINLLR_NF17	RESERVED	GAINLLR_NF_8PSK_9_10						
	R	R/W						

Address: 0xFA43 + (x-4) * 0x1 (x=4 to 17)

Type: R/W

Reset: 0x20

Description: GainLLR_NFn -> normal frame LLR gain for MODCOD n

GAINLLR_NF4: [6:0] **GAINLLR_NF_QPSK_1_2**: (unsigned)

GAINLLR_NF5: [6:0] **GAINLLR_NF_QPSK_3_5**: (unsigned)

GAINLLR_NF6: [6:0] **GAINLLR_NF_QPSK_2_3**: (unsigned)

GAINLLR_NF7: [6:0] **GAINLLR_NF_QPSK_3_4**: (unsigned)

GAINLLR_NF8: [6:0] **GAINLLR_NF_QPSK_4_5**: (unsigned)

GAINLLR_NF9: [6:0] **GAINLLR_NF_QPSK_5_6**: (unsigned)

GAINLLR_NF10: [6:0] **GAINLLR_NF_QPSK_8_9**: (unsigned)

GAINLLR_NF11: [6:0] **GAINLLR_NF_QPSK_9_10**: (unsigned)

GAINLLR_NF12: [6:0] **GAINLLR_NF_8PSK_3_5**: (unsigned)

GAINLLR_NF13: [6:0] **GAINLLR_NF_8PSK_2_3**: (unsigned)

GAINLLR_NF14: [6:0] **GAINLLR_NF_8PSK_3_4**: (unsigned)

GAINLLR_NF15: [6:0] **GAINLLR_NF_8PSK_5_6**: (unsigned)

GAINLLR_NF16: [6:0] **GAINLLR_NF_8PSK_8_9**: (unsigned)

GAINLLR_NF17: [6:0] **GAINLLR_NF_8PSK_9_10**: (unsigned)

GENCFG General Configuration

7	6	5	4	3	2	1	0
RESERVED							
R							

Address: 0xFA86

Type: R/W

Reset: 0x14

Description: General Configuration

LDPCERRx LDPC error counter

	7	6	5	4	3	2	1	0
LDPCERR1	LDPC_ERRORS[15:8]							
LDPCERR0	LDPC_ERRORS[7:0]							
	R							

Address: 0xFA97 - x * 0x1 (x=0 to 1)

Type: R

Reset: 0x0

Description: LDPC error counter

[7:0] **LDPC_ERRORS**: number of errors corrected by the LDPC decoder on the current output frame (unsigned)

BCHERR BCH error

7	6	5	4	3	2	1	0
RESERVED			ERRORFLAG	BCH_ERRORS_COUNTER			
R			R	R			

Address: 0xFA98

Type: R

Reset: 0x0

Description: BCH error

[4] **ERRORFLAG**: Comparison flag between the bch_errors_counter value and the corrected error number. If the GENCFG.2 bit is set to 1, the flag is valid for the current frame but available when the last output byte, otherwise, it is valid for the previous frame. (unsigned)

[3:0] **BCH_ERRORS_COUNTER**: BCH error number location polynomial degree for the current output frame.
Max values are 0xA = d10 for 2/3 and 5/6 coderates, 0x8 = d8 for 8/9 and 9/10 coderates, 0xC = d12 for all others (unsigned)

MAXEXTRAITER — LDPC Extra-iteration value

7	6	5	4	3	2	1	0
MAX_EXTRA_ITER							
R/W							

Address: 0xFAB1

Type: R/W

Reset: 0x7

Description: LDPC Extra-iteration value

[7:0] **MAX_EXTRA_ITER**: Number of extra-iteration allowed for path n. Recommended value is 7 for dual 45 Msps and 11 for dual 31.5 Msps. (unsigned)

STATUSITER — LDPC iteration number performed

7	6	5	4	3	2	1	0
STATUS_ITER							
R							

Address: 0xFABC

Type: R

Reset: 0x0

Description: LDPC iteration number performed

[7:0] **STATUS_ITER**: Number of iteration performed on last frame on path n (unsigned)

STATUSMAXITER — LDPC maximum iteration number performed

7	6	5	4	3	2	1	0
STATUS_MAX_ITER							
R							

Address: 0xFABD

Type: R

Reset: 0x0

Description: LDPC maximum iteration number performed

[7:0] **STATUS_MAX_ITER**: maximum number of iteration performed on path n since last read of this register. (unsigned)

17.8 TS register descriptions

TSSTATEM Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSDIL_ON	RESERVED	TSRS_ON	TSDESCRAMB_ON	RESERVED	TS_DISABLE	RESERVED	TSOUT_NOSYNC
R/W	R	R/W	R/W	R	R/W	R	R/W

Address: 0xF570

Type: R/W

Reset: 0xF0

Description: Configuration of merger-hardware stream line 1

[7] **TSDIL_ON**: use of deinterleaver (active in DVB-S1 and Legacy DTV only):
1: deinterleaver active if authorized.
0: inactive. (unsigned)

[5] **TSRS_ON**: use of Reed-Solomon decoder (active in DVB-S1 and Legacy DTV only) if tsskiprs_on = 0:
1: decode and correct the data flow
0: decode but do not correct (unsigned)

[4] **TSDESCRAMB_ON**: use of descrambler (active in DVB-S1 only) if tsskiprs_on=0 and if TSSTATUS2/scrambdetect=1 (scrambling type DVB-S1 has been detected):
1: descramble the data flow
0: do not descramble (even if scrambling is detected) (unsigned)

[2] **TS_DISABLE**: disable line
1: the line is stopped, nothing outputs.
0: normal function (unsigned)

[0] **TSOUT_NOSYNC**: output controls
In packet modes ISSYI, NPD:
1: hysteresis mode authorized at power up
0: immediate output of all ready packets or frames
Other modes (packet or frame):
1: integrated circuit latency regulation
0: immediate output of all ready packets or frames (unsigned)

TSCFGH Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_DVBCI	TSFIFO_SERIAL	TSFIFO_TEIUPDATE	TSFIFO_DUTY50	TSFIFO_HSGNLOUT	TSFIFO_ERRMODE		RST_HWARE
R/W	R/W	R/W	R/W	R/W	R/W		R/W

Address: 0xF572

Type: R/W

Reset: 0x0

Description: Configuration of merger-hardware stream line 1

[7] **TSFIFO_DVBCI**: treatment of the signals CLKOUT and Data/Parity
1: mode DVB-CI: CLKOUT continuous, D/P indicates the data pulses
0: normal mode: a CLKOUT pulse with each data, CLKOUT off if no data, D/P remains punctured
In order to avoid a “hole“ on D/P, there are 3 equivalent solutions:
-do not connect it
-program TSCFGL/tsfifo_dpunact = 1
-deprogram the associated GPIO (unsigned)

[6] **TSFIFO_SERIAL**: 1: serial output: note the restriction to 135 Mbit/s.
0: parallel output, up to 270 Mbit/s. (unsigned)

[5] **TSFIFO_TEIUPDATE**: MPEG packets only (TSSTATEL/tsdss_packet=0)
1: update of TEI bit in accordance with the output ERROR signal. (unsigned)

[4] **TSFIFO_DUTY50**: CLKOUT signal duty cycle:
1: guarantees 50% but causes larger granularity on the available frequencies.
0: maximum granularity on the available frequencies, but duty cycle not guaranteed (though always as close as possible to 50%). (unsigned)

[3] **TSFIFO_HSGNLOUT**: Header signaling
1: output the 16 byte Header Signaling.
0: no header output. (unsigned)

[2:1] **TSFIFO_ERRMODE**: treatment of ERROR signal:
00: ERROR label the packets or frames in error.
The packets or frames are all being output (even if they are false or TSSTATUS/tsfifo_lineok=0).
01: ERROR = reference start of packet for the regulation (packet mode)
ERROR = start of packet byte indicator (frame mode)
The packets or frames are deleted before being output when they are false or TSSTATUS/tsfifo_lineok=0.
10: ERROR = SOF reference for the latency regulation
The packets or frames are deleted before being output when they are false or TSSTATUS/tsfifo_lineok=0.
11: ERROR = 0
The packets or frames are deleted before being output when they are false or TSSTATUS/tsfifo_lineok=0. (unsigned)

[0] **RST_HWARE**: 1: reset of Merger/HWare Stream line 1. (unsigned)

TSCFGM Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_MANSPEED		TSFIFO_PERMDATA	RESERVED				TSFIFO_INVDATA
R/W		R/W	R				R/W

Address: 0xF573

Type: R/W

Reset: 0x4

Description: Configuration of merger-hardware stream line 1

[7:6] **TSFIFO_MANSPEED**: CLKOUT frequency processing:
00: automatic calculation
01: automatic calculation while progressively keeping only the highest frequency (for ACM without MIS or ISSYI).
10: automatic calculation of the instantaneous frequency without memorizing the highest frequency found.
11: manual (unsigned)

[5] **TSFIFO_PERMDATA**: (active in serial and parallel)
1: switch DATA7<->DATA0 (unsigned)

[0] **TSFIFO_INVDATA**: 1: inverse DATA7..0 (unsigned)

TSCFGL Configuration of merger-hardware stream line 1

7	6	5	4	3	2	1	0
TSFIFO_BCLKDEL1CK		BCHERROR_MODE		TSFIFO_NSGNL2DATA	TSFIFO_EMBINDVB	TSFIFO_BITSPEED	
R/W		R/W		R/W	R/W	R/W	

Address: 0xF574

Type: R/W

Reset: 0x20

Description: Configuration of merger-hardware stream line 1

[7:6] **TSFIFO_BCLKDEL1CK**: 270 MHz delay cycle on CLKOUT with respect to other signals (STROUT, D/P, ERROR, DATA7..0)
00: (0) no delay
01: (+1) advance by one 270 MHz cycle
11: (-1) move back by one 270 MHz cycle
10: (-2) CLKOUT inversion (test mode) (unsigned)

[5:4] **BCHERROR_MODE**: error packet construction
DVB-S1/Legacy DTV (Reed-Solomon active):
00: RSerror
01: RSerror(+BBHeader)
10: RSerror (default)
11: RSerror(+BBHeader+BCHerror)
(Disable RSerror by TSSTATEM/tsrs_on=0)
DVB-S2 Packet mode:
00: nothing
01: CRC8pkt+BBHeader
10: CRC8pkt (default)
11: (CRC8pkt+BBHeader+)BCHerror
DVB-S2 frame mode:
00: BBHeader +CRC8pkt if frame is packetised
01: BBHeader
10: BBHeader (default)
+CRC8pkt if frame is packetised
+BCHerror if generic stream
11: (CRC8pkt+BBHeader+)BCHerror
Note in Generic Continuous Stream, CRC8pkt does not exist. (unsigned)

[3] **TSFIFO_NSGNL2DATA**: 1: D/P=0 during Signaling Header and Footer
0: D/P=1 during Signaling Header and Footer (unsigned)

[2] **TSFIFO_EMBINDVB**: 1: load the short packets (Legacy DTV) in an MPEG packet (unsigned)

[1:0] **TSFIFO_BITSPEED**: Method of calculation of the bit rate, generating the packet rate and the frequency of the output clock, CLKOUT (TSSPEED/tsfifo_outspeed). The result may be read in the register TSBITRATE.
00: automatic mode (default).
- In broadcast mode (CCM and VCM) (set by ACM bit in MATYPE) bit rate calculated using 0b10 below (note: not valid when using MIS).
- For modes when NPD, ACM or MIS is selected. See 0b11 below.
01: Manual mode. The value written in TSBITRATE is the value used to calculate the packet rate and CLKOUT.
10: Symbol rate mode: Output clock rate (bit rate) is calculated from symbol rate and MODCOD using the table 13 in EN302307v1.1.1. The results are not smoothed (change with DFL, PLFRAME length of each frame) but are perfectly exact in the space of a frame.
11: Pragmatic smoothing mode: The TSBITRATE is calculated from the long term average of bits leaving the packet delineator. The incoming frames must arrive regularly for this mode to work effectively. The register TSDLYSET/soffifo_offset is used to define the mid-point load on the TS FIFO. (unsigned)

TSINSDELH Insertion/deletion mask of output packet parts

7	6	5	4	3 2	1	0
TSDEL_SYNCBYTE	TSDEL_XXHEADER	RESERVED	TSDEL_DATAFIELD	RESERVED	TSINSDEL_RSPARITY	TSINSDEL_CRC8
R/W	R/W	R	R/W	R	R/W	R/W

Address: 0xF576

Type: R/W

Reset: 0x0

Description: Insertion/deletion mask of output packet parts

[7] **TSDEL_SYNCBYTE**: (1 byte) deletion of synchro word. (unsigned)

[6] **TSDEL_XXHEADER**: (3 bytes) deletion of Packet Header. (unsigned)

[4] **TSDEL_DATAFIELD**: deletion of the payload
Generic Continuous Stream: entire DATAFIELD
packet mode: packet payload
frame mode: packet payload (unsigned)

[1] **TSINSDEL_RSPARITY**: more specific to DVB-S1/Legacy DTV (16 bytes), output/deletion of the Reed-Solomon part (if present). (unsigned)

[0] **TSINSDEL_CRC8**: (1 byte) output/deletion of CRC8 packet. (unsigned)

TSDIVN Output frequency control

7	6	5 4 3 2 1 0
TSFIFO_SPEEDMODE		RESERVED
R/W		R

Address: 0xF579

Type: R/W

Reset: 0x3

Description: Output frequency control

[7:6] **TSFIFO_SPEEDMODE**: Transport stream output speed mode control
00: Classical mode
- Parallel: Fclkout = 4*Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 12 (Fclkout < Mclk/3)
- Serial: Fclkout = 32*Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 32 (Fclkout < Mclk)
01: Mantissa-Exponent mode.
- Parallel: Fclkout = 4*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
- Serial: Fclkout = 32*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
10: divide by 32 mode:
- Parallel: Fclkout = Mclk / 8*tsfifo_outspeed. Limited totsfifo_outspeed >= 4 (Fclkout < Mclk/32)
- Serial: Fclkout = Mclk / tsfifo_outspeed. Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/4)
11: -- (unsigned)

TSCFG4 Stream merger line 1 hardware configuration

7	6	5	4	3	2	1	0
TSFIFO_TSSPEEDMODE		RESERVED					
R/W		R					

Address: 0xF57A

Type: R/W

Reset: 0x0

Description: Stream merger line 1 hardware configuration

[7:6] **TSFIFO_TSSPEEDMODE**: Method of calculating TSSPEED/tsfifo_outspeed:
11: “instantaneous“ mode, tsfifo_outspeed is the instantaneous value of the bit or byte currently running. This is appropriate for variable rate streams (e.g ACM with the output of all MODCODS and latency regulation turned off)
10: “Smoothed“ mode, tsfifo_outspeed is smoothed (temporal averaging) over a large number of frames.
Ideal for CCM modes and where smoothing is useful (NPD, ISSYI).
00: “automatic“ mode, selects the best mode.
“smoothed“ mode when: CCM, NPD and or ISSYI, MIS;
“instantaneous“ mode when: ACM non NPD, ISSYI or MIS, latency regulation is off (TSSTATEM/tsout_nosync=1), external packet/frame synchronization (TSSYNC/tsfifo_syncmode=10) mode, frame output mode or Generic Stream mode.
01: -- (unsigned)

TSSPEED CLKOUT frequency

7	6	5	4	3	2	1	0
TSFIFO_OUTSPEED							
R/W							

Address: 0xF580

Type: R/W

Reset: Undefined

Description: See the field TSDIVN/tsfifo_speedmode for TSSPEED calculation mode.
See the field TSCFG4/tsfifo_tsspeedmode for TSSPEED update mode.

[7:0] **TSFIFO_OUTSPEED**: stream output frequency.
There are three modes for calculating outspeed depending on the configuration of TSDIVN/tsfifo_speedmode.
00: Legacy calculation mode:
Parallel: Fclkout = 4*Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 12 (Fclkout < Mclk/3)
Serial: Fclkout = 32*Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 32 (Fclkout < Mclk)
01: mantissa+exponant mode (internal value on 19 bits):
Parallel: Fclkout = 4*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
Serial: Fclkout = 32*Mclk / tsfifo_outspeed[4:0] / 2^(2*tsfifo_outspeed[7:5])
10: division by 32 of the output speed.
Parallel: Fclkout = Mclk / 8*tsfifo_outspeed
Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/32)
Serial: Fclkout = Mclk / tsfifo_outspeed
Limited to tsfifo_outspeed >= 4 (Fclkout < Mclk/4)
11: -- (unsigned)

TSSTATUS Merger-hardware stream status

7	6	5	4	3	2	1	0
TSFIFO_LINEOK	TSFIFO_ERROR	RESERVED					DIL_READY
R	R	R					R

Address: 0xF581

Type: R

Reset: Undefined

Description: Merger-hardware stream status

[7] **TSFIFO_LINEOK**: inverse of the ERROR signal:
1: the ERROR signal is currently at 0
-> no packets with errors at the moment
-> line OK (unsigned)

[6] **TSFIFO_ERROR**: stored value of the ERROR signal
1: a packet in error has passed since the last I2C reading of TSSTATUS.
Automatically reset to 0 after an I2C read (read put to 0 on a read,unsigned)

[0] **DIL_READY**: 1: the output FIFO contains data
0: it is empty or does not contain enough data (unsigned)

TSSTATUS2 Additional status of merger-hardware stream

7	6	5	4	3	2	1	0
TSFIFO_DEMODSEL	TSFIFOSPEED_STORE	DILXX_RESET	RESERVED			SCRAMBDETECT	RESERVED
R/W	R	R/W	R			R/W	R

Address: 0xF582

Type: R/WH

Reset: Undefined

Description: Additional status of merger-hardware stream

[7] **TSFIFO_DEMODSEL**: signal source:
1: Reserved
0: demodulator 1 (unsigned)

[6] **TSFIFOSPEED_STORE**: 1: a CLKOUT speed change event (TSSPEED.tsfifo_outspeed) has occurred.
Reset to 0 by an I2C write (read put to 0 on a read,unsigned)

[5] **DILXX_RESET**: 1: a FIFO or deinterleaver DVB-S1 reset has occurred. There was a break in the data flow.
Reset to 0 by an I2C write (read put to 0 on a write,unsigned)

[1] **SCRAMBDETECT**: in DVB-S1 only
1: detection (stable) of inverse synchro word, indicating the presence of DVB-S1 scrambling. (unsigned)

TSBITRATEx Observation of raw bit rate

7	6	5	4	3	2	1	0
TSBITRATE1	TSFIFO_BITRATE[15:8]						
TSBITRATE0	TSFIFO_BITRATE[7:0]						
	R/W						

Address: 0xF584 - x * 0x1 (x=0 to 1)

Type: R/W

Reset: Undefined

Description: Observation of raw bit rate

[7:0] **TSFIFO_BITRATE**: Bit rate = Mclk * tsfifo_bitrate / 16384
It is possible to write in this register to reinitialize the bit rate calculation. (unsigned)

ERRCTRLx Configuration of error counter x

	7	6	5	4	3	2	1	0
ERRCTRL1	ERR_SOURCE1				RESERVED	NUM_EVENT1		
ERRCTRL2	ERR_SOURCE2				RESERVED	NUM_EVENT2		
	R/W				R	R/W		

Address: 0xF598 + (x-1) * 0x4 (x=1 to 2)

Type: R/W

Reset: 0x35, 0xC1

Description: Configuration of error counter x

ERRCTRL1: [7:4] **ERR_SOURCE1**: measurement unit (byte, packet, frame..), decimal point location, measurement point by mode (S1 or S2)
example: for option 0000, measurement unit is in bytes, the measurement value = Reg_value/ 2^19 and this option measures DVB-S1 demod errors only.

0000: byte 19 Demod bit errors (S1)
0001: frame 7 ldpc_errnbr (S2), LDPC errors
frame 15 regerr (S1), Viterbi errors
0010: frame 19 bch_errnbr (S2), BCH errors
byte 23 Viterbi (ReedSolo) bit error (S1)
0011: frame 23 bch_error_flag (S2)
packet 23 Viterbi (ReedSolo) byte error (S1)
0100: Mck / 4K 23 Frame Rate LDPC
0101: frame 23 bbheader_error (S2)
byte 23 Viterbi (ReedSolo) bit error ~BER (S1)
0110: packet 23 CRC-8 packet (S2)
byte 23 Viterbi (ReedSolo) byte error ~BER (S1)
0111: byte 23 Viterbi (ReedSolo) bit error BER (S1)
1000: byte 23 Viterbi (ReedSolo) byte error BER (S1)
1001: packet 23 Viterbi (ReedSolo) packet error (S1)
1010: packet 19 Viterbi (ReedSolo) packet error nbr (S1)
1011: frame 23 bad_dfl+syncd_up_dfl (S2)
1100: packet 23 TS error count, packet error final
1101: Mck/4K 7 TS FIFO
1110: frame 7 DFL
1111: Mck/512 23 Packet Rate

Notes:
- (S2): only in DVB-S2; (S1): only in DVB-S1/Legacy DTV
-errcpt_size: counting unit
-byte: bytes
-packet: packets
-frame: frames
-Mck/512: Master clock/512
-Mck/4K: Master clock/4096 (unsigned) (unsigned)

ERRCTRL1: [2:0] **NUM_EVENT1**: time constant
000: count mode (WITH reset of counter upon reading)
001: count mode (WITHOUT reset of counter upon reading)
The reset to 0 is achieved by writing (any value)
in any of the 3 bytes of ERRCNT12/11/10.
byte packet frame
010: 2^14 2^8 2^4
011: 2^16 2^10 2^6 | rate modes
100: 2^18 2^12 2^8 |
101: 2^20 2^14 2^10 |
110: 2^22 2^16 2^12 /
111: ---- average mode --- (unsigned)

ERRCTRL2: [7:4] **ERR_SOURCE2**: measuring point (unsigned)

ERRCTRL2: [2:0] **NUM_EVENT2**: time constant (unsigned)

ERRCNTx Result of error counter 2

	7	6	5	4	3	2	1	0
ERRCNT12	ERRCNT1_OLDVALUE				ERR_CNT1[22:16]			
	R				R/W			

	7	6	5	4	3	2	1	0
ERRCNT11	ERR_CNT1[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
ERRCNT10	ERR_CNT1[7:0]							
	R/W							

Address: 0xF59B - (x-10) * 0x1 (x=10 to 12)

Type: R/WH

Reset: Undefined

Description: Result of error counter 2

ERRCNT12: [7] **ERRCNT1_OLDVALUE**: validity of the information read
1: this value is old and has already been read by I2C. Do not use it.
0: new value (read put to 0 on a read,unsigned)

ERRCNT12: [6:0]

ERRCNT11: [7:0] **ERR_CNT1**: result of counting (read put to 0 on a write,unsigned)

ERRCNT10: [7:0]

ERRCNT22 Result of error counter 2

7	6	5	4	3	2	1	0
ERRCNT2_OLDVALUE				ERR_CNT2[22:16]			
R				R/W			

Address: 0xF59D

Type: R/WH

Reset: Undefined

Description: Result of error counter 2

[7] **ERRCNT2_OLDVALUE**: validity of the information read (read put to 0 on a read,unsigned)

[6:0] **ERR_CNT2**: result of counting (read put to 0 on a write,unsigned)

ERRCNT21 Result of error counter 2

7	6	5	4	3	2	1	0
ERR_CNT2[15:8]							
R/W							

Address: 0xF59E

Type: R/WH

Reset: Undefined

Description: Result of error counter 2

[7:0] **ERR_CNT2**: result of counting (read put to 0 on a write,unsigned)

ERRCNT20 Result of error counter 2

7	6	5	4	3	2	1	0
ERR_CNT2[7:0]							
R/W							

Address: 0xF59F

Type: R/WH

Reset: Undefined

Description: Result of error counter 2

[7:0] **ERR_CNT2**: result of counting (read put to 0 on a write,unsigned)

FECSPY FEC spy configuration

7	6	5	4	3	2	1	0
SPY_ENABLE	RESERVED	SERIAL_MODE	RESERVED	BERMETER_DATAMODE		BERMETER_LMODE	BERMETER_RESET
R/W	R	R/W	R	R/W		R/W	R/W

Address: 0xF5A0

Type: R/W

Reset: 0x88

Description: FEC spy configuration

[7] **SPY_ENABLE**: operational state of the spy
1: functioning
0: stopped/reset
To completely reset the spy, simply write a 0 on this bit. (unsigned)

[5] **SERIAL_MODE**: (read only)
1: serial flow
0: parallel flow (unsigned)

[3:2] **BERMETER_DATAMODE**: bermeter_datamode
0: bit error rate
1: packet error rate (unsigned)

[1] **BERMETER_LMODE**: 1: BER/PER long mode (fbermeter_cpt measured over 2^48 bytes)
0: BER/PER normal mode (fbermeter_cpt measured over 2^40 bytes) (unsigned)

[0] **BERMETER_RESET**: stop/reset of BER/PER only (not of FEC Spy)
1: freeze the BER/PER Meter.
A return to 0 will provoke a reset of the BER/PER meter.
0: the BER/PER is running (if spy_enable=1) (unsigned)

FSPYCFG FEC spy configuration

7	6	5	4	3	2	1	0
FECSPY_INPUT		RST_ON_ERROR	ONE_SHOT	I2C_MODE		SPY_HYSTERESIS	
R/W		R/W	R/W	R/W		R/W	

Address: 0xF5A1

Type: R/W

Reset: 0x2C

Description: FEC spy configuration

[7:6] **FECSPY_INPUT**: measured signal source
00: output of line 1
01: debug, FIFO 1 output or Reed-Solomon decoder line 1 according to TSTTS/tstts_fspybefrs bit (DVB-S1/Legacy DTV only).
10: debug, Viterbi decoder 1 output
11: Return Channel Line output (unsigned)

[5] **RST_ON_ERROR**: impact of an error detection
1: The FEC Spy searches a number of adjoining good packets.
0: The FEC Spy will give the global number of good packets. To obtain a ratio of good packets. (unsigned)

[4] **ONE_SHOT**: 1: stop once the operation is finished. Relaunch the FEC Spy by a positive edge on FECSPY.spy_enable.
0: the FEC Spy continuously restarts the test once finished. (unsigned)

[3:2] **I2C_MODE**: FEC Spy general function mode
00: reserved.
01: reserved.
10: reserved.
11: BER/PER Meter mode. FPACKCNT.fpacket_counter contains the previous result. The output signals represent the previous result. The BER/PER Meter is master of FEC Spy synchro. (unsigned)

[1:0] **SPY_HYSTERESIS**: number of packets measured for each test session
00: a test lasts 255 packets (maximum). FSTATUS/valid_sim=1 after 128 good packets.
01: a test lasts 511 packets (maximum). FSTATUS/valid_sim=1 after 255 good packets.
WARNING: consider saturation on the GOODPACK and PACKCNT registers.
10: a test lasts 63 packets (maximum). FSTATUS/valid_sim=1 after 32 good packets.
11: a test lasts 127 packets (maximum). FSTATUS/valid_sim=1 after 64 good packets.
(unsigned)

FSPYDATA — Tested packet contents

7	6	5	4	3	2	1	0
SPY_STUFFING	RESERVED	SPY_CNULLPKT	SPY_OUTDATA_MODE				
R/W	R	R/W	R/W				

Address: 0xF5A2

Type: R/W

Reset: 0x3A

Description: Tested packet contents

[7] **SPY_STUFFING**: 1: indicate the possible presence of stuffing packets to the FEC Spy. They will be specifically analyzed as stuffing packets.
0: all packets must be analyzed in the same way. (unsigned)

[5] **SPY_CNULLPKT**: presence of Packet Header
1: Null TS Packet mode,
1 synchro word:
DVB: 47
DirecTV: 1D
3 Packet Header bytes:
DVB: 1F,FE/FF,10
DirecTV: A0/20,00/01,04
184 payload bytes for an MPEG packet.
127 payload bytes for a Legacy DTV packet.
0: Non TS Packet mode
1 synchro word
DVB: 47
DirecTV: 1D
187 payload bytes for an MPEG packet.
130 payload bytes for a Legacy DTV packet. (unsigned)

[4:0] **SPY_OUTDATA_MODE**: form and type of data that the spy must expect to confirm:
43.210
00.000: no content verification, simply the form
00.001: Legacy DTV: auto increment, DVB (+others):auto decrement
00.010: auto increment, rising
00.011: auto decrement, falling
00.1xx: Toggling data:
00.100: 55/AA
00.101: 66/99
00.110: C3/3C
00.111: 00/FF
01.xxx: (Pseudo) Constants:
01.000: 00
01.001: 1 byte non null (value 0x01) every 256.
01.010: 55
01.011: 66
01.100: 99
01.101: AA
01.110: Legacy DTV null packet (the official DTV stuffing packet).
01.111: FF (the official MEPG stuffing packet).
1x.xxx: PRBS modes:
10.000 6: X^6 + X^5 + 1 Validated on BER Meter
10.001 7: X^7 + X^6 + 1 Unknown on BER Meter
10.010 9: X^9 + X^5 + 1 Validated on BER Meter
10.011 10: X^10 + X^7 + 1 Unknown on BER Meter
10.100 11: X^11 + X^9 + 1 Validated on BER Meter
10.101 15: X^15 + X^14 + 1 NON Validated on BER Meter
10.110 15: X^15 + X^14 Validated on BER Meter
10.111 17: X^17 + X^14 + 1 Validated on BER Meter
11.000 20: X^20 + X^17 + 1 Validated on BER Meter
11.001 23: X^23 + X^18 + 1 NON Validated on BER Meter
11.010 23: X^23 + X^18 Validated on BER Meter
11.011 31: X^31 + X^28 + 1 Unknown on BER Meter
11.100 41: X^41 + X^3 + 1
11.101 49: X^49 + x^9 + 1
11.110 --
11.111 -- (unsigned)

FSPYOUT FEC spy miscellaneous configuration

7	6	5	4	3	2	1	0
FSPY_DIRECT	RESERVED					STUFF_MODE	
R/W	R					R/W	

Address: 0xF5A3

Type: R/W

Reset: 0x7

Description: FEC spy miscellaneous configuration

[7] **FSPY_DIRECT**: 1: raw output flow test (without the SGNL[1:0] pins). The signaling bytes (if present) may cause test failure.
0: provide the signaling indications to the FEC Spy. The signaling bytes (if present) will be removed from the test. (unsigned)

[2:0] **STUFF_MODE**: payload description of a stuffing packet:
000: 0x00
001: DirecTV:auto increment, DVB (+others): auto decrement
010: (test bus)
011: Legacy DTV null packet (the official DTV stuffing packet).
100: PRBS 11
101: PRBS 15
110: PRBS 23
111: 0xFF (the official MEPG stuffing packet). (unsigned)

FSTATUS FEC spy status

7	6	5	4	3	2	1	0
SPY_ENDSIM	VALID_SIM	FOUND_SIGNAL	DSS_SYNCBYTE	RESULT_STATE			
R	R	R	R	R			

Address: 0xF5A4

Type: R

Reset: Undefined

Description: FEC spy status

[7] **SPY_ENDSIM**: 1: test finished, the number of packets designated by FSPYCFG.spy_hysteresis have been seen. (unsigned)

[6] **VALID_SIM**: 1: test positive, there is the right number of good packets (see FSPYCFG.spy_hysteresis). (unsigned)

[5] **FOUND_SIGNAL**: 1: good packet
0: false packet (unsigned)

[4] **DSS_SYNCBYTE**: 1: detection of Legacy DTV packets (syncbyte = 0x1D) (unsigned)

[3:0] **RESULT_STATE**: status of work in progress
0000: no signal
0001: data correct
0010: warning, packet declared false by the ERROR signal
0011: error, packet false
0100: warning, detection of inverse synchro word DVB-S1
0101: error, bad synchro word
0110: --
0111: error, packet too long
1000: --
1001: warning, packet correct but disconnected from previous
1010: warning, MPEG TEI bit at 1
1011: stuffing packet good
1100: warning, stuffing packet correct but disconnected from previous
1101: error, packet too short
1110: --
1111: -- (unsigned)

FBERCPTx BER/PER meter byte counter

	7	6	5	4	3	2	1	0
FBERCPT4	FBERMETER_CPT[39:32]							
FBERCPT3	FBERMETER_CPT[31:24]							
FBERCPT2	FBERMETER_CPT[23:16]							
FBERCPT1	FBERMETER_CPT[15:8]							
FBERCPT0	FBERMETER_CPT[7:0]							
	R/W							

Address: 0xF5AC - x * 0x1 (x=0 to 4)

Type: R/WH

Reset: Undefined

Description: BER/PER meter byte counter

[7:0] **FBERMETER_CPT**: BYTE counter or total packets
FECSPY.bermeter_lmode = 1 -> multiply the counting by 256: this therefore becomes a 48-bit counter, of which the 8 LSBs are not visible. Ensure that the value in fbermeter_cpt is big enough (and so waits long enough) so that the resulting imprecision becomes negligible. (read put to 0 on a write,unsigned)

FBERERRx BER/PER meter error bit counter

	7	6	5	4	3	2	1	0
FBERERR2	FBERMETER_ERR[23:16]							
FBERERR1	FBERMETER_ERR[15:8]							
FBERERR0	FBERMETER_ERR[7:0]							
	R/W							

Address: 0xF5AF - x * 0x1 (x=0 to 2)

Type: R/WH

Reset: Undefined

Description: BER/PER meter error bit counter

[7:0] **FBERMETER_ERR**: counter of BITs or packets in error
fbermeter_err is not affected by FECSPY/bermeter_lmode.
Important note:
Regardless of mode, fbermeter_cpt and fbermeter_err are read in coherence: reading register FBERCPT4 provokes a sampling of fbermeter_cpt and fbermeter_err in the register buffers. It is those register buffers that will be read as long as a new reading of the FBERCPT4 register has not been made.
In rate mode (FSPYBER/fspyber_ctime different from 000 and 001), if a new measuring result arrives while a read is in progress (ie: FBERCPT4 has been read, but FBERERR0 has not yet been read), it will be lost.
Writing in any of the FBERCPT4..FBERCPT0 or FBERERR2..FBERERR0 registers at any time resets fbermeter_cpt and fbermeter_err to 0 (reset). This also resets FSPYOBS7..0 (the FEC Spy observer, see below). (read put to 0 on a write,unsigned)

FSPYBER BER/PER meter configuration

7	6	5	4	3	2	1	0
RESERVED			FSPYBER_SYNCBYTE	FSPYBER_UNSYNC	FSPYBER_CTIME		
R			R/W	R/W	R/W		

Address: 0xF5B2

Type: R/W

Reset: 0x11

Description: BER/PER meter configuration

[4] **FSPYBER_SYNCBYTE**: 1: reset of BER/PER Meter if error on synchro word and if result_state = 0x7 or 0xD (that is, packet too short or too long). (unsigned)

[3] **FSPYBER_UNSYNC**: 1: reset of BER/PER Meter if desynchronization
0: no reset, wait for it to come back by itself (unsigned)

[2:0] **FSPYBER_CTIME**: BER/PER measuring time
000: counting the error bits or packets to infinity
001: reserved
010: measure on 2^16 bytes 2^9 packets
011: measure on 2^18 bytes 2^11 packets
100: measure on 2^20 bytes 2^13 packets
101: measure on 2^22 bytes 2^15 packets
110: measure on 2^34 bytes 2^17 packets
111: measure on 2^26 bytes 2^19 packets
The FECSPY.bermeter_lmode = 1 mode adds 8 to the exponent. (unsigned)

TSGENERAL General configuration of the stream merger hardware

7	6	5	4	3	2	1	0
RESERVED				MUXSTREAM_OUTMODE	TSFIFO_PERMPARAL		RESERVED
R				R/W	R/W		R

Address: 0xF630

Type: R/W

Reset: 0x40

Description: General configuration of the stream merger hardware

[3] **MUXSTREAM_OUTMODE**: 1: the lines 1, 2 and RC ore connected to the transport steams according to tsfifo_permparal.
0: the outputs are routed as follows
Line 1 -> TS3
Line 2 -> TS2
RC line -> TS1 (unsigned)

[2:1] **TSFIFO_PERMPARAL**: parallel bus allocation=.
00 Line1 -> TS3, Line 2 -> TS2, RC Line -> TS1
01 Line1 -> TS2, Line 2 -> TS3, RC Line -> TS1
10 Line1 -> TS1, Line 2 -> TS2, RC Line -> TS3
11 Line1 -> TS3, Line 2 -> TS2, Parallel bits D63..D03 common (Muxmode). (unsigned)

17.9 SFEC register descriptions

SFECSTATUS — Viterbi Super FEC Status

7	6	5 4	3	2	1	0
SFEC_ON	SFEC_OFF	RESERVED	LOCKEDSFEC	SFEC_DELOCK	SFEC_DEMODSEL	SFEC_OVFON
R/W	R/W	R	R/W	R/W	R/W	R

Address: 0xF5C3

Type: R/WH

Reset: Undefined

Description: Viterbi Super FEC Status

[7] **SFEC_ON**: (unsigned)

[6] **SFEC_OFF**: (read put to 0 on a write,unsigned)

[3] **LOCKEDSFEC**: (unsigned)

[2] **SFEC_DELOCK**: (read put to 0 on a write,unsigned)

[1] **SFEC_DEMODSEL**: (unsigned)

[0] **SFEC_OVFON**: (read put to 0 on a read,unsigned)

SFKDIV12 — Super FEC K divider 12

7	6 5 4 3 2 1 0
SFECKDIV12_MAN	RESERVED
R/W	R

Address: 0xF5C4

Type: R/W

Reset: 0x1F

Description: Super FEC K divider 12

[7] **SFECKDIV12_MAN**: (unsigned)

SFKDIV23 Super FEC K divider 23

7	6	5	4	3	2	1	0
SFECKDIV23_MAN	RESERVED						
R/W	R						

Address: 0xF5C5

Type: R/W

Reset: 0x22

Description: Super FEC K divider 23

[7] **SFECKDIV23_MAN**: (unsigned)

SFKDIV34 Super FEC K divider 34

7	6	5	4	3	2	1	0
SFECKDIV34_MAN	RESERVED						
R/W	R						

Address: 0xF5C6

Type: R/W

Reset: 0x24

Description: Super FEC K divider 34

[7] **SFECKDIV34_MAN**: (unsigned)

SFKDIV56 Super FEC K divider 56

7	6	5	4	3	2	1	0
SFECKDIV56_MAN	RESERVED						
R/W	R						

Address: 0xF5C7

Type: R/W

Reset: 0x24

Description: Super FEC K divider 56

[7] **SFECKDIV56_MAN**: (unsigned)

SFKDIV67 Super FEC K divider 67

7	6	5	4	3	2	1	0
SFECKDIV67_MAN	RESERVED						
R/W	R						

Address: 0xF5C8

Type: R/W

Reset: 0x29

Description: Super FEC K divider 67

[7] **SFECKDIV67_MAN**: (unsigned)

SFKDIV78 Super FEC K divider 78

7	6	5	4	3	2	1	0
SFECKDIV78_MAN	RESERVED						
R/W	R						

Address: 0xF5C9

Type: R/W

Reset: 0x2C

Description: Super FEC K divider 78

[7] **SFECKDIV78_MAN**: (unsigned)

SFSTATUS Super FEC status (delay line)

7	6	5	4	3	2	1	0
SFEC_LINEOK	SFEC_ERROR	SFEC_DATA7	SFEC_PKTDNBRFAIL	TSSFEC_DEMODSEL	SFEC_NOSYNC	SFEC_UNREGULA	SFEC_READY
R	R	R	R/W	R	R/W	R	R

Address: 0xF5CC

Type: R

Reset: Undefined

Description: Super FEC status (delay line)

[7] **SFEC_LINEOK**: invert of the ERROR signal (unsigned)

[6] **SFEC_ERROR**: ERROR signal memoization (read put to 0 on a read,unsigned)

[5] **SFEC_DATA7**: DATA7 signal image. (unsigned)

[4] **SFEC_PKTDNBRFAIL**: (read put to 0 on a write,unsigned)

[3] **TSSFEC_DEMODSEL**: (unsigned)

[2] **SFEC_NOSYNC**: (read put to 0 on a write,unsigned)

[1] **SFEC_UNREGULA**: (read put to 0 on a read,unsigned)

[0] **SFEC_READY**: (unsigned)

SFERRCTRL Configuration of the Super FEC error counter

7	6	5	4	3	2	1	0
SFEC_ERR_SOURCE				RESERVED	SFEC_NUM_EVENT		
R/W				R	R/W		

Address: 0xF5D8

Type: R/W

Reset: 0x94

Description: Configuration of the Super FEC error counter

[7:4] **SFEC_ERR_SOURCE**: measure point (unsigned)

[2:0] **SFEC_NUM_EVENT**: timebase (unsigned)

SFERRCNTx Super FEC error counter value

	7	6	5	4	3	2	1	0
SFERRCNT2	SFERRC_OLDVALUE				SFEC_ERR_CNT[22:16]			
	R	R/W						

	7	6	5	4	3	2	1	0
SFERRCNT1	SFEC_ERR_CNT[15:8]							
	R/W							

	7	6	5	4	3	2	1	0
SFERRCNT0	SFEC_ERR_CNT[7:0]							
	R/W							

Address: 0xF5DB - x * 0x1 (x=0 to 2)

Type: R/WH

Reset: Undefined

Description: Super FEC error counter value

SFERRCNT2: [7] **SFERRC_OLDVALUE**: (read put to 0 on a read,unsigned)

SFERRCNT2: [6:0]
SFERRCNT1: [7:0] **SFEC_ERR_CNT**: (read put to 0 on a write,unsigned)
SFERRCNT0: [7:0]

17.10 DISEQC register descriptions

DISIRQCFG DiSEqC interrupt enable register

7	6	5	4	3	2	1	0
RESERVED	ENRXEND	ENRXFIFO8B	ENTRFINISH	ENTIMEOUT	ENTXEND	ENTXFIFO64B	ENGAPBURST
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 0xF700

Type: R/W

Reset: 0x0

Description: DiSEqC interrupt enable register

[6] **ENRXEND**: 1: enable IRQRXEND interrupt (unsigned)

[5] **ENRXFIFO8B**: 1: enable IRQRXFIFO8B interrupt (unsigned)

[4] **ENTRFINISH**: 1: enable IRQTRFINISH interrupt (unsigned)

[3] **ENTIMEOUT**: 1: enable IRQTIMEOUT interrupt (unsigned)

[2] **ENTXEND**: 1: enable IRQTXEND interrupt (unsigned)

[1] **ENTXFIFO64B**: 1: enable IRQFIFO64B interrupt (unsigned)

[0] **ENGAPBURST**: 1: enable IRQGAPBURST interrupt (unsigned)

DISIRQSTAT DiSEqC interrupt status register

7	6	5	4	3	2	1	0
RESERVED	IRQRXEND	IRQRXFIFO8B	IRQTRFINISH	IRQTIMEOUT	IRQTXEND	IRQTXFIFO64B	IRQGAPBURST
R	R	R	R	R	R	R	R

Address: 0xF701

Type: R

Reset: Undefined

Description: DiSEqC interrupt status register

[6] **IRQRXEND**: 1: interrupt generated when Rx finished (unsigned)

[5] **IRQRXFIFO8B**: 1: interrupt generated if Rx FIFO has already 8 bytes (half full). (unsigned)

[4] **IRQTRFINISH**: 1: interrupt generated when the transaction TX + possibly RX is finished (unsigned)

[3] **IRQTIMEOUT**: 1: interrupt generated if DiSEqC Rx receives no response after end of Tx plus DISTXTIMEO delay. (unsigned)

[2] **IRQTXEND**: 1: interrupt generated when Tx finished (unsigned)

[1] **IRQTXFIFO64B**: 1: interrupt generated if Tx FIFO has space for 64 more bytes (half full). (unsigned)

[0] **IRQGAPBURST**: 1: interrupt generated at end of gap burst (unsigned)

DISTXCFG DiSEqC Transmitter Control

7	6	5	4	3	2	1	0
DISTX_RESET	TIM_OFF	TIM_CMD		ENVELOP	DIS_PRECHARGE	DISEQC_MODE	
R/W	R/W	R/W		R/W	R/W	R/W	

Address: 0xF702

Type: R/W

Reset: 0x0

Description: DiSEqC Transmitter Control

[7] **DISTX_RESET**: 1: FIFO content is cleared (unsigned)

[6] **TIM_OFF**: 1: time offset enabled
0: time offset disabled (unsigned)

[5:4] **TIM_CMD**: timer control.
00: Tim = 15 ms at f22 = 22 kHz
01: Tim = 20 ms at f22 = 22 kHz
10: Tim = 25 ms at f22 = 22 kHz
11: Tim = 30 ms at f22 = 22 kHz (unsigned)

[3] **ENVELOP**: 1:envelop mode is selected (unsigned)

[2] **DIS_PRECHARGE**: 1:FIFO precharge disabled (unsigned)

[1:0] **DISEQC_MODE**: DiSEqC transmission configuration
00: continuous (22 kHz) tone
01: reserved
10: DiSEqC 2/3
11: DiSEqC 3/3 (unsigned)

DISTXSTATUS DiSEqC Transmitter Status

7	6	5	4	3	2	1	0
RESERVED	TX_FIFO_FULL	TX_IDLE	GAP_BURST	TX_FIFO64B	TX_END	TR_TIMEOUT	TR_FINISH
R	R	R	R	R	R	R	R

Address: 0xF703

Type: R

Reset: Undefined

Description: DiSEqC Transmitter Status

[6] **TX_FIFO_FULL**: 1: Tx FIFO is full (unsigned)

[5] **TX_IDLE**: 1: Tx FIFO is empty (unsigned)

[4] **GAP_BURST**: 1: Tx gap (as programmed in DiSEqC.tim_cmd) has not yet expired (unsigned)

[3] **TX_FIFO64B**: 1: the Tx FIFO has now less than 64 bytes into it (unsigned)

[2] **TX_END**: 1: the transmission is done (unsigned)

[1] **TR_TIMEOUT**: 1: The transaction timeout is over (unsigned)

[0] **TR_FINISH**: 1: The transaction is finished (unsigned)

DISTXBYTES DiSEqC Tx Number of bytes in FIFO

7	6	5	4	3	2	1	0
TXFIFO_BYTES							
R							

Address: 0xF704

Type: R

Reset: Undefined

Description: DiSEqC Tx Number of bytes in FIFO

[7:0] **TXFIFO_BYTES**: number of bytes in Tx FIFO (waiting to be transmitted) (unsigned)

DISTXFIFO DiSEqC Transmitter FIFO

7	6	5	4	3	2	1	0
DISEQC_TX_FIFO							
R/W							

Address: 0xF705

Type: R/W

Reset: 0x0

Description: DiSEqC Transmitter FIFO

[7:0] **DISEQC_TX_FIFO**: DiSEqC transmitter FIFO. 128 bytes deep. (unsigned)

DISTXF22 DiSEqC 22 kHz Transmitter Frequency Tone Control

7	6	5	4	3	2	1	0
F22TX							
R/W							

Address: 0xF706

Type: R/W

Reset: 0xC0

Description: DiSEqC 22 kHz Transmitter Frequency Tone Control

[7:0] **F22TX**: Tone modulation frequency control.
F22TX = MClk/FDiSEqC / 32.
For 22 kHz operation and M_CLK = 135 MHz, F22TX = 192 or 0xC0. (unsigned)

DISTIMEOCFG DiSEqC Interrupt Timer Configuration

7	6	5	4	3	2	1	0
RESERVED					RXCHOICE		TIMEOUT_OFF
R					R/W		R/W

Address: 0xF708

Type: R/W

Reset: 0x2

Description: DiSEqC Interrupt Timer Configuration

[2:1] **RXCHOICE**: Conditions for IRQTIMEOUT response
00: no rxactive within timeout period
01: no rxdetect within timeout period
10: no rxend within timeout period
11: reserved
The timeout period is configured by DISTIMEOUT (unsigned)

[0] **TIMEOUT_OFF**: 1: switch off the reply timeout (unsigned)

DISTIMEOUT DiSEqC Interrupt Timer

7	6	5	4	3	2	1	0
TIMEOUT_COUNT							
R/W							

Address: 0xF709

Type: R/W

Reset: 0x8C

Description: DiSEqC Interrupt Timer

[7:0] **TIMEOUT_COUNT**: IRQ timer duration for Rx response after Tx.
Timeout_count in number of periods of diseqc tx bit.
So, it can be configurable from 0ms to 255*33*f22tx = 382.5ms at 22khz with a step of 1.5ms.
(unsigned)

DISRXCFG DiSEqC Receiver Control

7	6	5	4	3	2	1	0
RESERVED	EXTENVELOP	PINSELECT			IGNORE_SHORT22K	SIGNED_RXIN	DISRX_ON
R	R/W	R/W			R/W	R/W	R/W

Address: 0xF70A

Type: R/W

Reset: 0x4

Description: DiSEqC Receiver Control

[6] **EXTENVELOP**: 0: receives the 22KHz tone from the analog pin
1: DiSEqC Rx expects a digital 1 or 0 representing the envelope of the tone of the selected GPIO via pin_select (unsigned)

[5:3] **PINSELECT**: Select DiSEqC input pin and polarity in envelope mode (if extenvelop = 1).
000: GPIO0
001: /GPIO0
010: GPIO1
011: /GPIO1
100: GPIO2
101: /GPIO2
110: --
111: -- (unsigned)

[2] **IGNORE_SHORT22K**: 1: ignore short glitch when detecting a 22Khz signal (unsigned)

[1] **SIGNED_RXIN**: The Rx data in from the ADC is
1: signed (from -512 to 511)
0: unsigned (from 0 to 1023) (unsigned)

[0] **DISRX_ON**: 0: Disable the DiSEqC Receiver. FIFO content is cleared.
1: Enable the DiSEqC Receiver (unsigned)

DISRXSTATx DiSEqC Receiver Status

	7	6	5	4	3	2	1	0
DISRXSTAT1	RXEND	RXACTIVE	RXDETECT	CONTTONE	8BFIFOREADY	FIFOEMPTY	RESERVED	
DISRXSTAT0	RXFAIL	FIFOPFAIL	RXNONBYTE	FIFOOVF	SHORT22K	RXMSGLOST	RESERVED	
	R	R	R	R	R	R	R	

Address: 0xF70C - x * 0x1 (x=0 to 1)

Type: R

Reset: 0x0

Description: DiSEqC Receiver Status

DISRXSTAT1: [7] **RXEND**: 1: reception is ended (unsigned)

DISRXSTAT1: [6] **RXACTIVE**: 1: receiver is active (there is some activity detected on the DiSEqC line and the decoding is on-going) (unsigned)

DISRXSTAT1: [5] **RXDETECT**: 1: A well-formed bit has been detected (unsigned)

DISRXSTAT1: [4] **CONTTONE**: 1: more than 33 pulse-widths of tone burst have been detected (continuous tone present) (unsigned)

DISRXSTAT1: [3] **8BFIFOREADY**: 1: there 8 or more bytes in the FIFO ready for reading (unsigned)

DISRXSTAT1: [2] **FIFOEMPTY**: 1: the FIFO is empty (unsigned)

DISRXSTAT0: [7] **RXFAIL**: 1: reception problem (short 22 kHz or continuous tone sequence) (unsigned)

DISRXSTAT0: [6] **FIFOPFAIL**: 1: transmission error. The parity checks fail (unsigned)

DISRXSTAT0: [5] **RXNONBYTE**: 1: transmission error. The number of received bits does not correspond to a full data byte (8 bits + parity). (unsigned)

DISRXSTAT0: [4] **FIFOOVF**: 1: DiSEqC receiver FIFO overflow. More than 16 bytes are waiting (unsigned)

DISRXSTAT0: [3] **SHORT22K**: 1: A short signal at 22KHz has been detected (less than the length programmed in DISRXSHORT22K). (unsigned)

DISRXSTAT0: [2] **RXMSGLOST**: 1: A message in the FIFO has been lost when receiving the previous one. Maybe the FIFO wasn't cleared before starting the reception or something went wrong. (unsigned)

DISRXBYTES — DiSEqC Rx Number of bytes in FIFO

7	6	5	4	3	2	1	0
RESERVED			RXFIFO_BYTES				
R			R				

Address: 0xF70D

Type: R

Reset: Undefined

Description: DiSEqC Rx Number of bytes in FIFO

[4:0] **RXFIFO_BYTES**: number of bytes contained in the DiSEqC receiver FIFO (unsigned)

DISRXPARITYx — DiSEqC Receiver Parity Bytes

	7	6	5	4	3	2	1	0
DISRXPARITY1	DISRX_PARITY[15:8]							
DISRXPARITY0	DISRX_PARITY[7:0]							
	R							

Address: 0xF70F - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: DiSEqC Receiver Parity Bytes

[7:0] **DISRX_PARITY**: Parity Bytes : each bit is the parity of the corresponding byte in the RX FIFO (unsigned)

DISRXFIFO — DiSEqC Receiver FIFO

7	6	5	4	3	2	1	0
DISEQC_RX_FIFO							
R/W							

Address: 0xF710

Type: R/W

Reset: 0x0

Description: DiSEqC Receiver FIFO

[7:0] **DISEQC_RX_FIFO**: DiSEqC receiver FIFO, 16 bytes deep. (unsigned)

DISRXDCx DiSEqC Rx DC Value observation

	7	6	5	4	3	2	1	0
DISRXDC1	RESERVED						DC_VALUE[9:8]	
	R						R	

	7	6	5	4	3	2	1	0
DISRXDC0	DC_VALUE[7:0]							
	R							

Address: 0xF712 - x * 0x1 (x=0 to 1)

Type: R

Reset: Undefined

Description: DiSEqC Rx DC Value observation

DISRXDC1: [1:0]
DISRXDC0: [7:0] **DC_VALUE**: DC Value of the signal at the DiSEqC input pin. May be used to measure the LNB DC value (signed)

DISRXF221 DiSEqC 22 kHz Receiver Frequency Tone Control

7	6	5	4	3	2	1	0
RESERVED				F22RX[11:8]			
R				R/W			

Address: 0xF714

Type: R/W

Reset: 0x1

Description: DiSEqC 22 kHz Receiver Frequency Tone Control

[3:0] **F22RX**: 22KHz frequency for the receiver.
Defined on 12bits from the AD frequency by F22RX = (22000/CkAD) * 2^14 (unsigned)

DISRXF220 DiSEqC 22 kHz Receiver Frequency Tone Control

7	6	5	4	3	2	1	0
F22RX[7:0]							
R/W							

Address: 0xF715

Type: R/W

Reset: 0x2B

Description: DiSEqC 22 kHz Receiver Frequency Tone Control

[7:0] **F22RX**: 22KHz frequency for the receiver.
Defined on 12bits from the AD frequency by F22RX = (22000/CkAD) * 2^14 (unsigned)

DISRXF100 DiSEqC Rx 100 kHz Frequency Control

7	6	5	4	3	2	1	0
F100RX							
R/W							

Address: 0xF716

Type: R/W

Reset: 0xA9

Description: DiSEqC Rx 100 kHz Frequency Control

[7:0] **F100RX**: 100KHz frequency for the receiver.
Defined on 8bits from the MClk frequency by F100RX = MClk/100000 / 8. (unsigned)

DISRXSHORT22K DiSEqC Rx Short22k length

7	6	5	4	3	2	1	0
RESERVED				SHORT22K_LENGTH			
R				R/W			

Address: 0xF71C

Type: R/W

Reset: 0xF

Description: DiSEqC Rx Short22k length

[4:0] **SHORT22K_LENGTH**: short22k length in 10us steps (unsigned)

ACRPRESC Auxiliary clock control

7	6	5	4	3	2	1	0
RESERVED					ACR_PRESC		
R					R/W		

Address: 0xF71E

Type: R/W

Reset: 0x1

Description: Auxiliary clock control

[2:0] **ACR_PRESC**: Auxiliary clock prescaler
000: reserved
001: prescaler divided by 2
010: prescaler divided by 16
011: prescaler divided by 128
100: prescaler divided by 1024
101: prescaler divided by 8192
110: prescaler divided by 65536
111: prescaler divided by 524288 (unsigned)

ACRDIV Auxiliary clock division control

7	6	5	4	3	2	1	0
ACR_DIV							
R/W							

Address: 0xF71F

Type: R/W

Reset: 0x14

Description: Auxiliary clock division control

[7:0] **ACR_DIV**: Auxiliary clock division
Faux = MCLK/(acr_div x acr_presc), MCLK = 270 MHz
The obtained signal is square wave,
with 0 = divided by 256 (unsigned)

17.11 TST register descriptions

TCTL4 Test of demodulator Carrier loop

7	6	5	4	3	2	1	0
CFR2TOCFR1_DVBS1		RESERVED					
R/W		R					

Address: 0xFF48

Type: R/W

Reset: 0x0

Description: Test of demodulator Carrier loop

[7:6] **CFR2TOCFR1_DVBS1**: These bits control how the value in CFR2 is transferred by small increments to CFR1 in DVB-S1/Legacy DTV mode:
00: stop Carrier loop 2 in DVB-S1/Legacy DTV mode.
01: accelerated carrier loop 2 operation during start-up to improve locktime (DSTATUS/car_lock=1). As soon as DSTATUS/car_lock=1, the value in carrier 2 is transferred to carrier 1 in increments of 2^-16 symbols until CFR2 is within +-1/1024 of a symbol. After which this loop is stopped (for ever).
10: Continuous transfer of CFR2->CFR1.
11:Continuous transfer ofCFR2->CFR1 as soon as |CFR2| exceeds1/1024th of a symbol. (unsigned)

18 Revision history

Table 44. Document revision history

Date	Revision	Changes
23-Feb-2012	1	Initial release.

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