STV2001

I²C SINGLE FREQUENCY DEFLECTION PROCESSOR AND 120 MHz RGB PREAMPLIFIER

TARGET SPECIFICATION

FEATURES

Horizontal deflection

- Single Frequency, Self Adaptive Oscillator.
- TTL compatible positive going sync.
- Chip does not accept sync on RGB or any video signal.
- I²C controlled: H-position, pin cushion, keystone, parallelogram, side pin balance.
- I²C controlled EW corner : top and bottom corrections.
- I²C controlled corner: top and bottom phase corrections.
- EW output
- I²C controlled H-amplitude
- DC controlled H-width breathing compensation with I²C controlled gain (0.5x to 2x).
- Xray shut-down on ABL, H output latch, reset by power OFF/ON.
- Soft start on H-duty.

Vertical deflection

- Vertical ramp generator.
- Wide range AGC loop.
- TTL compatible positive going sync, no extra pulses.
- I²C controlled vertical position.
- I²C controlled S linearity correction.
- DC controlled height breathing compensation with I²C controlled gain (0.5X TO 2X).
- Vertical dynamic focus output with fixed amplitude (1Vpp).

Video preamplifier

- 3-Channel 120MHz bandwidth video amplifier.
- 3.5ns typical rise and fall time at $2.5V_{PP}$.
- I²C controlled individual RGB contrast (8bit)>8db
- I²C controlled overall brightness.
- Activation of ABL results in contrast gain decrease.
- Gain window (1.5X) controlled by input pulse and I²C. Pulse height controls the gain variation from 1x to 1.5x.
- 0.514V typical video input signal for normal display.
- I²C controlled contrast (7bits) update during vertical retrace time.

I²C main features

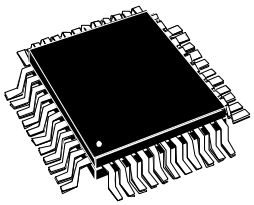
- I²C interface (slave) 100kHz max.
- All I²C controlled DAC are 7 bits, except RGB gain.
- Power on reset on 5 V (V_{DD}).

Supply voltage & power

- 5 V/10.5 V dual supply.
- Max power consumption: 1.2W

DESCRIPTION

The STV2001 is an I²C-controlled monolithic integrated circuit assembled in a TQFP44 plastic package. It combines both a deflection block (horizontal and vertical, single frequency with very powerful geometry correction) and a 120MHz RGB pre-amplifier.



TQFP44/SLUG DOWN

ORDER CODE :

Version 1.2

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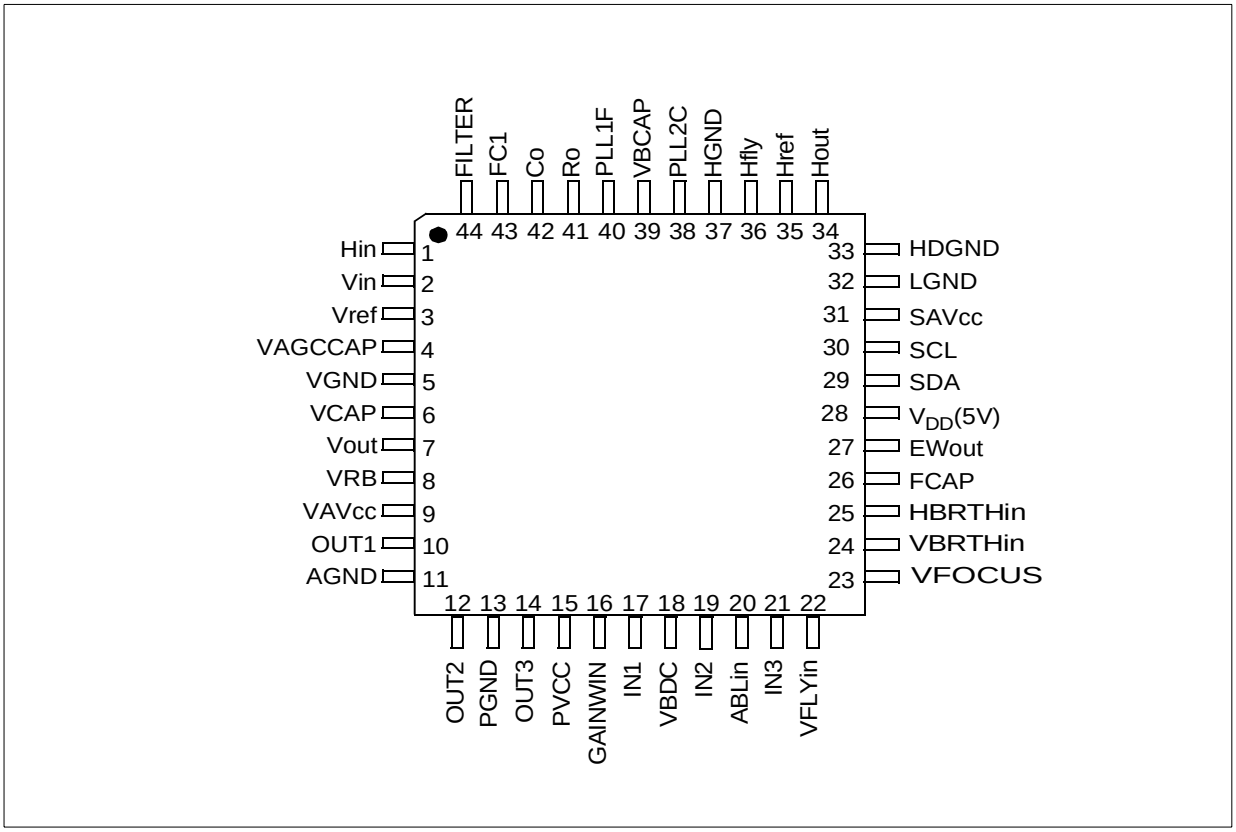
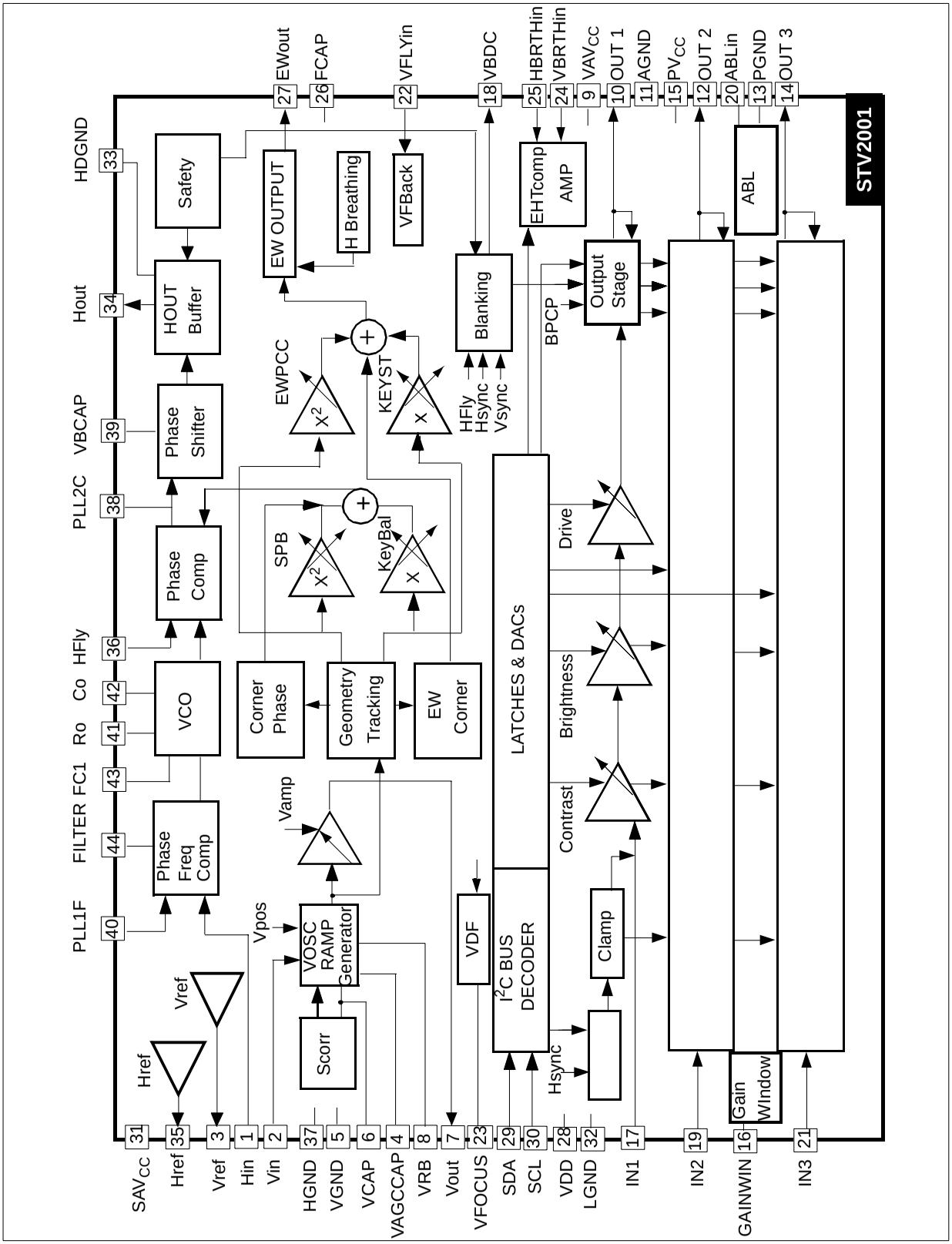
1 - PIN CONNECTIONS



2 - PIN DESCRIPTION

Pin	Name	Function
1	Hin	Horizontal Sync Input
2	Vin	Vertical Sync Input
3	Vref	Vertical Section Reference Voltage
4	VAGCCAP	Vertical AGC Loop Capacitor
5	VGND	Vertical Section Ground
6	VCAP	Vertical Sawtooth Generator Capacitor
7	Vout	Vertical Output
8	VRB	Vertical Ramp Filter
9	VAVcc	Video Section Analog Supply (10.5V typ)
10	OUT1	Video Output 1
11	AGND	Video Analog Ground
12	OUT2	Video Output 2
13	PGND	Video Section Power Ground
14	OUT3	Video Output 3
15	PVcc	Video Section Power Supply (10.5V typ)
16	GAINWIN	Gain Window Input
17	IN1	Video Input 1
18	VBDC	Vertical Blanking Output with DC Level adjusted by DAC
19	IN2	Video Input 2
20	ABLin	Video Automatic Beam Current Compensation Input
21	IN3	Video Input 3
22	VFLYin	Vertical Fly Back Pulse Input
23	VFOCUS	Vertical Dynamic Focus Output
24	VBRTHin	Vertical Breathing DC Input
25	HBRTHin	Horizontal Breathing Compensation DC Input
26	FCAP	Filter Capacitor
27	EWout	EW Output
28	V_{DD}	Bus, Scanning Logic and Video Logic Supply (5V typ)
29	SDA	I^2C Data Input
30	SCL	I^2C Clock Input
31	SAVcc	Scanning Section Analog Supply (10.5Vtyp)
32	LGND	Bus and Scanning Power Ground
33	HDGND	H Driver Output Ground
34	Hout	Horizontal Driver Output, open collector
35	Href	Horizontal Section Reference Voltage
36	Hfly	Horizontal Flyback Input, Positive
37	HGND	Horizontal Section Ground
38	PLL2C	PLL2 Loop Filter
39	VBCAP	PLL2 Top Comparator Filter
40	PLL1F	PLL1 Loop Filter
41	Ro	Horizontal Oscillator Resistor
42	Co	Horizontal Oscillator Capacitor
43	FC1	PLL1 Filter Capacitor
44	FILTER	Horizontal Filter Capacitor (HPOS)

3 - BLOCK DIAGRAM



4 - ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
SAVcc	Scanning Section Analog Supply Voltage	13.5	V
VAVcc	Video Section Analog Supply Voltage	13.5	V
PVcc	Supply Voltage for Video Pre-Amp Section	13.5	V
Vdd	Logic Section Supply Voltage	5.5	V
V_{ESD}	ESD susceptibility HBM model 100pF & 1.5kΩ EIAJ Norm 200pF & 0Ω	2 300	kV V
Tstg	Storage Temperature	-40 to 150	^{o}C
Tj	Junction Temperature	150	^{o}C
Toper	Operating Temperature (Device ambient)	0 to 70	^{o}C

5 - THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-a)}$	Junction to Ambient Thermal Resistance (MAX)	46	^{o}C/W

6 - SYNC INPUT

Operating Conditions (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HSVR	Voltage on Hin		0		5	V
MinD	Min Hin pulse duration		0.7			us
Mduty	Max Hin Duty Cycle				25	%
VSVR	Voltage on Vin		0		5	V
VSW	Min Vin pulse duration		5			us
VSD	Max Vin Duty Cycle				15	%

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

V_{INTH}	Horizontal & Vertical Input Logic Level	Low Level High Level	 2.2		0.8	V V
RIN	Horizontal & Vertical Pull-Up Resistor			200		kΩ

7 - I²C READ/WRITE

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
F_{SCL}	Maximum Clock Frequency				100	kHz
T_{LOW}	Low Period of the SCL Clock		1.3			us
T_{HIGH}	High Period of SCL Clock		0.6			us
V_{INL}	SDA & SCL Input Low Level Voltage				1.5	V
V_{INH}	SDA & SCL Input High Level Voltage		3			V
V_{ACK}	Acknowledge Output Voltage on SDA input with 3mA				0.4	V

8 - HORIZONTAL SECTION

Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCO						
Ro(min)	Minimum Oscillator Resistor		6			kΩ
Co(min)	Minimum Oscillator Capacitor		390			pF
Fmax	Maximum Oscillator Frequency				150	kHz
OUTPUT SECTION						
I_{HFB}	Horizontal FlyBack Input Maximum Current				5	mA
I_{HOUT}	Horizontal Drive Output Maximum Sink Current				15	mA

Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY AND REFERENCE VOLTAGES						
Vcc	Supply Voltage		9.5	10.5	11.5	V
Vdd	Supply Voltage		4.5	5	5.5	V
Icc	Supply Current			30		mA
Idd	Supply Current			5		mA
V_{HREF}	Horizontal Reference Voltage	I=-2mA	7.4	8	8.6	V
VVREF	Vertical Reference Voltage	I=-2mA	7.4	8	8.6	V
I_{HREF}	Horizontal Reference Maximum Source Current				5	mA
I_{VREF}	Vertical Reference Maximum Source Current				5	mA

Operating Conditions

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
1st PLL SECTION						
V_{clamp}	VCO clamp Voltage range	V_{HREF}=8V	3.0		3.8	V
V_{VCO}	VCO clamp Voltage, at POR	V_{HREF}=8V		3.8		V
A_{VCO}	VCO Gain	Ro=4868Ω, Co=820pF, dF/dV=1/11RoCo		23		kHz/V
H_{PHASE}	Horizontal Phase Adjustment Range	% of Horizontal Period		+/-10		%
VPMIN VPTYP VPMAX	Horizontal Phase Setting Minimum Typical Maximum	SubAdd 07 X1111111 X1000000 X0000000		 2.8 3.4 4.0		 V V V
$I_{PLL1-UL}$ $I_{PLL1-L1}$ $I_{PLL1-L2}$	PLL1 Charge Pump Current Unlocked Locked Locked	Sub-Address 11 x1xx xxxx x0xx xxxx		 +/-40 +/-1 ±300		 µA mA µA
f_O	Free Running Frequency, no input at POR, lower clamp voltage at max.	Ro=4868Ω, Co=820pF		86		kHz
dfo/dT	Free Running Frequency Thermal Drift				-150	ppm/^{o}C
2nd PLL SECTION & HORIZONTAL OUTPUT SECTION						
V_{THFB}	Flyback Input Threshold Voltage		0.65	0.75		V
$Jitter_H$	Horizontal Jitter	At 80KHz		70		ppm
H_{DC}	Horizontal Drive Output Duty Cycle (Ratio of Power Transistor OFF time to Period)			55		%
Vphi2	Internal Clamp Level on PLL2 Filter	Low Level High Level		1.6 4.0		V V
VSCinh	Threshold Voltage to Stop H-Out, V-Out, Reset ABL when Vcc<VSCinh			6.9		V
$Vsat_{HD}$	Horizontal Drive Output Saturation Voltage	Iout=15mA			0.4	V

9 - VERTICAL SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Electrical Characteristics (V_{DD} = 5V, T_{amb} = 25°C)						
VERTICAL RAMP SECTION						
V_{RBOT}	Voltage at Ramp Bottom Point	V_{VREF}=8V		2		V
V_{RTOP}	Voltage at Ramp Top Point with Sync	V_{VREF}=8V		5		V
V_{RTOPF}	Voltage at Ramp Top Point without Sync	V_{VREF}=8V		V_{RTOP}-0.1		V
T_{VDIS}	Vertical Sawtooth Discharge Time	C_{OSC}=150nF		70		µs
F_{FRV}	Vertical Free Running Frequency (S correction inhibited)	C_{OSC}=150nF		100		Hz
ASFR	Auto-Sync Frequency Range	C_{OSC}=150nF	50		165	Hz
RAFD	Ramp Amplitude Drift Versus Frequency at Maximum Vertical Amplitude	C_{OSC}=150nF 50Hz - 165Hz		200		ppm/Hz
R_{LIN}	Ramp Linearity at Vcap pin with S Correction inhibited	2.5V < VOSC < 4.5V		0.5		%
V_{POS}	Vertical Position Adjustment Voltage with V_{OUT} mean value	Sub-Add=09 X0000000 X1000000 X1111111	 3.65	 3.2 3.5 3.8	 3.3	 V V V
VOR	Vertical Output Peak to Peak Voltage	Sub-Add=08 10000000 11000000 11111111	 3.5	 2.25 3 3.75	 2.5	 V V V
I_{VOUT}	Vertical Output Maximum Current			+/-5		mA
V_{VRB}	Vertical Ramp Filter Voltage			2		V
dVS	Max Vertical S-Correction Amplitude S-Correction inhibited, DV/Vpp at TV/4 S-correction Maximum, DV/Vpp at 3TV/4	Sub-Add 0A 0XXXXXXX 11111111		 -4 +4		 % %

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
EAST/WEST FUNCTION (available without feedback connection)						
EW_{DC}	DC Output Voltage with: -Typical VPOS and Keystone inhibited -External driver connected as unity gain buffer			2.0		V
$TDEW_{DC}$	DC Output Voltage Thermal Drift (Non-test Parameter)			100		ppm/^{o}C
EW_{PARA}	Parabola Amplitude with: -Max VAMP -Typ VPOS -Keystone inhibited	Sub-add 0C 11111111 11000000 10000000		 1.0 0.5 0		 V V V
EW_{track}	Parabola Amplitude Function of VAMP Control (tracking between VAMP & EW) with: -Typ VPOS=typ. -Keystone=typ. -EW Amplitude=typ.	Sub-address 08 10000000 11000000 11111111		 0.18 0.35 0.57		 V V V
KeyAdj	Keystone Adjustment Capability with: -VPOS=typ. -EW= inhibited -Vertical Amplitude= Max.	Sub-address 0B 10000000 11111111		 0.2 0.2		 V_{pp} V_{pp}
KeyTrack	Intrinsic Keystone Function of VPOS Control (tracking between VPOS and EW) with : -EW Amplitude= Max -Vertical Amplitude=Max A/B Ratio B/A Ratio	Sub-address 09 X0000000 X1111111		 0.52 0.52		
EW Corner Top	Corner Adjustment capability with : -VPS=typ, -EW = inhibited -VAMP = max -HSize = Min -HBreath>VREF -Keystone = inhibited	Sub-address 04 1111 1111 1100 0000 1000 0000		 +1.25 0 -1.25		 Vpp Vpp Vpp
EW Corner Bottom	Corner Adjustment capability with : -VPS=Typ, -EW = inhibited -VAMP = Max -HSize = Min -HBreath>VREF -Keystone = inhibited	Sub-address 15 1111 1111 1100 0000 1000 0000		 +1.25 0 -1.25		 Vpp Vpp Vpp

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
INTERNAL DYNAMIC HORIZONTAL PHASE CONTROL						
SBPpara	Side Pin Balance Parabola Amplitude with: -VAMP=Max, -VPOS=typ. -Parallelogram inhibited	Sub-add 0E 11111111 10000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$
SPBtrack	Side Pin Balance Parabola Amplitude function of VAMP Control (tracking between VAMP & SPB) with -SPB=Max -VPO=typ. -Parallelogram= inhibited	Sub-add 08 10000000 11000000 11111111		 0.5 0.9 1.4		 $\%T_H$ $\%T_H$ $\%T_H$
ParAdj	Parallelogram Adjustment Capability with: -VAMP=Max -POS =Typ -SPB=Max	Sub-add 0F 11111111 10000000		 +1.4 -1.4		 $\%T_H$ $\%T_H$
Partrack	Intrinsic Parallelogram Function of VPOS Control (tracking between VPOS and DHPC) with -VAMP=Max -SPB=Max -Parallelogram= inhibited A/B Ratio B/A Ratio	Sub-add 09 X0000000 X1111111		 0.52 0.52		
VERTICAL BREATHING COMPENSATION						
VBRrng	Input DC Breathing Control Range		1		10.5	V
VSC	Vertical Size Compensation Variation of V output vs full range of VBRrng	Sub-address 14 XX00 0000 X100 0000 XX11 1111		 -5 -20		 % % %
VERTICAL DYNAMIC FOCUS OUTPUT						
VDF_{DC}	DC Output Level RL=10kΩ			4		V
VDFamp	VDF Parabola Amplitude with: Vamp = typ VPOS = typ.			1		Vpp
V_{FOCPOL}	Parabola Polarity at Output = Inverted “U”					
VERTICAL FLYBACK INPUT						
V_{FLYTH}	Vertical Flyback Threshold			1		V
V_{FLYINH}	Inhibition of Vertical Flyback input (id pulse in action instead of VFlyback)		6.5			V
HORIZONTAL SIZE CONTROL						
Hsize	Hsize output DC voltage sitting on top of EWDC=2.0V	sub-add 0D X0000000 X1111111		 0 2.4		 V V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HORIZONTAL BREATHING COMPENSATION						
HBRrng	Breathing input DC Control Range		1		10.5	V
HSC	Horizontal size compensation, EW DC voltage variation under full range of HBRrng	Sub-address 12 X000 0000 X100 0000 X111 1111		0.2 0.8		V V
CORNER PHASE CORRECTION						
Corner Phase Top	Corner Phase Top Adjustment with: Vamp = max Vpos = Typ. SPB = OFF Parrallelogram = OFF	Sub-address 05 1000 0000 1111 1111		 -2.8 +2.8		 % %
Corner Phase Bottom	Corner Phase Bottom Adjustment with: Vamp = max Vpos = Typ. SPB = OFF Parrallelogram = OFF	Sub-address 06 0000 0000 0111 1111		 -2.8 +2.8		 % %

10 - VIDEO PRE-AMP SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DC Electrical Characteristics (VAV_{CC} = PV_{CC} = 10.5V, Tamb = 25°C)						
VAV_{cc}	Video Section Analog Supply Voltage		9.5	10.5	11.5	V
PVcc	Power Section Supply Voltage		9.5	10.5	11.5	V
IS	Supply Current of VAVcc & PVcc			63		mA
V_{IN}	Video Input Voltage Amplitude			0.7	1	Vpp
V_{OUT}	Typical Output Voltage Range		0.5		7	V
V_{Black}	Output (Black level)			1.5		V

AC Electrical Characteristics (VAV_{CC} = PV_{CC} = 10.5V, CL = 5pF, RL = 1KΩ, Tamb = 25°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
AV	Maximum Gain	Max Contrast and Drive I^2C Gainwin = 1		18		dB
CAR	Contrast Attenuation Range	V_{IN} = 0.7Vpp Contrast and Drive at POR		30		dB
DAR	Drive Attenuation Range			30		dB
GM	Gain Match	V_{IN} = 0.7Vpp, V_{OUT} = 4Vpp, Contrast and Drive= 0.87Max		+-0.1		dB
BW	Large Signal Bandwidth	V_{IN}=0.7Vpp, V_{OUT} = 2.5Vpp, Contrast and Drive = 0.87Max At -3dB		120		MHz

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DIS	Video Output Distortion	f=1MHz, V_{IN}=1Vpp, V_{OUT} = 1Vpp		0.3		%
t_R, t_F	Video Output Rise and Fall Time	V_{IN} = 0.7Vpp, V_{OUT} =2.5Vpp,Contrast and Drive=0.87Max		3.5	4	ns
dVo	Overshoot of output with respect to actual output amplitude	C_{LOAD}=5pF		5	7	%
BRT	Brightness max DC level Brightness min DC level			2.5 0		V V
R_L	Equivalent Load on Video Output	$Tj<Tj_{MAX}$		1		kΩ
Tsample	Hold time		100			ms
Thold	Sample time		1			µs
CT	Crosstalk Between Video Channels	V_{IN} = 0.7Vpp, V_{OUT} = 2.5Vpp, Contrast and Drive=0.7Max f=1MHz	44			dB
ABL COMPENSATION						
R_{ABL}	ABL Input resistor			10		kΩ
G_{ABL}	ABL minimum Attenuation ABL maximum Attenuation	V_{ABL}=5.3V V_{ABL}=2.8V		0 12		dB dB
TH_{ABL}	ABL latch function activation threshold (High beam current detection)		0		1	V
GAIN WINDOW						
V_{INL}	Input Low Level Voltage				0.7	V
V_{INH}	Input High Level Voltage		1.5			V
Gain	Contrast Gain Increase during High Input VIN = 1.5V VIN = 5.0V			 1 1.5		 V/V V/V
T_D	Total Delay Time				100	ns

11 - LOGIC SECTION

DC Electrical Characteristics ($VAV_{CC} = PV_{CC} = 10.5V$, Tamb = 25^oC)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VBDC OUTPUT SECTION						
VBDC	Blanking output high voltage		7			V
	Blanking output low voltage I2C adjustable	sub-add10 1X000000 1X111111		 1 4.5		 V V
I_{BLK}	Output sink current				0.3	mA
T_{BLK}	Vertical blanking time (start by VSync 2 and by VFly)					
SUPPLY VOLTAGE THRESHOLD						
V_{THPD1}	Supply first threshold voltage			8.5		V
V_{THPD2}	Supply second threshold voltage			6.9		V

12 - I²C BUS ADDRESS TABLE

[0] denotes POR value, X denotes unused data bit and must be set to 0.

	D8	D7	D6	D5	D4	D3	D2	D1
WRITE MODE (SLAVE ADDRESS= 8C)								
00	Video 1, on [0], off	**Contrast**						
		[1]	[0]	[1]	[1]	[0]	[1]	[0]
01	**Drive 1**							
	[1]	[0]	[1]	[1]	[0]	[1]	[0]	[0]
02	**Drive 2**							
	[1]	[0]	[1]	[1]	[0]	[1]	[0]	[0]
03	**Drive 3**							
	[1]	[0]	[1]	[1]	[0]	[1]	[0]	[0]
04	EWCorner Top/Bottom 0 off [1], on	**EW Corner Top**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
05	Corner phase Top/Bottom 1, on [0],off	**Corner Phase Top**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
06	Ipump2 1, high [0], low	**Corner Phase Bottom**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
07	Hout 0, off [1], on	**Horizontal Phase Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
08	Vramp 0, off [1], on	**Vertical Ramp Amplitude Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
09	Xray 1, reset [0]	**Vertical Position Adjustment**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0A	S Select 1, on [0], off	**S Correction**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0B	EW Key 0, off [1], on	**Keystone**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0C	EW Select 0, off [1], on	**EW Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0D	x	**Horizontal Amplitude**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0E	SPB Sel 0, off [1], on	**Side Pin Balance**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
0F	Parallelog 0, off [1], on	**Parallelogram**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
10	VBDC 1, on [0], off	Gainwin [0], 1X 1, 1.5X	**Vertical Blanking DC level**					
			[1]	[1]	[1]	[1]	[1]	[1]

	D8	D7	D6	D5	D4	D3	D2	D1
11	POR [0], off 1, reset	Ipump 1, 1mA [0], 0.3mA	**Brightness**					
			[1]	[0]	[1]	[1]	[0]	[1]
12		**HEHT Comp Gain**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]
13	x	x	x	x	**PLL1 filter voltage clamp (FVC)**			
					[0]	[0]	[0]	[0]
14			**VEHT Comp Gain**					
			[1]	[0]	[0]	[0]	[0]	[0]
15		**EWCorner Bottom**						
		[1]	[0]	[0]	[0]	[0]	[0]	[0]

READ MODE (SLAVE ADDRESS = 8D)

	Hlock 0, lock [1], unlock		Xray 1, on [0], off					

Note: Both EW Corner Top and EW Corner Bottom are switched ON/OFF by reg (sub-address 04/D8).

Figure 1. EW Output Referred Voltage

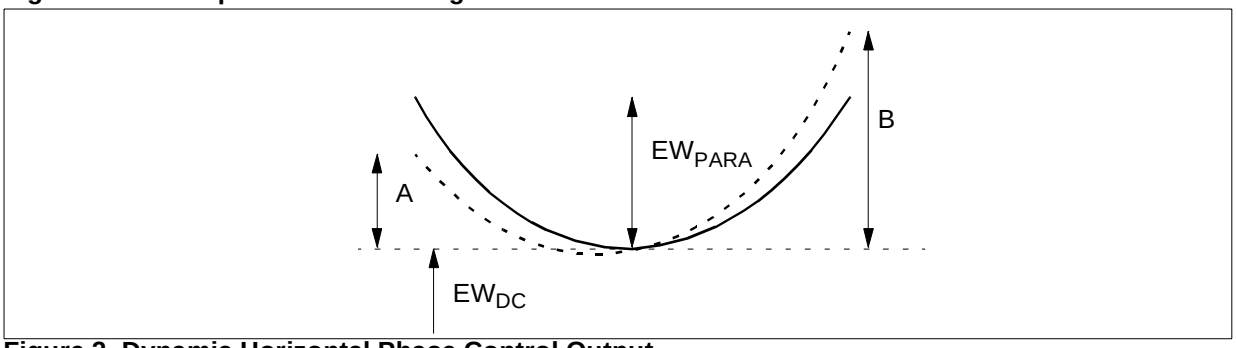


Figure 2. Dynamic Horizontal Phase Control Output

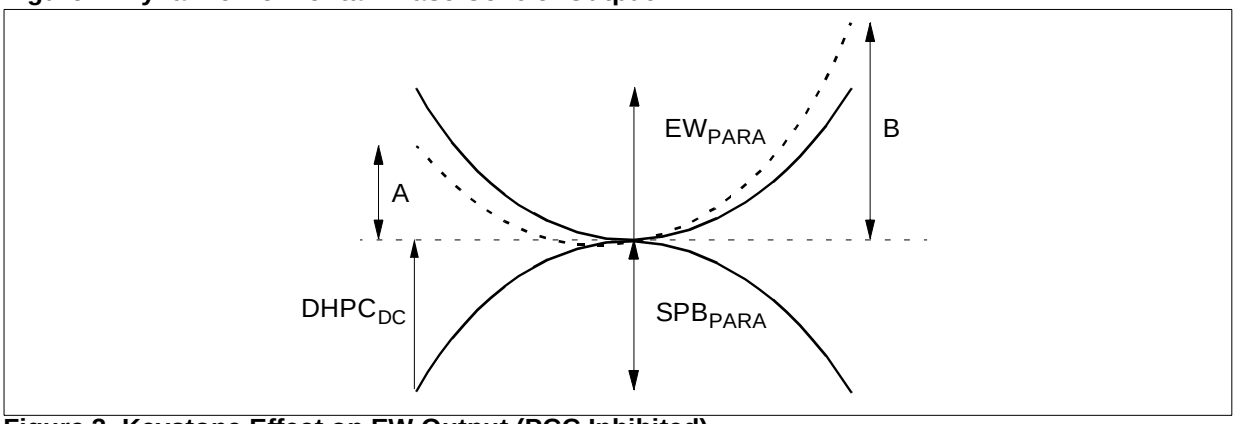


Figure 3. Keystone Effect on EW Output (PCC Inhibited)

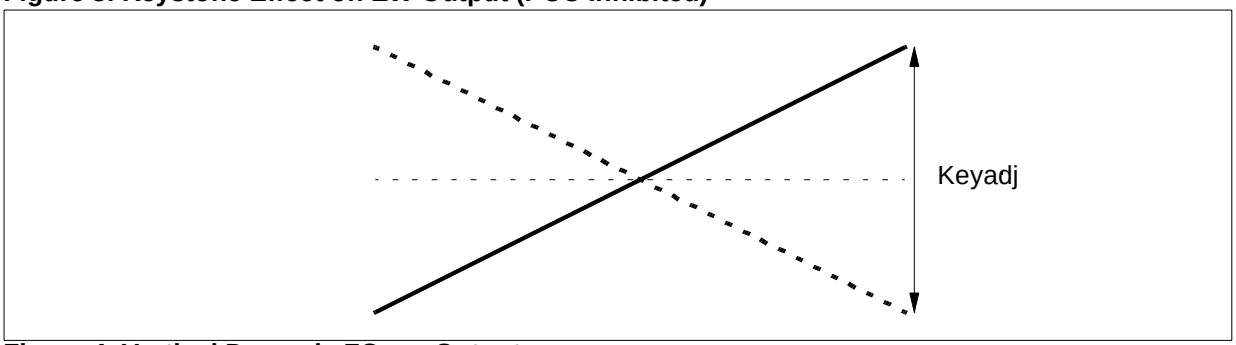
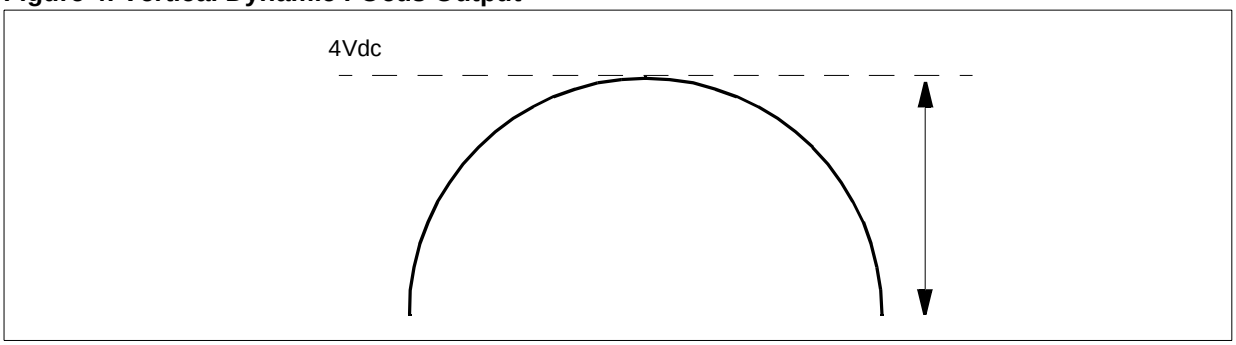
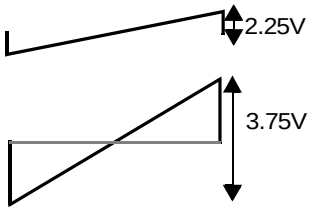
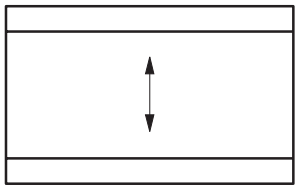
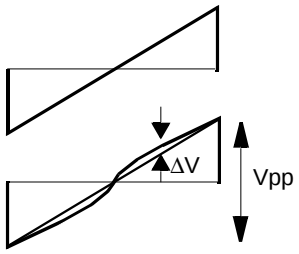
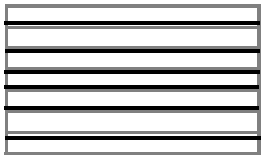
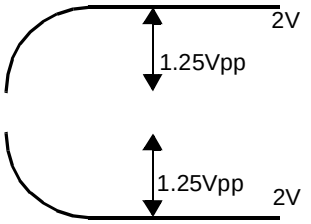
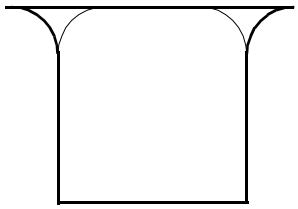
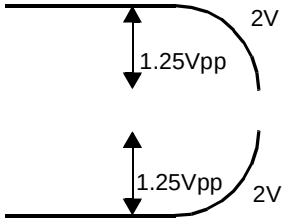
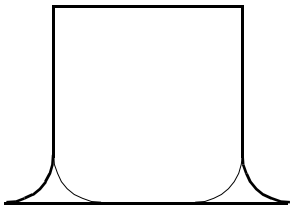
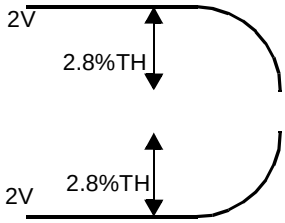
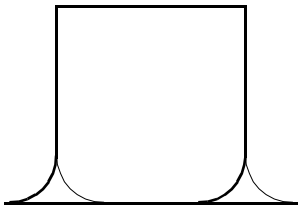
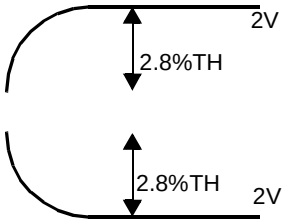
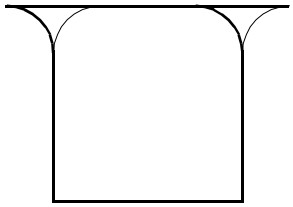
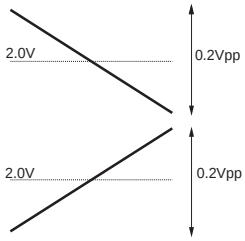


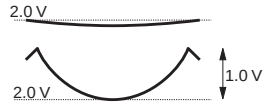
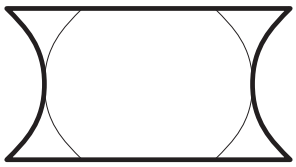
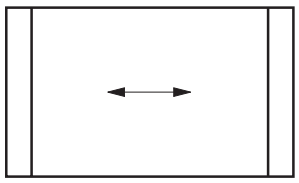
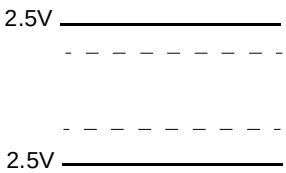
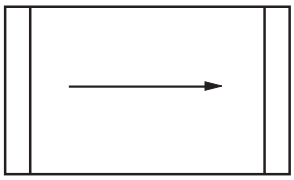
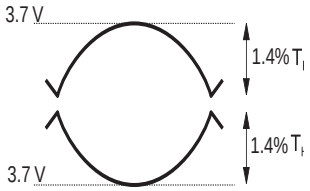
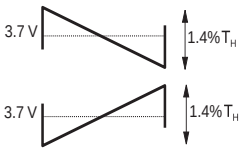
Figure 4. Vertical Dynamic FOcus Output



13 - TYPICAL OUTPUT WAVEFORMS

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
Vertical Size			1000 0000 1111 1111		
Vertical Position			x000 0000 x100 0000 x111 1111	V_{OUTDC} = 3.2 V V_{OUTDC} = 3.5 V V_{OUTDC} = 3.8 V	
Vertical S Linearity			0000 0000 Inhibited 1111 1111		
EW Corner Top (Symmetri-cal)			Keystone, EW Inhibited 1000 0000 1111 1111		

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
EW Corner Bottom (Sym-metrical)			Keystone, EW Inhibited 1000 0000 1111 1111		
Corner Phase Bottom (Asym-metrical)			Keystone, EW Inhibited 1000 0000 1111 1111		
Corner Phase Top (Asym-metrical)			Keystone, EW Inhibited 1000 0000 1111 1111		
Keystone			EW Inhibited 1000 0000 1111 1111		

Function	Sub Address	Pin	Byte	Specification	Effect on Screen
EW Pin Cushion			EW Inhibited 1000 0000 1111 1111		
H Amplitude			1000 0000 1111 1111		
H Phase			0000 0000 0111 1111		
Side Pin Ballance Control			Parallelogram Inhibited 1000 0000 1111 1111		
Parallelo-gram Control			SPB Inhibited 1000 0000 1111 1111		

Contrast Register (Video IN = 0.5V_{PP}, Drive at maximum, I^2C Gainwin=1)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	Vpp	G(dB)	POR
	0	0	0	0	0	0	0	0	0	-	
	0	0	0	0	0	0	0	1	0.015	-30	
	0	0	0	0	0	0	1	0	0.031	-24	
	0	0	0	0	0	1	0	0	0.062	-18	
	0	0	0	0	1	0	0	0	0.125	-12	
	0	0	0	1	0	0	0	0	0.25	-6	
	0	0	1	0	0	0	0	0	0.5	0	
	0	1	0	0	0	0	0	0	2	12	
	0	1	0	1	1	0	1	0	2.812	15	X
	0	1	1	1	1	1	1	1	4	18	

Brightness Register (Drive at maximum)

Hex	b5	b4	b3	b2	b1	b0	Vpp	POR
	0	0	0	0	0	0	0	
	0	0	0	0	0	1	0.010	
	0	0	0	0	1	0	0.020	
	0	0	0	1	0	0	0.040	
	0	0	1	0	0	0	0.08	
	0	1	0	0	0	0	0.16	
	1	0	0	0	0	0	0.32	
	0	0	0	0	0	0	0.64	
	0	0	0	0	0	0	1.28	
	1	0	1	1	0	1	1.8	X
	1	1	1	1	1	1	2.56	

Drive1, Drive2, Drive3 Registers (Video IN = 0.5V_{PP}, Contrast at maximum, I^2C Gainwin=1)

Hex	b7	b6	b5	b4	b3	b2	b1	b0	Vpp	G(dB)	POR
00	0	0	0	0	0	0	0	0	0	-	
01	0	0	0	0	0	0	0	1	0.015	-30	
02	0	0	0	0	0	0	1	0	0.031	-24	
04	0	0	0	0	0	1	0	0	0.062	-18	
08	0	0	0	0	1	0	0	0	0.125	-12	
10	0	0	0	1	0	0	0	0	0.25	-6	
20	0	0	1	0	0	0	0	0	0.5	0	
40	0	1	0	0	0	0	0	0	1	6	
80	1	0	0	0	0	0	0	0	2	12	
B4	1	0	1	1	0	1	0	0	2.812	15	X
FF	1	1	1	1	1	1	1	1	4	18	

Vertical Blanking Output DC voltage

Hex	b5	b4	b3	b2	b1	b0	Output dc	POR
	0	0	0	0	0	0	1.0	
	0	0	0	0	0	1		
	0	0	0	0	1	0		
	0	0	0	1	0	0		
	0	0	1	0	0	0		
	0	1	0	0	0	0		
	1	0	0	0	0	0		
	0	0	0	0	0	0		
	0	0	0	0	0	0		
	1	1	0	1	0	0		
	1	1	1	1	1	1	4.5	X

14 - OPERATING DESCRIPTION

SCANNING PART

14.1 - GENERAL CONSIDERATIONS

14.1.1 - Power Supply

Typical power supply voltages are 10.5 V for the Deflection and Preamplifier sections (SAV_{CC}, VAV_{CC} and PV_{CC}) and 5.0 V for the logic section (Vdd). Optimum operation is obtained between 9.5 and 11.5 for V_{CC}, and between 4.5 and 5.5 V for V_{DD}.

V_{CC} is monitored during the transient phase when switched either on or off, to avoid erratic operation of the circuit. If V_{CC} is inferior to 5.0 V typ., the circuit outputs are inhibited. Similarly, before V_{DD} reaches 4 V, all the I^2C registers are reset to their default value (see I^2C Control Table).

The circuit is internally supplied by several voltage references (typ. value: 8 V) to ensure a good power supply rejection. Two of these voltage references are externally accessible respectively for the vertical and horizontal parts. They can be used to bias external circuitry if I_{LOAD} is inferior to 5 mA. To minimize the noise and consequently the "jitter" on vertical and horizontal output signals, the reference voltages must be filtered by external capacitors connected to the ground.

To further improve the jitter on both vertical and horizontal sections, FCAP and FILTER pins are used to filter the internal 5V regulator with external decoupling capacitors.

14.1.2 - I^2C Control

STV2001 belongs to the I^2C-controlled device family. Each adjustment can be made via the I^2C Interface, instead of being controlled by DC voltages on dedicated control pins. The I^2C bus is a serial bus with a clock and a data input. General function and bus protocol are specified in the Philips-bus data sheets. The interface (Data and Clock) is TTL-compatible. Spikes up to 50 ns are filtered by an integrator and the maximum clock speed is limited to 100 kHz.

The data line (SDA) can be used bidirectionally. In read mode, the IC sends reply information (1 byte) to the micro-processor.

The bus protocol prescribes a full-byte transmission in all cases. The first byte after the start condition is used to transmit the IC address (hexa 8C for write, 8D for read).

All bytes are sent MSB bit first and the write data transfer is closed by a stop.

14.1.3 - Write Mode

In write mode, the second byte contains the subaddress of the selected function to adjust (or controls to effect) and the third byte the corresponding data byte. More than one data byte can be sent to the IC. If after the third byte no stop or start condition is detected, the circuit automatically increments the momentary subaddress in the subaddress counter (auto-increment mode) by one. Thus it is possible to immediately transmit the following data bytes without sending the IC address or subaddress. This can be useful for reinitializing all the controls very quickly (flash manner). This procedure is ended with a stop condition.

There are 22 adjustment capabilities for the circuit: 3 for the horizontal part, 3 for the vertical, 3 for the E/W correction, 2 for the dynamic horizontal phase control, 5 for the preamplifier, 4 for the corners, 2 for EHT compensation and 1 for the blanking DC. 14 bits are also dedicated to several controls (ON/OFF).

14.1.4 - Read Mode

In the read mode the second byte transmits the reply information. The reply byte contains the horizontal and vertical lock/unlock status, the XRAY activation status. A stop condition always stops all the activities of the bus decoder and switches both the data and clock line (SDA and SCL) to high impedance. See I^2C subaddress and control tables.

14.1.5 - Sync Processor

The internal sync processor allows the device to receive separate horizontal & vertical TTL-compatible sync signals.

14.1.6 - IC Status

The IC informs the MCU about both the 1st horizontal PLL (locked or not) and the XRAY protection (activated or not). The XRAY internal latch is reset either directly via the I^2C interface or by decreasing the V_{CC} supply.

14.1.7 - Sync Inputs

Both HIN and VIN inputs are TTL compatible triggers with hysterisis to avoid erratic detection. Both inputs include a pull-up resistor connected to V_{DD}. Synchro pulses must be positive.

14.1.8 - Sync Processor Output

The sync processor indicates whether 1st PLL is locked to an incoming horizontal sync or not. This is indicated on the D8 bit of the status register . PLL1 level is low when locked.

14.2 - HORIZONTAL PART

14.2.1 - Internal Input Conditions

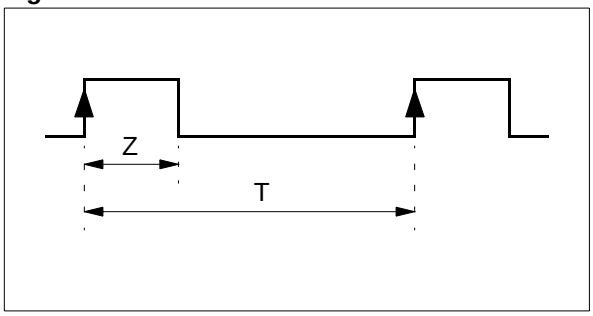
A digital signal (horizontal sync pulse) is sent by the sync processor to the horizontal input. It must be positive (see Figure 5).

Synchronization occurs on the leading edge of the internal sync signal.

The minimum value of Z is 0.7 µs.

Vertical synchro extraction is not allowed.

Figure 5.



14.2.2 - PLL1

The PLL1 consists of a phase comparator, an external filter and a voltage-controlled oscillator (VCO). The phase comparator is a "phase frequency" type designed in CMOS technology. This kind of phase detector avoids locking on wrong frequencies. It is followed by a "charge pump", composed of two current sources: sunk and sourced (typically I =1 mA when locked and I = 40 µA when unlocked). This difference between lock/unlock allows smooth catching of the horizontal frequency by PLL1. This effect is reinforced by an internal original slow down system when PLL1 is locked, preventing the horizontal frequency from changing too quickly. The dynamic behaviour of PLL1 is fixed by an external filter which integrates the current of the charge pump. A "CRC" filter is generally used (see Figure 6). One bit I^2C Ipump is used to set the pump current to 1mA or 0.3mA in locked condition.

Figure 6.

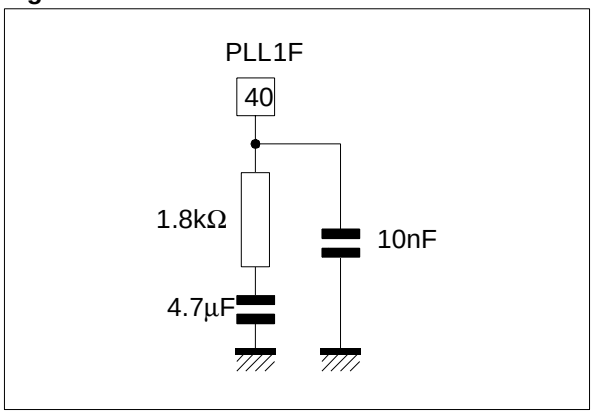


Figure 7. Block Diagram ²&

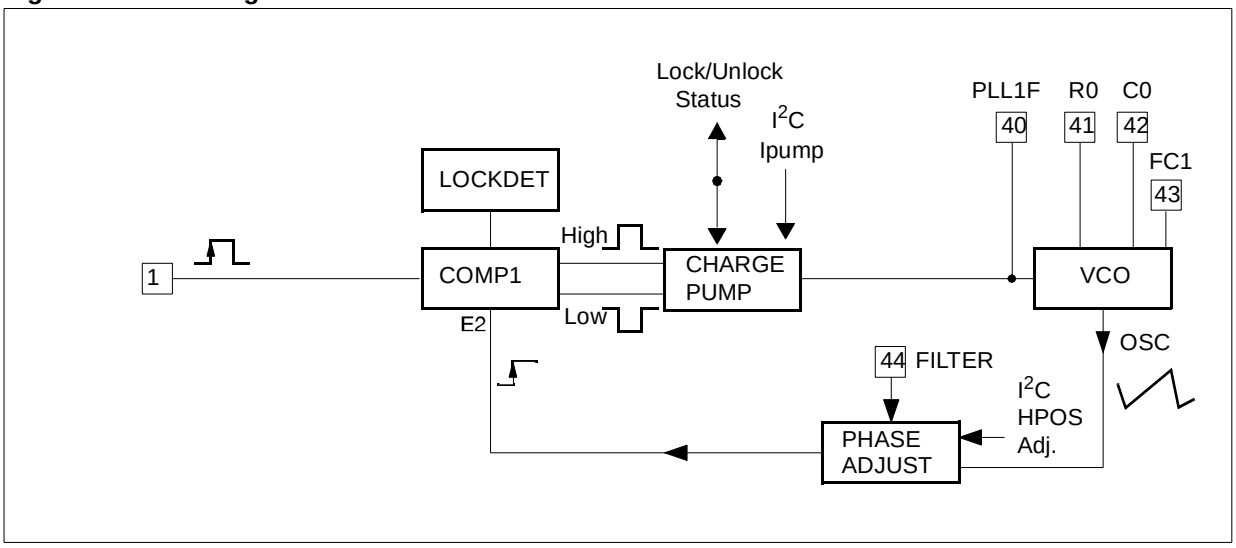
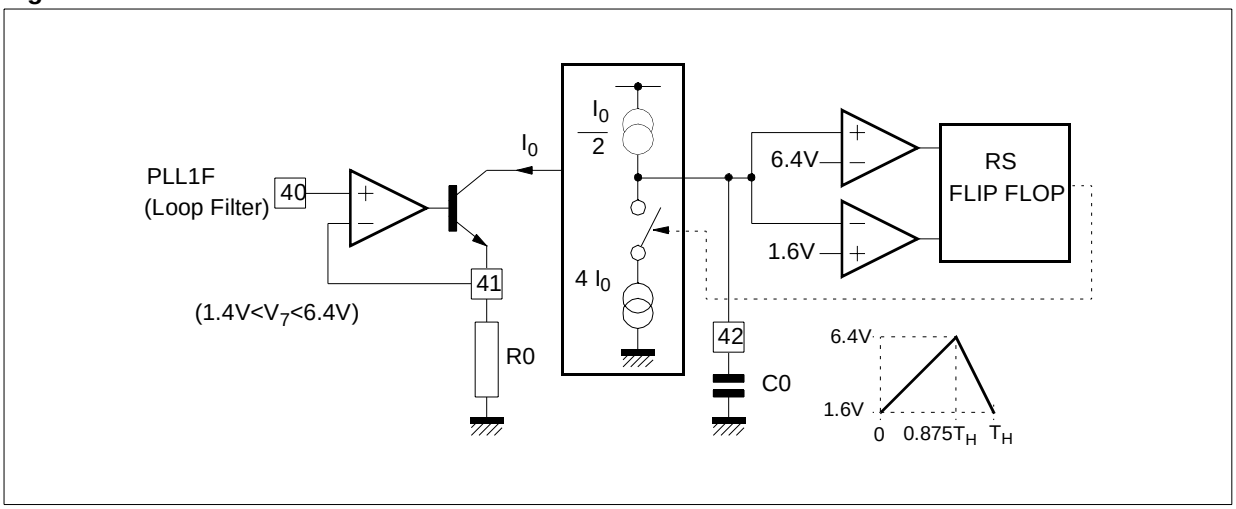


Figure 8. Details of VCO



The VCO uses an external RC network. It delivers a linear sawtooth resulting from the capacitor charge and discharge . The current is proportional to the one in the resistor. Typical thresholds for the sawtooth are 1.6 V and 6.4 V.

The VCO control voltage varies between 3.0 V and 3.8 V (see Figure 8). This VCO frequency range is very small. The small effective frequency is due to clamp intervention on the lowest filter value. The PLL1F filter voltage is set by a 4-bit DAC with a voltage range of 3.0 to 3.8 V.

The sync frequency must always be higher than the free running frequency. For example, when using a 60 kHz synchro range, the suggested free running frequency is 56 kHz.

PLL1 ensures the coincidence between the leading edge of the sync signal and a phase reference resulting from the comparison of:

– the VCO sawtooth

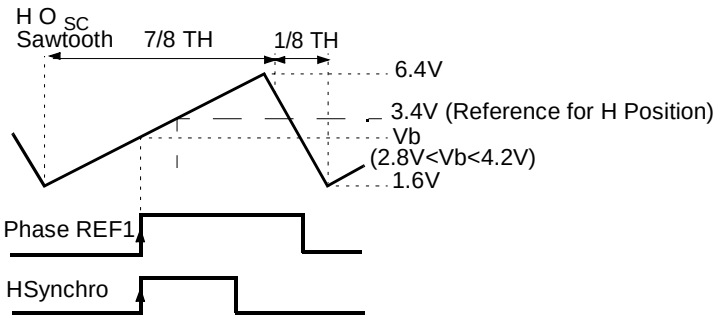
– an internal DC voltage I2C adjustable within the range of 2.9V to 4.2V (corresponding to ±10%) (see Figure 9).

A Lock/Unlock identification block, also included, detects in real time whether PLL1 is locked on the incoming horizontal sync signal or not.

The lock/unlock information is available through the I^2C read.

The FC1 Pin (Pin 43) is used for decoupling the internal 6.4 V reference by a capacitor.

Figure 9. PLL1 Timing Diagram



Phase REF1 is obtained by comparison between the sawtooth and a DC voltage adjustable between 2.9 V and 4.2 V.

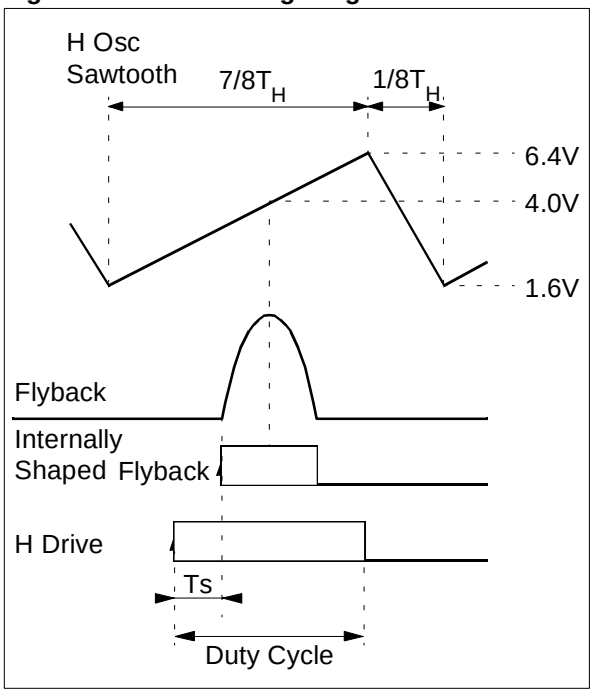
The PLL1 ensures the exact coincidence between the signal phase REF and HSYNC.

A ±10% T_H phase adjustment is possible around the 3.5V point.

14.2.3 - PLL2

PLL2 ensures a constant position of the shaped flyback signal in comparison with the sawtooth of the VCO, taking into account the saturation time Ts (see Figure 10).

Figure 10. PLL2 Timing Diagram



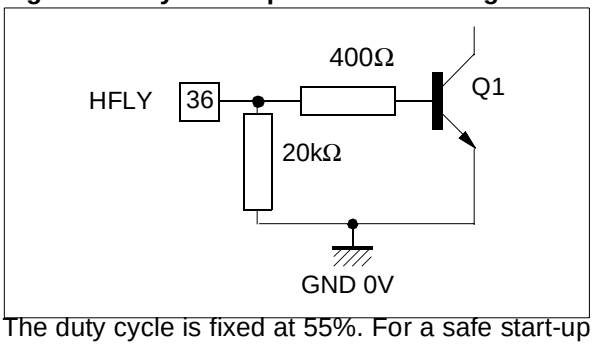
The phase comparator of PLL2 (phase type comparator) is followed by a charge pump (typical output current: 0.5 mA).

VBCAP pin is used to filter noise on PLL2 top comparator via an external capacitor.

The flyback input consists of an NPN transistor.

This input must be current driven. The maximum recommended input current is 5 mA (see Figure 11).

Figure 11. Flyback Input Electrical Diagram



The duty cycle is fixed at 55%. For a safe start-up operation, the initial duty cycle (after power-on reset) is 85% in order to avoid having too long a conduction period of the horizontal scanning transistor.

The maximum storage time (Ts Max.) is :
$0.44T_H - T_{FLY}/2)$.
Typically, T_{FLY}/T_H corresponds to around 20 % which means that Ts max represents approximtively 34 % of T_H.

14.2.4 - Output Section

The H-drive signal is sent to the output through a shaping stage which also controls the fixed H-drive duty cycle (see Figure 10). In order to secure the scanning power part operation, the output is inhibited in the following cases :

-when V_{CC} is too low,

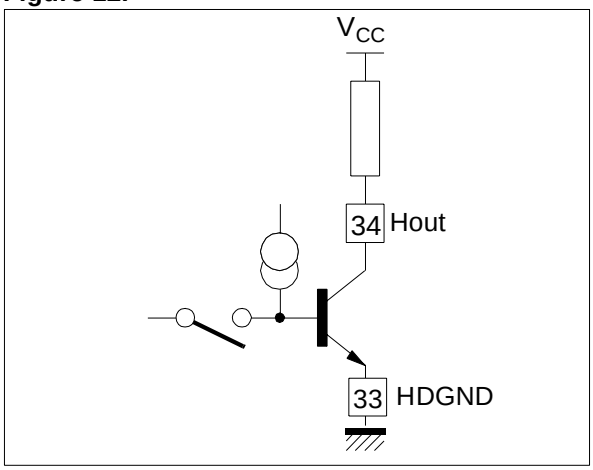
-when the ABL protection is activated,

-during the Horizontal flyback,

-when the HDrive I^2C bit control is off.

The output stage consists of a NPN bipolar transistor. Only the collector is accessible (see Figure 12). Emitter is connected directly to a separate ground pin.

Figure 12.



This output stage is intended for "reverse" base control, where setting the output NPN in off-state will control the power scanning transistor in off-state.

The maximum output current is 15 mA, and the corresponding voltage drop of the output V_{CEsat} is 0.4 V Max.

Obviously, the power scanning transistor cannot be directly driven by the integrated circuit. An interface either bipolar or MOS type has to be added between the circuit and the power transistor.

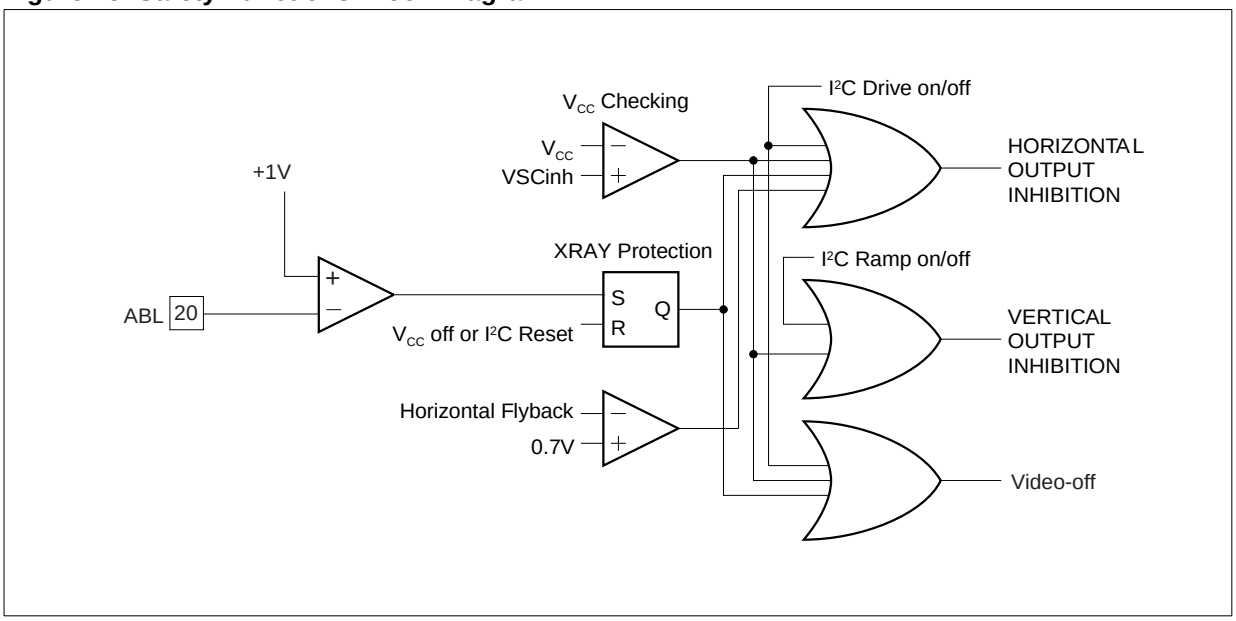
14.2.5 - X-RAY Protection

X-Ray protection is activated when the ABL input (1 V on Pin 20) is at a low level. It inhibits both H-Drive, and Vout while Video goes into off-mode.

This activation is internally delayed by 2 lines to avoid erratic detection (short parasitics).

This protection is latched; it may be reset either by switching V_{CC} off or by I^2C (see Figure 13).

Figure 13. Safety Functions Block Diagram



14.3 - VERTICAL PART

14.3.1 - Function

When the synchronization pulse is not present, an internal current source sets the free running frequency. For an external capacitor, C_{OSC} = 150nF, the typical free running frequency is 100Hz.

The typical free running frequency can be calculated according to:

$$fo(Hz) = 1.5 \cdot 10^{-5} \cdot \frac{1}{C_{OSC}}$$

A positive TTL level pulse applied on Pin 2 (Vin) is used to synchronize the ramp in the range [fmin, fmax] (see Figure 14). This frequency range depends on the external capacitor connected on Pin 6 (VCAP). A 150nF (± 5%) capacitor is recommended for 50 Hz to 165 Hz applications.

The typical maximum and minimum frequency, at 25°C and without any correction (S correction), can be calculated as follows:
f(Max.) = 3.5 x f_o and f(Min.) = 0.33 x f_o

When an S correction is applied, these values are slightly modified.

With a synchronization pulse, the internal oscillator is synchonized immediately but its amplitude changes. An internal correction then adjusts it in less than half a second. The ramp top value (Pin 6) is sampled on the AGC capacitor (Pin 4) at each clock pulse. A transconductance amplifier modifies the charge current of the capacitor so as to make the amplitude constant again. We recommend using an AGC capacitor with a low leakage current. A value lower than 100nA is mandatory.

A good level of stability for the internal closed loop is obtained by a 470nF ± 5% capacitor value on Pin 4 (VAGC).

VRB (Pin 8) is used for decoupling the internal 2V reference voltage by a capacitor.

14.3.2 - I^2C Control Adjustments

S correction shapes can then be added to this ramp. This frequency-independent S correction is generated internally. Its amplitudes is adjustable via the I^2C. S correction can be inhibited by applying the selected bits.

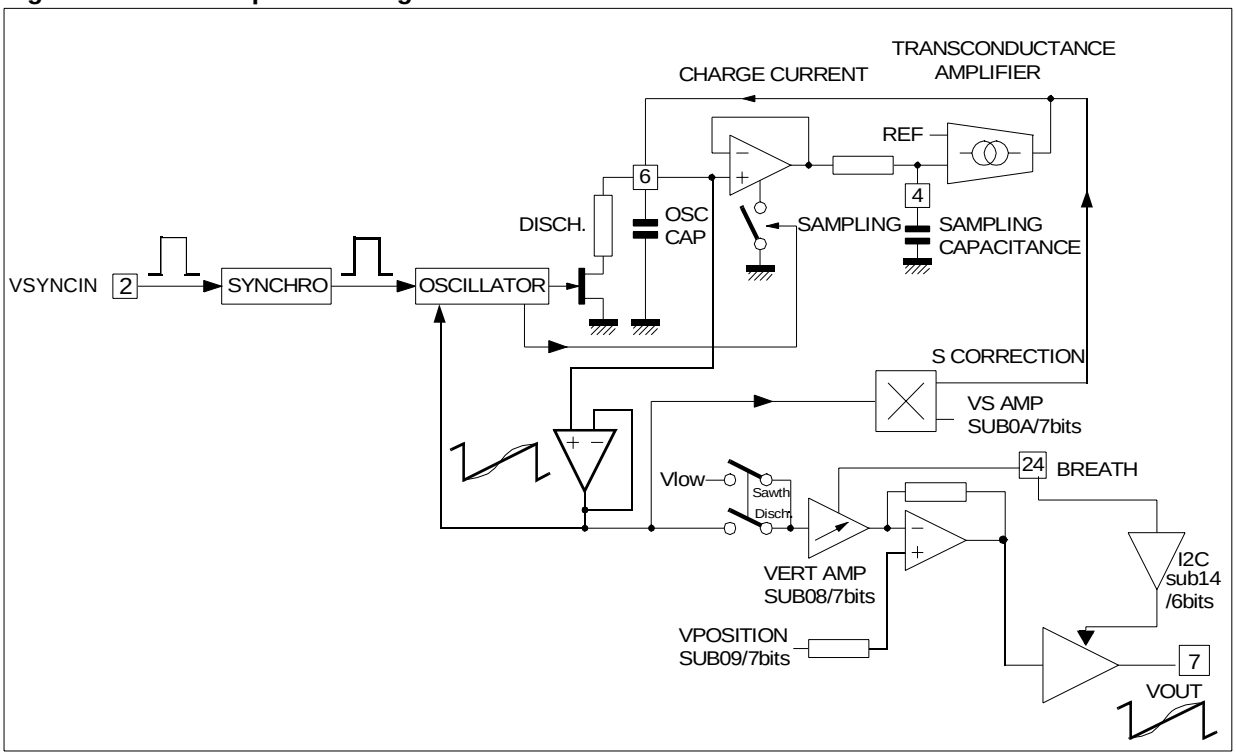
Finally, the amplitude of the S corrected ramp is adjustable via the vertical ramp amplitude control register.The adjusted ramp is available on Pin 7 (V_{OUT}) to drive an external power stage.

The gain of this stage can be adjusted (± 25%) depending on its register value.

The mean value of this ramp is driven by its own I^2C register (vertical position) with :
VPOS = 7/16 x V_{REF-V} = ± 300 mV.

Usually V_{OUT} is sent through a resistive divider to the inverting input of the booster. Since VPOS derives from V_{REF-V}, the bias voltage sent to the non-inverting input of the booster should also derive from V_{REF-V} to optimize the accuracy (see Figure 14).

Figure 14. AGC Loop Block Diagram



14.3.3 - Basic Equations

As a first approximation, the amplitude of the ramp on Pin 7 (VOUT) is calculated as follows:

V_{OUT} - VPOS = (V_{OSC} - V_{DCMID}) x (1 + 0.25 (V_{AMP}))

where :

V_{DCMID} = 7/16 x V_{REF} (middle value of the ramp on Pin 5, typically 3.6V)

V_{OSC} = V_5 (ramp with fixed amplitude)

V_{AMP} = -1 as minimum vertical amplitude register value and +1 as maximum value.

VPOS is calculated according to:

VPOS = V_{DCMID} + (0.4x V_P)

where V_P = -1 and +1 as respectively minimum and maximum vertical position register value.

The current available on Pin 6 is:

$$I_{OSC} = \frac{3}{8} \times V_{REF} \times C_{OSC} \times f$$

where
C_{OSC} = capacitor connected on Pin 6
f = synchronization frequency.

14.3.4 - Geometric Corrections

The principle is represented in Figure 15.

Starting from the vertical ramp, a parabola-shaped current is generated for E/W correction (also known as Pin Cushion correction), dynamic horizontal phase control correction.

The parabola generator consists of an analog multiplier, the output current of which is equal to :

$\Delta I = k \times (V_{OUT} - V_{DCMID})^2$

where V_{OUT} is the vertical output ramp (typically between 2 and 5 V) and V_{DCMID} is 3.6 V (for V_{REF-V} = 8.2V). The VOUT sawtooth is typically centered on 3.6 V. By changing the vertical position, the sawtooth shifts by ±0.4 V.

The "geometry tracking" feature ensures a correct screen geometry for any end user adjustment. It generates non-symmetric parabola dependent on the vertical position. To avoid Vertical EHT compensation (VBreathing) from affecting the geometry correction, an additional Buffer Amplifier is used for VBreathing.

Due to the large output stage voltage range (E/W Pin Cushion, Keystone), the combination of the tracking function, maximum vertical amplitude, maximum or minimum vertical position and maximum gain on the DAC control may lead to output stage saturation. This must be avoided by limiting the output voltage with appropriate I^2C register values. For the E/W part and the dynamic horizontal phase control part, a sawtooth-shaped differential current in the following form is generated:
$\Delta I' = k' \cdot (V_{OUT} - V_{DCMID})$.

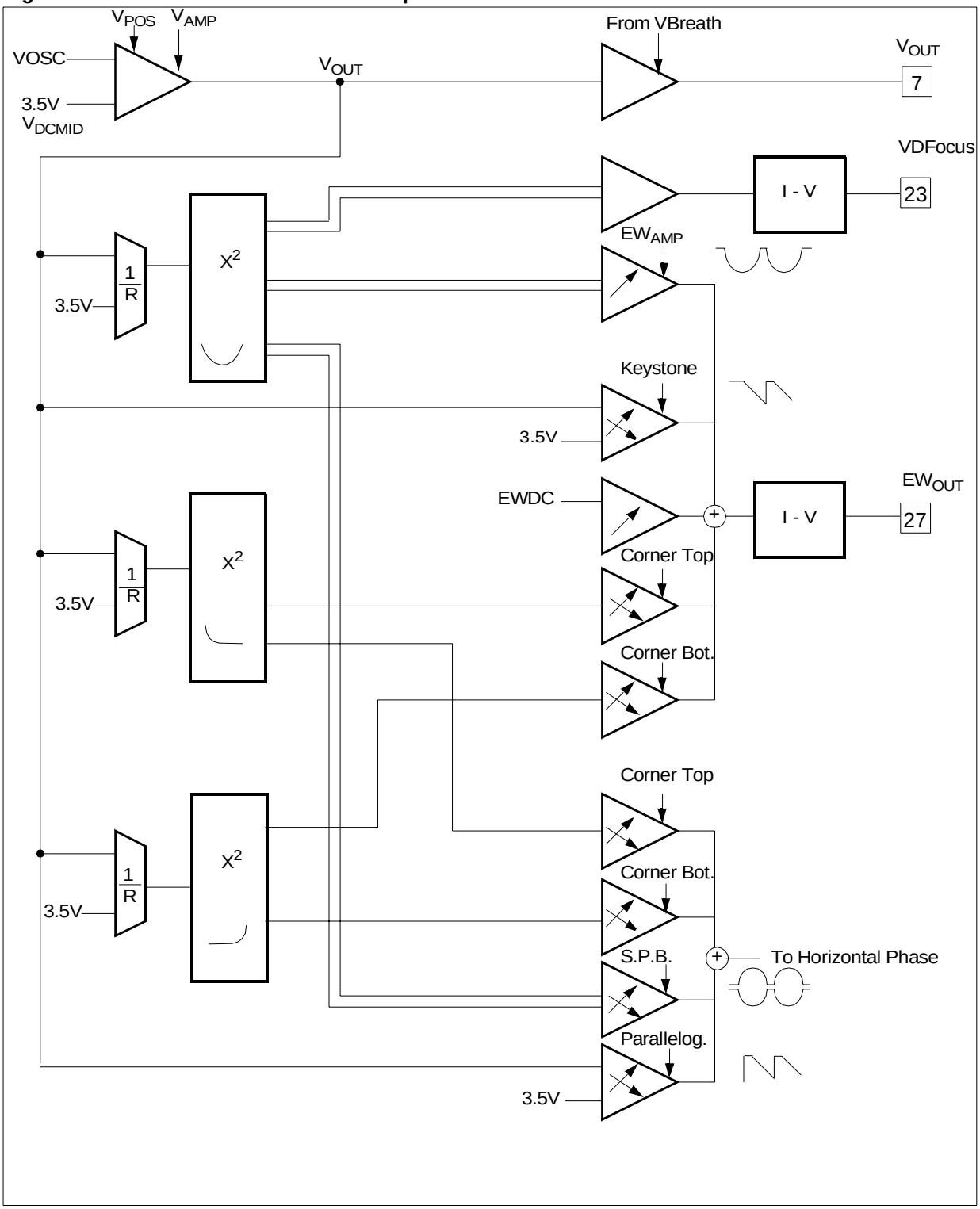
Then ΔI and $\Delta I'$ are added and converted into voltage for the E/W part.

Each of the two E/W components or the two dynamic horizontal phase control components may be inhibited by their own I^2C select bit.

EW output voltage is available at EWout pin directly. External buffer circuit is required to drive Darlington pair transistor, which is sinking the DIODE MODULATOR current in order to achieve EW correction. Additionally, an I^2C controlled DC shift is used for H-width.

The dynamic horizontal phase control drives the H-position internally, moving the HFLY position on the horizontal sawtooth in the range of $\pm$ 2.8 $\%T_H$ both for side pin balance and parallelogram.

Figure 15. Geometric Corrections Principle



14.3.5 - E/W

$EWOUT = EW_{DC} + K1 (V_{OUT} - V_{DCMID}) + K2 (V_{OUT} - V_{DCMID})^2$

K1 is adjustable via the keystone I^2C register. K2 is adjustable via the E/W amplitude I^2C register.

14.3.6 - Dynamic Horizontal Phase Control

$I_{OUT} = K4 (V_{OUT} - V_{DCMID}) + K5 (V_{OUT} - V_{DCMID})^2$

K4 is adjustable via the parallelogram I^2C register.

K5 is adjustable via the side pin balance I^2C register.

14.3.7 - Vertical Dynamic Focus

Vertical Dynamic Focus waveform is available on Pin 23. It is the parabolic waveform with downwards concavity, at vertical frequency. Its amplitude is fixed at 1 Vpp.

14.3.8 - Corner Correction

There are 4 types of corner correction in the device: EW Corner Top, EW Corner Bottom, Corner Phase Top and Corner Phase Bottom. EW Corner Top and EW Corner Bottom are used to modulate the EW amplitude. Corner Phase Top and Corner Phase Bottom are used to modulate the Horizontal Phase. These 4 types of correction are used to compensate the distortion appearing at the corners of the CRT.

EW Corner Top and EW Corner Bottom corrections add a half parabola current to the EW voltage. Since the E/W output voltage range is limited, it was necessary to add EW Corner Correction to decrease both EW amplitude and Keystone by I^2C.

Corner Phase Top and Corner Phase Bottom corrections add a half parabola current to the Horizontal Phase. Top and Bottom Corrections can be adjusted separately by I^2C with 7 Bits DAC.

14.3.9 - Horizontal Breathing

Horizontal breathing is performed through the EW stage with V-I Converter and an I^2C controlled variable gain stage. This DC controlled input provides the Horizontal Width correction required to offset width changes due to EHT variation. Gain attenuation is set by a 7 bits DAC with I^2C.

14.3.10 - Vertical Breathing

Vertical breathing compensation is performed through gain modulation of the vertical ramp. This DC-controlled input allows the vertical height corrections needed to offset height changes due to EHT variations. Input is received at the output of the EHT compensation Amplifier. Gain attenuation is set by 6 Bits DAC via I^2C.

PRE-AMPLIFIER PART

14.4 - GENERAL CONSIDERATIONS

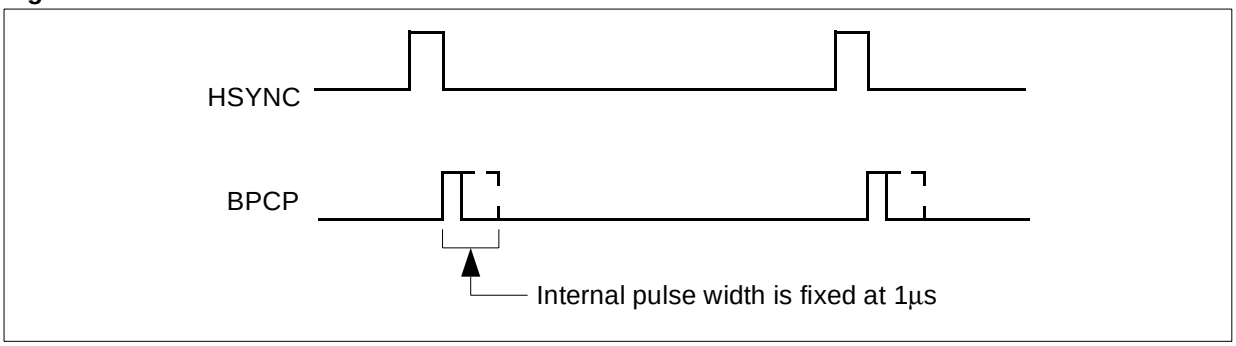
14.4.1 - Input Stage

The R, G and B signals must be supplied to the three inputs through coupling capacitors (100nF). The maximum input peak-to-peak video amplitude is 1 V.

The input stage includes a clamping function. This clamp uses the input serial capacitor as "memory capacitor" and is gated by an internally generated "Back-Porch-Clamping-Pulse (BPCP)".

The BPCP is synchronized on the second edge of the horizontal pulse HIN inputs on Pin 1.

Figure 16. .



In both cases, BPCP width is fixed.

14.4.2 - Contrast Adjustment (7 bits)

The contrast adjustment is made by simultaneously controlling the gain of three internal variable gain amplifiers through the I^2C bus interface. The contrast adjustment allows covering a range higher than 40 dB. This adjustment is refreshed during the vertical retrace time.

14.4.3 - ABL Control

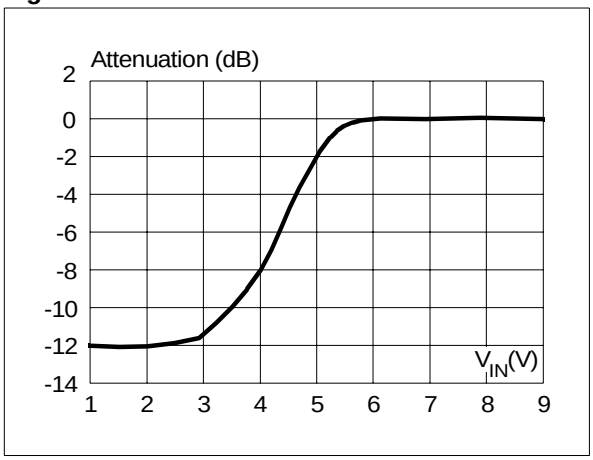
The STV2001 has an ABL input (automatic beam limitation) to attenuate RGB video signals according to beam intensity.

The operating range is typically 2.5 V, from 5.3 V to 2.8 V. A typical 12 dB Max. attenuation is applied to the signal whatever the current gain. Refer to Figure 16 for ABL input attenuation range.

In the case of software control, the ABL input must be pulled to AV_{CC} through a resistor to limit power consumption.

ABL input voltage must not exceed VAV_{CC}. Input resistor is 10kΩ.

Figure 17.



14.4.4 - Brightness Adjustment (6 bits)

As with contrast adjustment, brightness is controlled by I^2C.

The brightness function consists of adding the same DC offset to the three R, G, B signals after contrast amplification. This DC-Offset is present only outside the blanking pulse (see Figure 19).

The DC output level is forced to "INFRA-BLACK" level (V_{DC}) during the blanking pulse.

14.4.5 - Drive Adjustment (3 x 8 bits)

To adjust the white balance, the device offers the possibility of separately adjusting the overall gain of each complete video channel. Each channel gain is controlled by I^2C (8 bits each). The very large drive adjustment range (48dB) allows different standard or custom color temperatures.

The drive adjustment is also used to adjust the output voltages at the optimum amplitude to drive the C.R.T drivers, keeping the whole contrast control for end-users only. The drive adjustment is made after the contrast and brightness so that the white balance remains correct when BRT is adjusted.

14.4.6 - Output Stage

The three output stages (see Figure 18) incorporate three functions:

- The blanking stage: when the internal generated blanking pulse is high, the three outputs are switched to a voltage which is 400 mV lower than the BLACK level. The black level is the output voltage with minimum brightness when the input signal video amplitude is equal to "0".
- The output stage itself: a large bandwidth output amplifier which can deliver up to $5V_{PP}$ on the three outputs (for 0.7 V video signal on the inputs).
- The output CLAMP: the IC also incorporates three internal output clamps (sample and hold system) to fix the "INFRA-BLACK" level (VDC) at 1.1V during blanking.

The overall waveforms of the output signal according to the different adjustments are shown in Figure 19. and Figure 20.

Figure 18.

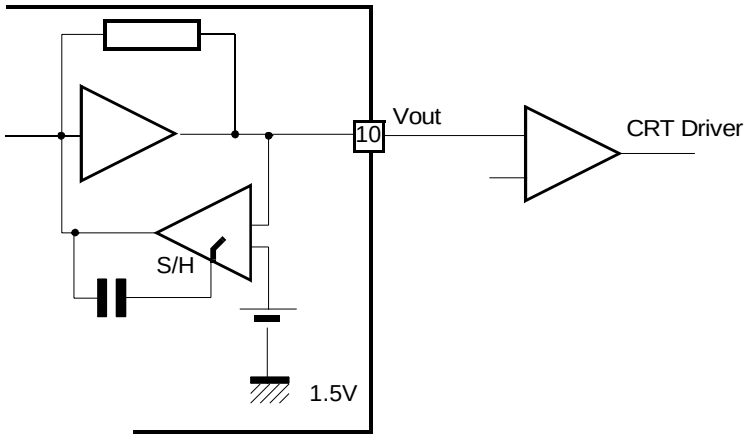
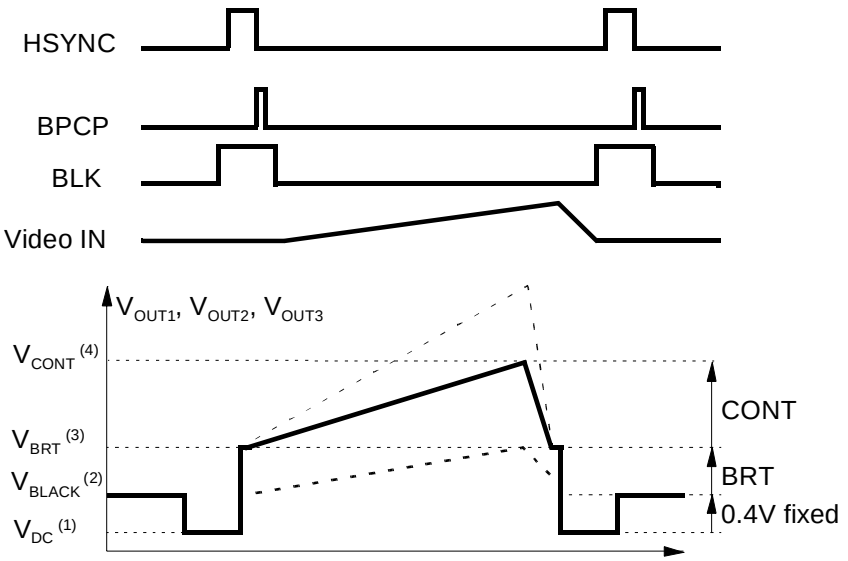
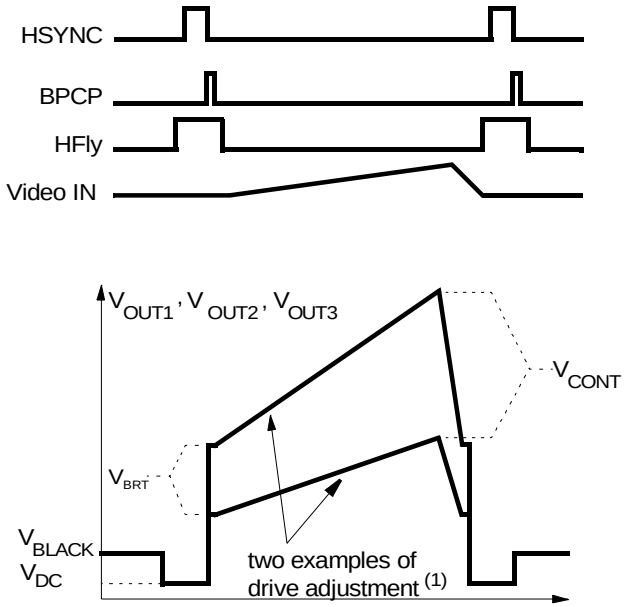


Figure 19. Waveforms VOUT, BRT, CONT



Note : 1. V_{DC} = 1.5V
2. $V_{BLACK} = V_{DC} + 0.4V$
3. $V_{BRT} = V_{BLACK}$ + BRT (with BRT = 0 to 2.5V)
4. $V_{CONT} = V_{BRT}$ + CONT with CONT = k x video (CONT = 5VPP max. for $V_{IN} = 0.7V_{PP}$)

Figure 20. Waveforms (DRIVE adjustment)



Note : 1. Drive adjustment modifies the following voltages : V_{CONT}, V_{BRT}.
Drive adjustment does not modify the following voltages : V_{DC} and V_{BLACK}.

14.4.7 - Bright Window

Contrast Gain can be increased by 1.5X when the I2C command “GainWin” is issued or GWIN (Pin 16) pulse value reaches its Turn-ON threshold.

Bright Window gain can be controlled separately by I^2C command or pulse voltage at “GAINWIN” pin. Although both controls are independent, max gain is still limited to 1.5x, not 1.5x + 1.5x.

14.4.8 - Blanking Generator

A vertical blanking pulse is generated (see Figure 21). The output level is a positive going pulse of 9.5V. The vertical blanking is started by the vertical sync pulse and by the falling edge of VFly pulse. If there is no VFly pulse (VFly>6.5V), the vertical blanking the vertical blanking start coincides with the beginning of the vertical capacitor discharge time.

The blanking output generates a superimposed variable DC voltage. The 6-bit adjustment range is 1 V to 4.5 V. This is used to allow brightness control through G1. Additionally, this pin is used for spot killer suppression. The 0.8 V of Vcc threshold will trigger the output into a high level state resulting from the Vcc decay.

Figure 21. VBDC (Pin 18) Output Voltage Waveform

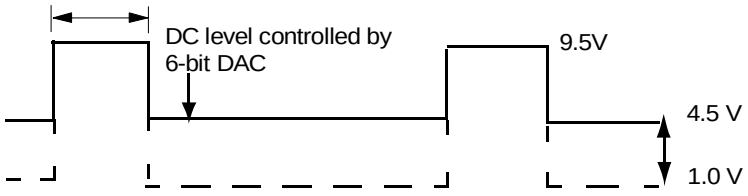


Table 1: Logic Table

Conditions	Hout	Vout	Video-off	Low Power
V_{cc} at 0 to 6.9 V (PD2 mode)	no	no	video-off	NA (1)
V_{cc} at 6.9 V to 8.5 V (PD1 mode)	yes	yes	video-off	NA(1)
Hlock/unlock detection = unlock	yes	yes	video-off	no
Video ABL input pin < 1 V	no	no	video-off	no
5 V POR or I^2C POR=1, (default=0)	yes	yes	video-off	no
I^2C Hout on/off, (default=1=on)	on/off	yes	on/off	no
I^2C Vout on/off, (default=1=on)	yes	on/off	on/off	no
I^2C Video on/off, (default=0=video-off)	yes	yes	on/off	no
V_{cc} at >8.5 V	yes	yes	video-on (2)	NA (1)
V_{cc} at >8.5 V, I^2C video=1=on	yes	yes	video-on (2)	no

Note 1 NA= Not applicable.
Note 2 I^2C video=on will be reset by Low V_{cc}.

STAND-BY MODE AND PROTECTIONS

14.5 - GENERAL CONSIDERATIONS

14.5.1 - POR (Power On Reset) - Subad. 11-D8

POR is activated on 5 V with default values for each adjustment and in addition video off (see 1.3). It can be activated via the I^2C command.

14.5.2 - Supply Voltage Threshold.

Two built-in thresholds (see figure 21) are used to enter the following modes:

- PDI mode:
  - Activated for Vcc < 8.5V
  - Video off (see 1.13)
- PD2 mode:
  - Activated for Vcc < 5.0V
  - Video off (see 1.13)
  - H_{OUT} and V_{OUT} disabled

14.5.3 - Video Off (I^2C control) - Subad. 00-D8

Activates blanking of the 3 video output stages. During this time the outputs are switched to VDC level, regardless of the presence of Hsync or Hfly-back. Activation time is inferior to 1µs.

This also activates the blanking output at pin 18 into a high level state close to 9.5V as long as “video off” is activated. When the device enters the “Video-off” mode, voltage on pin 8 is 8V.

14.5.4 - Vertical Output Off

This command will switch off output VAMP. The vertical output swing is reduced to 0V.

14.5.5 - X-Ray, Set Operation - Subad. 09-D8

When ABL voltage is below 1 V threshold, Xray latch will be activated. This I^2C command will reset the Xray latch. Activation time below 100ms.

15 - INTERNAL SCHEMATICS

Figure 22.

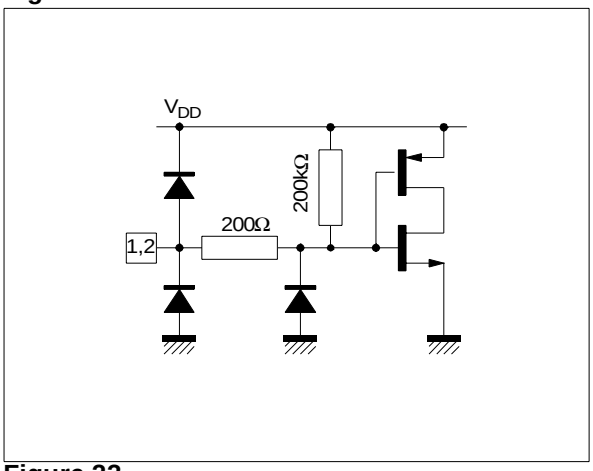


Figure 23.

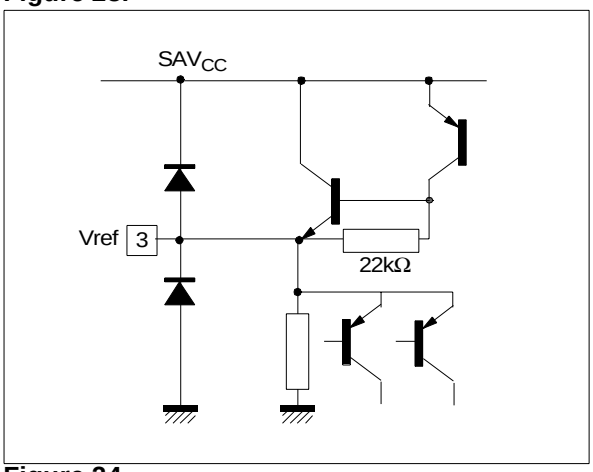


Figure 24.

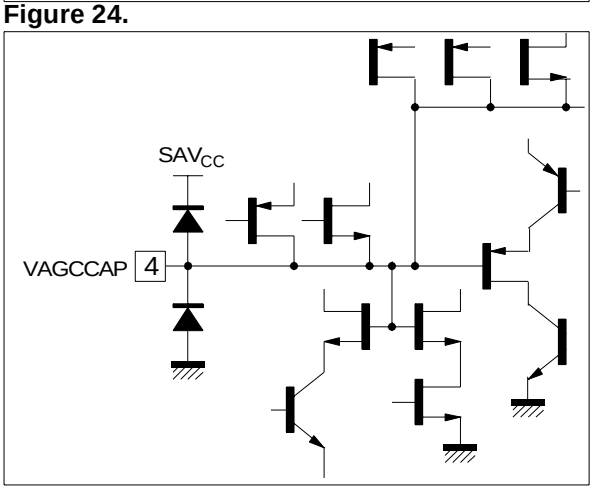


Figure 25.

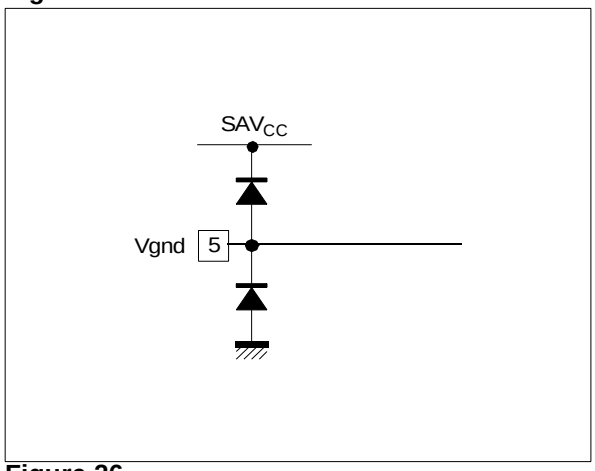


Figure 26.

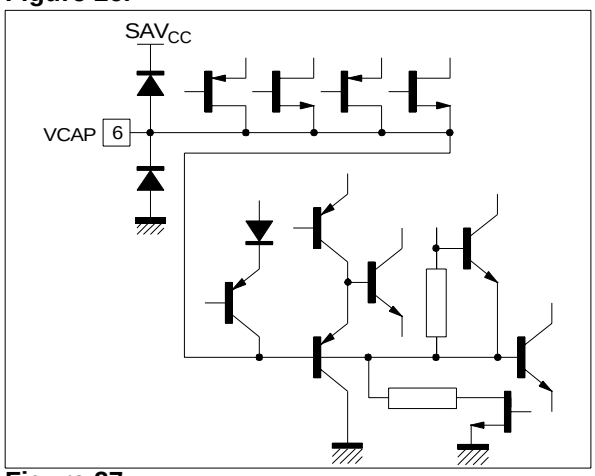
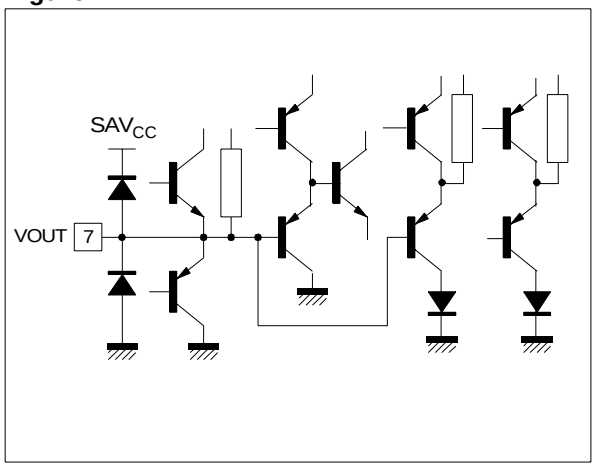


Figure 27.



INTERNAL SCHEMATICS (continued)

Figure 28.

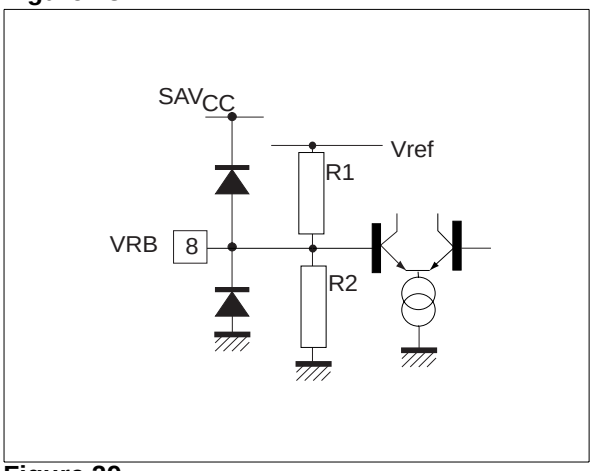


Figure 29.

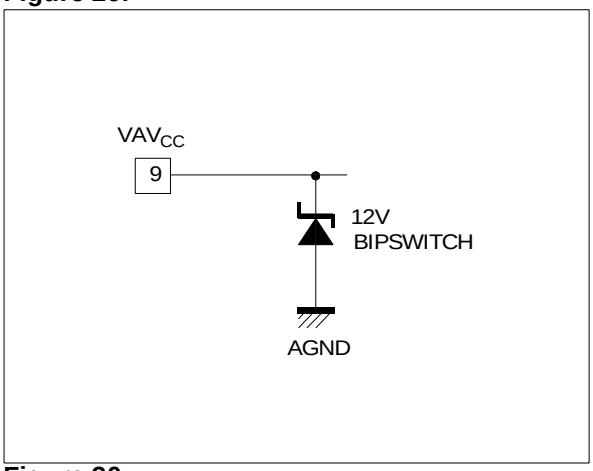


Figure 30.

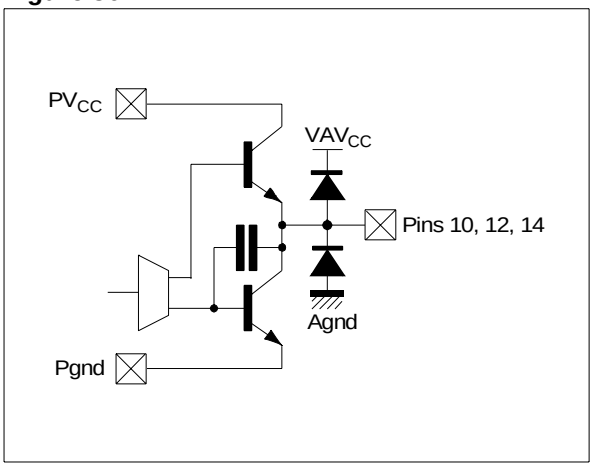


Figure 31.

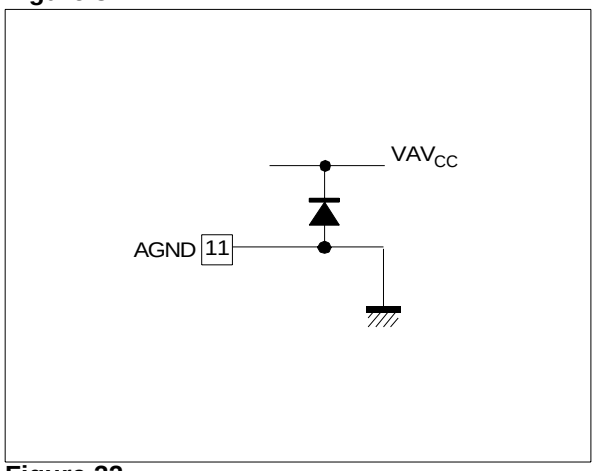


Figure 32.

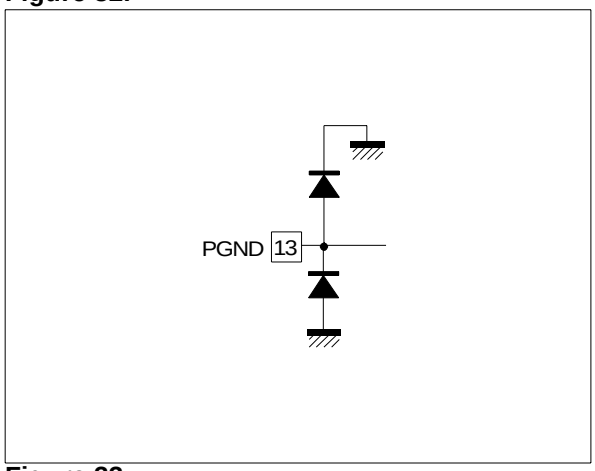
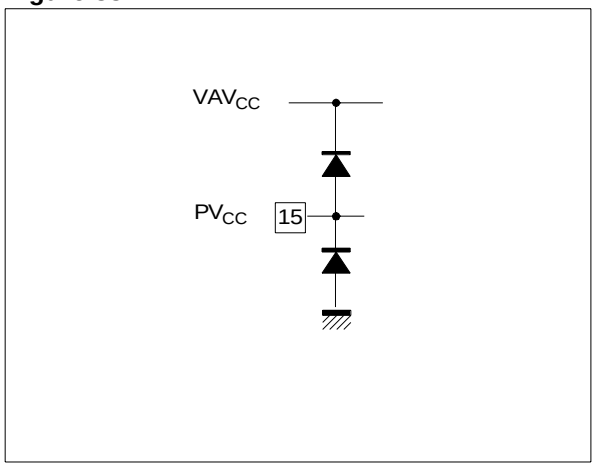


Figure 33.



INTERNAL SCHEMATICS (continued)

Figure 34.

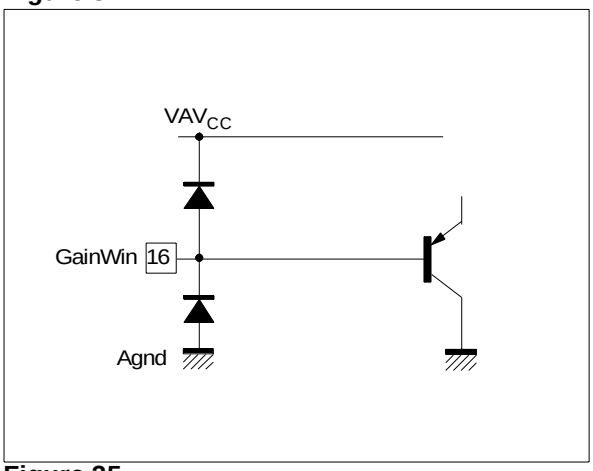


Figure 35.

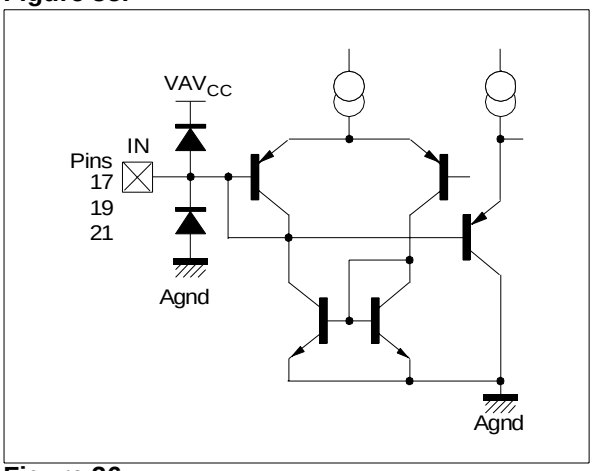


Figure 36.

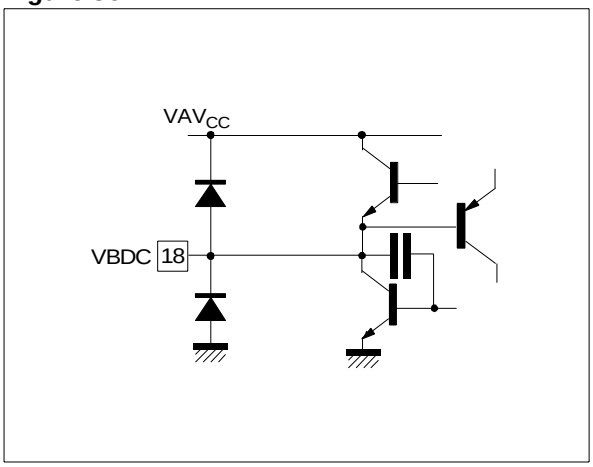


Figure 37.

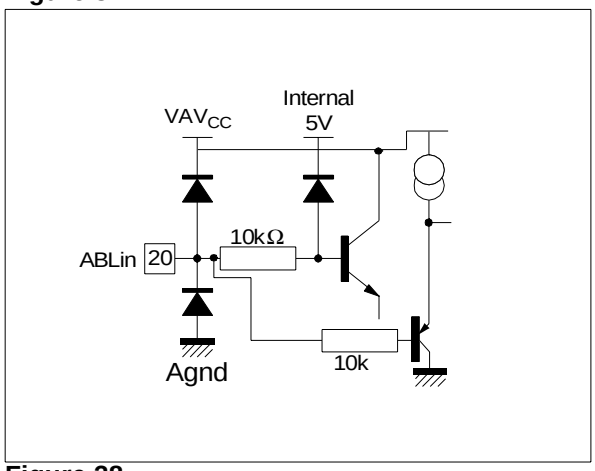


Figure 38.

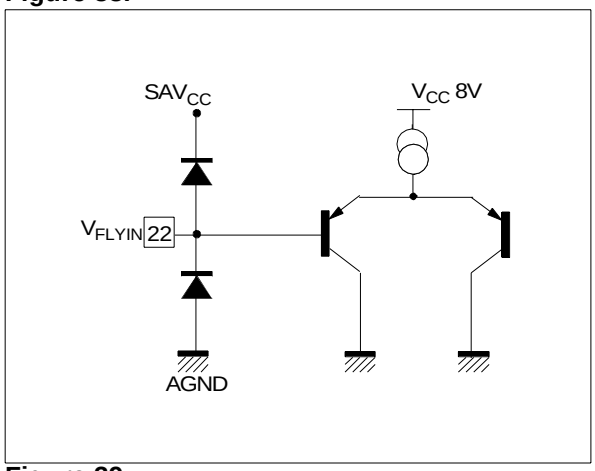
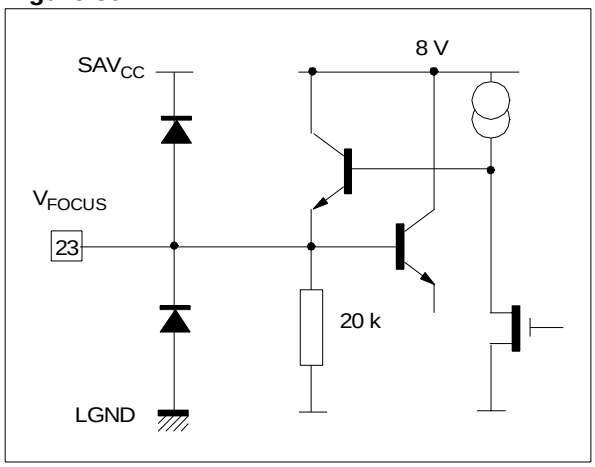


Figure 39.



INTERNAL SCHEMATICS (continued)

Figure 40.

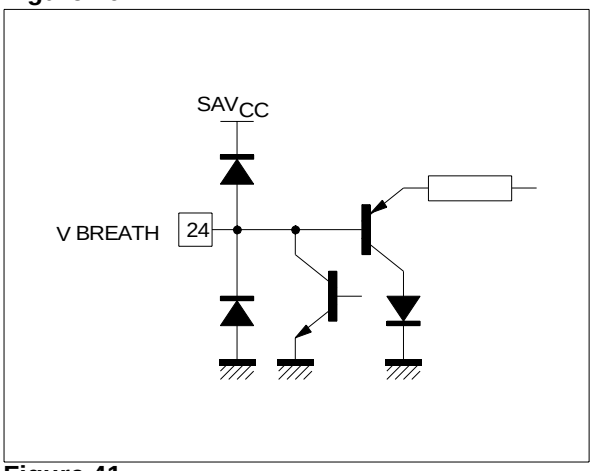


Figure 41.

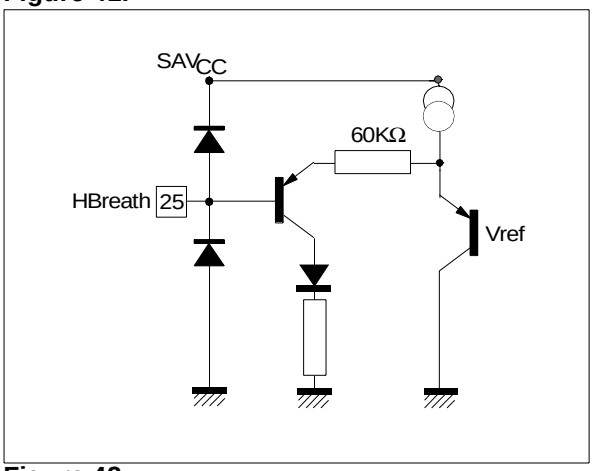


Figure 42.

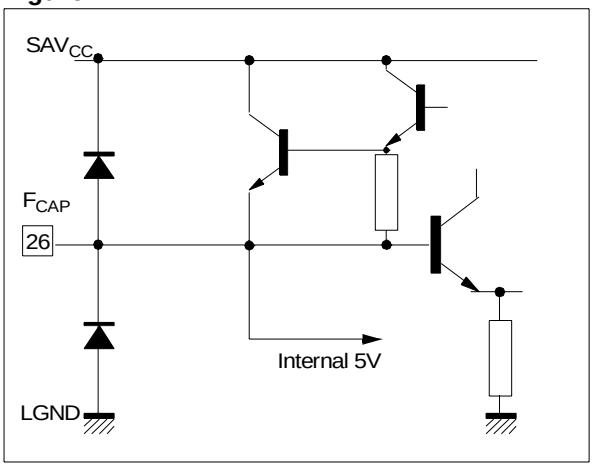
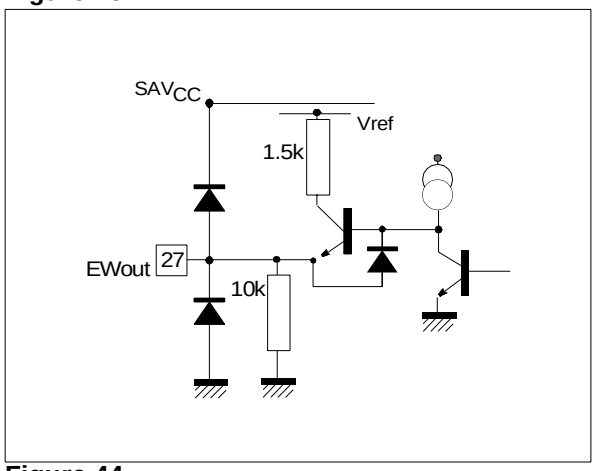


Figure 43.



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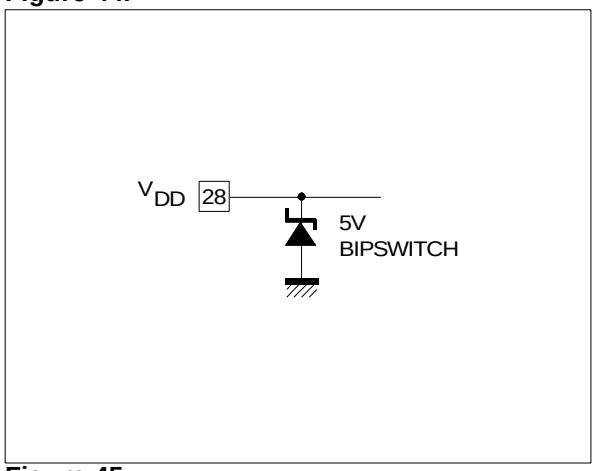
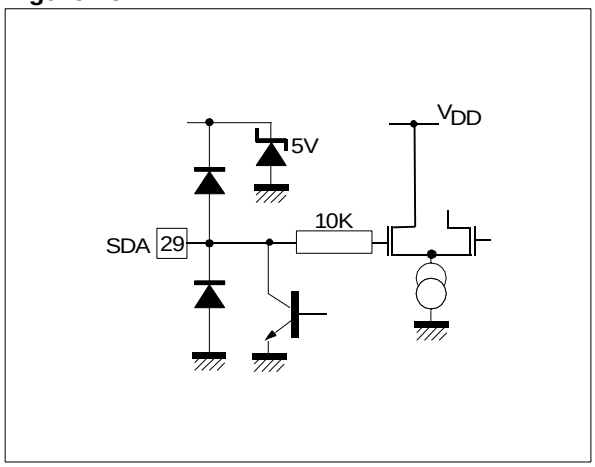


Figure 45.



INTERNAL SCHEMATICS (continued)

Figure 46.

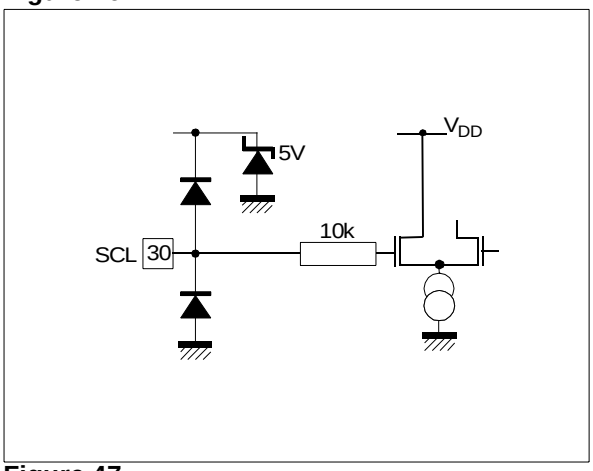
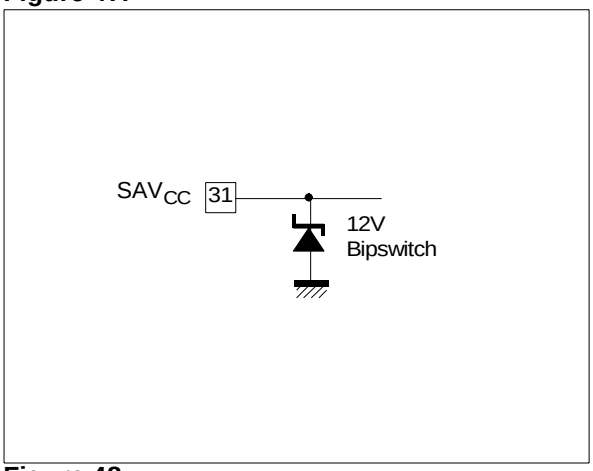


Figure 47.



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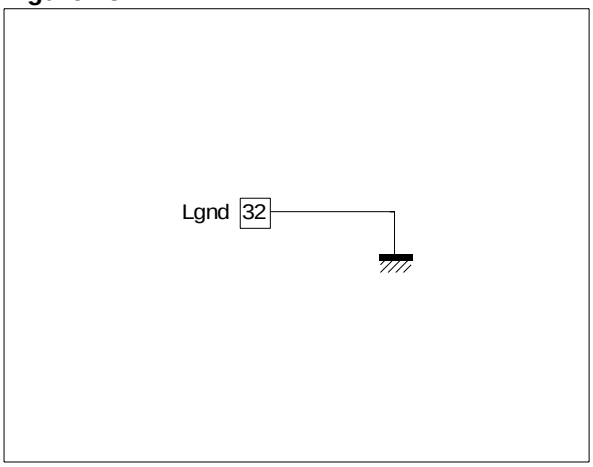

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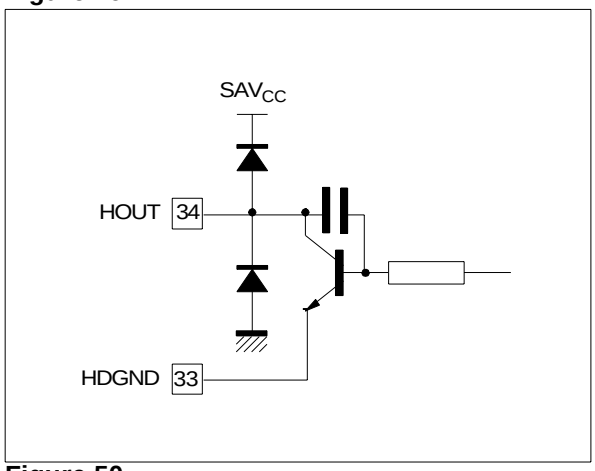


Figure 50.

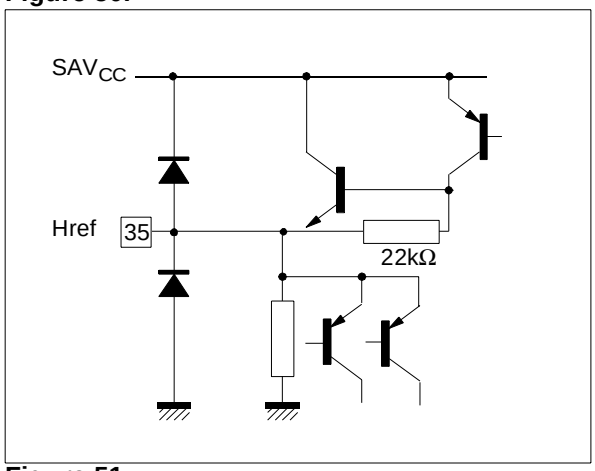
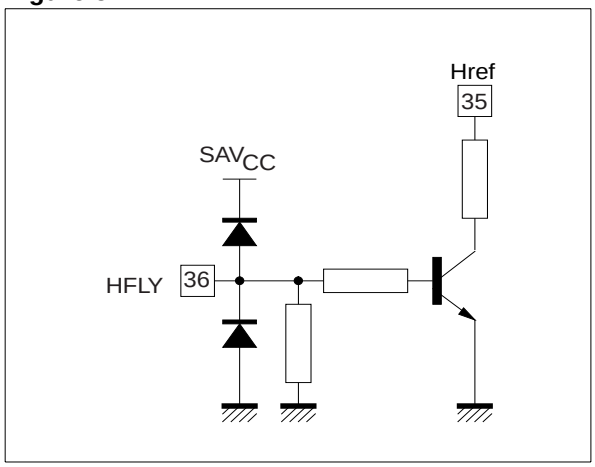


Figure 51.



INTERNAL SCHEMATICS (continued)

Figure 52.

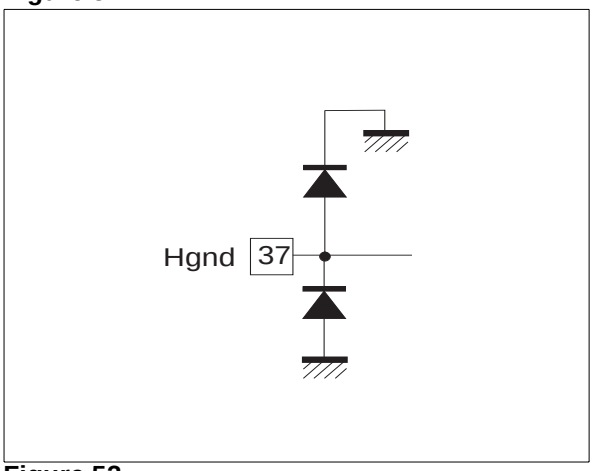


Figure 53.

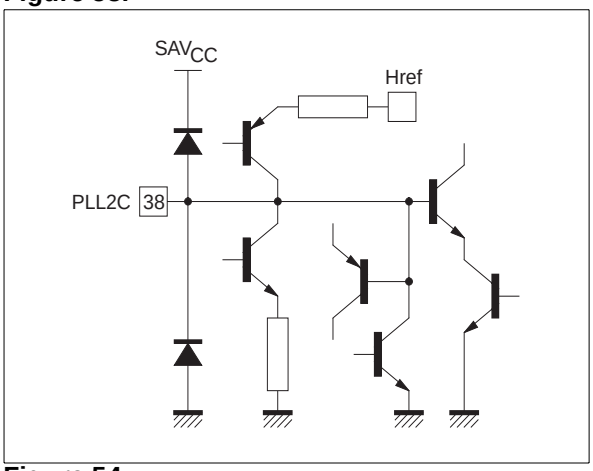


Figure 54.

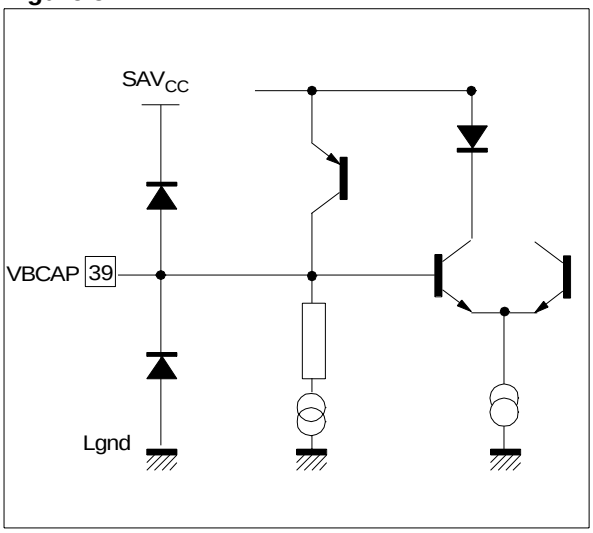


Figure 55.

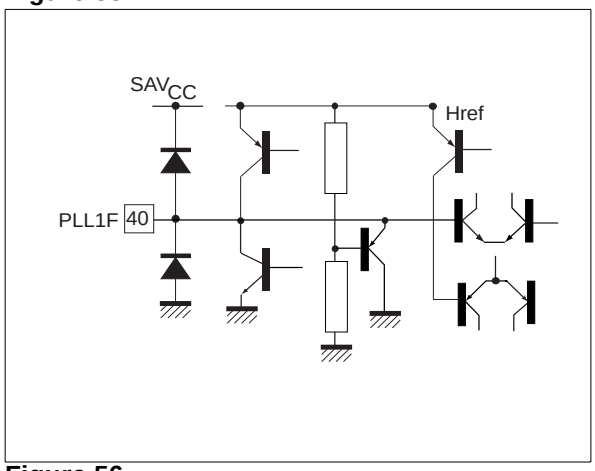


Figure 56.

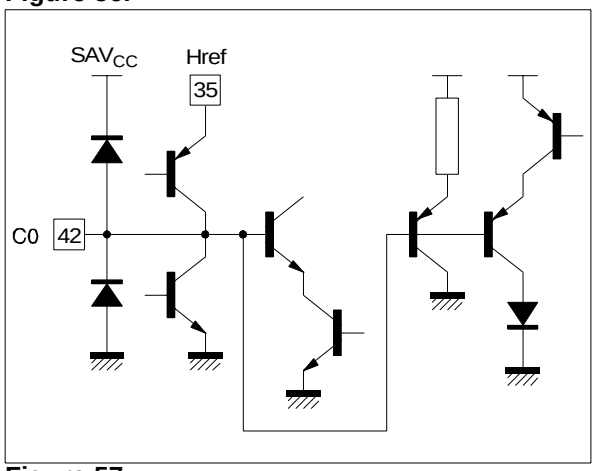
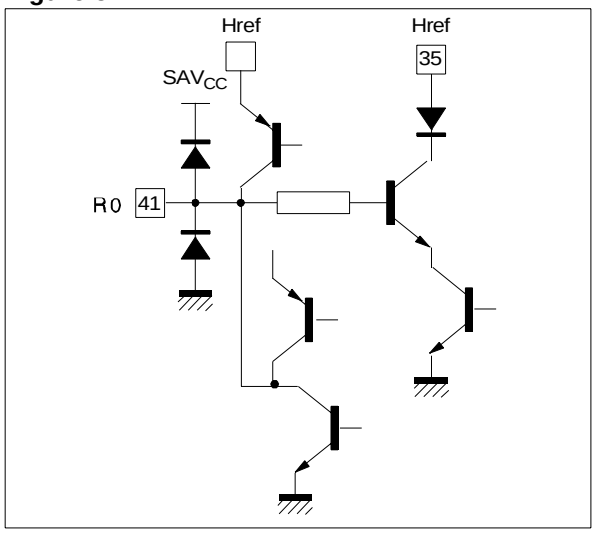


Figure 57.



INTERNAL SCHEMATICS (continued)

Figure 58.

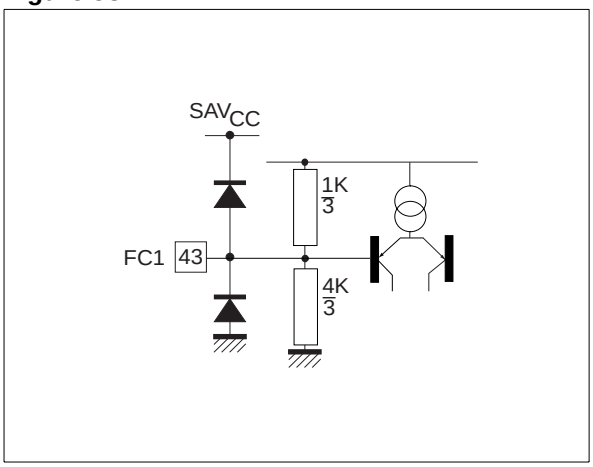


Figure 59.

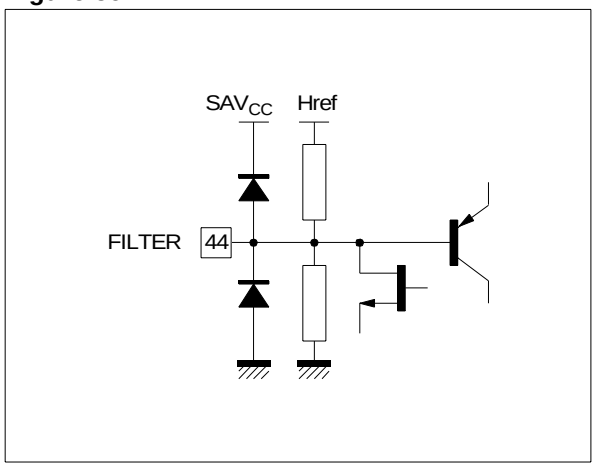
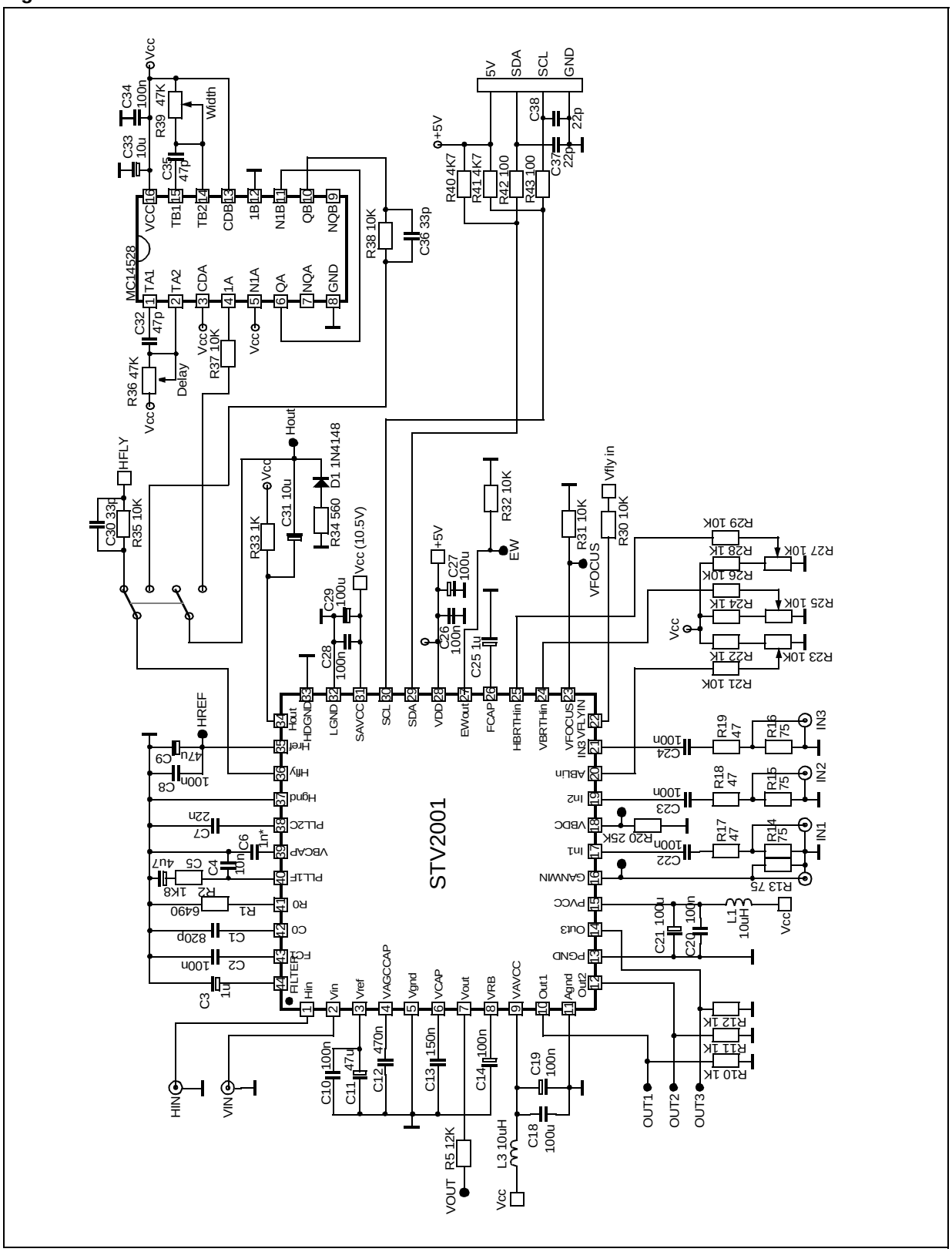
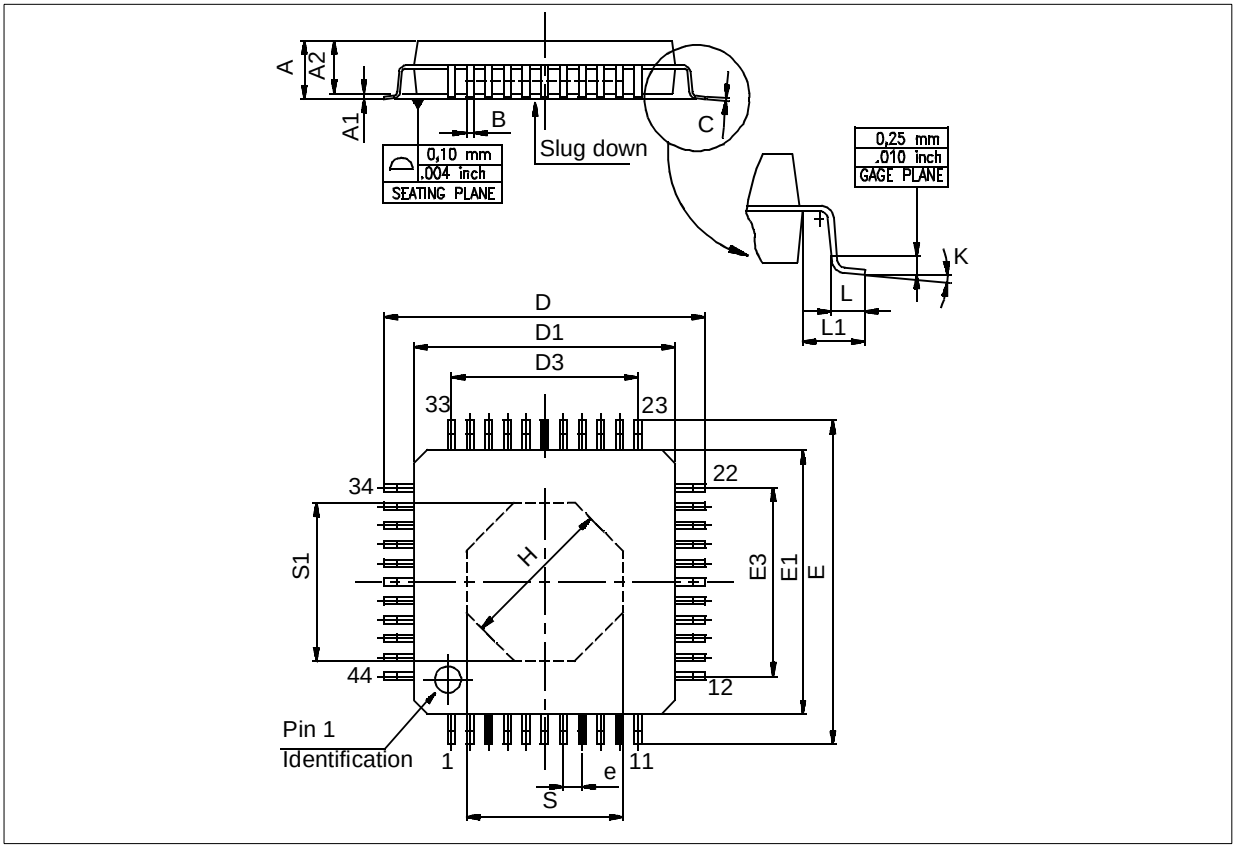


Figure 60. Demonstration board schematic



16 - PACKAGE MECHANICAL DATA

TQFP 44 L SLUG DOWN BODY



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.420		1.540	0.056		0.061
A1	0.065	0.100	0.135	0.003	0.004	0.005
A2	1.360	1.400	1.440	0.054	0.055	0.057
B	0.325	0.350	0.375	0.013	0.014	0.015
c			0.165			0.006
D	11.900	12.000	12.100	0.469	0.472	0.476
D1	9.975	10.000	10.025	0.393	0.394	0.395
D3	7.950	8.000	8.050	0.313	0.315	0.317
e	0.750	0.800	0.850	0.030	0.031	0.033
E	11.900	12.000	12.100	0.469	0.472	0.476
E1	9.975	10.000	10.025	0.393	0.394	0.395
E3	7.950	8.000	8.050	0.313	0.315	0.317
H	5.840	5.890	5.940	0.230	0.232	0.234
L	0.450			0.018		
L1	0.938	1.000	1.063	0.037	0.039	0.042
S	6.000		6.100	0.236		0.240
S1	6.000		6.100	0.236		0.240
K	1.5d	3.5d	5.5d	1.5d	3.5d	5.5d