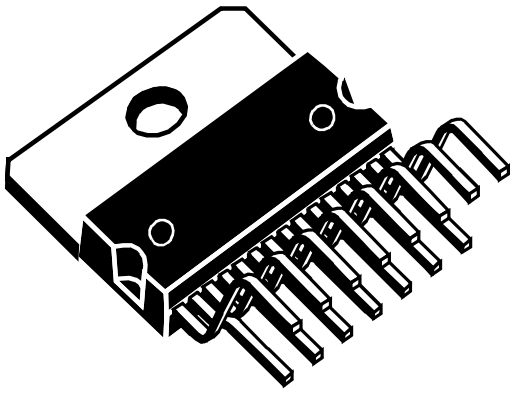
STV9306B

Bus-Controlled Vertical Deflection System with East/West Correction Output Circuit

PRODUCT PREVIEW

Main Features

- **Fully I²C controlled**
- **DMOS Power Half-bridge Amplifier**
- **DC Coupled Operation**
- **Internal Flyback Generator (Up to 60 V)**
- **Self Adapted Sawtooth (50/60 Hz)**
- **100 Hz Operation**
- **Vertical Linearity, Amplitude and Centering Adjustments**
- **Horizontal Width, Pincushion, Trapezoid and Corner Adjustments**
- **4:3 and 16:9 CRT Applications**
- **Thermal Protection**
- **Linear Vertical Zoom Function**
- **E/W Class A Output**
- **Positive/Negative East/West Corner Correction**
- **Few External Components**



Multiwatt15
(Plastic Package)
Order Code: STV9306B

Description

The STV9306B is a fully I²C controlled vertical deflection IC designed for use in 110°, 4:3 or 16:9 CRT applications. It integrates both the vertical deflection and E/W correction circuits required for 110° chassis.

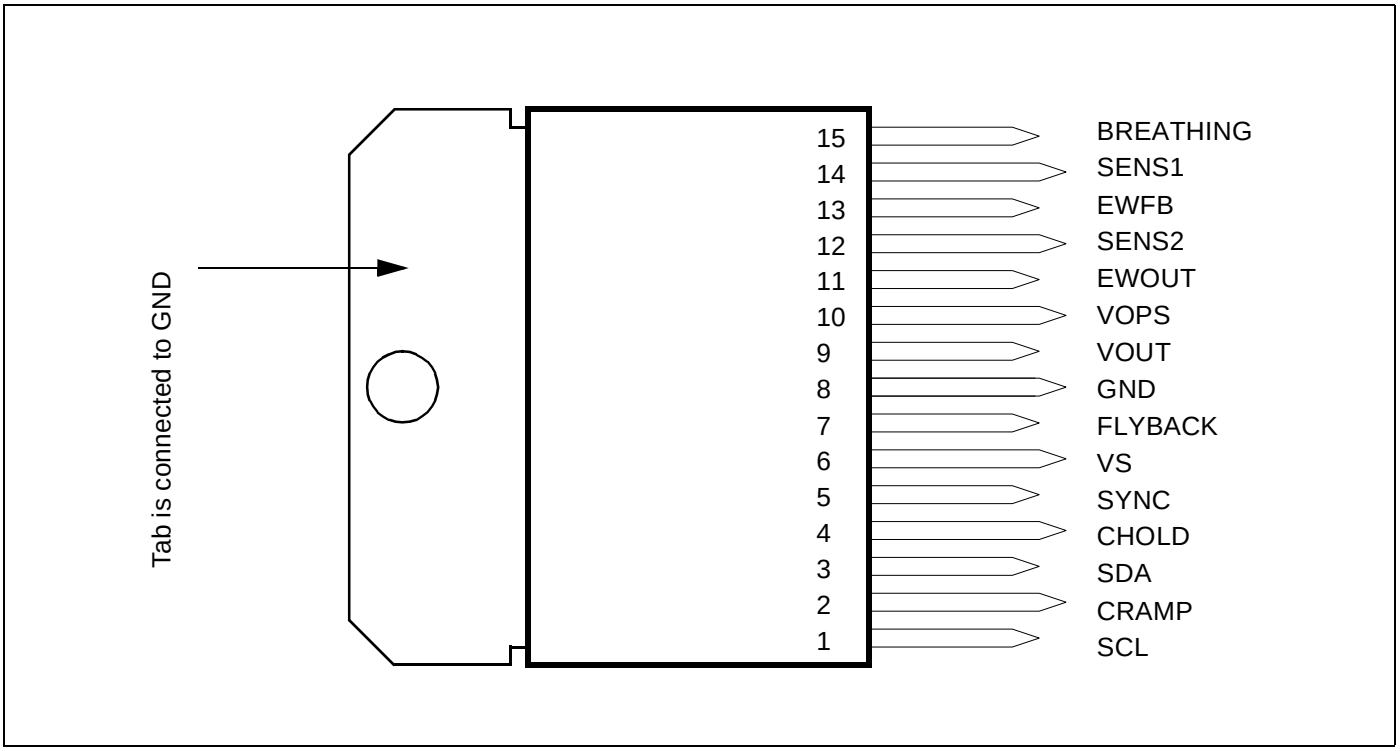


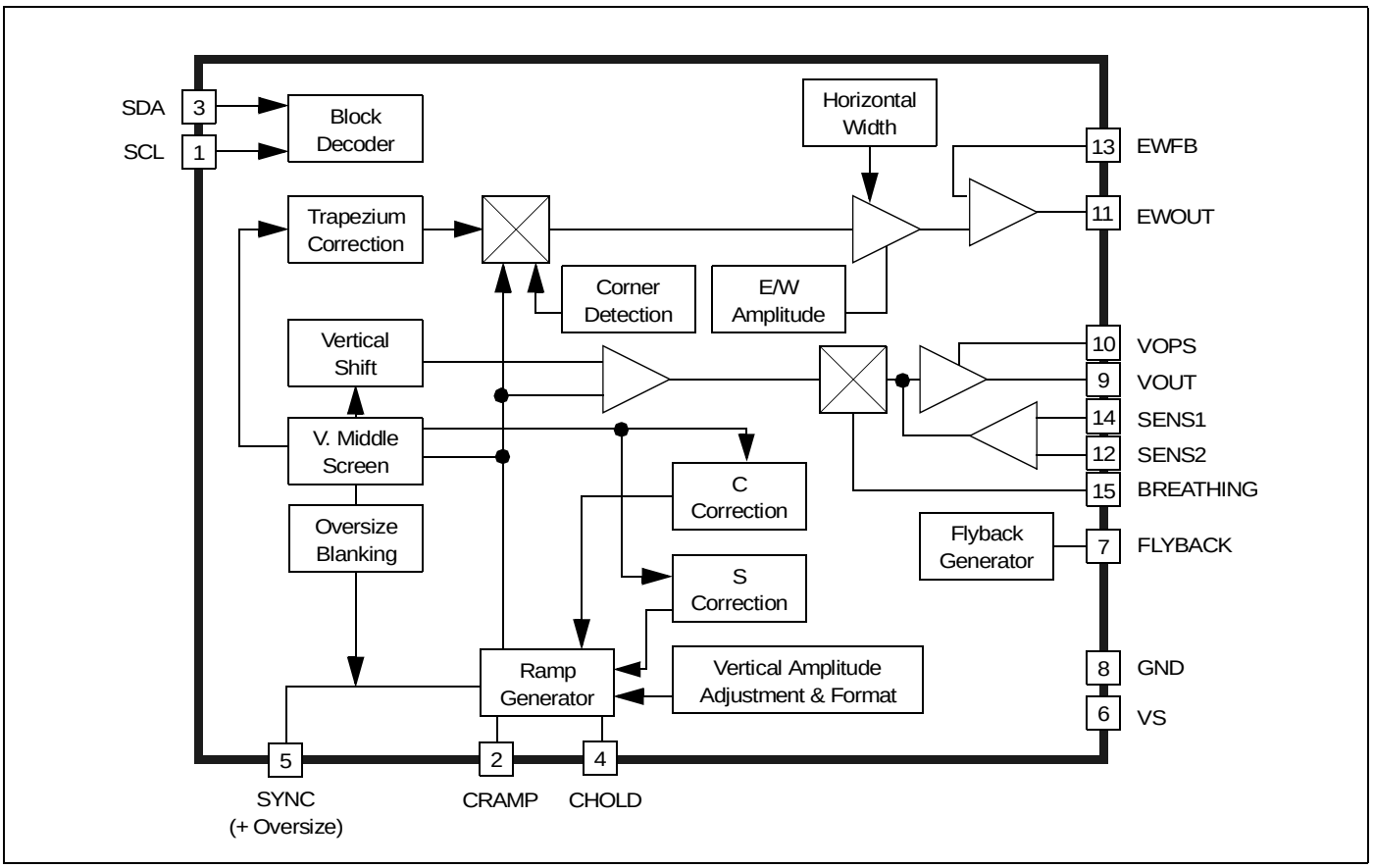
Table of Contents

1 General Description

1.1 I/O Pin Description

Pin No.	Name	Function
1	SCL	I^2C Bus Clock
2	CRAMP	Ramp Capacitor
3	SDA	I^2C Bus Data
4	CHOLD	Hold Capacitor
5	SYNC	Sync Input
6	VS	Supply Voltage
7	FLYBACK	Flyback Output
8	GND	Ground
9	VOUT	Vertical Output
10	VOPS	Vertical Output Power Supply
11	EWOUT	E/W Output
12	SENS2	Vertical Current Sense 2
13	EWFB	E/W Feedback
14	SENS1	Vertical Current Sense 1
15	BREATHING	Breathing Input

Figure 1: STV9306B Block Diagram



2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_S	Supply Voltage	35	V
$V_{FLYBACK}$	Flyback Peak Voltage	60	V
V_I	Input Voltage at Pins 1-3-5-12-13-14-15	-0.3, V_S	V
V_{IS}	Input Voltage at Pins 2-4	10	V
E/W OUT	East/West Output	60	V
T_{OPER}	Operating Temperature	-10, +70	^oC
T_{STG}	Storage Temperature	-55, +150	^oC
T_J	Junction Temperature	+150	^oC

2.2 Thermal Data

Symbol	Parameter		Value	Units
R_{thJC}	Junction-to-Case Thermal Resistance	Max.	3	$^oC/W$
T_{TS}	Junction Temperature for Thermal Shutdown	Min.	140	^oC

2.3 Electrical Characteristics

V_S = 24 V, R_{SENS} = 0.5 Ω, Normal mode, T_{AMB} = 25^o C, unless otherwise specified.

Supply

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_S	Operating Supply Voltage		16		28	V
I_S	Supply Current on Pins 6-10	I_O = 0		40	60	mA

Ramp Generator Control

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{Rlow}	Minimum V_{RAMP} Voltage at Pin 2		1.8	2	2.2	V
t_D	Discharge Time at Pin 2			50		µs
I_{ISY}	Sync Input Current at Pin 5	V_{SY} = 0	-6	-3		µA
V_{THSY}	Sync Threshold Voltage at Pin 5		2.5	3	3.5	V
I_{OB}	Oversize Blank Input Current at Pin 5		70	100		µA
f_{IN}	Input Frequency Range	CRAMP = 100 nF V_SAW = 100000	40		70	Hz

Vertical Power Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{IBR}	Breathing Current Input Current at Pin 15	V_{BREATH} = 0V	-10	-5		µA
V_{BREATH}	Breathing Operating Voltage at Pin 15		0		9	V
V_{7H}	Saturation Voltage to supply at Pin 7	I_O = -1.5A, $V_9 > V_S$ 5V		2.5	3.5	V
V_{7L}	Saturation Voltage to Ground at Pin 7	I_O = 100mA		1.5	2.5	V
I_{SENS1} I_{SENS2}	Bias Input Current at Pin 14 Bias Input Current at Pin 12	V_{14} = 0V V_{12} = 0V	-20 -20	-10 -10		µA
V_{9H}	Saturation Voltage to supply at Pin 9 versus Pin 10	I_O = -1.5A		2.5	3.5	V
dV_{9H}/dT	Saturation Voltage Thermal Drift			10		mV/ºC
V_{9L}	Saturation Voltage to Ground at Pin 9	I_O = 1.5A		1.5	2.5	V
dV_{9L}/dT	Saturation Voltage Thermal Drift			5		mV/ºC

Vertical Output (Pin 9)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{PP}	Vertical Deflection Peak-to-Peak Current (see Figure 2)	V_SAW = 000000 V_SAW = 111111		1.8 3.0		A
I_{DC}	Average Current (Vertical Shift) at V_SAW = 111111	V_SH = 01111 V_SH = 11111		-0.35 0.35		A
Z_{SLP}	$Z_{SLP} = \frac{\text{slope in zoom mode}}{\text{slope in normal mode}}$ See Figure 3	V_ZOOM = 000 V_ZOOM = 111		106 130		%
Unzoom	Vertical Current (Peak-to-Peak) in Unzoom mode versus Normal mode	I_{PP}(Unzoom mode)/ I_{PP}(Normal mode)		75		%
Subtitle	Vertical Current Shift versus Peak-to-Peak Current (Normal mode)	I_{SHIFT}/I_{PP}		$\frac{Z_{SLP} - 100}{2}$		%
I_{SC}	S Correction = I_{SC}/I_{PP} (see Figure 4)	V_SC = 0000 V_SC = 1111		0 6		%
I_{CC}	C Correction = I_{CC}/I_{PP} (see Figure 5)	V_CC = 0111 V_CC = 1111		-3 3		%
BR	$\text{Breathing BR} = \frac{I_{PP} - I_{PPB}}{I_{PP}}$ See Figure 6	BR_{Min}. V_{15} = 9V BR_{Max}. V_{15} = 1V		0 10		%
R_{SENS}	Minimum External Sense Resistor		0.5			Ohm

East/West Correction

(V_SAW = 100000, V_SH = 10000, V_SC = 0000, V_CC = 1000) (see Figure 7)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{BIAS}	Input Bias Current at Pin 13		-1	-0.5		µA
V_{PAR}	Parabola Amplitude (Pincushion Correction) at Pin 13 (see Figure 8)	EW_AMP = 00000 EW_AMP = 11111		0 5		V V
V_{DCEW}	Horizontal Width Adjustment at Pin 13 (see Figure 9)	EW_DC = 00000 EW_DC = 11111 HShrink active		1 6 +5.5		V
Trap	Trapezium Correction at Pin 13 Trap = $V_{PARTUP}/V_{PARTLOW}$ (see Figure 10)	EW_TRAP = 01111 EW_TRAP = 11111		0.6 1.7		
Corner	Parabola Corner Correction at Pin 13 (see Figure 11) Corner = V_{COR}/V_{PAR}	EW_CORNER = 00000 EW_CORNER = 11111		0 60		%
No Corner	EW_CORNER Code for Parabola with No Corner Correction			0 1111		Binary Code
V_{11L}	Saturation Voltage	I_{OUT} = 500 mA			2	V
I_{MAX}	E/W Sink Average Current				0.5	A

Figure 2: Vertical Amplitude and Position

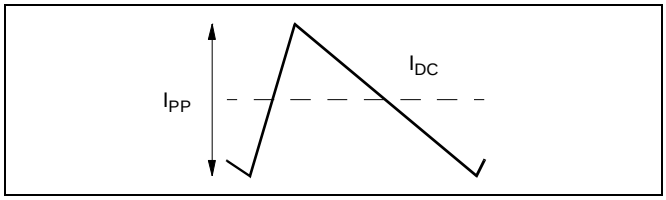


Figure 3: Zoom Mode

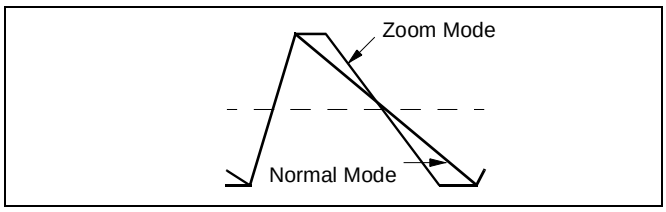


Figure 4: S Correction

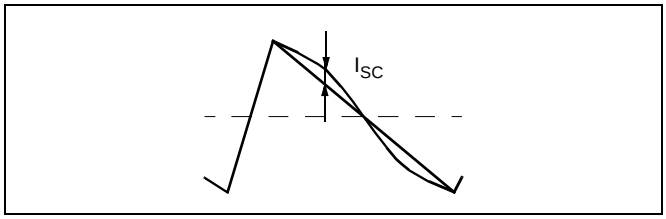


Figure 5: C Correction

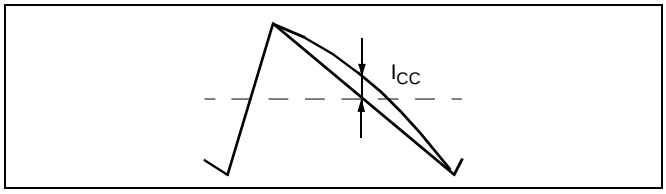


Figure 6: Breathing Correction

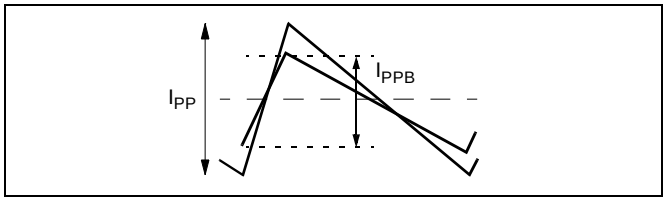


Figure 7: E/W Output

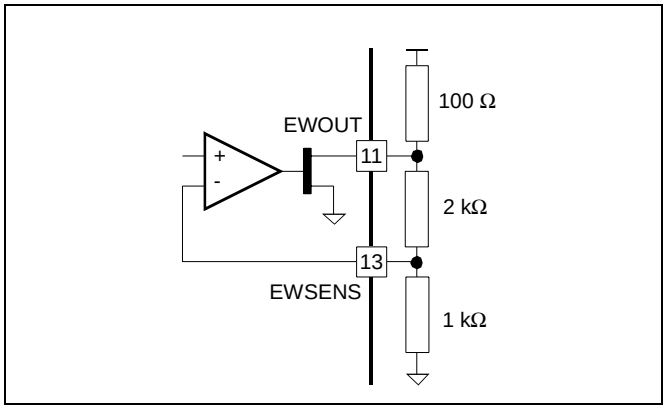


Figure 8: Pincushion Correction

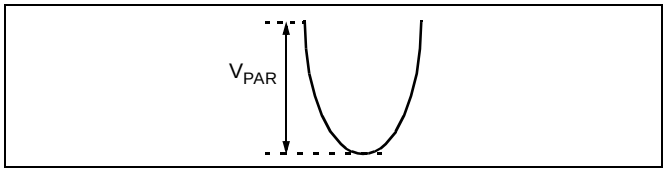


Figure 9: Horizontal Width Adjustment

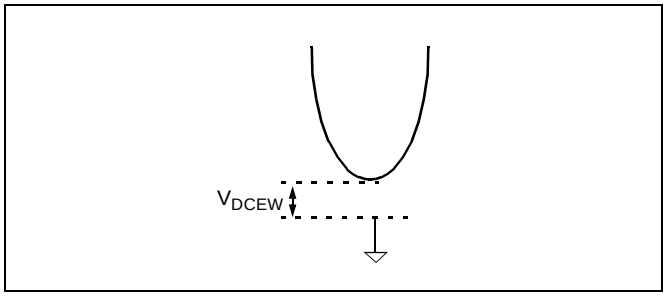


Figure 10: Trapezium Correction

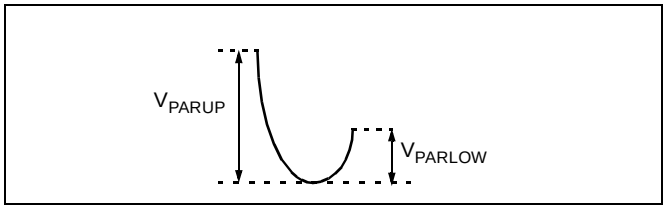
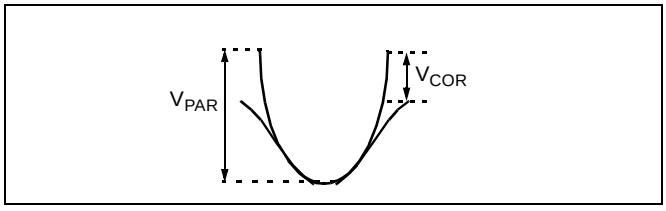


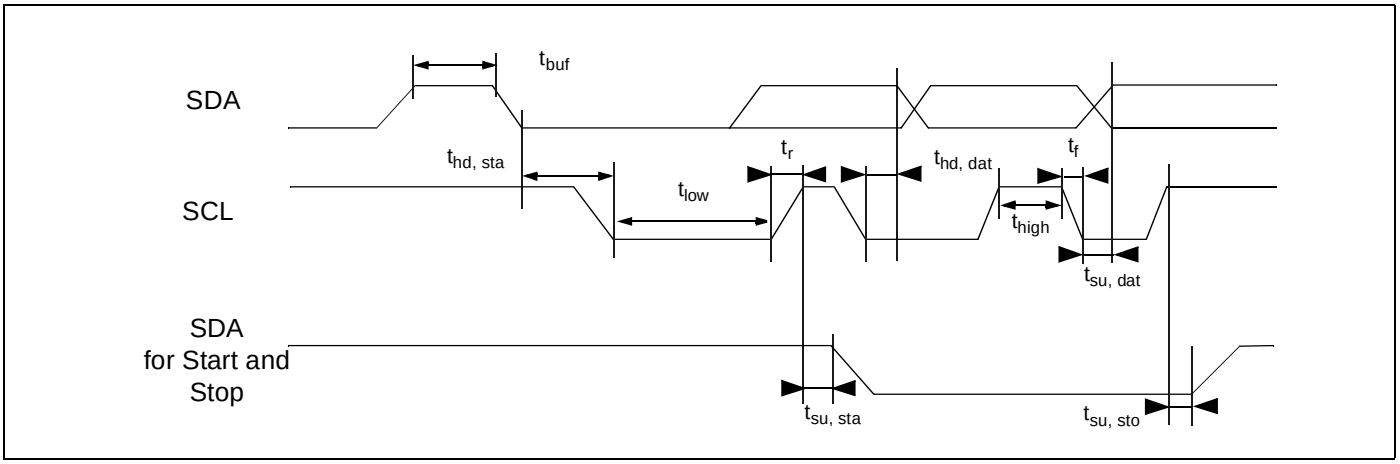
Figure 11: Corner Correction



2.4 I²C Bus Interface

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
SCL (Pin 1)						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3.0		5.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5V	-10		10	µA
f_{SCL}	Clock Frequency		0		100	kHz
t_R	Input Rise Time	1.5V to 3V			1000	ns
t_F	Input Fall Time	1.5V to 3V			300	ns
C_I	Input Capacitance				10	pF
SDA (Pin 3)						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		3.0		5.5	V
I_{LI}	Input Leakage Current	V_{IN} = 0 to 5V	-10		10	µA
C_I	Input Capacitance				10	pF
t_R	Input Rise Time	1.5V to 3V			1000	ns
t_F	Input Fall Time	1.5V to 3V			300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3mA			0.4	V
t_F	Output Fall Time	3V to 1.5V			250	ns
C_L	Load Capacitance				400	pF
Timing						
t_{LOW}	Clock Low Period		4.7			µs
t_{HIGH}	Clock High Period		4.0			µs
t_{SU}, DAT	Data Set-up Time		250			ns
t_{HD}, DAT	Data Hold Time		0		340	ns
t_{SU}, STO	Set-up Time from Clock High to Stop		4.0			µs
t_{BUF}	Start Set-up Time following a Stop		4.7			µs
t_{HD}, STA	Start Hold Time		4.0			µs
t_{SU}, STA	Start Set-up Time following Clock Low-to High Transition		4.7			µs

Figure 12: Serial Bus Timing



2.5 I²C Bus Selection

2.5.1 Write Mode: Slave Address: 1000 1100 (8C)

Subaddress								Data							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	X	X	X	X	0	Vertical Amplitude						X	1
0	0	1	X	X	X	X	0	Sign	Vertical Shift				X	X	1
0	1	0	X	X	X	X	0	S. Correction				Zoom Mode		Subtitle	1
0	1	1	X	X	X	X	0	Sign	C. Correction			Zoom Amplitude			1
1	0	0	X	X	X	X	0	Horizontal Width					Hshr	X	1
1	0	1	X	X	X	X	0	E/w Correction					X	X	1
1	1	0	X	X	X	X	0	E/w Corner Correction					Ext. Transistor	X	1
1	1	1	X	X	X	X	0	Sign	Trap. Correction				HiZ	X	1

Data

B7	B6	B5	B4	B3	B2	B1	B0	
Vertical Amplitude (V_SAW)								
0	0	0	0	0	0	X	1	Min. Amplitude
1	1	1	1	1	1	X	1	Max. Amplitude
Vertical Shift (V_SH)								
X	0	0	0	0	X	X	1	Min. Shift Level
X	1	1	1	1	X	X	1	Max. Shift Level
1	X	X	X	X	X	X	1	Positive Shift
0	X	X	X	X	X	X	1	Negative Shift
S Correction (V_SC) & Zoom Position								
0	0	0	0	X	X	X	1	Min. S Correction
1	1	1	1	X	X	X	1	Max. S Correction
X	X	X	X	0	0	X	1	Normal Mode
X	X	X	X	0	1	X	1	Unzoom
X	X	X	X	1	X	X	1	Zoom
X	X	X	X	X	X	0	1	Subtitle Disabled
X	X	X	X	X	X	1	1	Subtitle Enabled
C Correction (V_CC) & Progressive Zoom (V_ZOOM)								
1	X	X	X	X	X	X	1	Positive C Correction
0	X	X	X	X	X	X	1	Negative C Correction
X	0	0	0	X	X	X	1	Min. C Correction
X	1	1	1	X	X	X	1	Max. C Correction
X	X	X	X	0	0	0	1	Min. Zoom Magnitude
X	X	X	X	1	1	1	1	Max. Zoom Magnitude
Horizontal Width Adjustment (EW_VDC)								
0	0	0	0	0	X	X	1	Hwidth Min. Level
1	1	1	1	1	X	X	1	Hwidth Max. Level
X	X	X	X	X	0	X	1	Hwidth Shrink Disabled
X	X	X	X	X	1	X	1	Hwidth Shrink Enabled

B7	B6	B5	B4	B3	B2	B1	B0	
Pincushion Correction (EW_AMP)								
0	0	0	0	0	X	X	1	Min. Amplitude
1	1	1	1	1	X	X	1	Max. Amplitude
E/W Corner (EW_CORNER)								
0	0	0	0	0	X	X	1	Min. Corner Correction
1	1	1	1	1	X	X	1	Max. Corner Correction
X	X	X	X	X	1	X	1	External E/W Transistor
X	X	X	X	X	0	X	1	Internal E/W Transistor
Trapezium Correction (EW_TRAP) & High Impedance								
1	X	X	X	X	X	X	1	Positive Trapezium Correction
0	X	X	X	X	X	X	1	Negative Trapezium Correction
X	0	0	0	0	X	X	1	Min. Level Correction
X	1	1	1	1	X	X	1	Max. Level Correction
X	X	X	X	X	0	X	1	Normal Mode
X	X	X	X	X	1	X	1	High Impedance Mode

2.5.2 Read Mode: Slave Address: 1000 1101 (8D)

Data

B7	B6	B5	B4	B3	B2	B1	B0	
Thermal Security Status								
0	X	X	X	X	X	X	1	Normal Temperature
1	X	X	X	X	X	X	1	Thermal Security Active
Flyback Pulse Detection Status								
X	0	X	X	X	X	X	1	Flyback Pulse detected
X	1	X	X	X	X	X	1	Lack of Flyback Pulse
Sync Pulse Detection Status								
X	X	0	X	X	X	X	1	Sync Pulse Present
X	X	1	X	X	X	X	1	Lack of Sync Pulse

3 Input/Output Pin Configuration

Figure 13: I²C Bus Clock

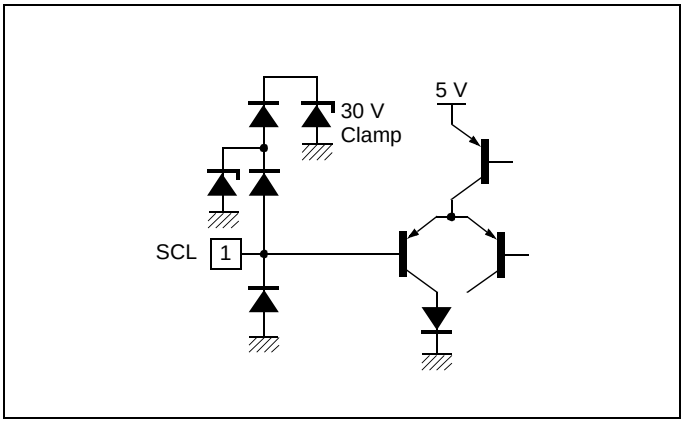


Figure 14: Ramp Capacitor

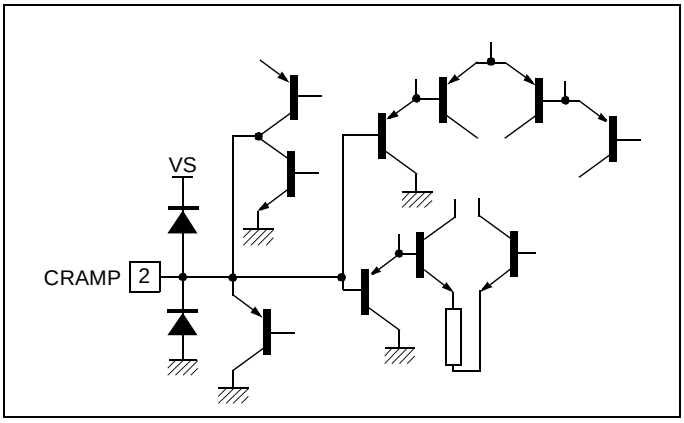


Figure 15: I²C Bus Data

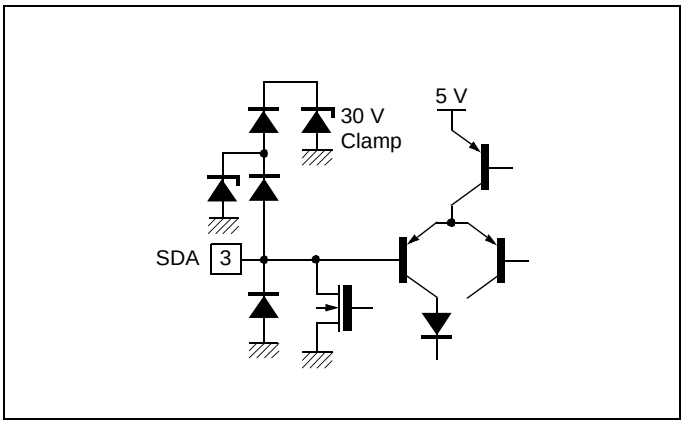


Figure 16: Hold Capacitor

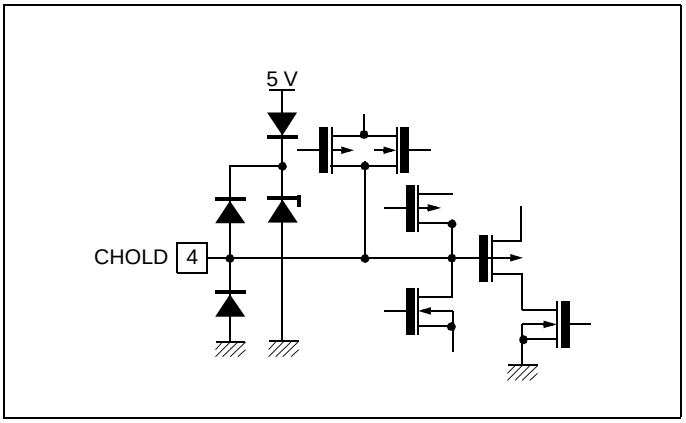


Figure 17: Sync Input

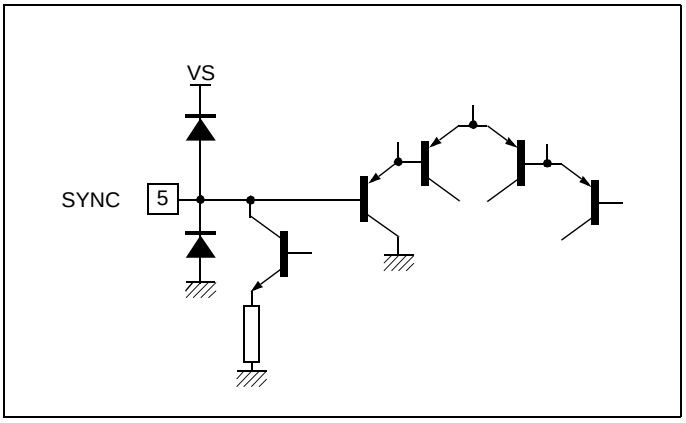


Figure 18: Flyback Output

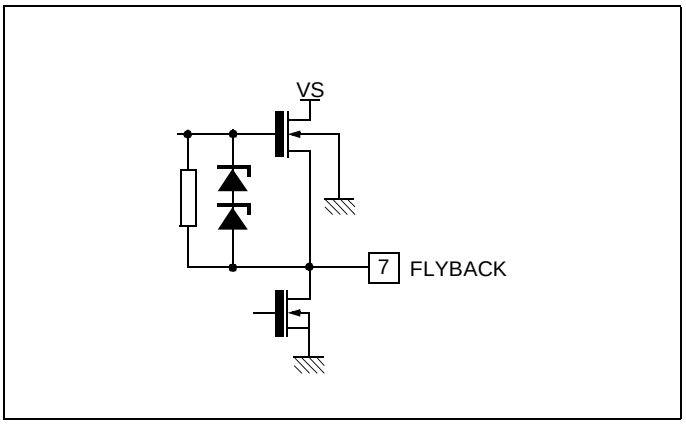


Figure 19: Vertical Output

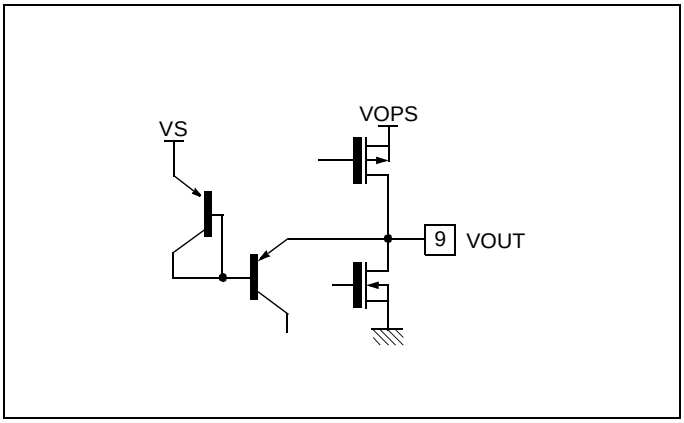


Figure 20: Vertical Output Power Supply

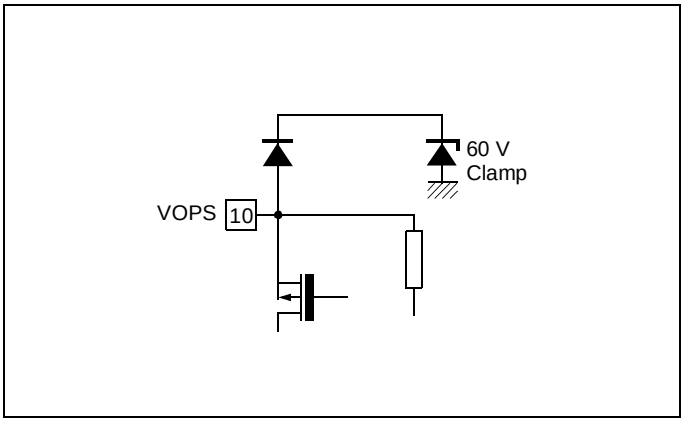


Figure 21: E/W Output

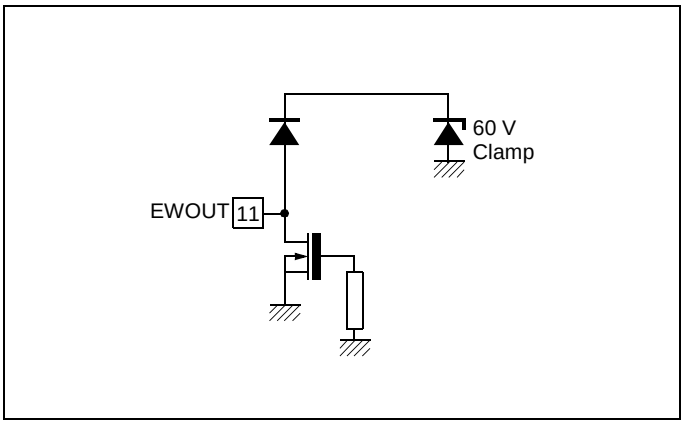


Figure 22: Vertical Current Sense

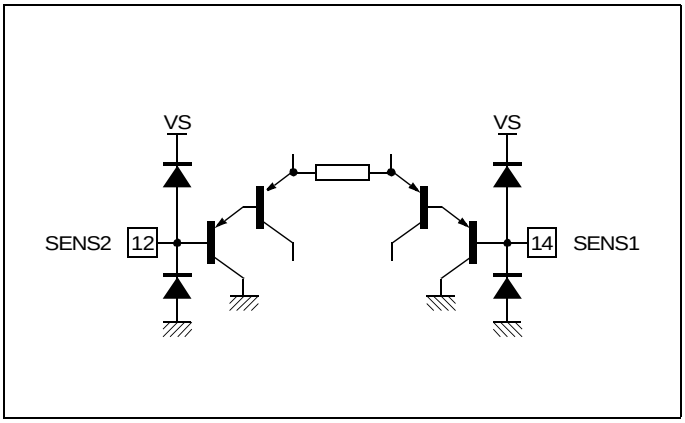


Figure 23: E/W Feedback

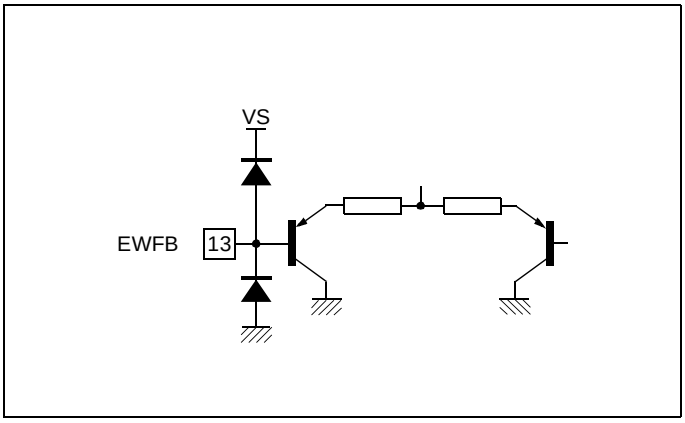
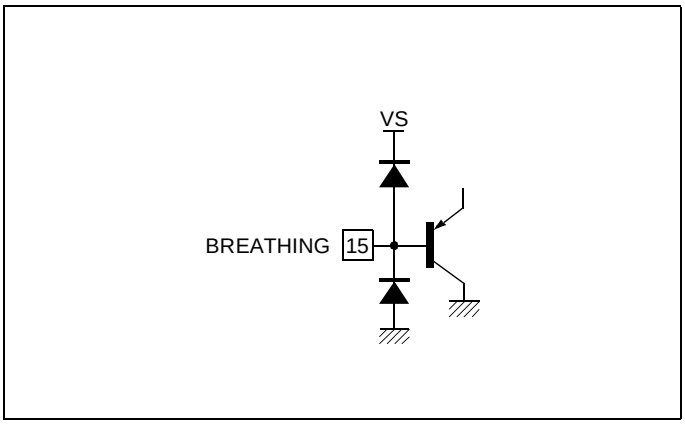
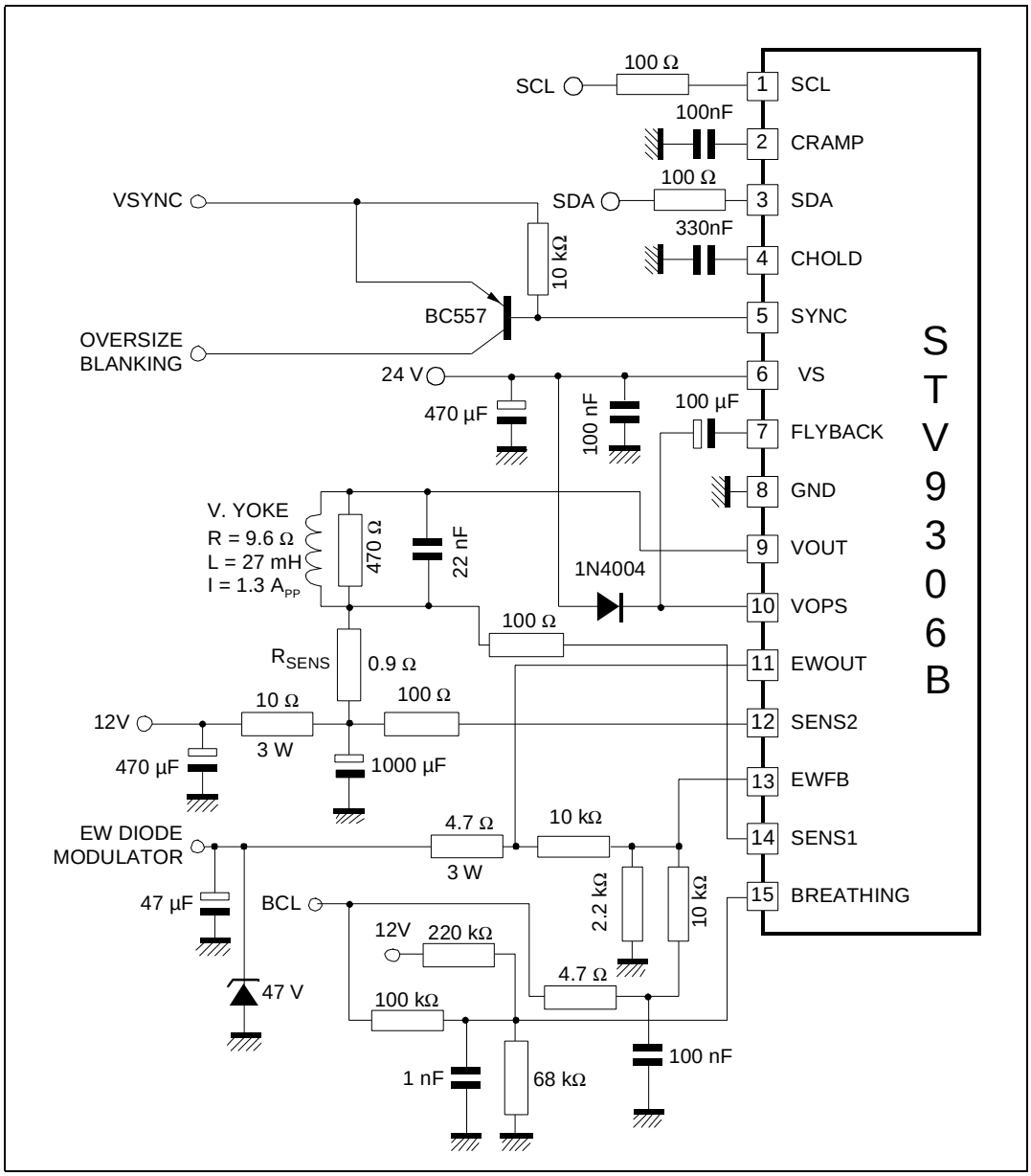


Figure 24: Breathing Input



4 Application Diagram

Figure 25: STV9306B Application Diagram

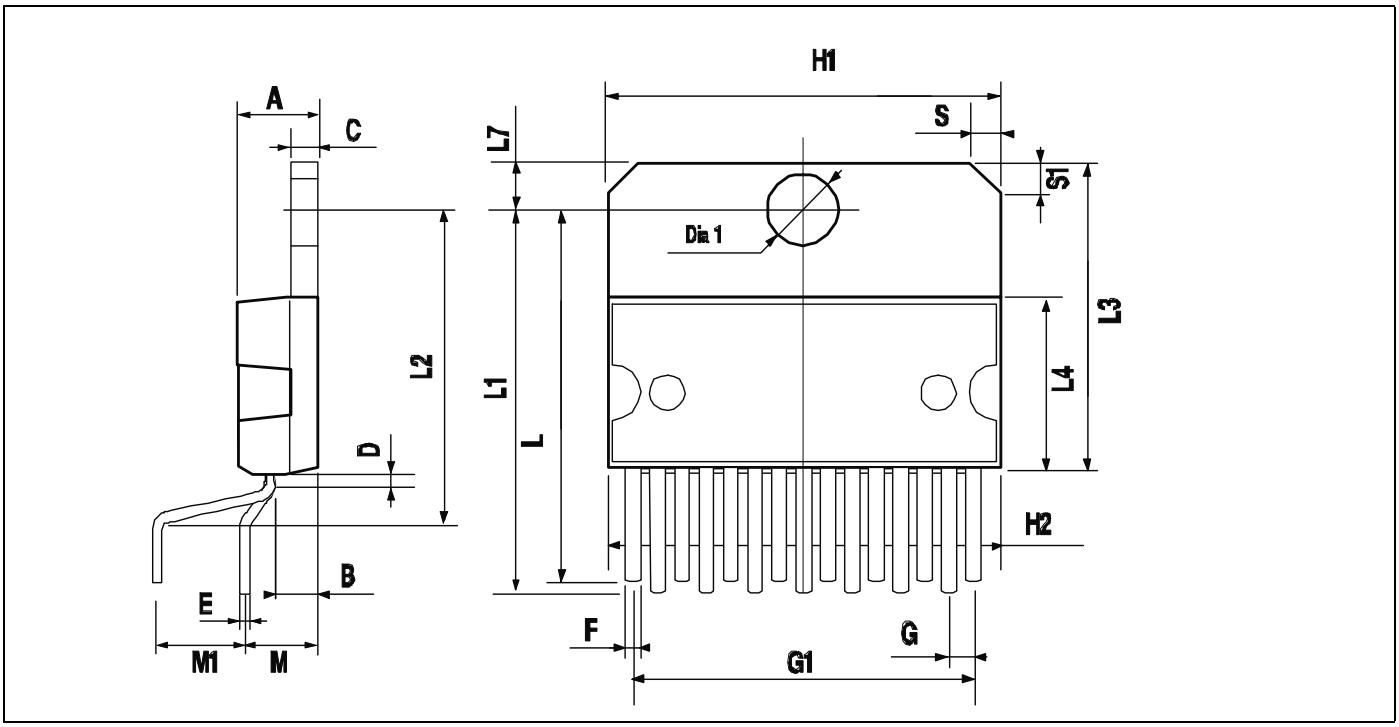


5 List of Modifications

Revision	Modification	Date
0.1	First Issue	14 June 2002
0.2	Modification of Figure 21: E/W Output.	21 June 2002

6 Package Description

Figure 26: 15-Pin Plastic Multiwatt Package



Dimension	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.02	1.27	1.52	0.040	0.050	0.060
G1	17.53	17.78	18.03	0.690	0.700	0.710
H1	19.60			0.772		
H2			20.2			0.795
L	21.9	22.2	22.5	0.862	0.874	0.886
L1	21.7	22.1	22.5	0.854	0.870	0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.50	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.25	4.55	4.85	0.167	0.179	0.191
M1	4.63	5.08	5.53	0.182	0.200	0.218
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia1	3.65		3.85	0.144		0.152

NOTES: