

## N-channel 1500 V, 1.6 $\Omega$ typ., 7 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

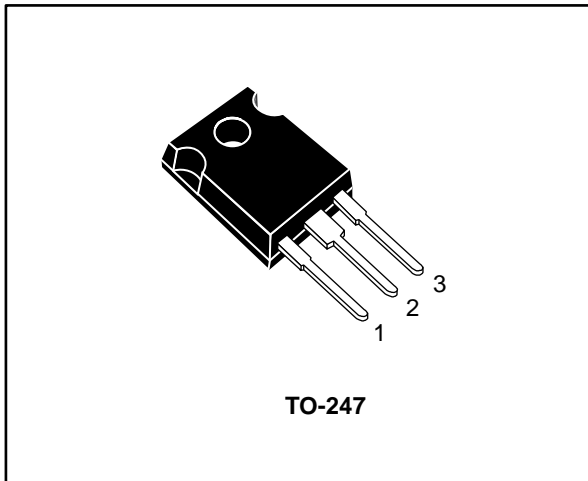
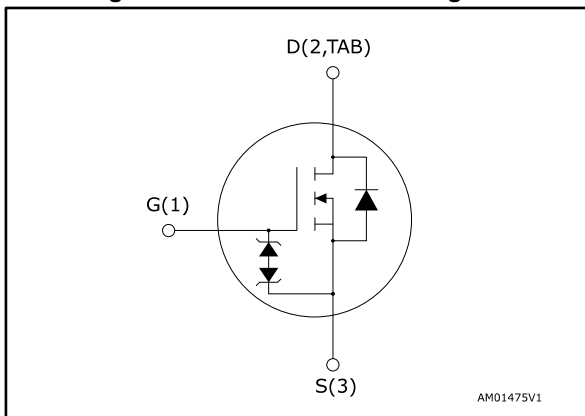


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STW12N150K5	1500 V	1.9 $\Omega$	7 A	250 W

- Industry's lowest R<sub>DS(on)</sub> \* area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW12N150K5	12N150K5	TO-247	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current at $T_C = 25\text{ }^\circ\text{C}$	7	A
$I_D$	Drain current at $T_C = 100\text{ }^\circ\text{C}$	4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_j$	Operating junction temperature	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area

<sup>(2)</sup> $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$

<sup>(3)</sup> $V_{DS} \leq 1200\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb	50	$^\circ\text{C}/\text{W}$

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Max current during repetitive or single pulse avalanche	2	A
$E_{AS}$	Single pulse avalanche energy	900	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 1500\text{ V}$ , $T_C = 125\text{ °C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.5\text{ A}$		1.6	1.9	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	1360	-	pF
$C_{oss}$	Output capacitance		-	80	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.7	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ V to }1200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	82	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	32	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 1200\text{ V}$ , $I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16: "Gate charge test circuit"</a> )	-	47	-	nC
$Q_{gs}$	Gate-source charge		-	8	-	nC
$Q_{gd}$	Gate-drain charge		-	32	-	nC

**Notes:**

<sup>(1)</sup> Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when VDS increases from 0 to 80% VDSS.

<sup>(2)</sup> Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when VDS increases from 0 to 80% VDSS.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 750 \text{ V}$ , $I_D = 3.5 \text{ A}$ , $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 18: "Unclamped inductive load test circuit"</a> )	-	25	-	ns
$t_r$	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
$t_f$	Fall time		-	37	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	302		ns
$Q_{rr}$	Reverse recovery charge		-	3.71		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	24.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 17: "Test circuit for inductive load switching and diode recovery times"</a> )	-	432		ns
$Q_{rr}$	Reverse recovery charge		-	4.71		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	21.8		A

**Notes:**

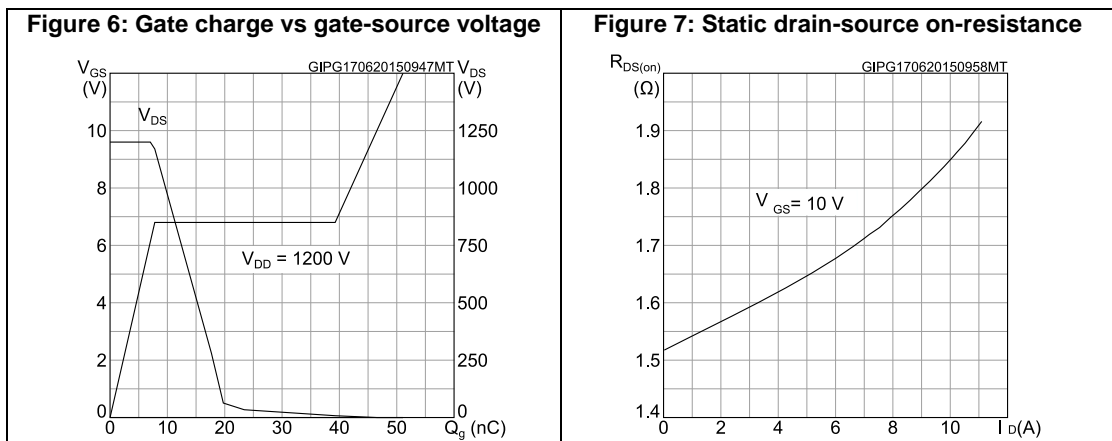
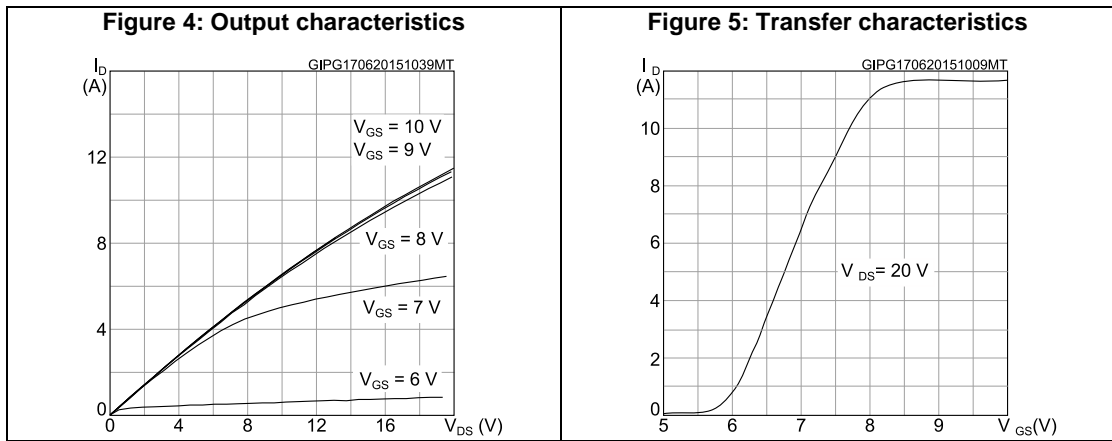
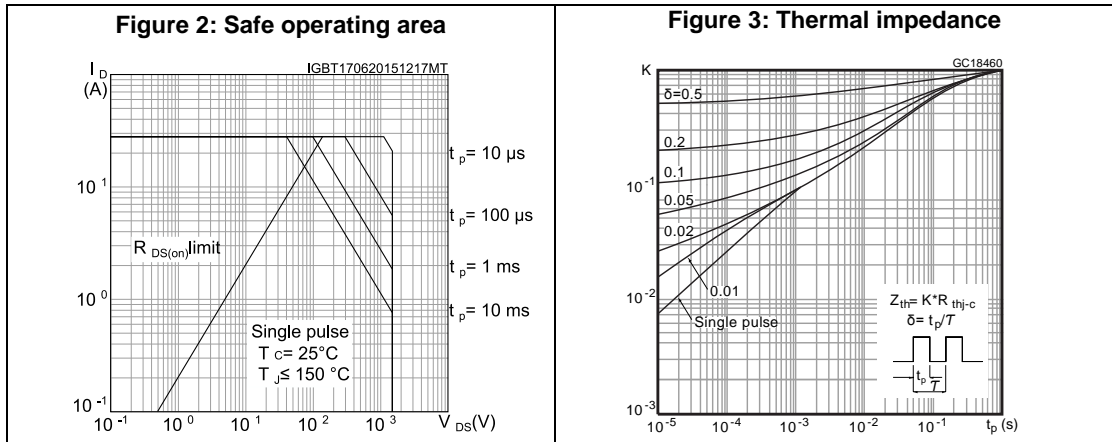
<sup>(1)</sup>Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0 \text{ A}$	30		-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)



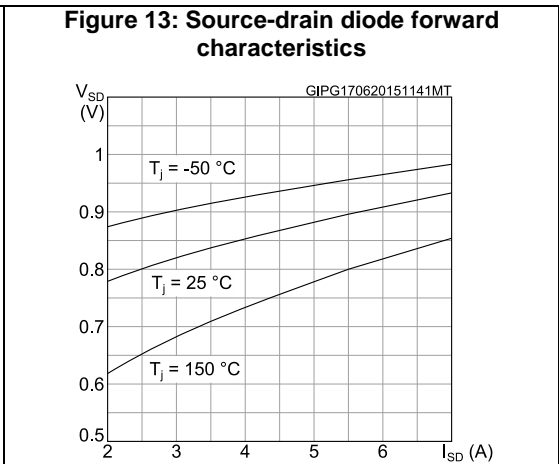
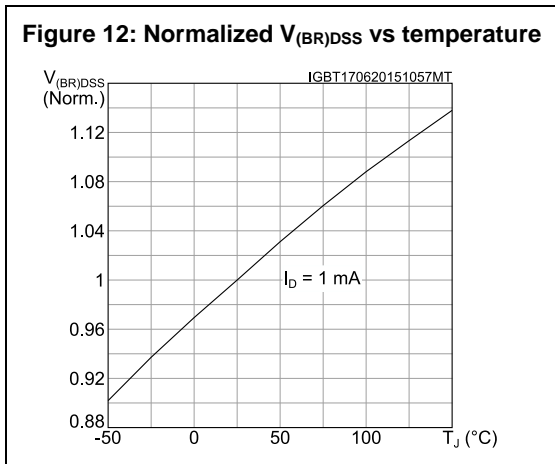
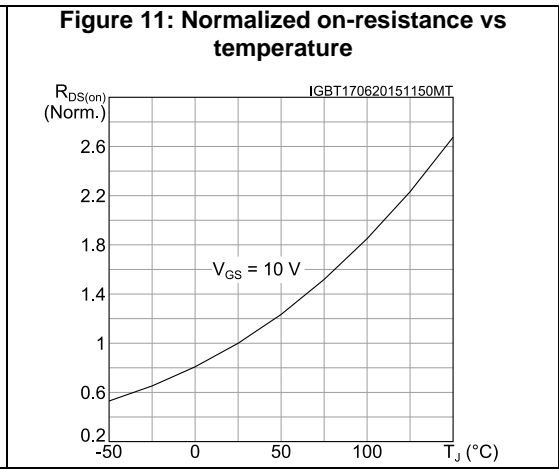
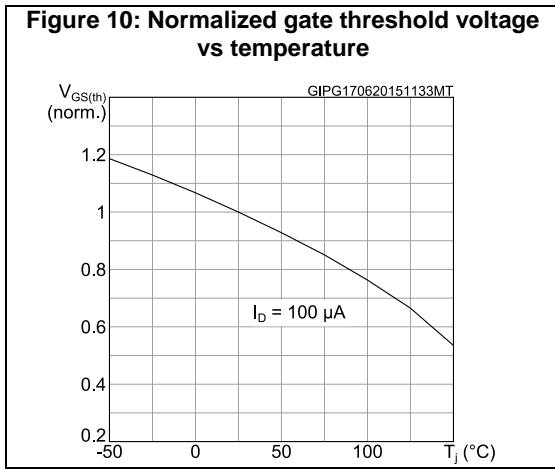
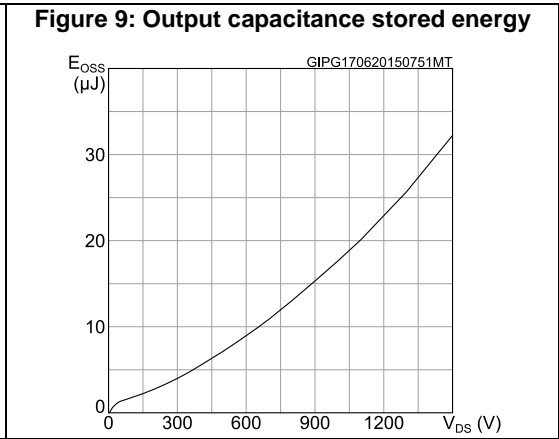
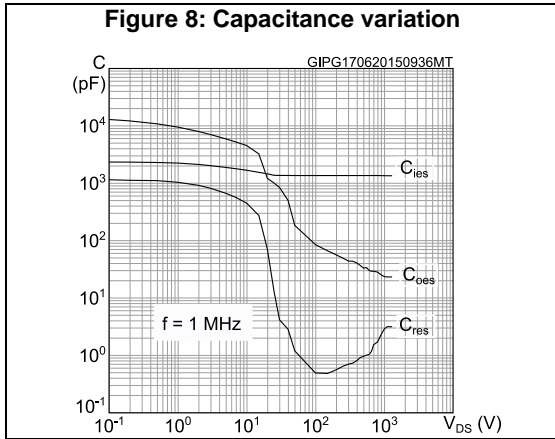
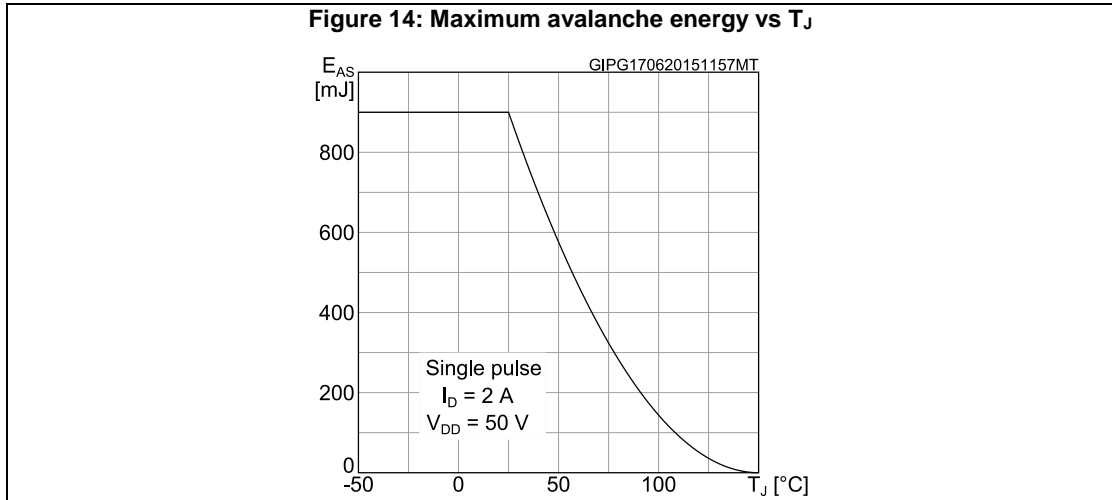
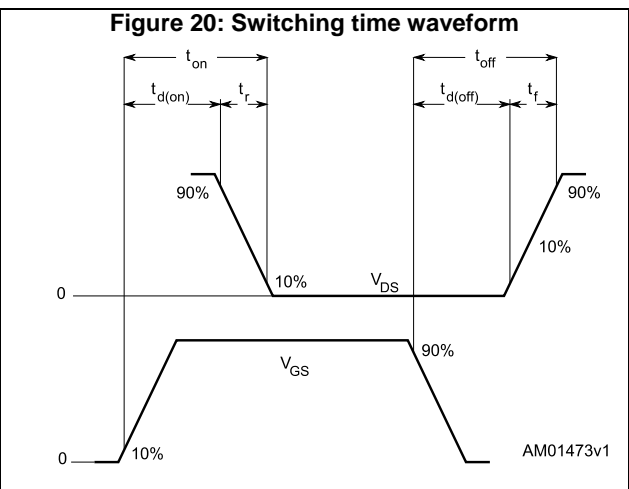
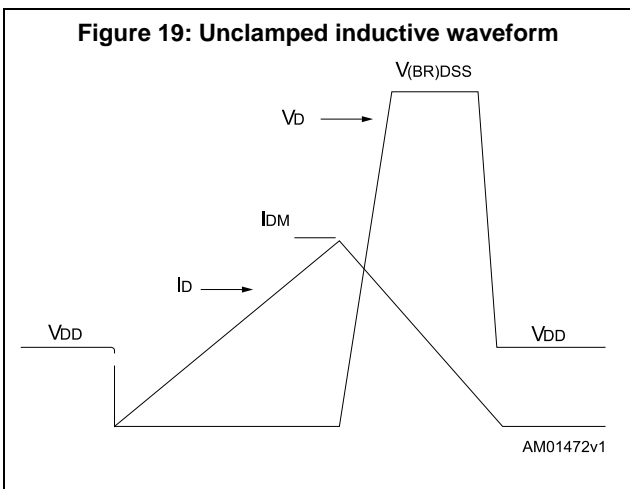
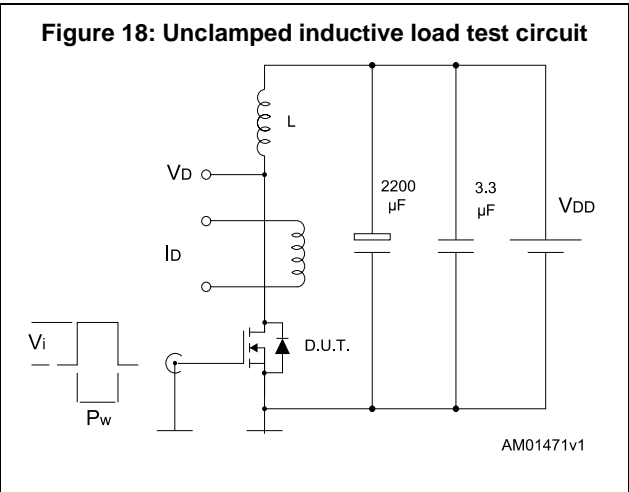
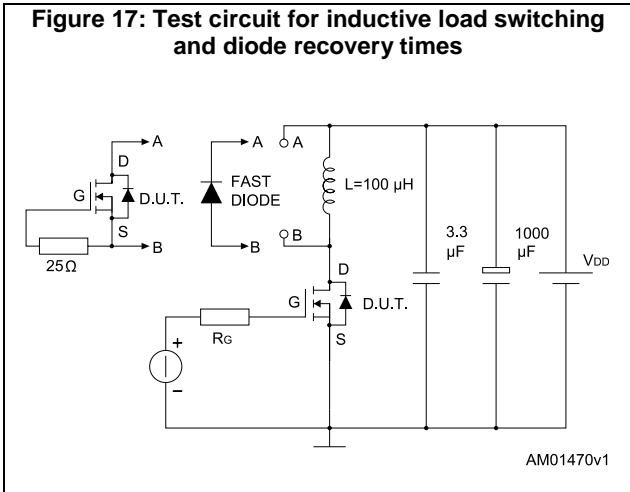
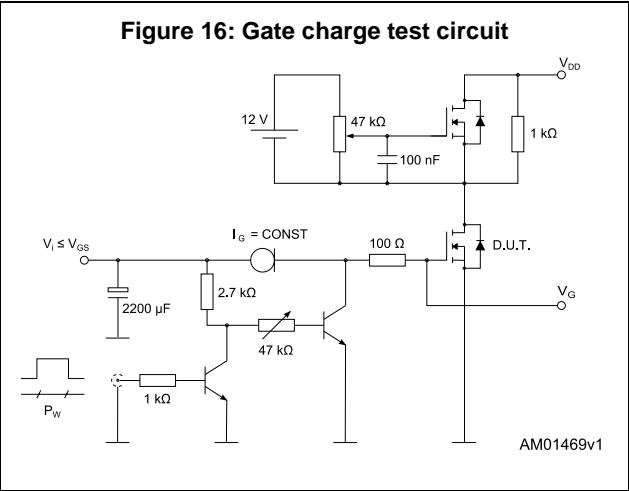
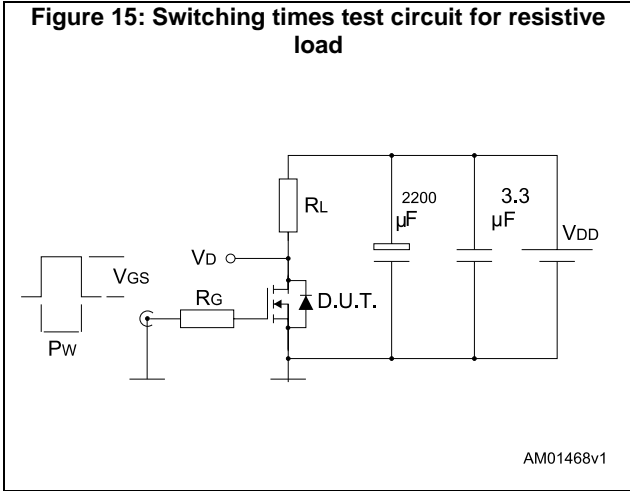


Figure 14: Maximum avalanche energy vs T<sub>J</sub>





### 3 Test circuits



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 21: TO-247 package outline

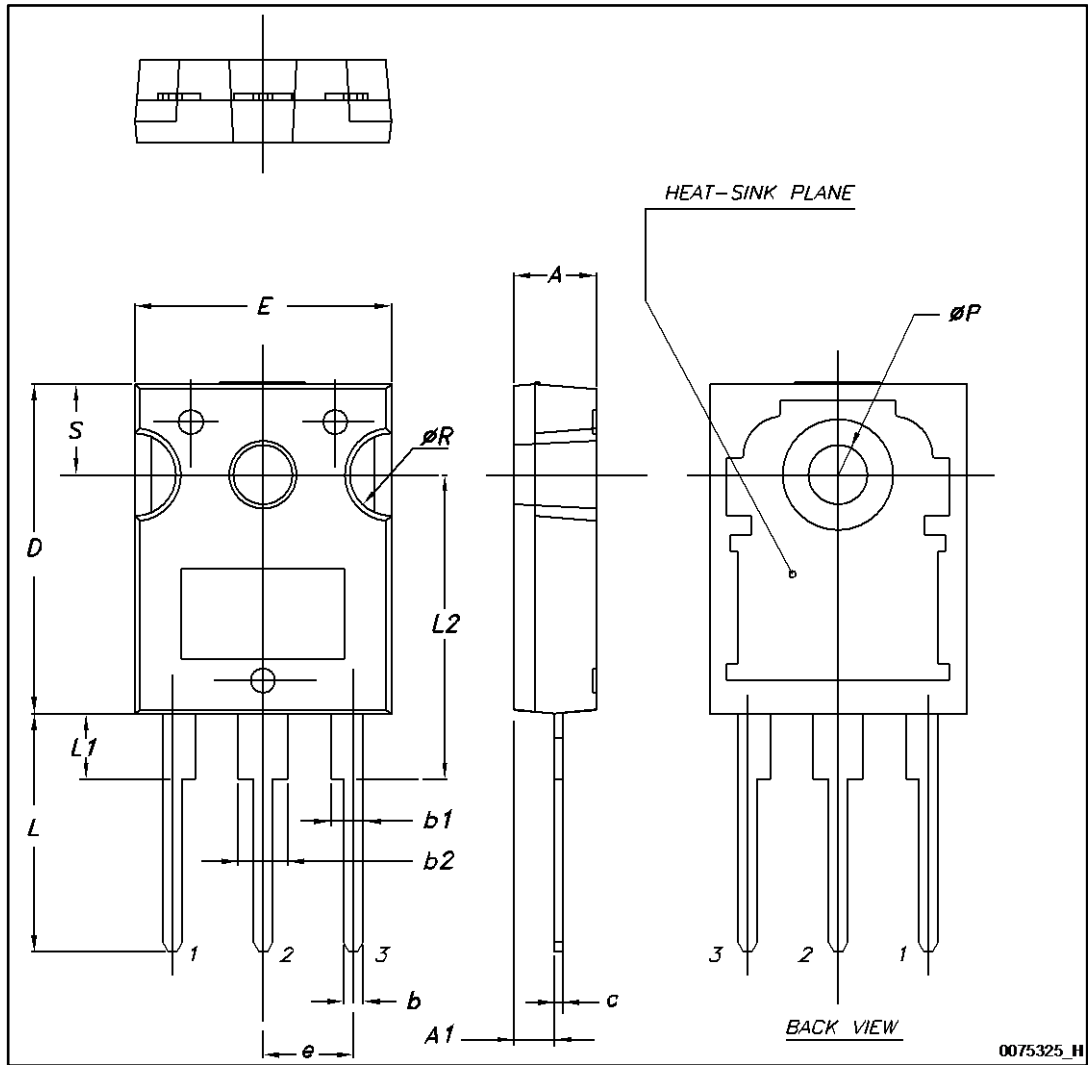


Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
11-May-2015	1	First release.
30-Jun-2015	2	Updated title and features in cover page. Updated <i>Section 4: "Electrical ratings"</i> , <i>Section 5: "Electrical characteristics"</i> . Added <i>Section 5.1: "Electrical characteristics (curves)"</i> . Minor text changes.
07-Jul-2015	3	Updated <i>Section 5.1: "Electrical characteristics (curves)"</i> . Minor text changes.

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