



# STP12NK60Z STF12NK60Z, STW12NK60Z

N-channel 650 V @Tjmax, 0.53 Ω, 10 A TO-220, TO-220FP, TO-247  
Zener-protected SuperMESH™ Power MOSFET

## Features

Type	V <sub>DSS</sub> (@Tjmax)	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>W</sub>
STP12NK60Z	650 V	<0.640 Ω	10 A	150 W
STF12NK60Z	650 V	<0.640 Ω	10 A	35 W
STW12NK60Z	650 V	<0.640 Ω	10 A	150 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability

## Application

- Switching applications

## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, specialties is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage Power MOSFETs.

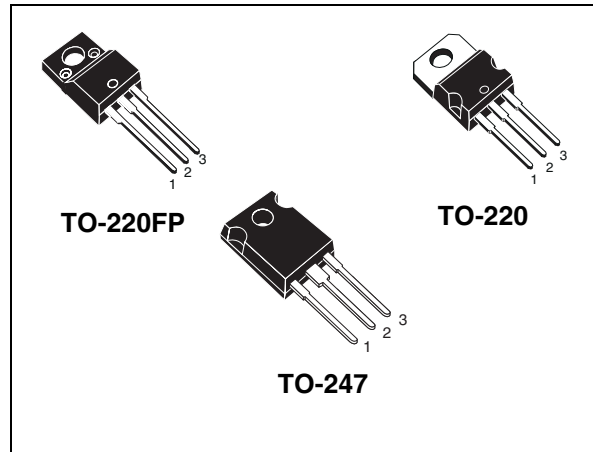


Figure 1. Internal schematic diagram

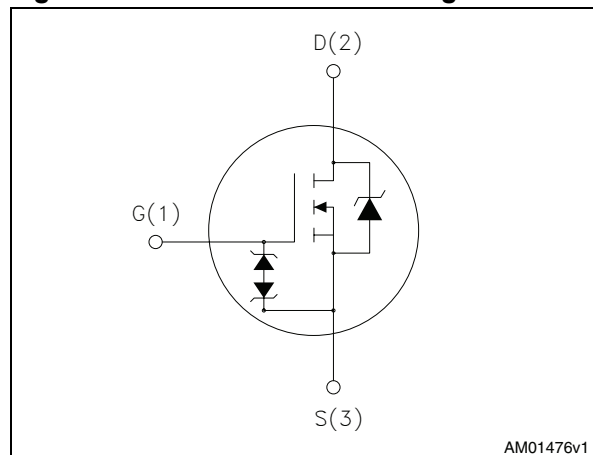


Table 1. Device summary

Order codes	Marking	Package	Packaging
STP12NK60Z	P12NK60Z	TO-220	Tube
STF12NK60Z	F12NK60Z	TO-220FP	Tube
STW12NK60Z	W12NK60Z	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220, TO-247	TO-220FP	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600		V
$V_{GS}$	Gate-source voltage	$\pm 30$		V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	10	10 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6.3	6.3 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	40	40 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	35	W
	Derating factor	1.2	0.27	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 k $\Omega$ )		2500	V
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	4.5		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )		2500	V
$T_{stg}$	Storage temperature	-55 to 150		$^\circ\text{C}$
$T_j$	Max operating junction temperature	150		$^\circ\text{C}$

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 10\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value			Unit
		TO-220	TO-247	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case max	0.83		3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	50	62.5	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300			$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	260	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5\text{ A}$		0.53	0.64	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 5\text{ A}$	-	9	-	S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1740 195 49	-	pF pF pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	101	-	pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 300\text{ V}$ , $I_D = 5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ <i>(see Figure 19)</i>	-	22.5 18.5 55 31.5	-	ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 480\text{ V}$ , $I_D = 10\text{ A}$ , $V_{GS} = 10\text{ V}$ <i>(see Figure 20)</i>	-	59 10 32	-	nC nC nC

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 10\text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	358		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50\text{ V}$	-	3		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 24)	-	17		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	-	460		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 50\text{ V}, T_j = 150\text{ }^\circ\text{C}$	-	4.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 24)	-	18.2		A

1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$BV_{GSO}^{(1)}$	Gate-Source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30	-	-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

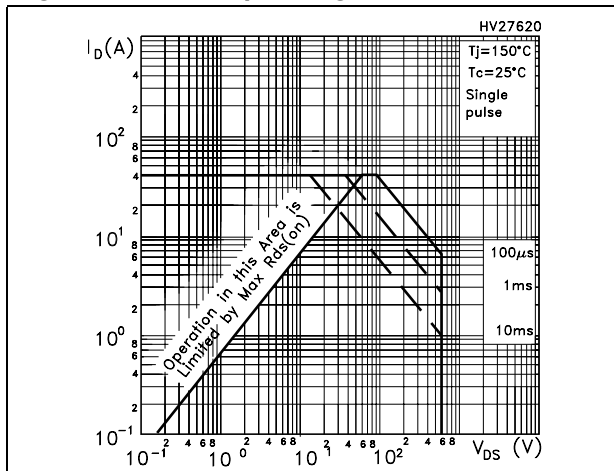


Figure 3. Thermal impedance for TO-220

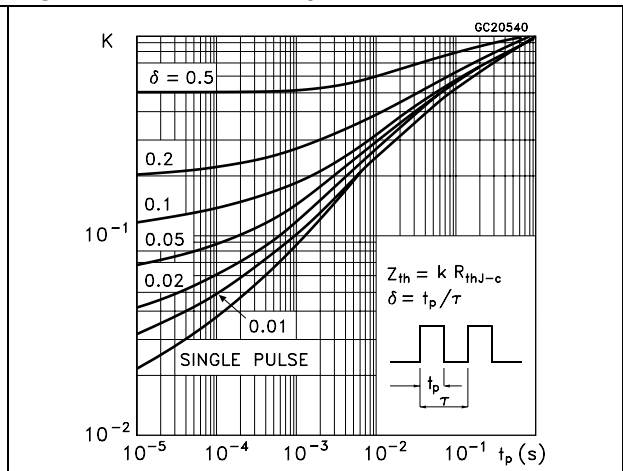


Figure 4. Safe operating area for TO-247

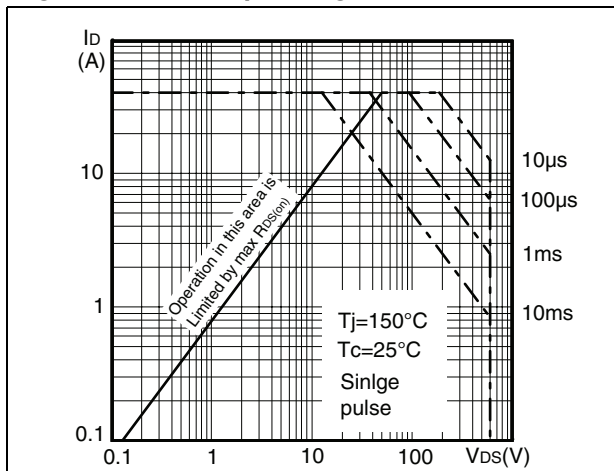


Figure 5. Thermal impedance for TO-247

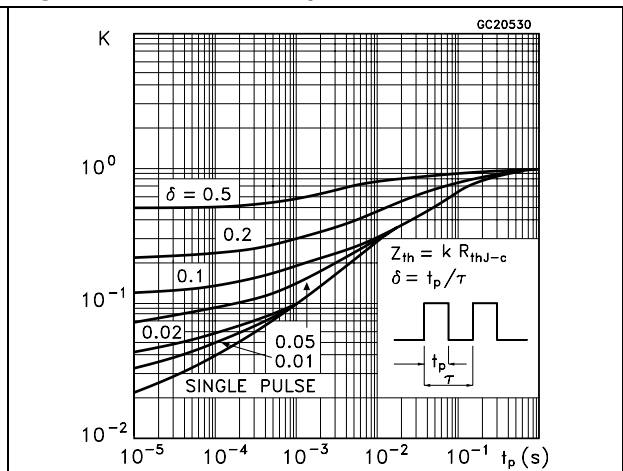


Figure 6. Safe operating area for TO-220FP

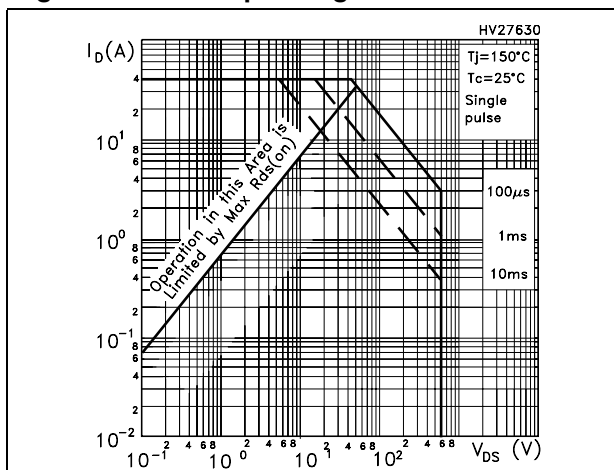


Figure 7. Thermal impedance for TO-220FP

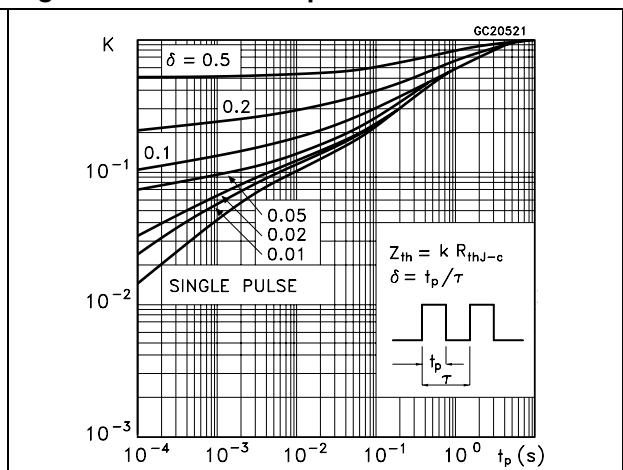


Figure 8. Output characteristics

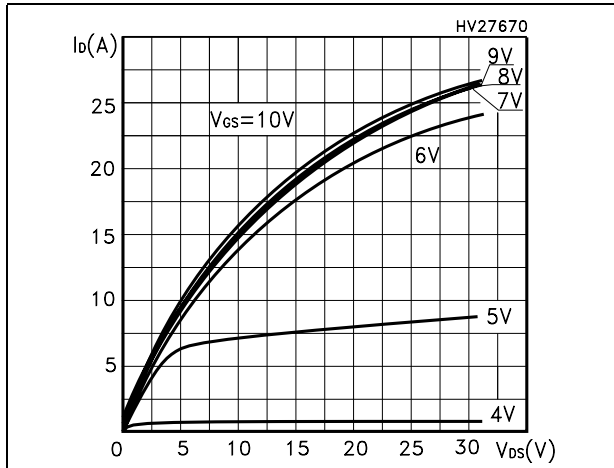


Figure 9. Transfer characteristics

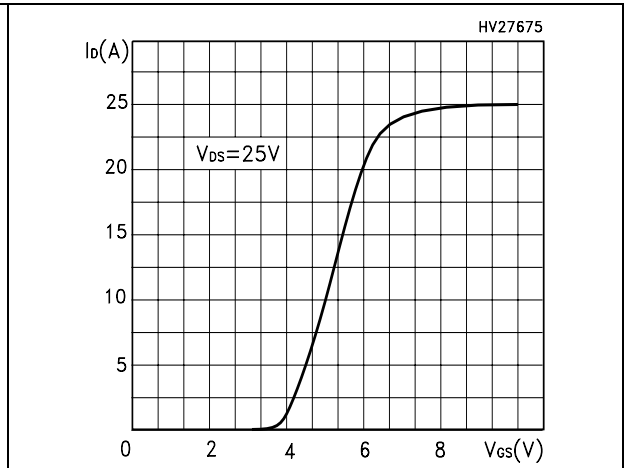


Figure 10. Transconductance

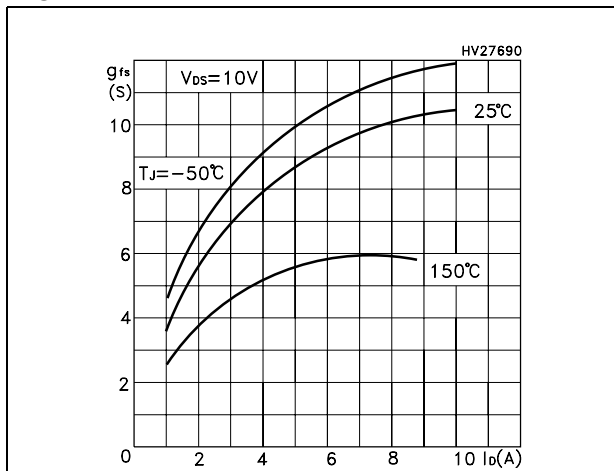


Figure 11. Static drain-source on resistance

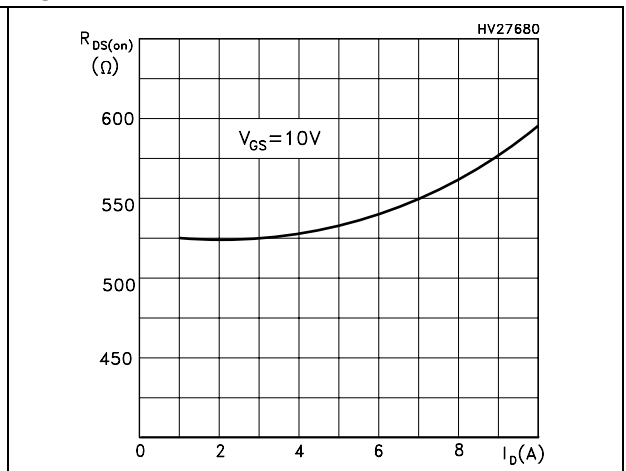


Figure 12. Gate charge vs gate-source voltage Figure 13. Capacitance variations

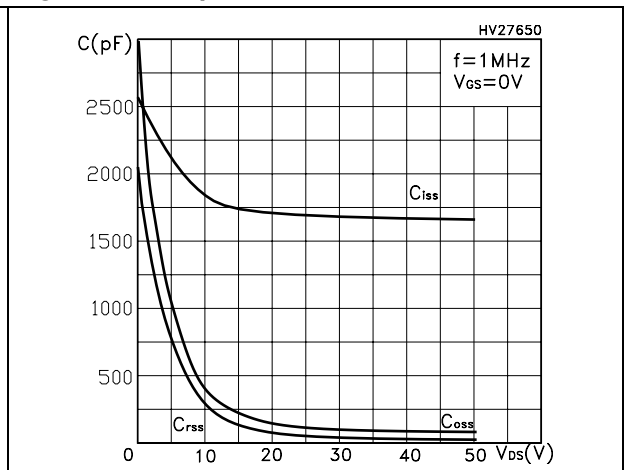
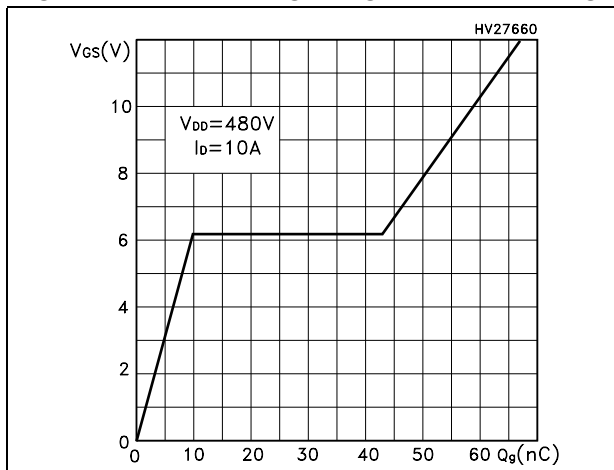


Figure 14. Normalized gate threshold voltage vs temperature

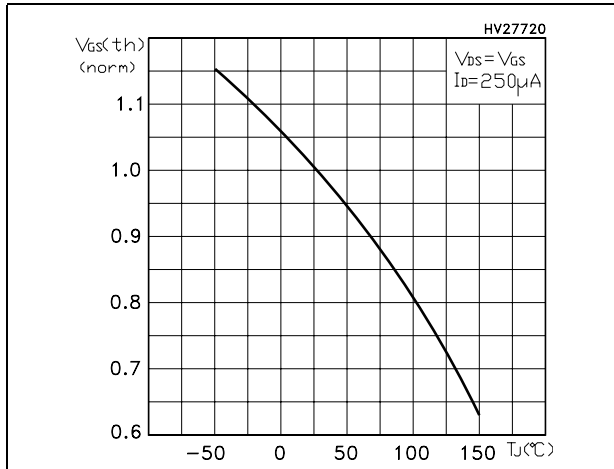


Figure 15. Normalized on resistance vs temperature

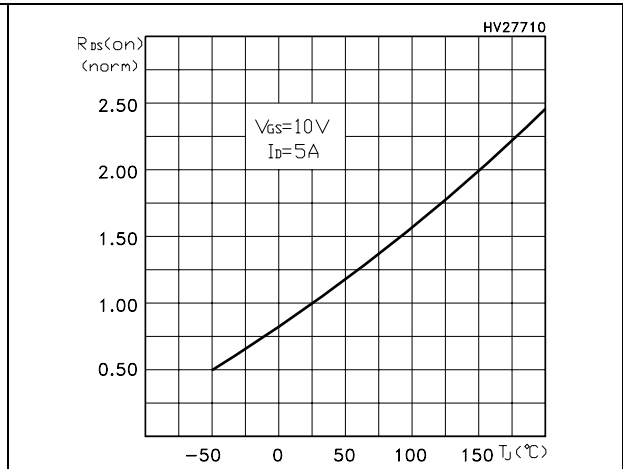


Figure 16. Source-drain diode forward characteristics

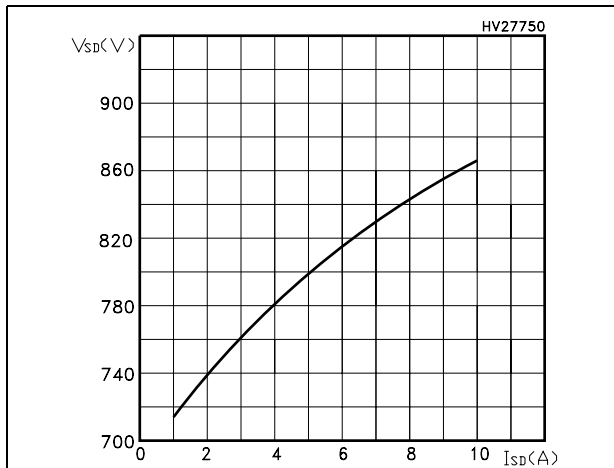


Figure 17. Normalized breakdown voltage vs temperature

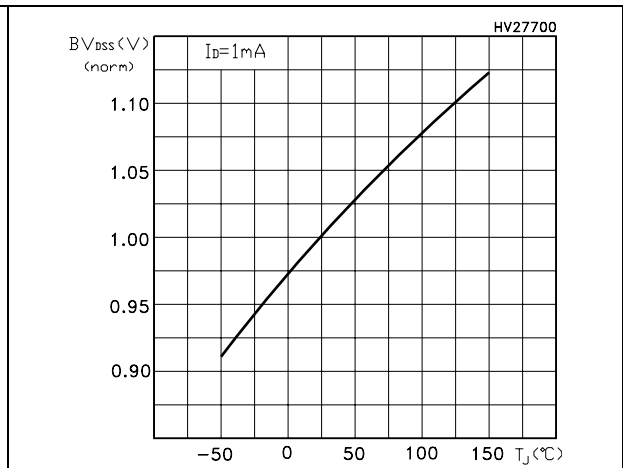
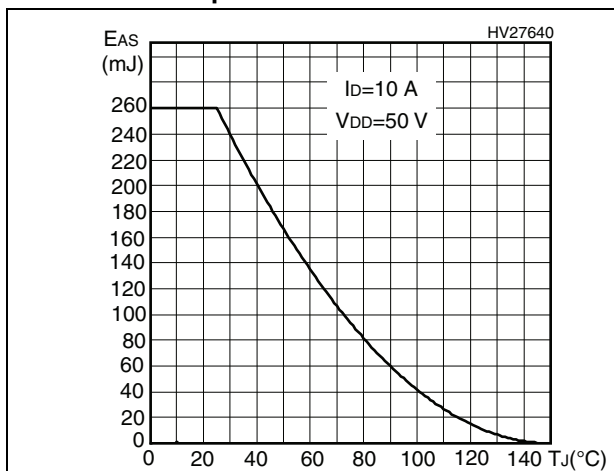


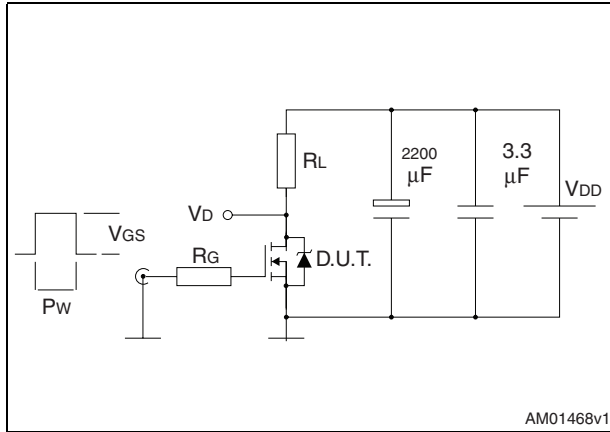
Figure 18. Maximum avalanche energy vs temperature



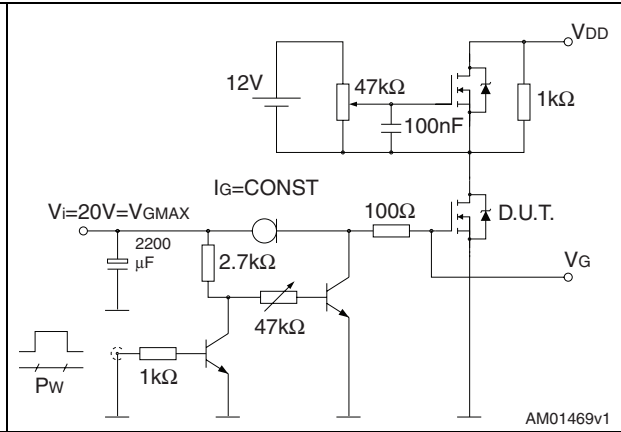


### 3 Test circuits

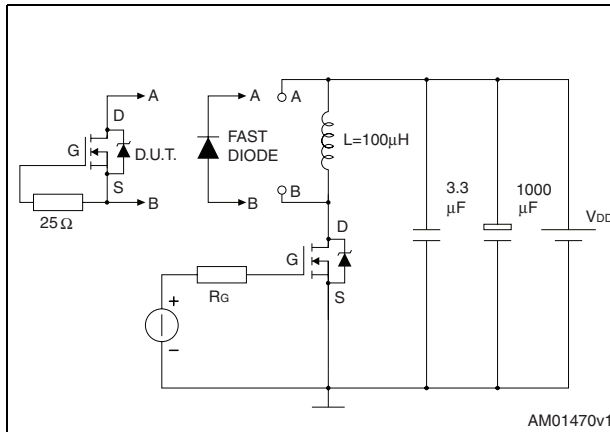
**Figure 19. Switching times test circuit for resistive load**



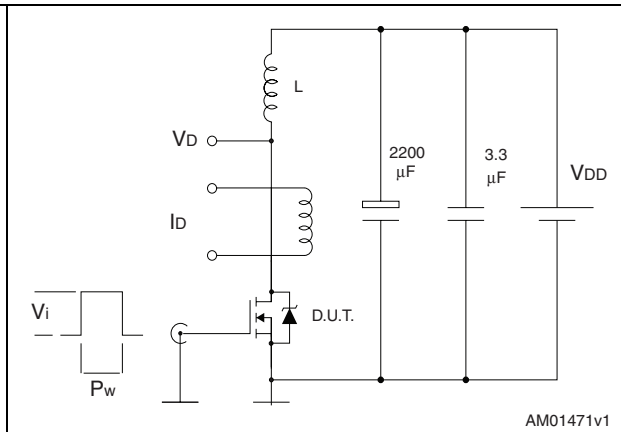
**Figure 20. Gate charge test circuit**



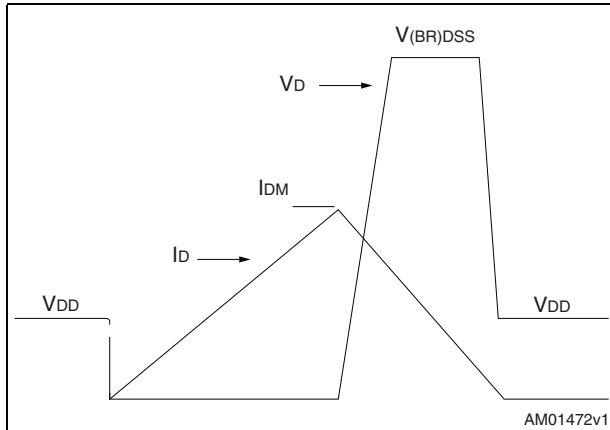
**Figure 21. Test circuit for inductive load switching and diode recovery times**



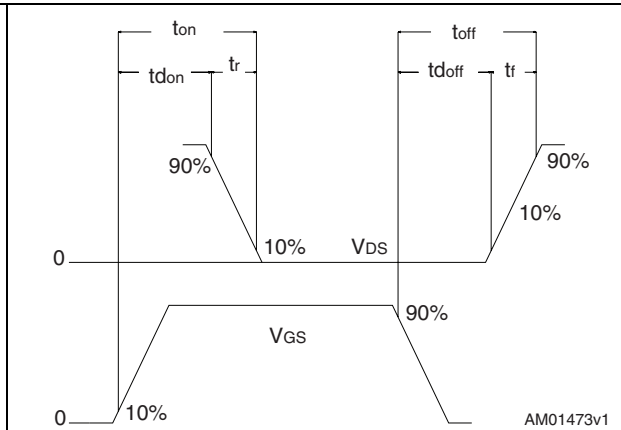
**Figure 22. Unclamped inductive load test circuit**



**Figure 23. Unclamped inductive waveform**



**Figure 24. Switching time waveform**

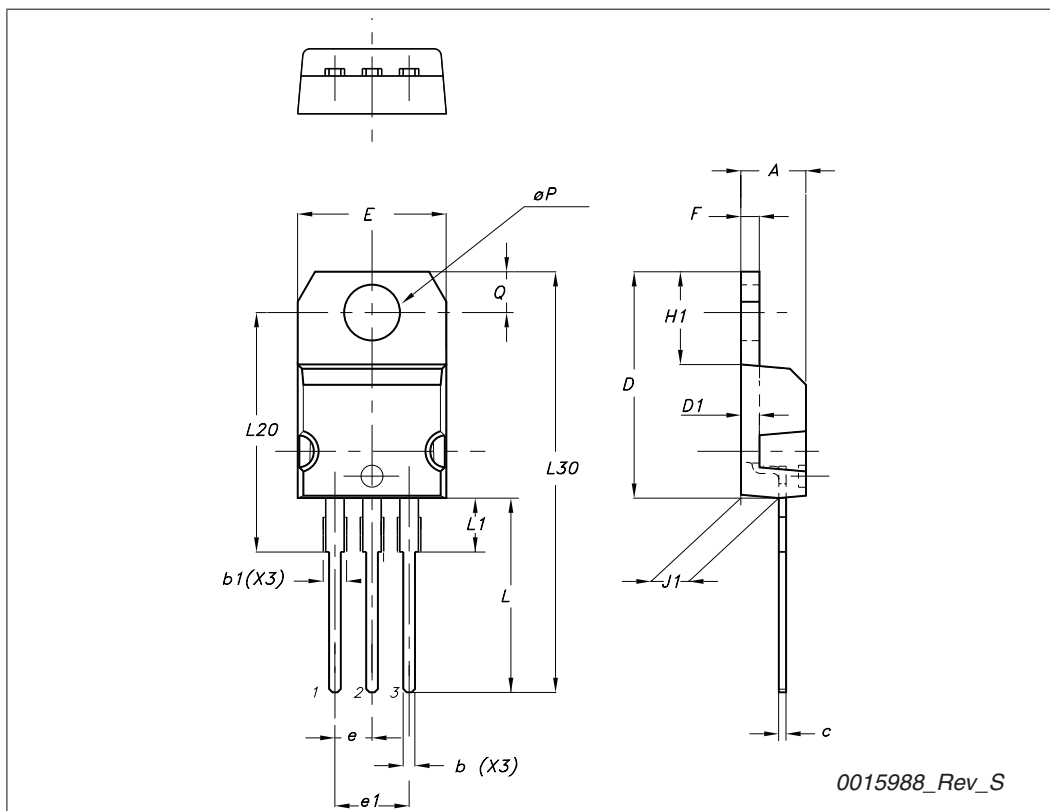


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

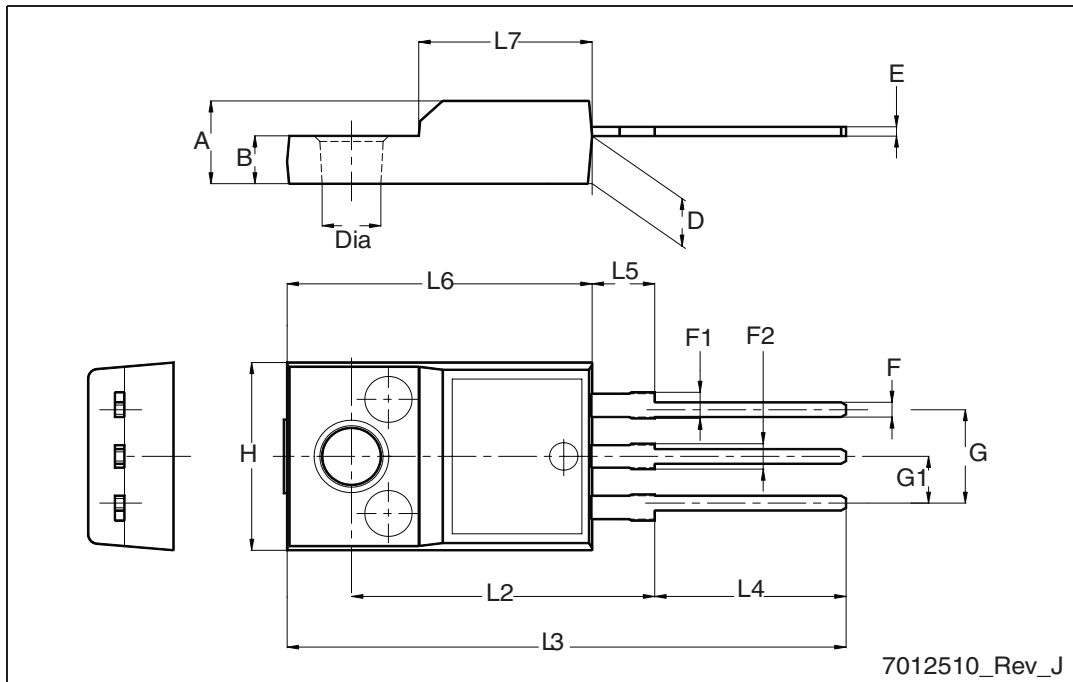
## TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



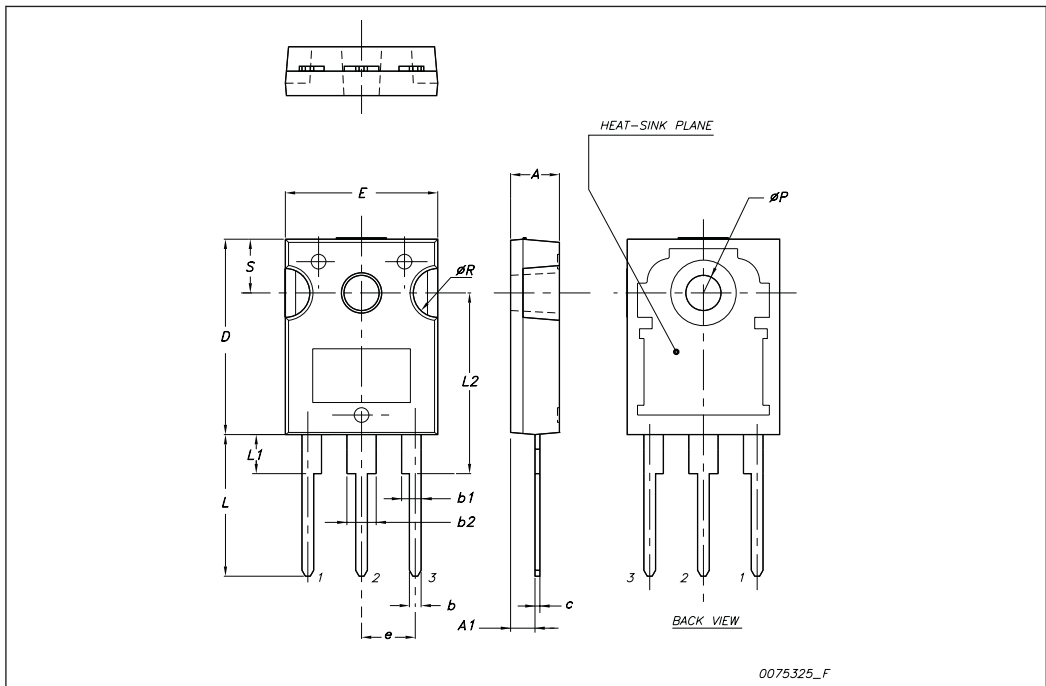
TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.5
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2



**TO-247 mechanical data**

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
12-Apr-2004	1	First release
06-Sep-2005	2	Inserted ecopack indication
13-Sep-2005	3	Final version
05-Sep-2006	4	The document has been reformatted
26-Apr-2007	5	The document has been updated on <a href="#">1: Electrical ratings</a>
25-Jan-2008	6	Modified: dv/dt value on <a href="#">Table 2: Absolute maximum ratings</a>
13-Oct-2009	7	Added new package, mechanical data: TO-247

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