



# STW14NM50

N-CHANNEL 550V @ Tjmax - 0.32Ω - 14A TO-247  
MDmesh™ MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub> (@Tjmax)	R <sub>DS(on)</sub>	I <sub>D</sub>
STW14NM50	550 V	< 0.35 Ω	14 A

- TYPICAL R<sub>DS(on)</sub> = 0.32 Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE RATED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE
- TIGHT PROCESS CONTROL AND HIGH MANUFACTURING YIELDS

## DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprieterati strip technique yields overall dynamic performance that is significantly better than that of similar completion's products.

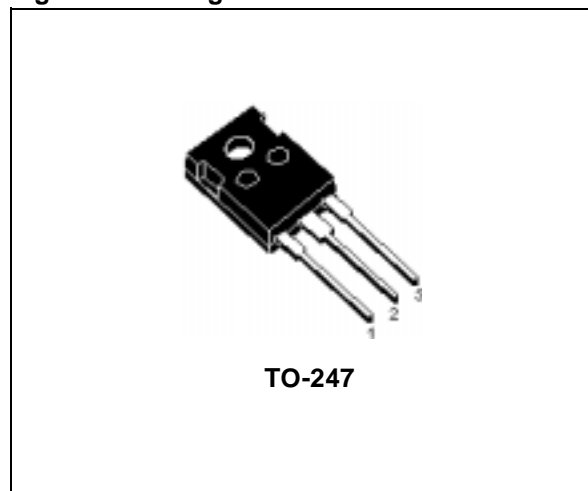
## APPLICATIONS

The MDmesh™ family is very suitable for increase the power density of high voltage converters allowing system miniaturization and higher efficiencies.

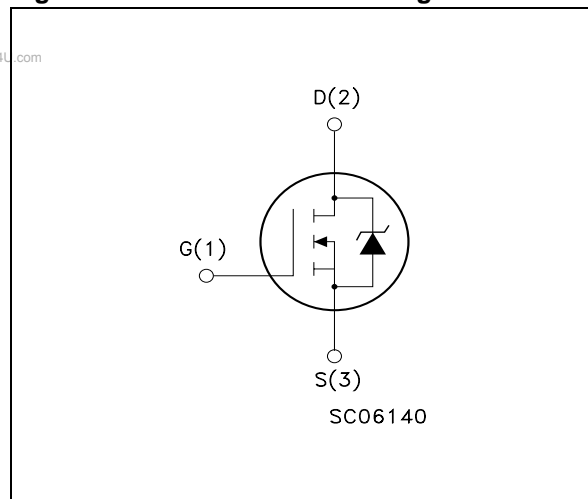
**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STW14NM50	W14NM50	TO-247	TUBE

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source Voltage	$\pm 30$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	14	A
$I_D$	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	8.8	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	56	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	175	W
	Derating Factor	1.28	W/ $^\circ\text{C}$
dv/dt	Peak Diode Recovery voltage slope	6	V/ns
$T_{stg}$	Storage Temperature	-65 to 150	$^\circ\text{C}$
$T_j$	Max. Operating Junction Temperature	150	$^\circ\text{C}$

(\*)Pulse width limited by safe operating area

(\*)Limited only by maximum temperature allowed

(1) $I_{SD} \leq 14\text{A}$ ,  $di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 4: Thermal Data**

Rthj-case	Thermal Resistance Junction-case Max	0.715	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	30	$^\circ\text{C}/\text{W}$
$T_I$	Maximum Lead Temperature For Soldering Purpose	300	$^\circ\text{C}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)	12	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{V}$ )	400	mJ

**ELECTRICAL CHARACTERISTICS ( $T_{CASE} = 25^\circ\text{C}$  UNLESS OTHERWISE SPECIFIED)**
**Table 6: On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$ , $I_D = 6\text{A}$		0.32	0.35	$\Omega$

## ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ , $I_D = 6A$		5.2		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V$ , $f = 1 MHz$ , $V_{GS} = 0$		1000 180 25		pF pF pF
$C_{OSS eq}$ (3).	Equivalent Output Capacitance	$V_{GS} = 0 V$ , $V_{DS} = 0$ to 400 V		90		pF
$R_G$	Gate Input Resistance	$f=1 MHz$ Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		1.6		$\Omega$
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 250 V$ , $I_D = 6 A$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 V$ (see Figure 15)		20 10 19 8		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400 V$ , $I_D = 12 A$ , $V_{GS} = 10 V$ (see Figure 18)		28 8 15	38	nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				14 56	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 12 A$ , $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12 A$ , $di/dt = 100 A/\mu s$ $V_{DD} = 100V$ (see Figure 16)		270 2.23 16.5		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12 A$ , $di/dt = 100 A/\mu s$ $V_{DD} = 100V$ , $T_j = 150^\circ C$ (see Figure 16)		340 3 18		ns $\mu C$ A

(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

(3)  $C_{OSS eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Figure 3: Safe Operating Area

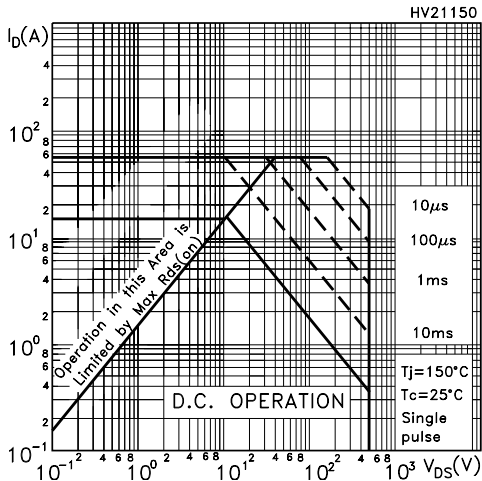


Figure 4: Output Characteristics

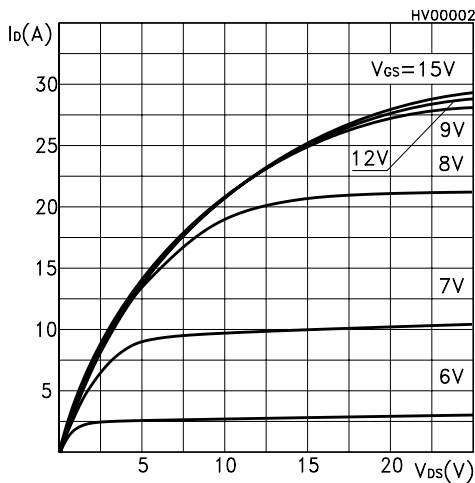


Figure 5: Transconductance

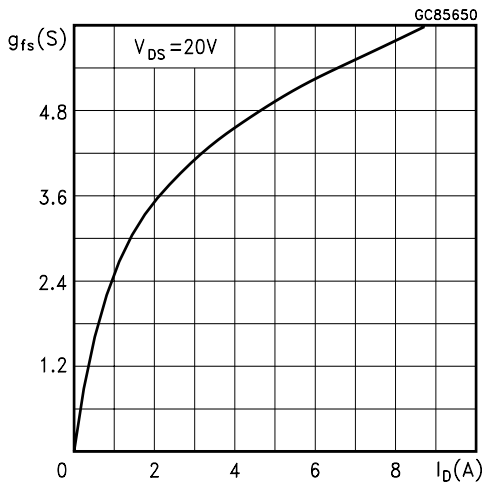


Figure 6: Thermal Impedance

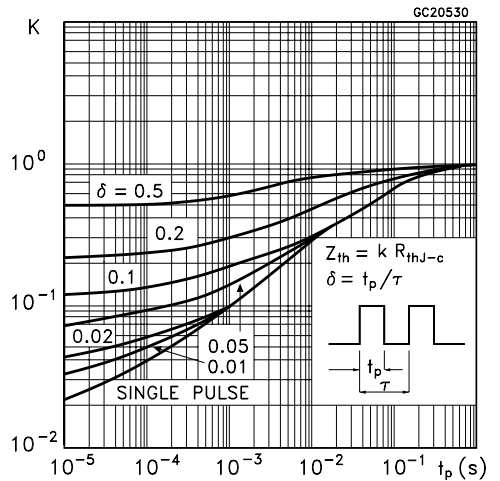


Figure 7: Transfer Characteristics

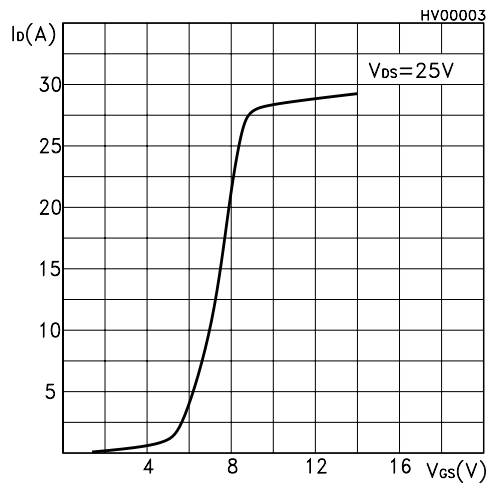


Figure 8: Static Drain-source On Resistance

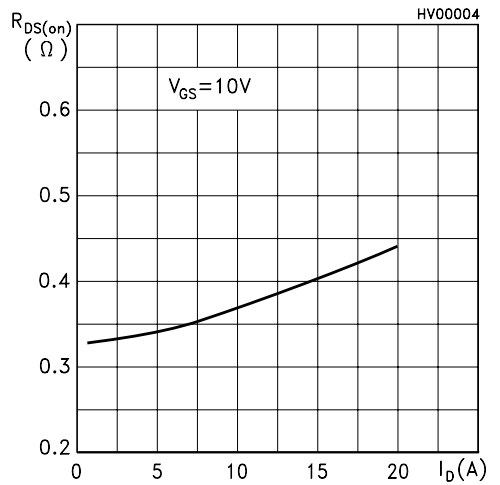


Figure 9: Gate Charge vs Gate-source Voltage

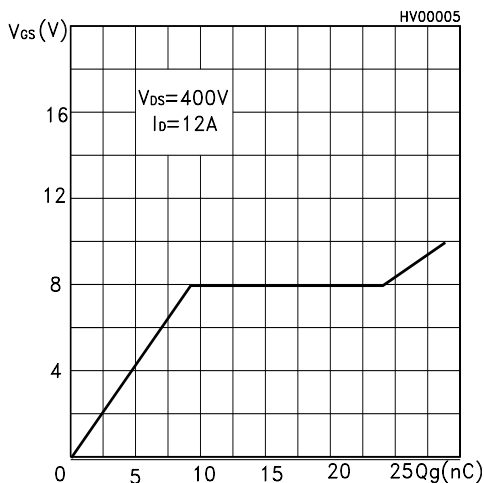


Figure 10: Normalized Gate Threshold Voltage vs Temperature

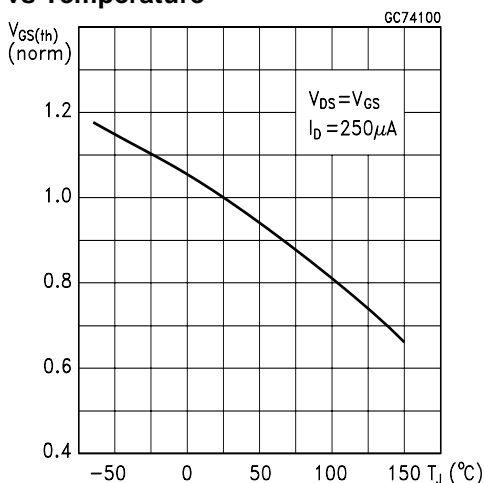


Figure 11: Dource-Drain Diode Forward Characteristics

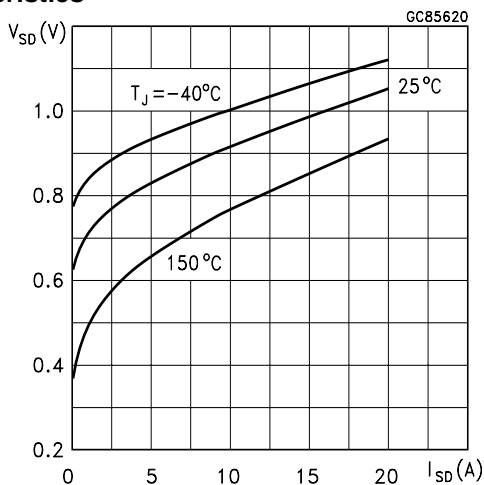


Figure 12: Capacitance Variations

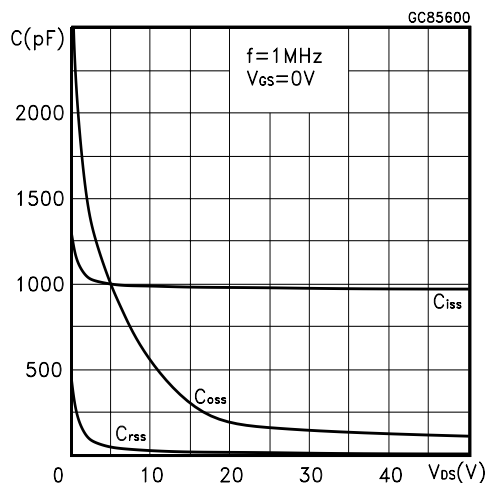


Figure 13: Normalized On Resistance vs Temperature

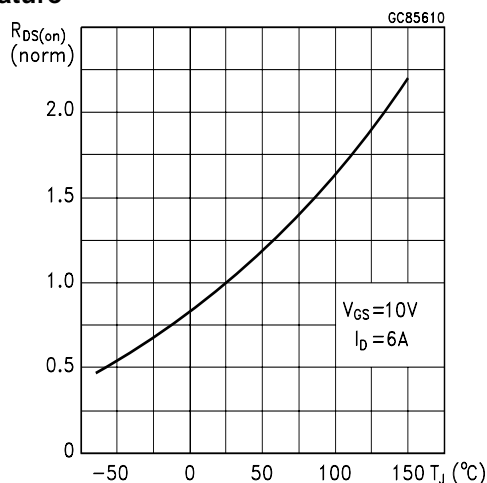


Figure 14: Unclamped Inductive Load Test Circuit

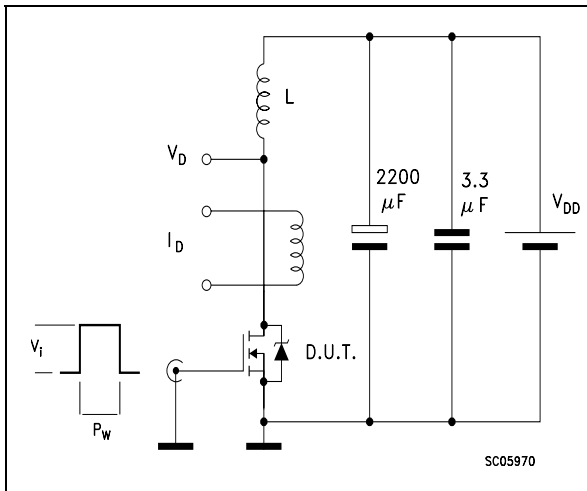


Figure 15: Switching Times Test Circuit For Resistive Load

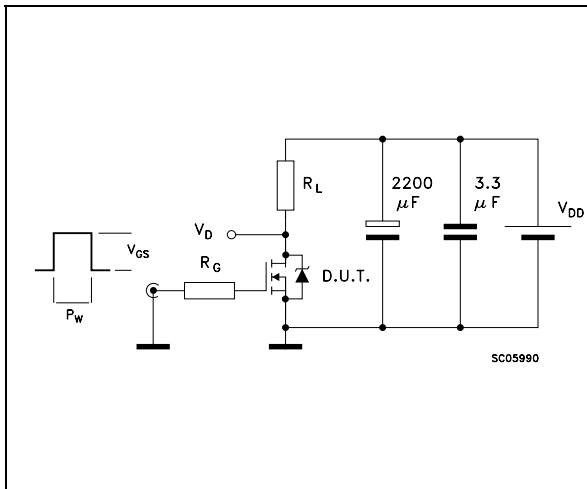


Figure 16: Test Circuit For Inductive Load Switching and Diode Recovery Times

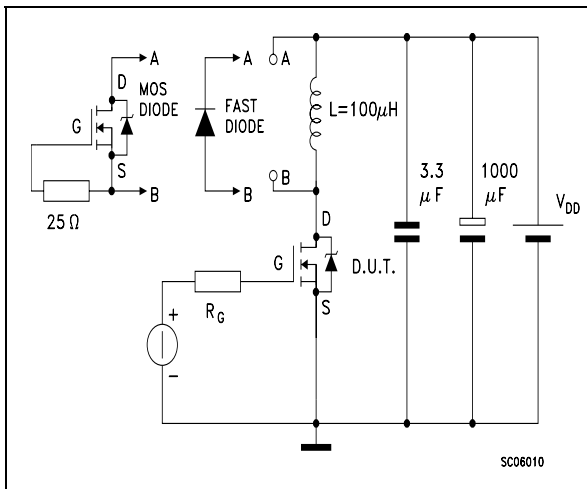


Figure 17: Unclamped Inductive Waferform

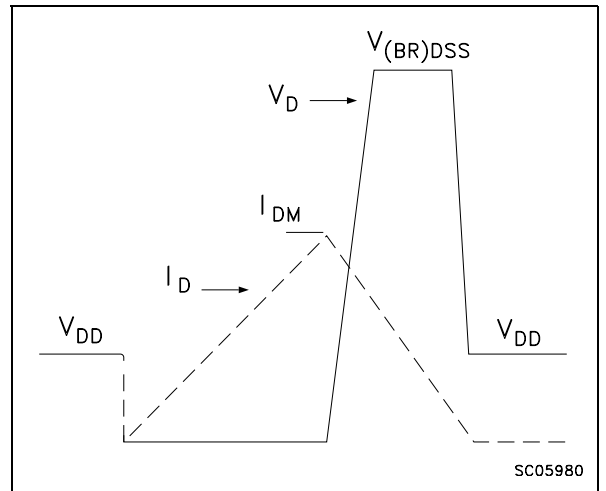
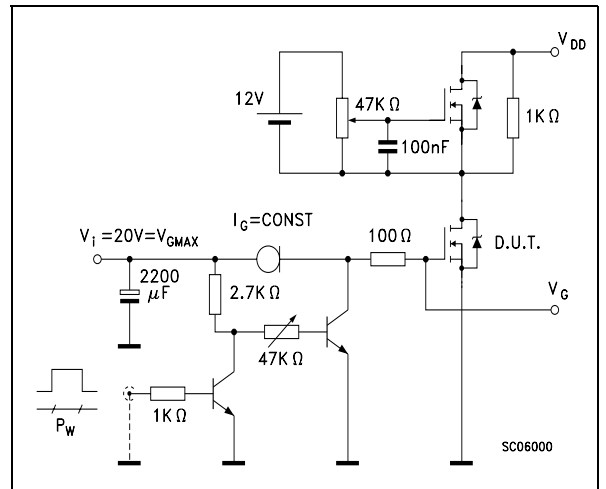
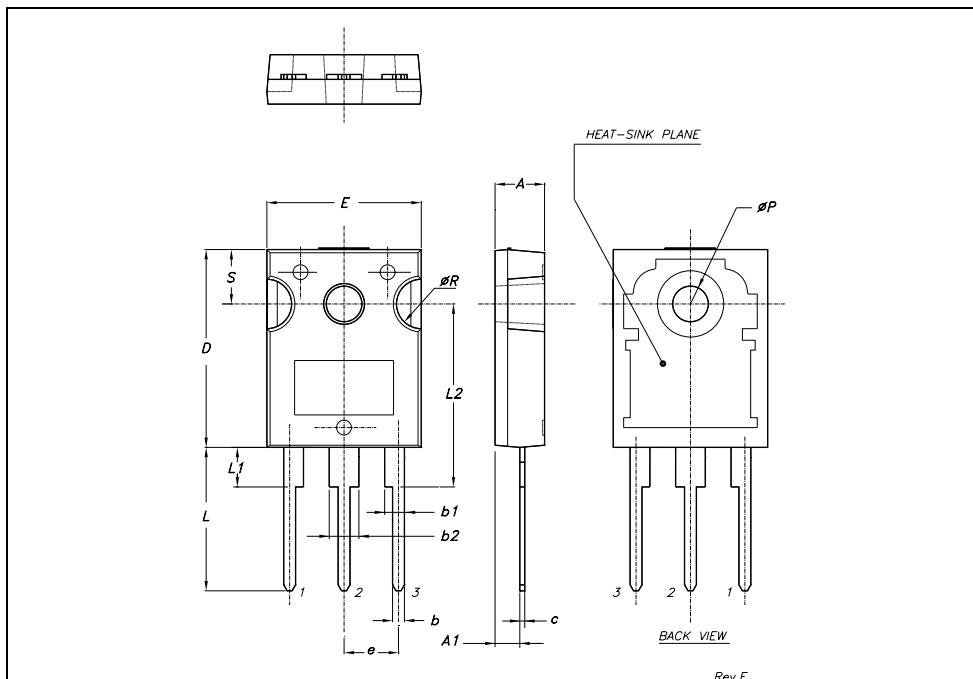


Figure 18: Gate Charge Test Circuit



## TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



**Table 9: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
05-July-2004	5	The document change from "PRELIMINARY" to "COMPLETE". New Stylesheet.



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