

N-channel 950 V, 0.275 Ω typ., 17.5 A MDmesh™ K5
Power MOSFETs in D²PAK, TO-220FP, TO-220 and TO-247

Datasheet - production data

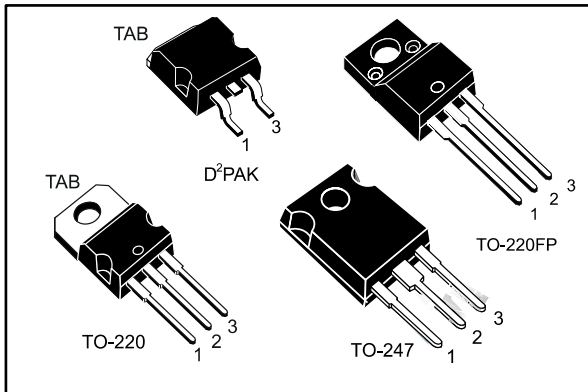
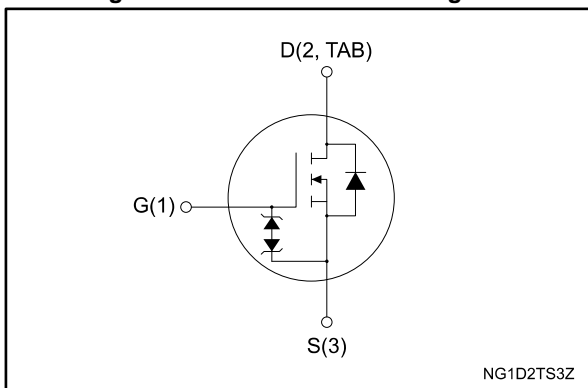


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STB20N95K5	950 V	0.330 Ω	17.5 A	250 W
STF20N95K5				40 W
STP20N95K5				250 W
STW20N95K5				

- Industry's lowest R_{DS(on)} x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These very high voltage N-channel Power MOSFETs are designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STB20N95K5	20N95K5	D ² PAK	Tape and reel
STF20N95K5		TO-220FP	Tube
STP20N95K5		TO-220	
STW20N95K5		TO-247	

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	9
4	Package information	10
	4.1 D ² PAK package information	10
	4.2 TO-220FP package information	13
	4.3 TO-220 type A package information	15
	4.4 TO-247 package information	17
	4.5 D ² PAK packing information	19
5	Revision history	21

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK TO-220 TO-247	TO-220FP	
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	17.5		A
I _D	Drain current (continuous) at T _C = 100 °C	11		A
I _D ⁽¹⁾	Drain current (pulsed)	70		A
P _{TOT}	Total dissipation at T _C = 25 °C	250	40	W
ESD	Gate-source human body model (R= 1,5 kΩ, C = 100 pF)	2		kV
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500		V
dv/dt ⁽²⁾	Peak diode recovery voltage slope	6		V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50		
T _j	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

Notes:

- (1) Pulse width limited by safe operating area.
- (2) I_{SD} ≤ 17.5 A, di/dt ≤ 100 A/μs; V_{DS} peak ≤ V_{(BR)DSS}
- (3) V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value				Unit
		D ² PAK	TO-220	TO-247	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	0.5			3.1	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5	50	62.5	
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30				

Notes:

- (1) When mounted on 1 inch² FR-4 board, 2 Oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	6	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	200	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	950			V
I _{DSS}	Zero-gate voltage drain current	V _{GS} = 0 V, V _{DS} = 950 V			1	μA
		V _{GS} = 0 V, V _{DS} = 950 V T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 9 A		0.275	0.330	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iSS}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	1550	-	pF
C _{oSS}	Output capacitance		-	140	-	pF
C _{rSS}	Reverse transfer capacitance		-	1	-	pF
C _{o(er)} ⁽¹⁾	Equivalent capacitance energy related	V _{GS} = 0 V, V _{DS} = 0 to 760 V	-	65	-	pF
C _{o(tr)} ⁽²⁾	Equivalent capacitance time related			178	-	pF
R _g	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	3.5	-	Ω
Q _g	Total gate charge	V _{DD} = 760 V, I _D = 17.5 A V _{GS} = 10 V (see Figure 20: "Test circuit for gate charge behavior")	-	48	-	nC
Q _{gs}	Gate-source charge		-	9	-	nC
Q _{gd}	Gate-drain charge		-	32.5	-	nC

Notes:

⁽¹⁾C_{o(er)} is a constant capacitance value that gives the same stored energy as C_{oSS} while V_{DS} is rising from 0 to 80% V_{DSS}.

⁽²⁾C_{o(tr)} is a constant capacitance value that gives the same charging time as C_{oSS} while V_{DS} is rising from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see Figure 19 : "Test circuit for resistive load switching times" and Figure 24 : "Switching time waveform")	-	18	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	65	-	ns
t_f	Fall time		-	18	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		70	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17.5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 17.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 21 : "Test circuit for inductive load switching and diode recovery times")	-	513		ns
Q_{rr}	Reverse recovery charge		-	12		μC
I_{RRM}	Reverse recovery current		-	46		A
t_{rr}	Reverse recovery time	$I_{SD} = 17.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 21 : "Test circuit for inductive load switching and diode recovery times")	-	670		ns
Q_{rr}	Reverse recovery charge		-	15		μC
I_{RRM}	Reverse recovery current		-	44		A

Notes:

(1)Pulse width limited by safe operating area

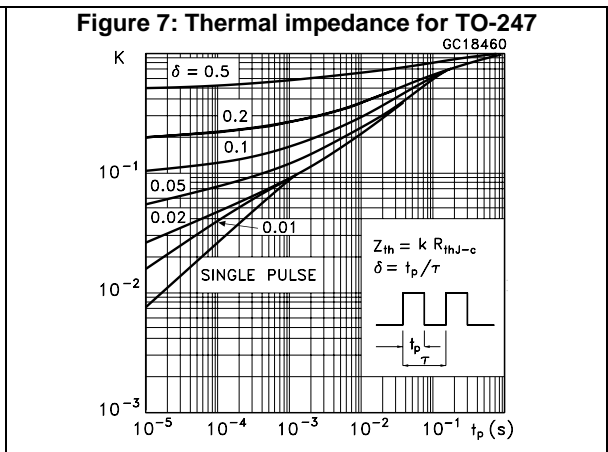
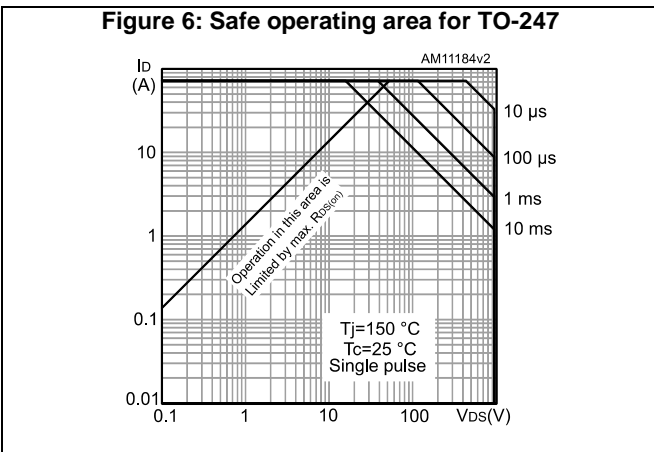
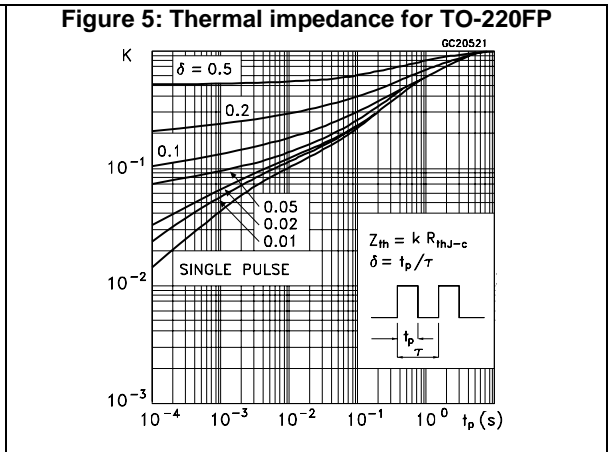
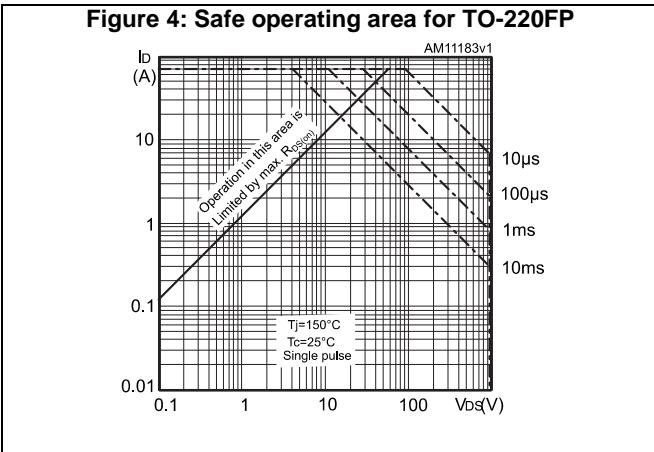
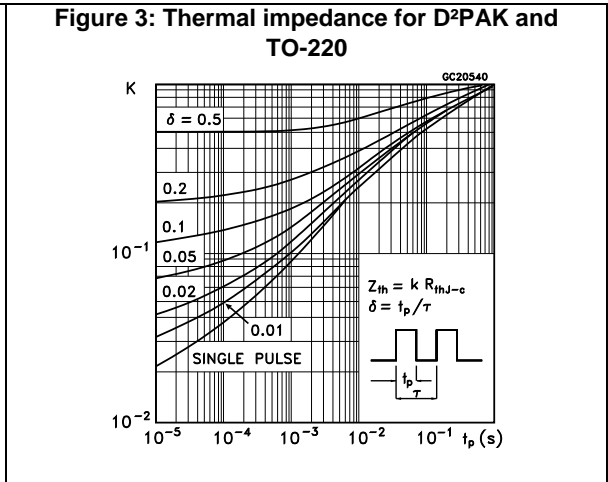
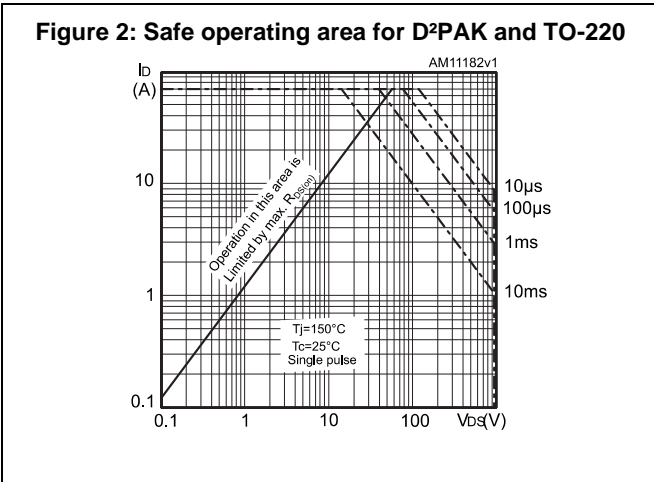
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

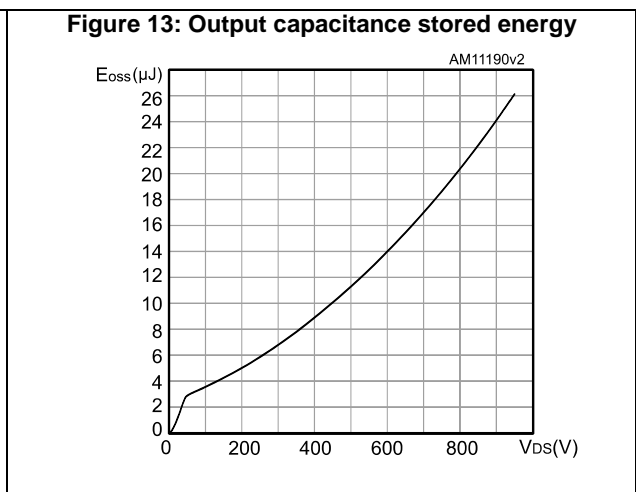
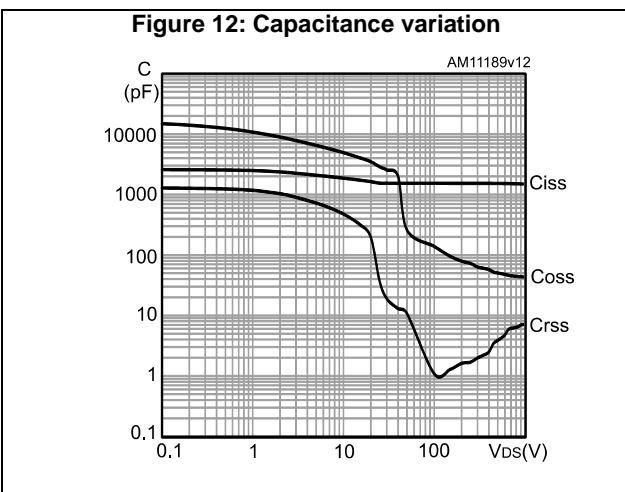
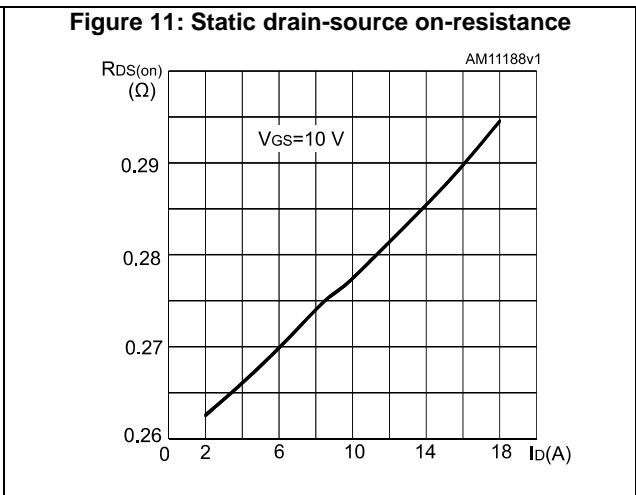
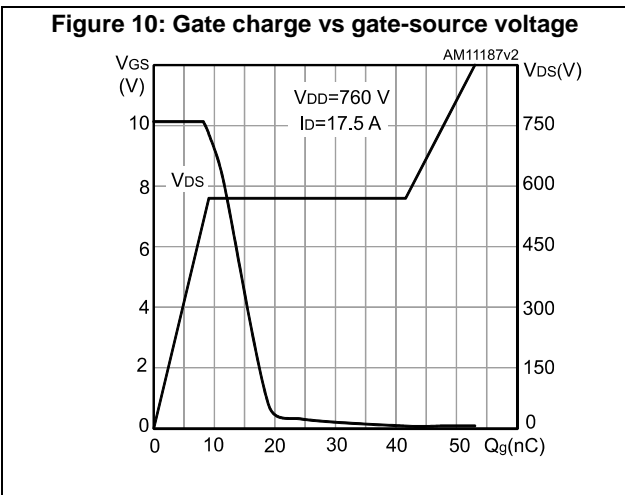
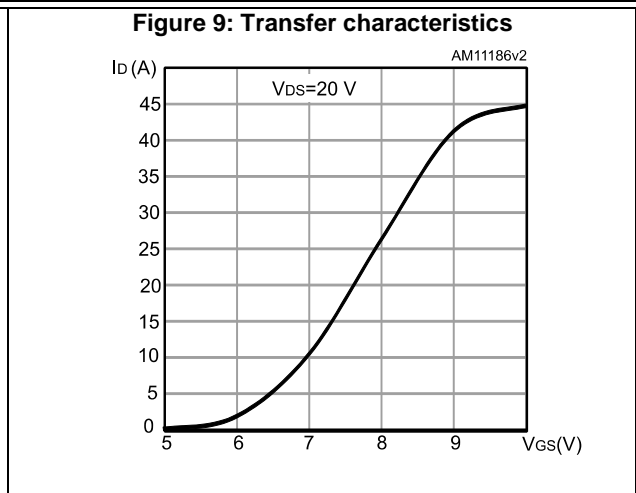
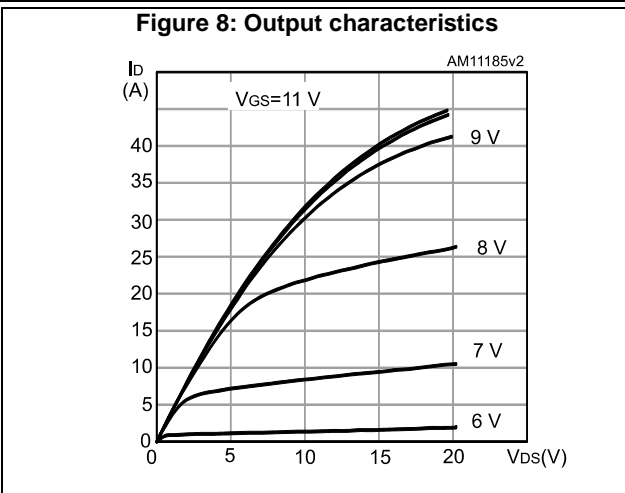
Table 9: Gate-source Zener diode

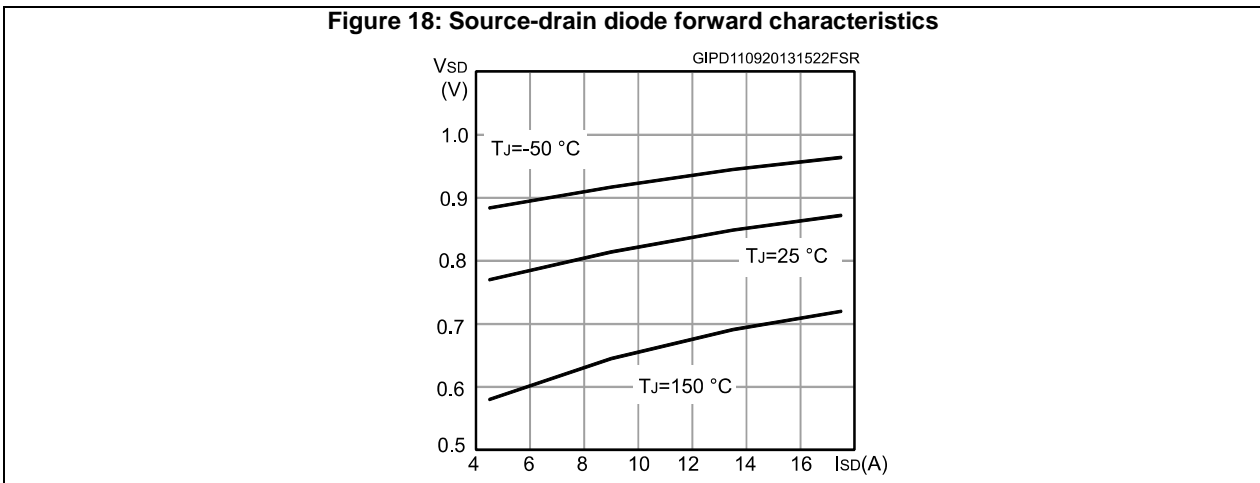
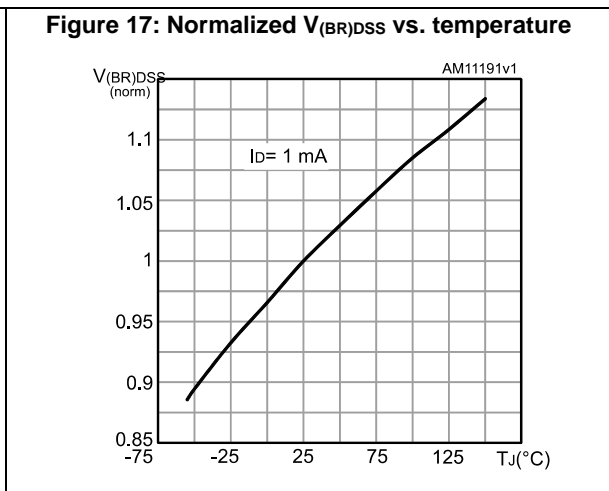
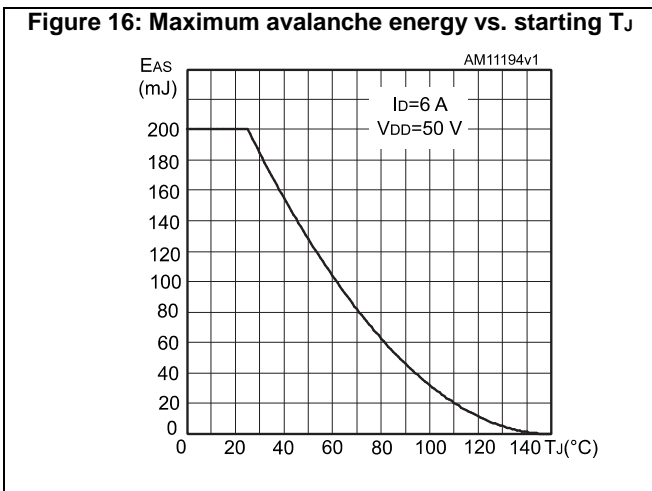
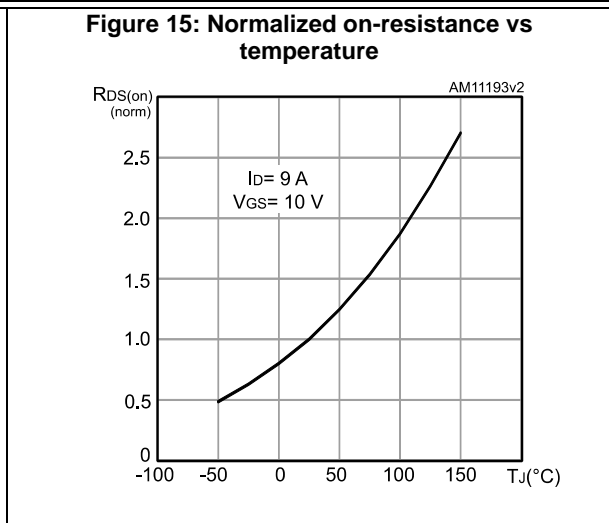
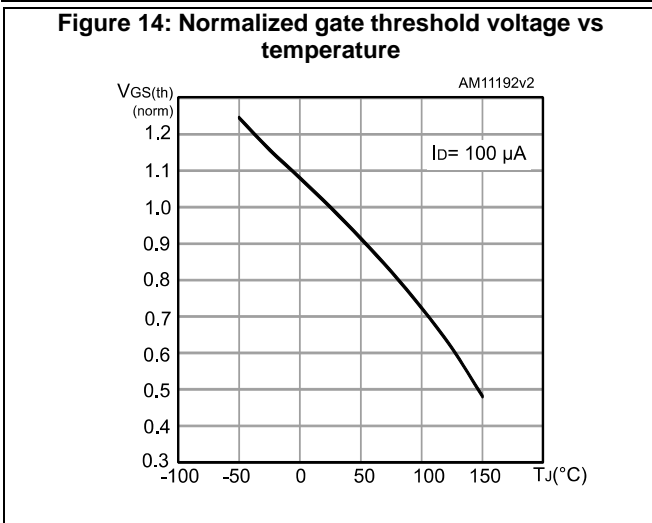
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

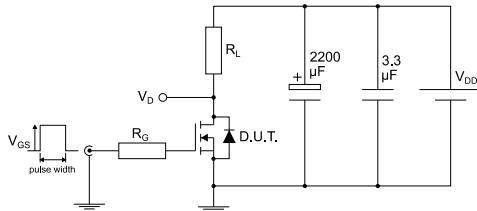






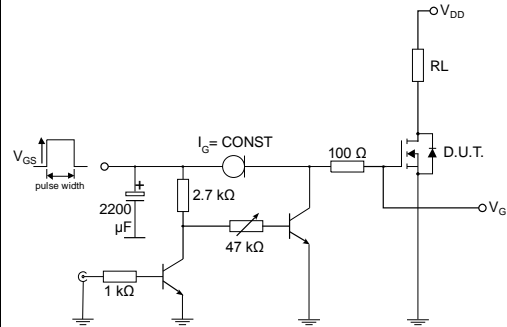
3 Test circuits

Figure 19: Test circuit for resistive load switching times



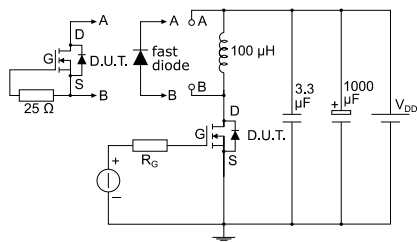
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Figure 20: Test circuit for gate charge behavior



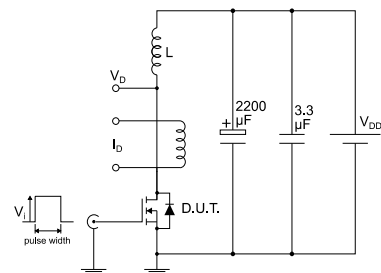
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Figure 21: Test circuit for inductive load switching and diode recovery times



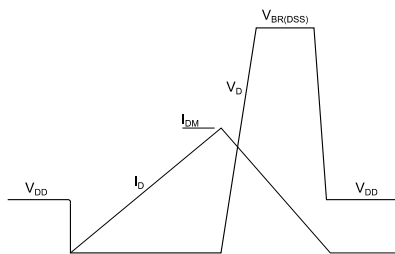
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Figure 22: Unclamped inductive load test circuit



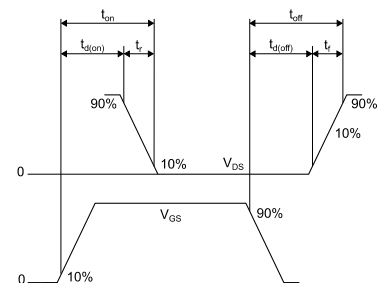
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Figure 23: Unclamped inductive waveform



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Figure 24: Switching time waveform



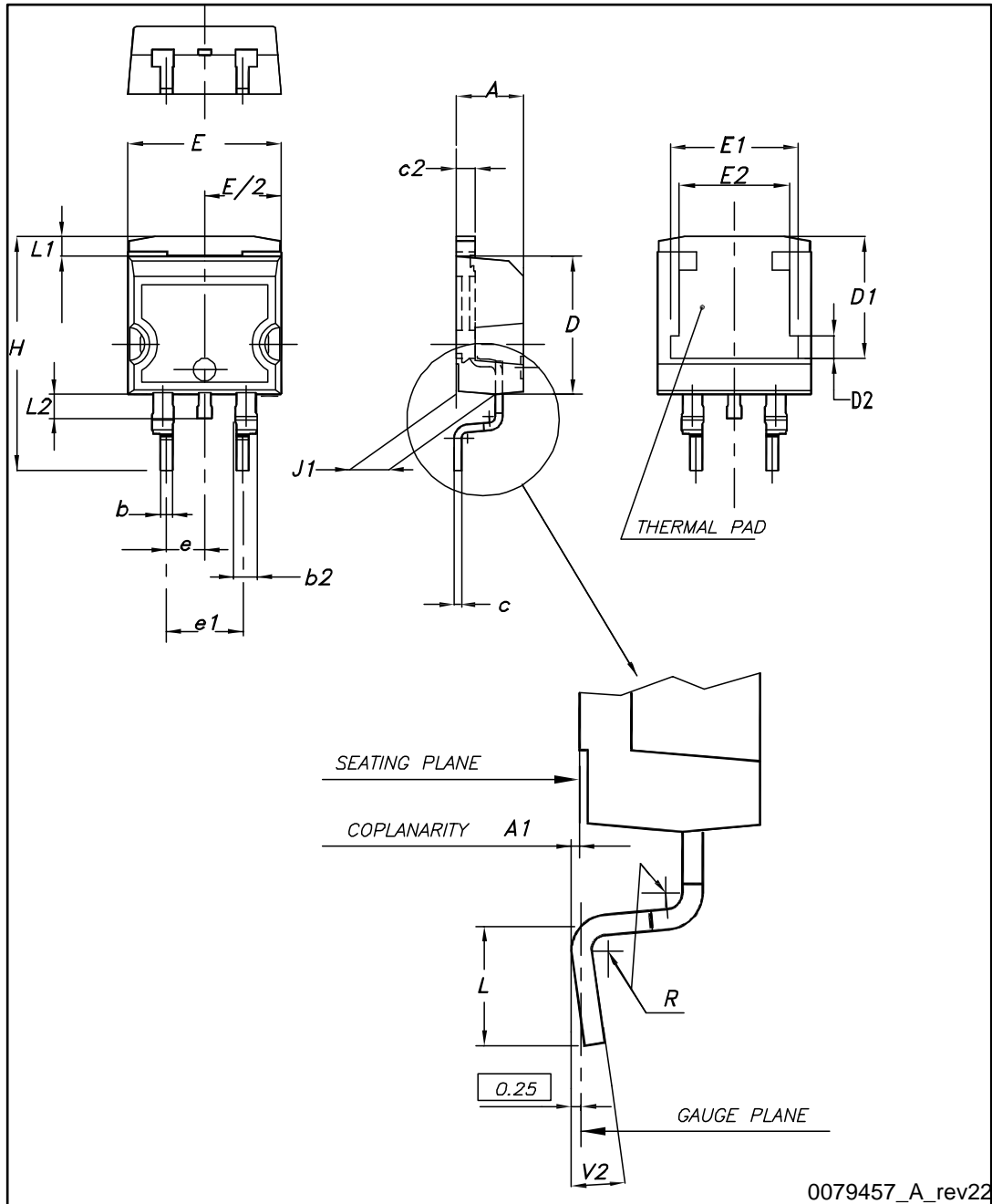
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 25: D²PAK (TO-263) type A package outline

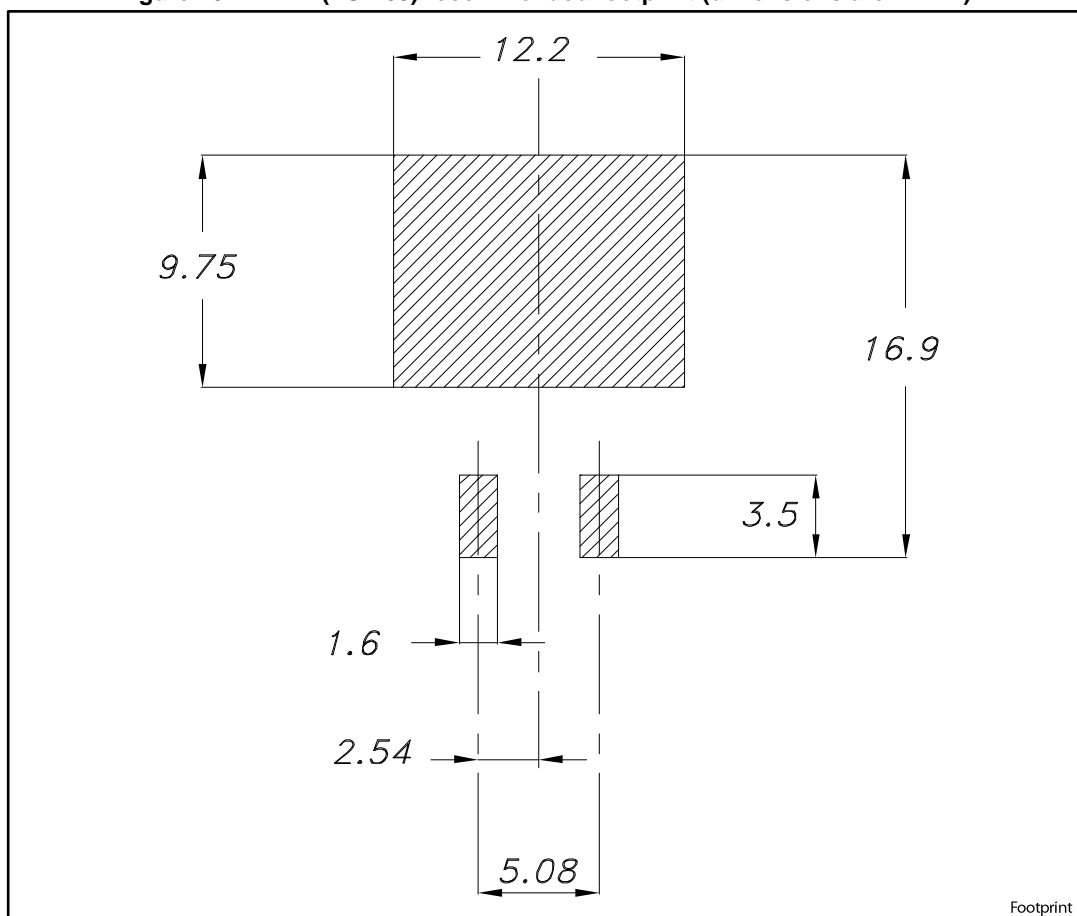


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Table 10: D²PAK (TO-263) type A package mechanical data

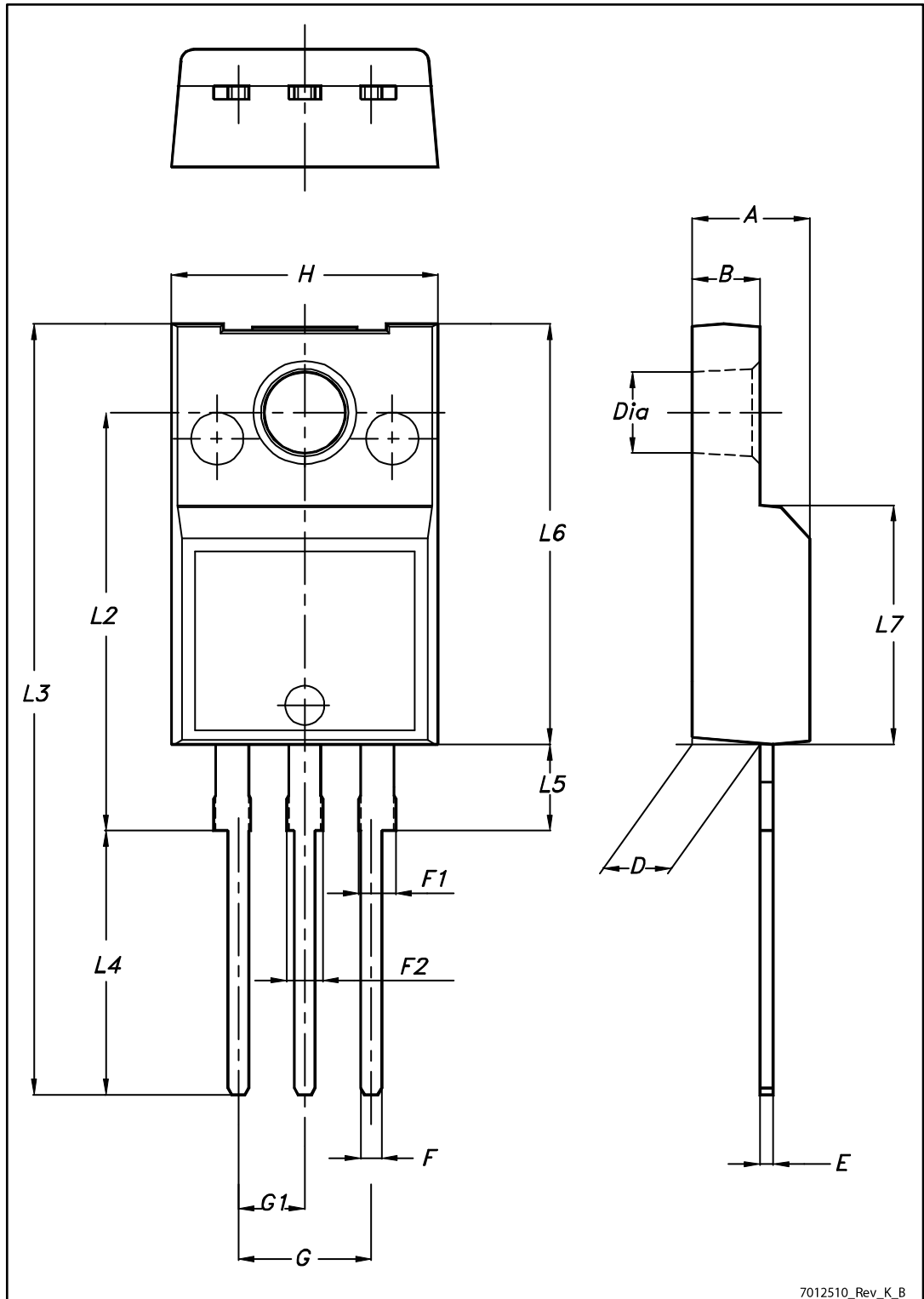
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 26: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220FP package information

Figure 27: TO-220FP package outline



7012510_Rev_K_B

Table 11: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.3 TO-220 type A package information

Figure 28: TO-220 type A package outline



Table 12: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 29: TO-247 package outline

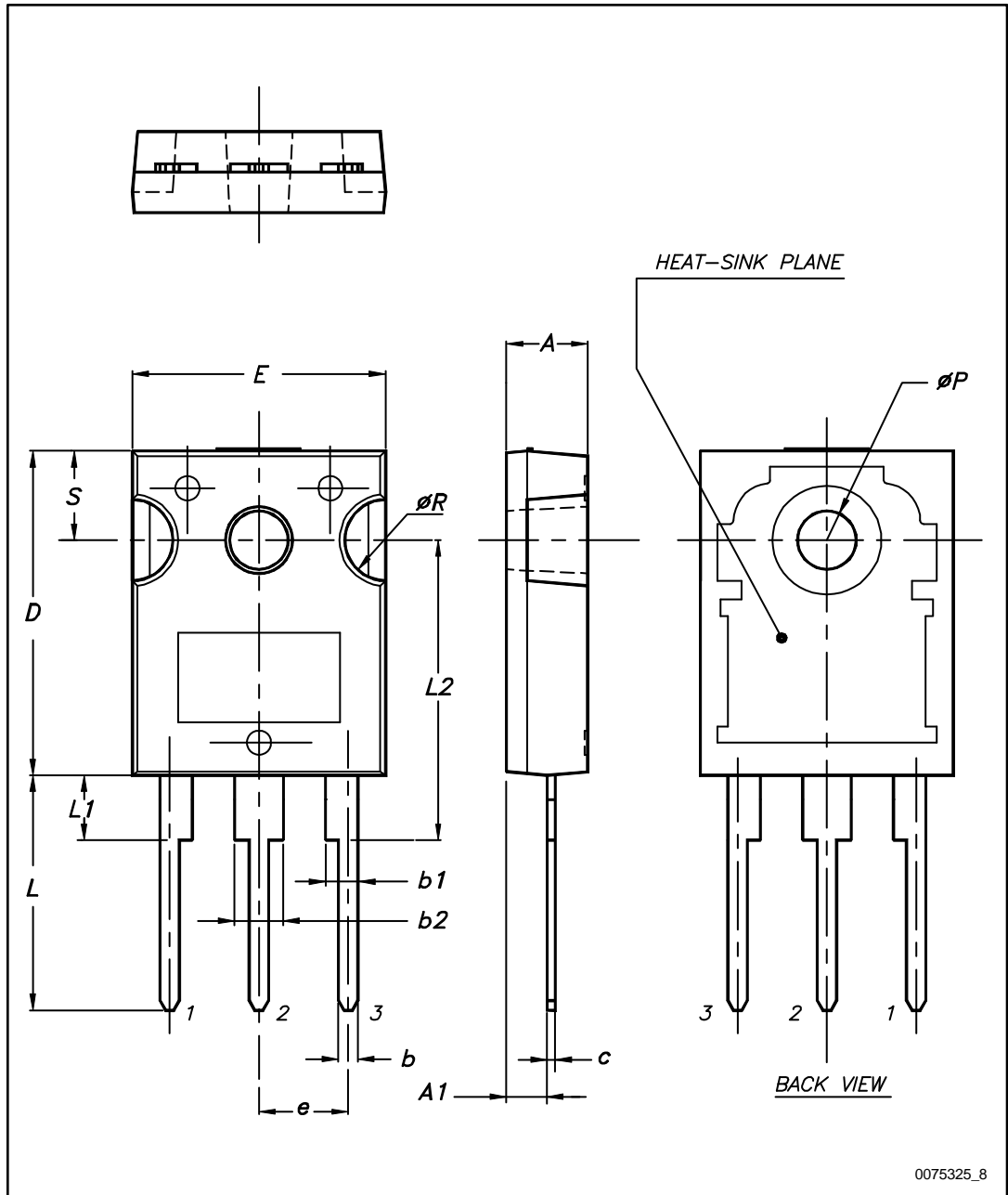


Table 13: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.5 D²PAK packing information

Figure 30: Tape outline

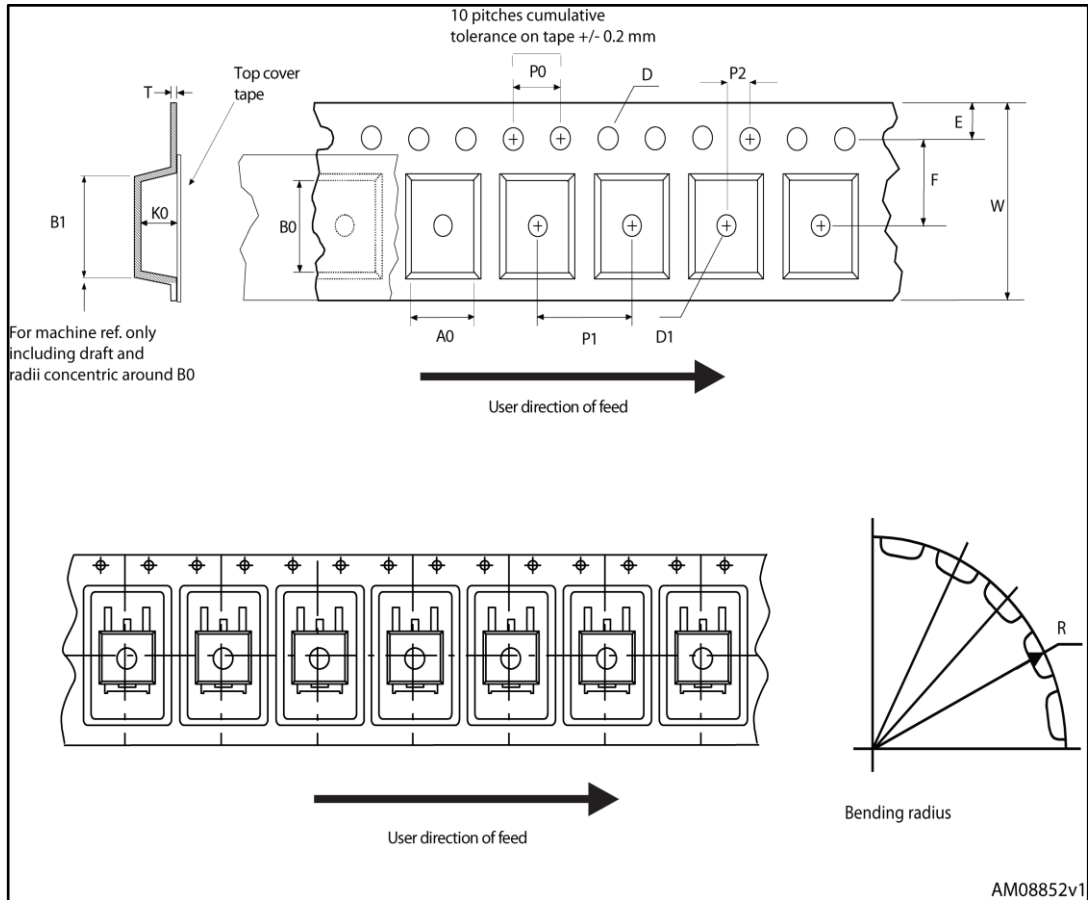


Figure 31: Reel outline

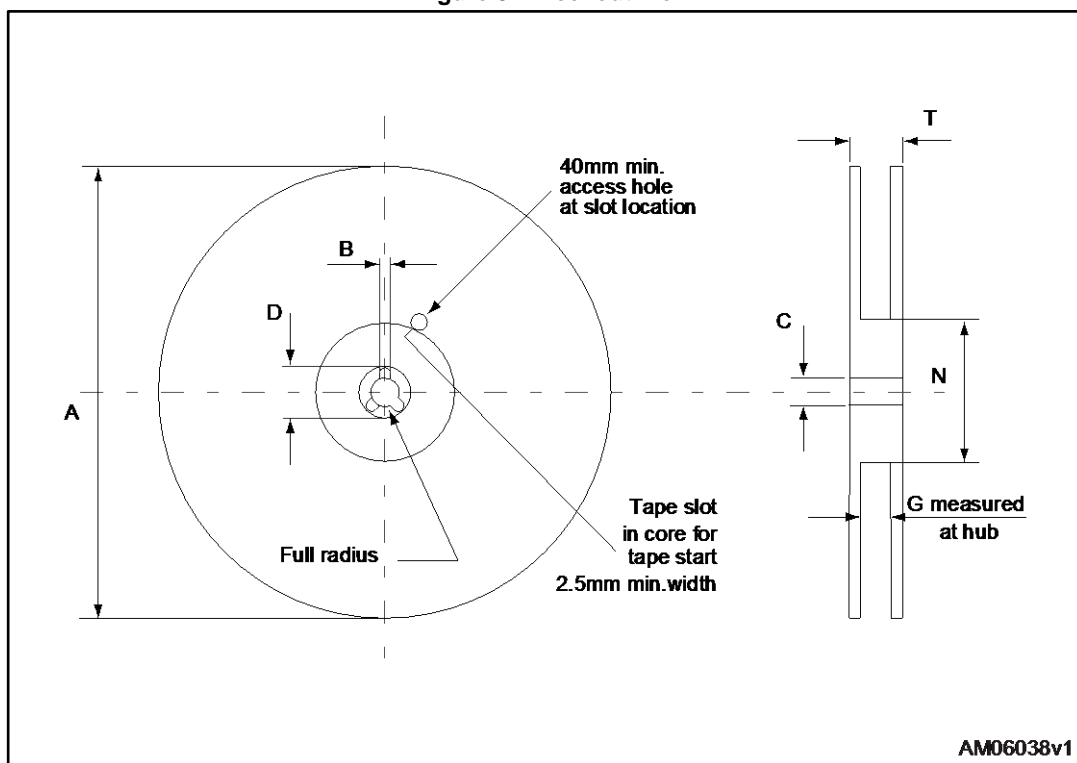


Table 14: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 15: Document revision history

Date	Revision	Changes
25-Nov-2009	1	First release.
12-Jan-2010	2	Corrected V_{GS} value in <i>Table 2: Absolute maximum ratings</i> .
22-Dec-2011	3	Inserted device in D ² PAK. Document status promoted from preliminary data to datasheet. Added: <i>Section 2.1: Electrical characteristics (curves)</i> Updated <i>Section 4: Package mechanical data</i> . Added <i>Section 5: Packaging mechanical data</i> . Minor text changes.
06-Jun-2012	4	<i>Figure 9: Transfer characteristics</i> has been updated.
16-Jan-2017	5	Updated title, features, description and schematic diagram in cover page. Minor text changes in <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Updated <i>Section 2.1: "Electrical characteristics (curves)"</i> Updated package information section.

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