

## N-channel 1500 V, 0.7 $\Omega$ typ., 14 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

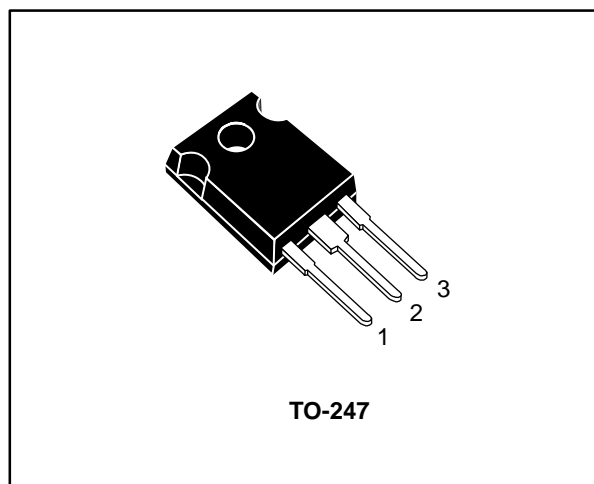
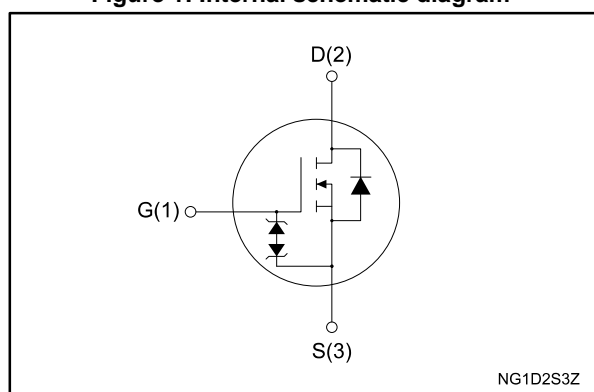


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STW21N150K5	1500 V	0.9 $\Omega$	14 A	446 W

- Industry's lowest R<sub>DS(on)</sub> \* area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW21N150K5	21N150K5	TO-247	Tube

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current at $T_C = 25\text{ }^\circ\text{C}$	14	A
$I_D$	Drain current at $T_C = 100\text{ }^\circ\text{C}$	8.7	A
$I_{DM}^{(1)}$	Drain current (pulsed)	56	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	446	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_j$	Operating junction temperature	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

**Notes:**

(1)Pulse width limited by safe operating area

(2) $I_{SD} \leq 14\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$

(3) $V_{DS} \leq 1200\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.28	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb	50	$^\circ\text{C}/\text{W}$

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Max current during repetitive or single pulse avalanche	5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	1100	mJ

**Notes:**

(1)Pulse width limited by  $T_{Jmax}$

(2)Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = I_{AS}$ ,  $V_{DD} = 50\text{ V}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	1500			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 1500\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 1500\text{ V}$ , $T_C = 125\text{ °C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 7\text{ A}$		0.7	0.9	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	3145	-	pF
$C_{oss}$	Output capacitance		-	172	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ V to }1200\text{ V}$ , $V_{GS} = 0\text{ V}$	-	161	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	65	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	2.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 1200\text{ V}$ , $I_D = 7\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	89	-	nC
$Q_{gs}$	Gate-source charge		-	16	-	nC
$Q_{gd}$	Gate-drain charge		-	59	-	nC

**Notes:**

<sup>(1)</sup>Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

<sup>(2)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 750\text{ V}$ , $I_D = 3.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17: "Unclamped inductive load test circuit"</a> )	-	34	-	ns
$t_r$	Rise time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	134	-	ns
$t_f$	Fall time		-	26	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}, V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i> )	-	448		ns
$Q_{rr}$	Reverse recovery charge		-	8.24		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	36.8		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}, V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times"</i> )	-	564		ns
$Q_{rr}$	Reverse recovery charge		-	9.48		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	33.6		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	30	-		V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

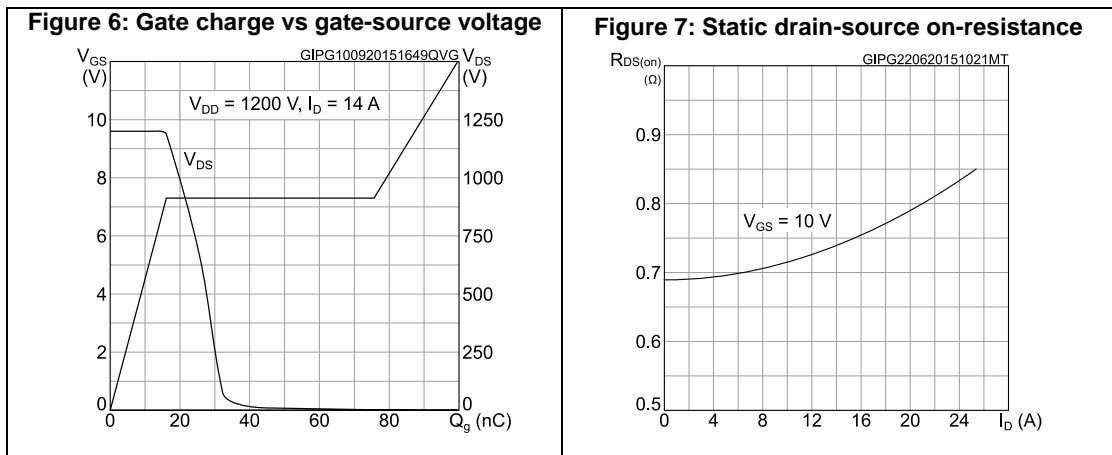
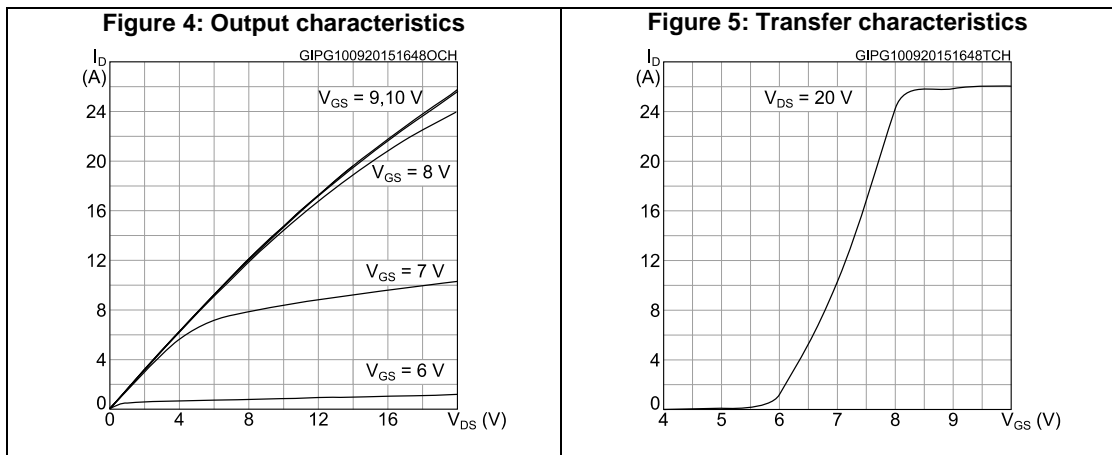
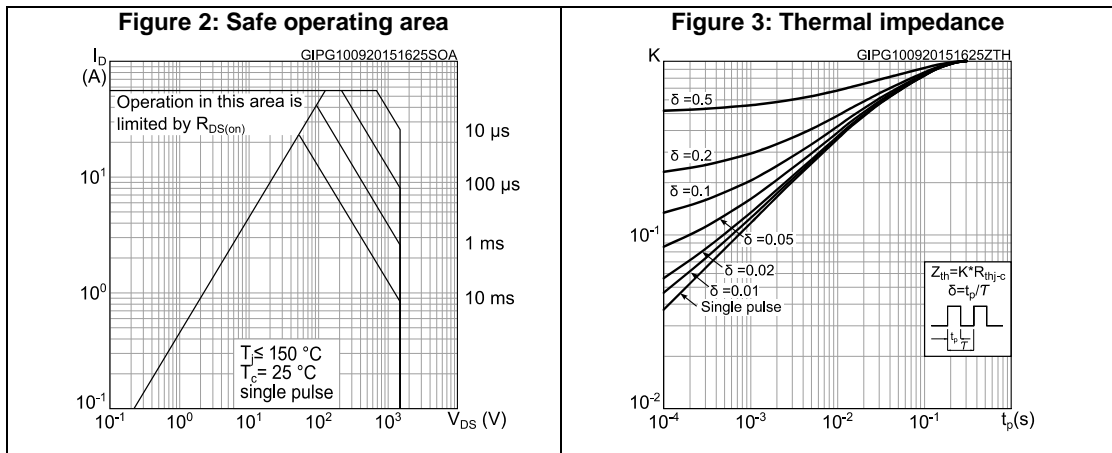


Figure 8: Capacitance variations

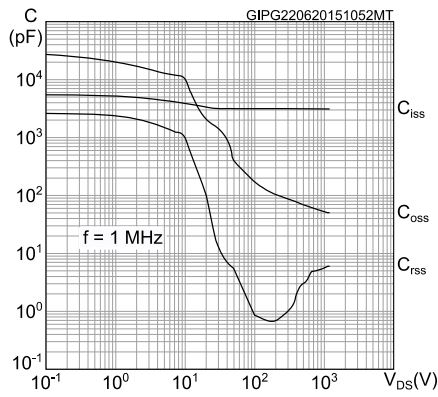


Figure 9: Normalized gate threshold voltage vs temperature

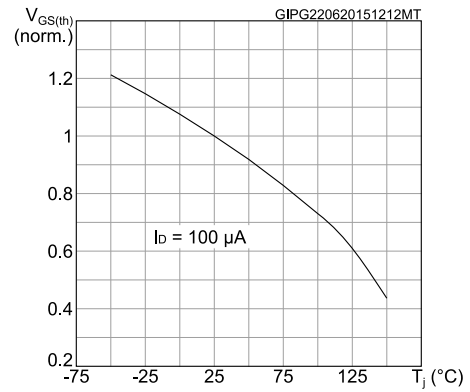


Figure 10: Normalized on-resistance vs temperature

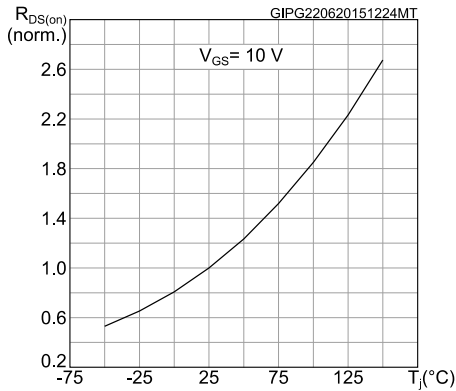


Figure 11: Normalized V(BR)DSS vs temperature

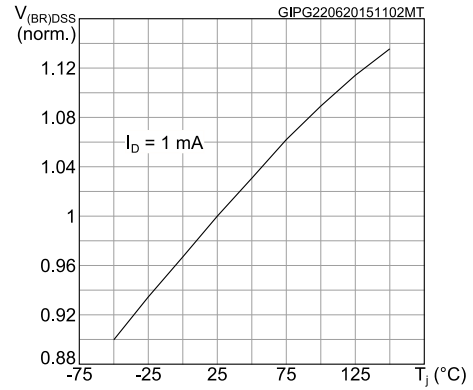


Figure 12: Maximum avalanche energy vs temperature

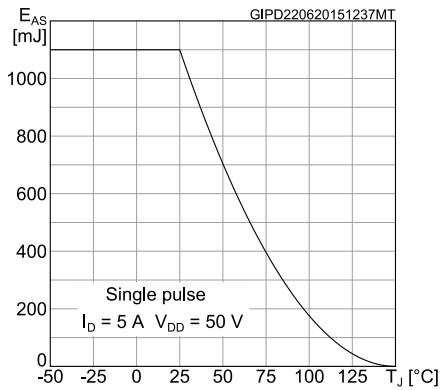
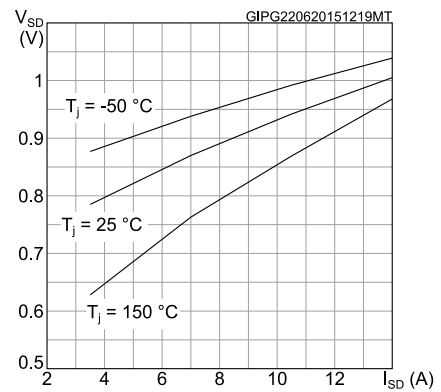
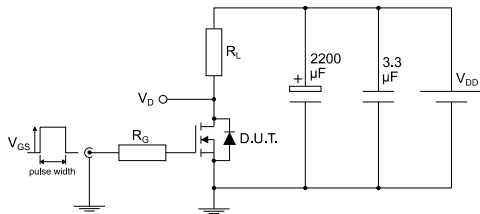


Figure 13: Source-drain diode forward characteristics



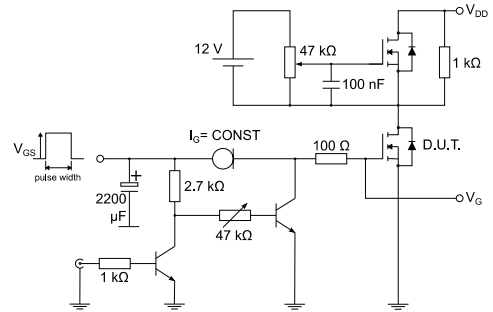
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



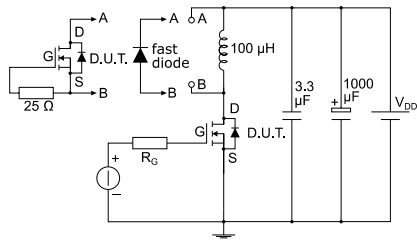
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**Figure 15: Test circuit for gate charge behavior**



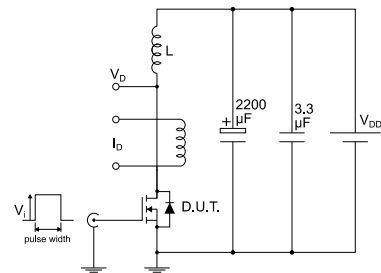
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



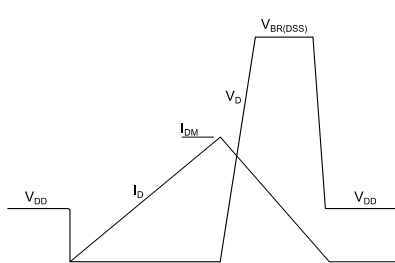
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**Figure 17: Unclamped inductive load test circuit**



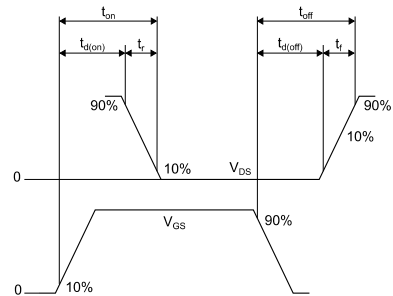
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**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

Figure 20: TO-247 package outline

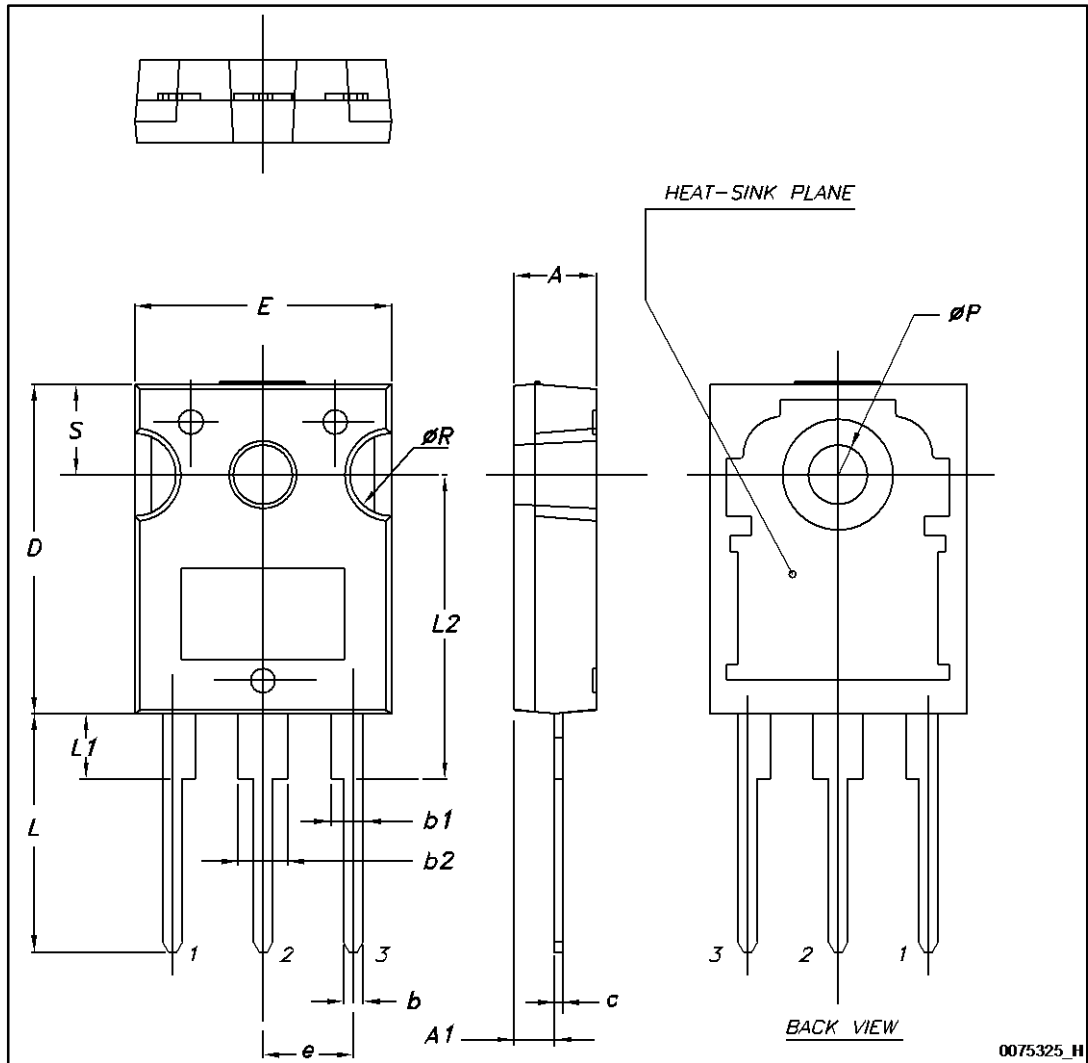


Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
26-Aug-2015	1	First release.
10-Sep-2015	2	Text and formatting changes throughout document. Updated features on cover page. Updated sections <i>Electrical ratings</i> and <i>Electrical characteristics</i> . Added section <i>Electrical characteristics (curves)</i> . Updated section <i>TO-247 package information</i> .
01-Oct-2015	3	On cover page: - updated figure Internal schematic diagram In section Electrical characteristics: - updated and renamed table Static (was On/off states).

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