

N-channel 950 V, 0.110 Ω typ., 38 A MDmesh™ K5 Power MOSFET in a TO-247 package

Datasheet - production data

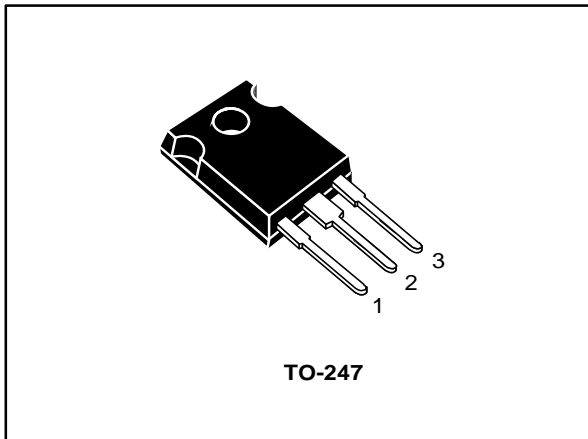
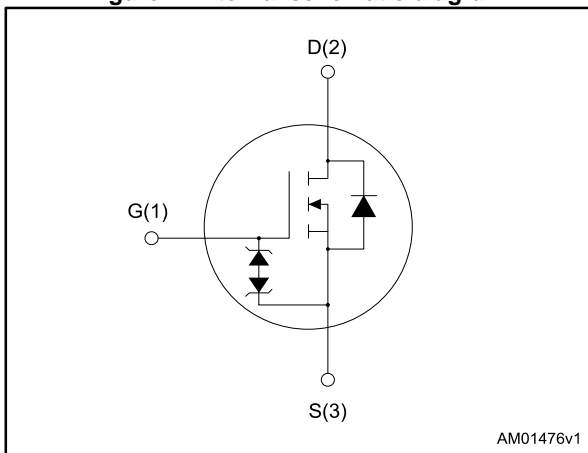


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D	P _{TOT}
STW40N95K5	950 V	0.130 Ω	38 A	450 W

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STW40N95K5	40N95K5	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate- source voltage	± 30	V
I _D	Drain current (continuous) at T _C = 25 °C	38	A
I _D	Drain current (continuous) at T _C = 100 °C	24	A
I _{DM} ⁽¹⁾	Drain current (pulsed)	152	A
P _{TOT}	Total dissipation at T _C = 25 °C	450	W
I _{AR}	Max current during repetitive or single pulse avalanche	13	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = 13 A, V _{DD} = 50 V)	700	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _j T _{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾I_{SD} ≤ 19 A, di/dt ≤ 100 A/μs, V_{DS(peak)} ≤ V_{(BR)DSS}.

⁽³⁾V_{DS} ≤ 760 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.28	°C/W
R _{thj-amb}	Thermal resistance junction-amb max	50	°C/W

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	950			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 950\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 950\text{ V}, T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$		0.110	0.130	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	3300	-	pF
C_{oss}	Output capacitance		-	250	-	pF
C_{riss}	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }760\text{ V}$	-	398	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	142	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}, I_D = 38\text{ A}$	-	93	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$	-	18.7	-	nC
Q_{gd}	Gate-drain charge	(see Figure 16: "Gate charge test circuit")	-	63.4	-	nC

Notes:

(1) Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

(2) Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}, I_D = 19\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 15: "Switching times test circuit for resistive load")	-	33.5	-	ns
t_r	Rise time		-	51	-	ns
$t_{d(off)}$	Turn-off-delay time		-	91.5	-	ns
t_f	Fall time		-	10	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		38	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		152	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 38 \text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 38 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 18: "Unclamped inductive load test circuit")	-	706		ns
Q_{rr}	Reverse recovery charge		-	22		μC
I_{RRM}	Reverse recovery current		-	62		A
t_{rr}	Reverse recovery time	$I_{SD} = 38 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 18: "Unclamped inductive load test circuit")	-	886		ns
Q_{rr}	Reverse recovery charge		-	28.2		μC
I_{RRM}	Reverse recovery current		-	64		A

Notes:

(1)Pulse width limited by safe operating area.

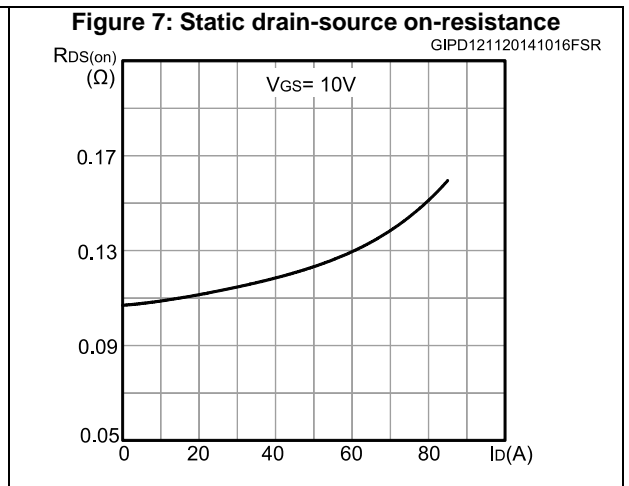
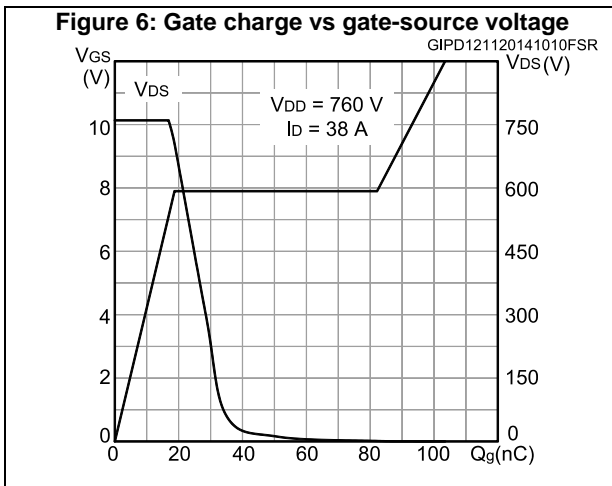
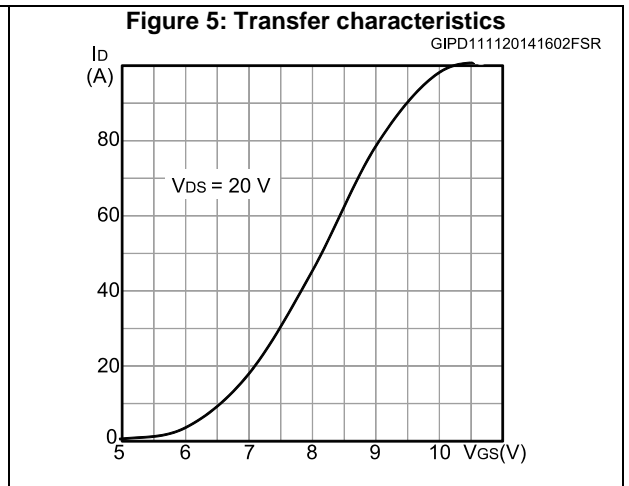
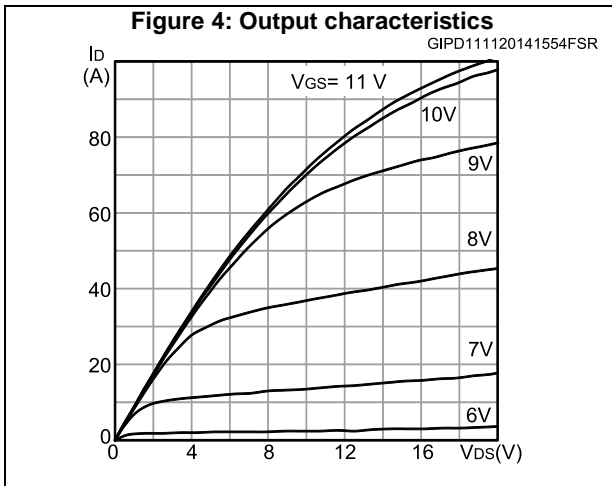
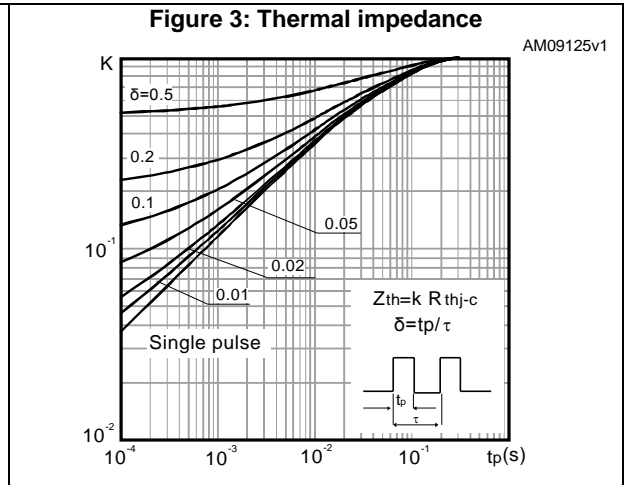
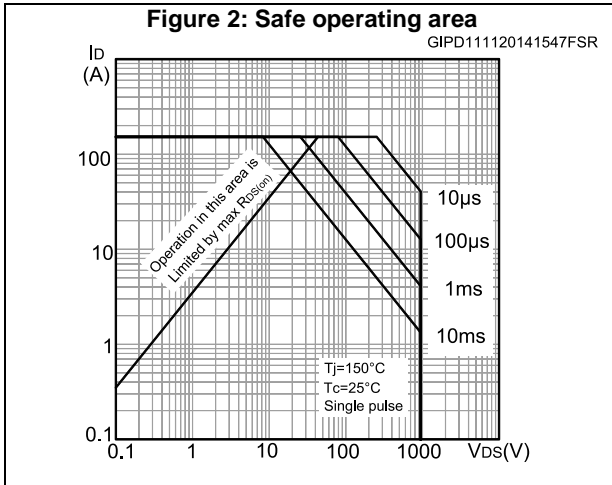
(2)Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)



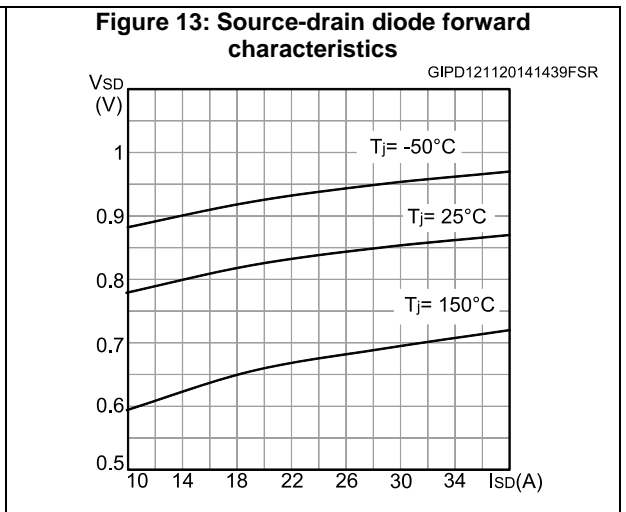
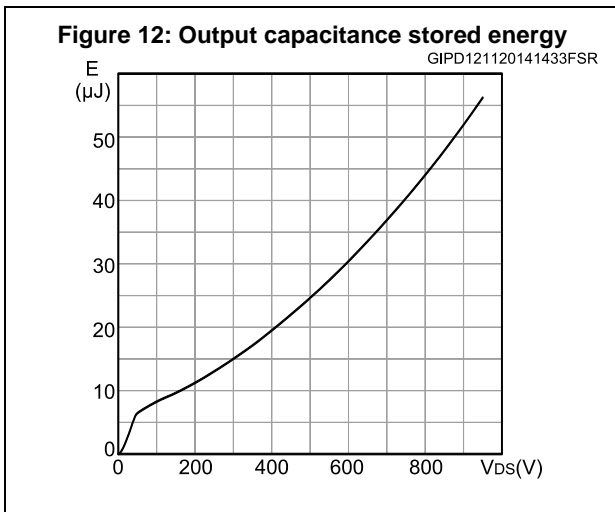
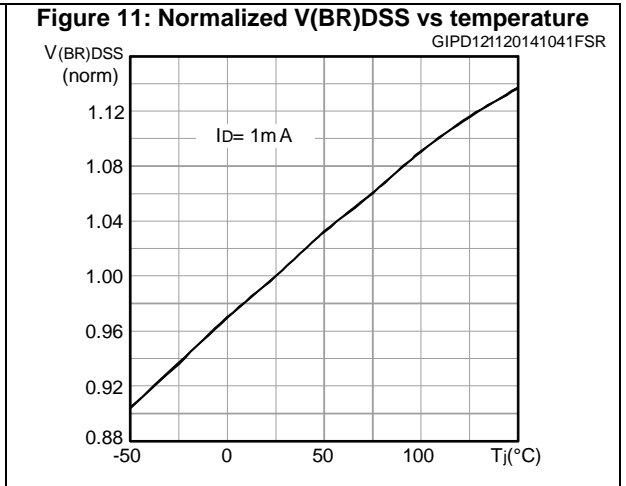
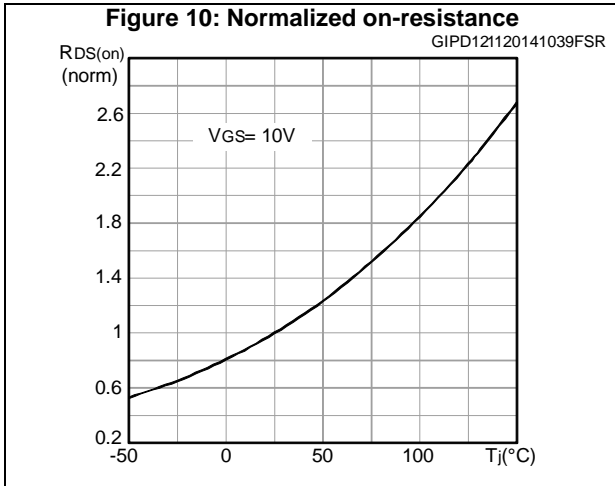
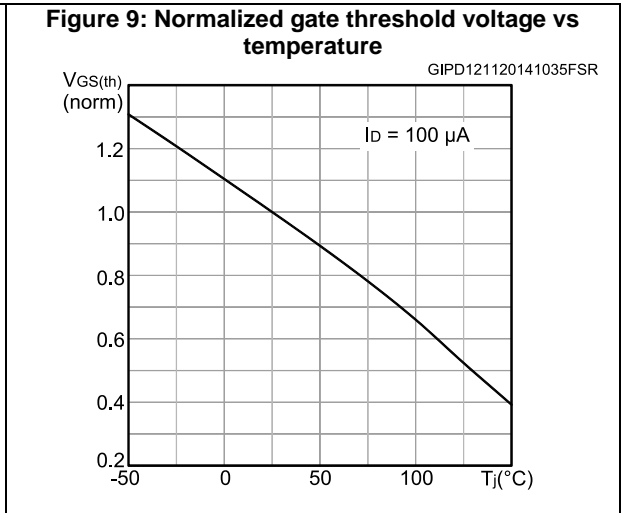
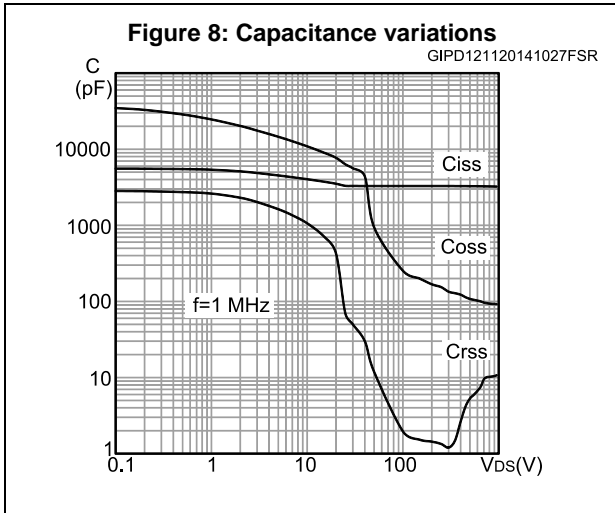
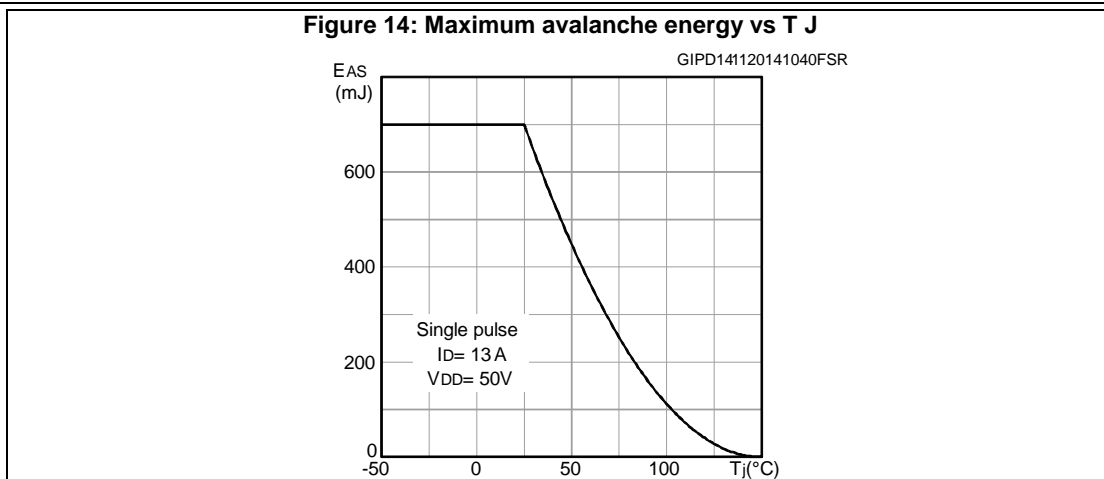


Figure 14: Maximum avalanche energy vs T J



3 Test circuits

Figure 15: Switching times test circuit for resistive load

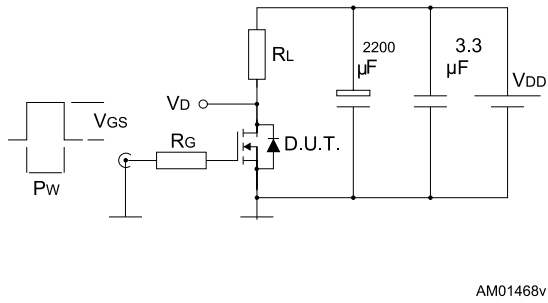


Figure 16: Gate charge test circuit

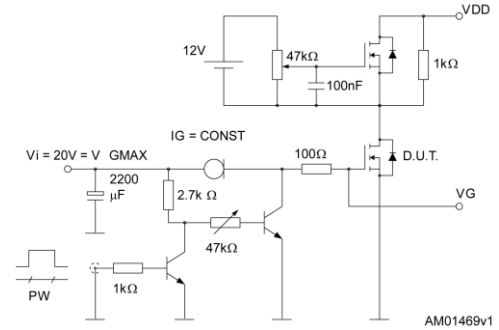


Figure 17: Test circuit for inductive load switching and diode recovery times

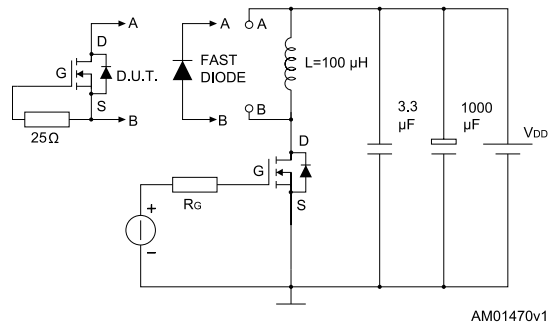


Figure 18: Unclamped inductive load test circuit

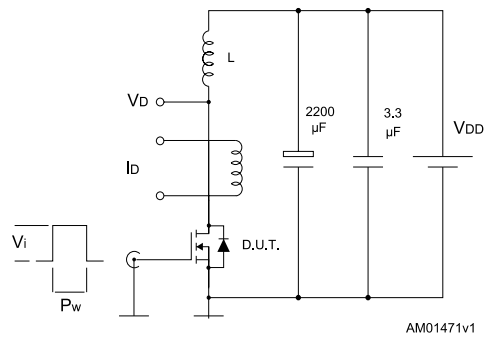


Figure 19: Unclamped inductive waveform

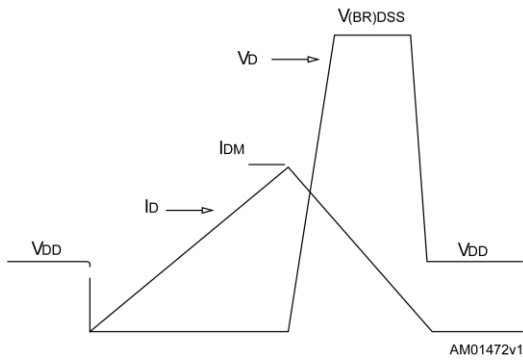
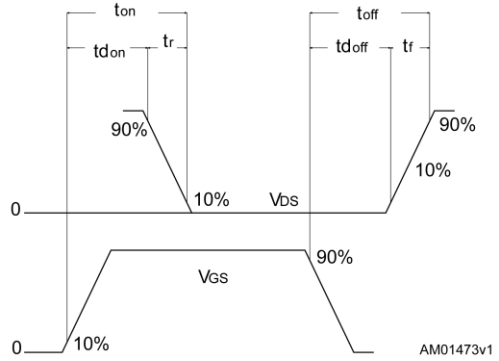


Figure 20: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 21: TO-247 drawing

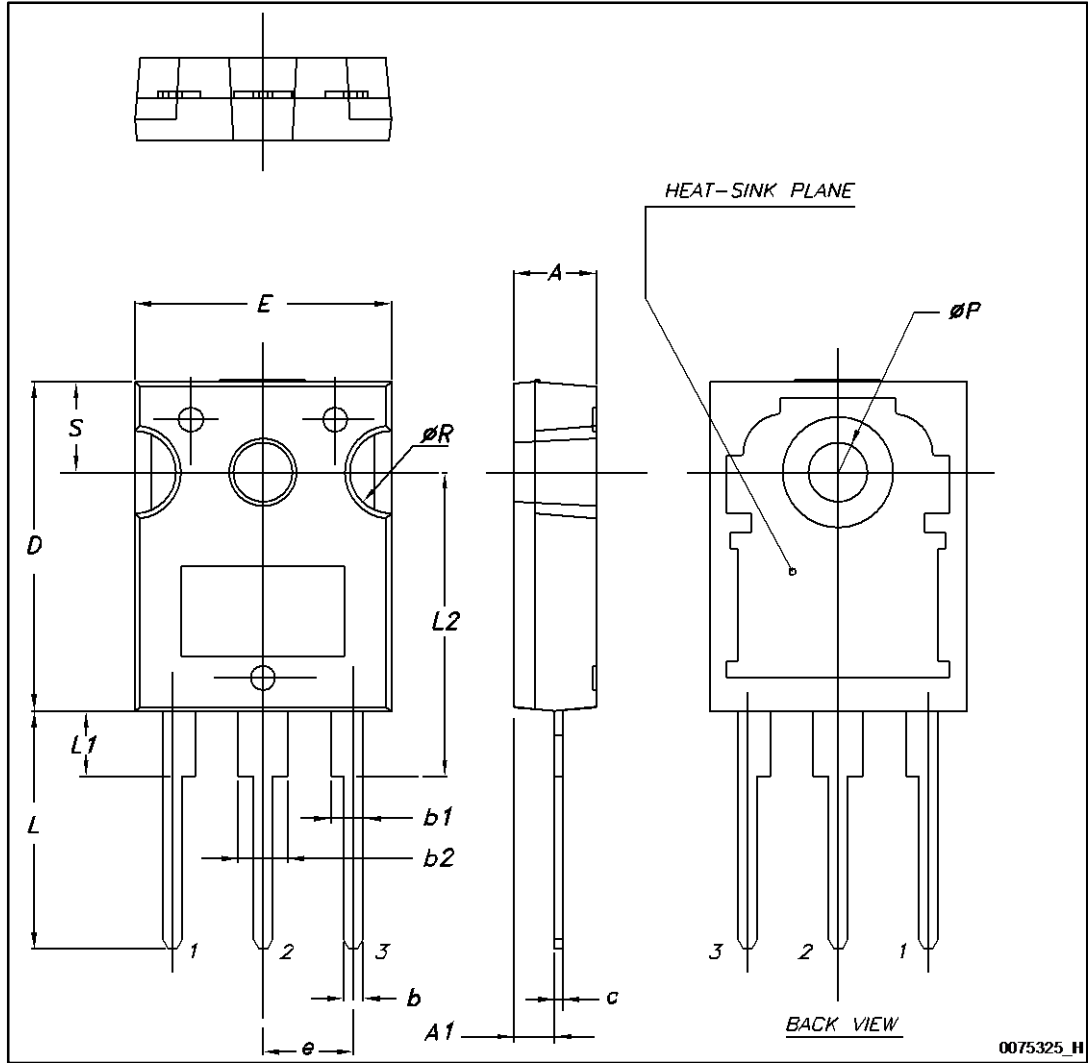


Table 9: TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
03-Jun-2014	1	First release.
14-Nov-2014	2	Document status promoted from preliminary to production data. Added Section 2.1: "Electrical characteristics (curves)" .

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