



STW40NS15

N-CHANNEL 150V - 0.042Ω - 40A TO-247

MESH OVERLAY™ MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW40NS15	150 V	<0.052Ω	40A

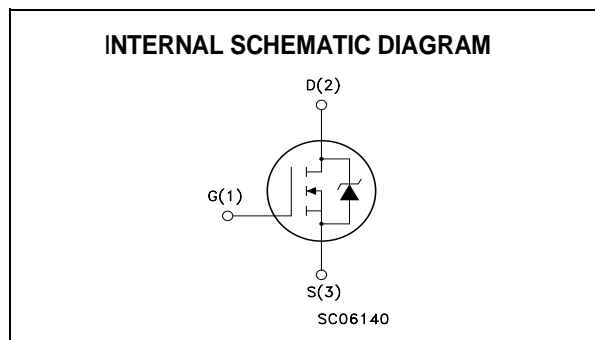
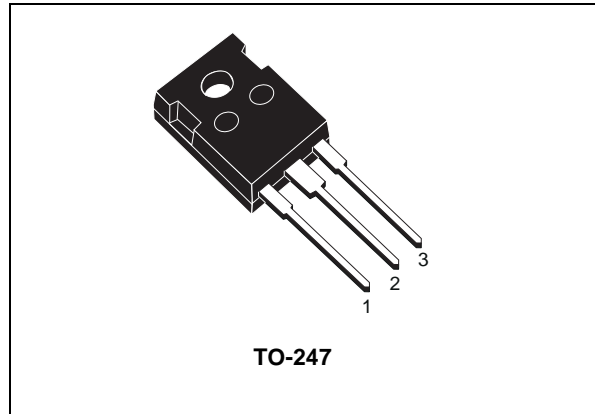
- TYPICAL R_{DS(on)} = 0.042Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

This powermos MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- PRIMARY SWITCH IN ISOLATED DC-DC CONVERTERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	150	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	150	V
V _{GS}	Gate- source Voltage	±20	V
I _D	Drain Current (continuous) at T _C = 25°C	40	A
I _D	Drain Current (continuous) at T _C = 100°C	25	A
I _{DM} ⁽¹⁾	Drain Current (pulsed)	160	A
P _{TOT}	Total Dissipation at T _C = 25°C	180	W
	Derating Factor	0.933	W/°C
dv/dt	Peak Diode Recovery voltage slope	9	V/ns
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(*)Pulse width limited by safe operating area

STW40NS15

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.83	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	40	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	500	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	150			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON ⁽¹⁾

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 40 A		0.044	0.052	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)max} , V _{GS} = 10V	40			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} , I _D = 20A		20		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		2400		pF
C _{oss}	Output Capacitance			380		pF
C _{rss}	Reverse Transfer Capacitance			160		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		25		ns
t_r	Rise Time			45		ns
Q_g	Total Gate Charge	$V_{DD} = 120V, I_D = 40A,$ $V_{GS} = 10V$		100	110	nC
Q_{gs}	Gate-Source Charge			17		nC
Q_{gd}	Gate-Drain Charge			47		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 75V, I_D = 20A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		85		
T_f	Fall Time					
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{clamp} = 120V, I_D = 20A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		47		ns
t_f	Fall Time			35		ns
t_c	Cross-over Time			70		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				40	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				160	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 40A, V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$ (see test circuit, Figure 5)		270		ns
Q_{rr}	Reverse Recovery Charge			200		nC
I_{RRM}	Reverse Recovery Current			1.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

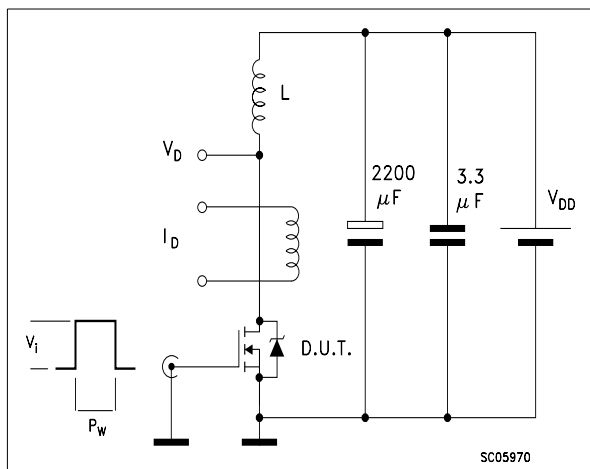


Fig. 2: Unclamped Inductive Waveform

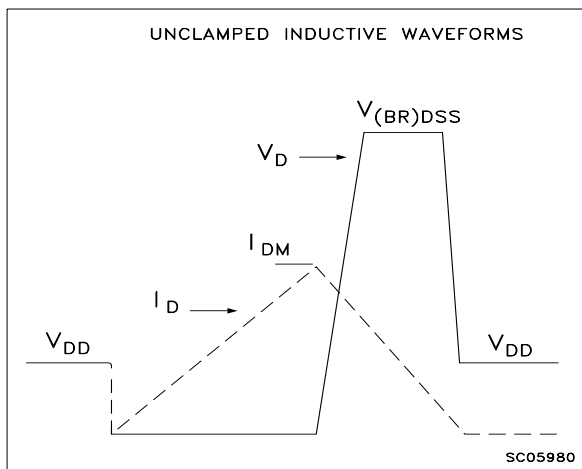


Fig. 3: Switching Times Test Circuit For Resistive Load

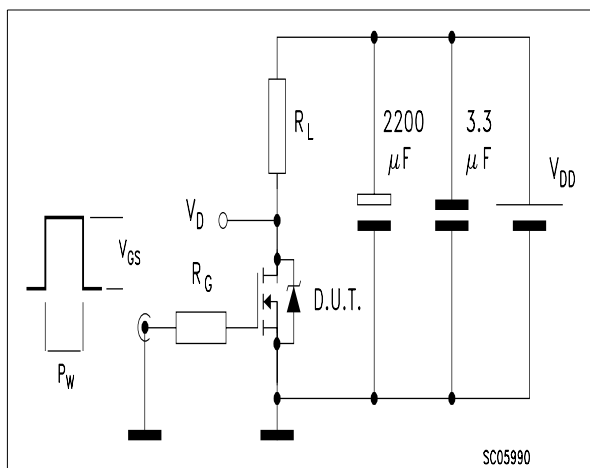


Fig. 4: Gate Charge test Circuit

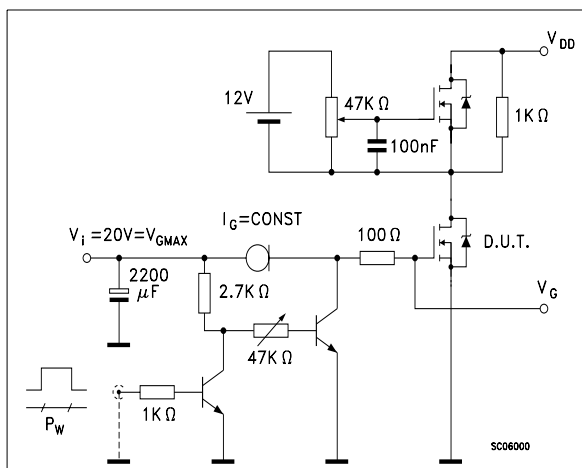
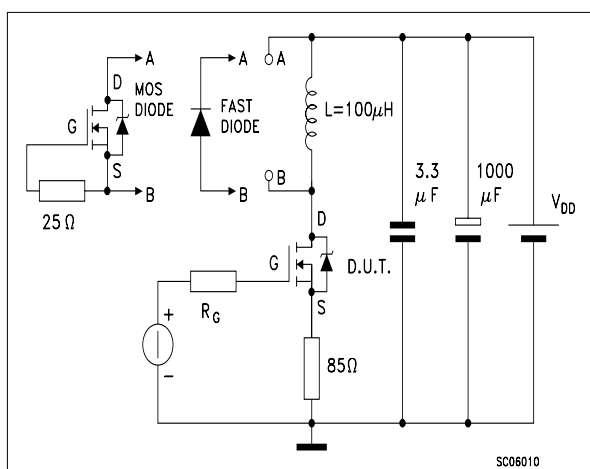
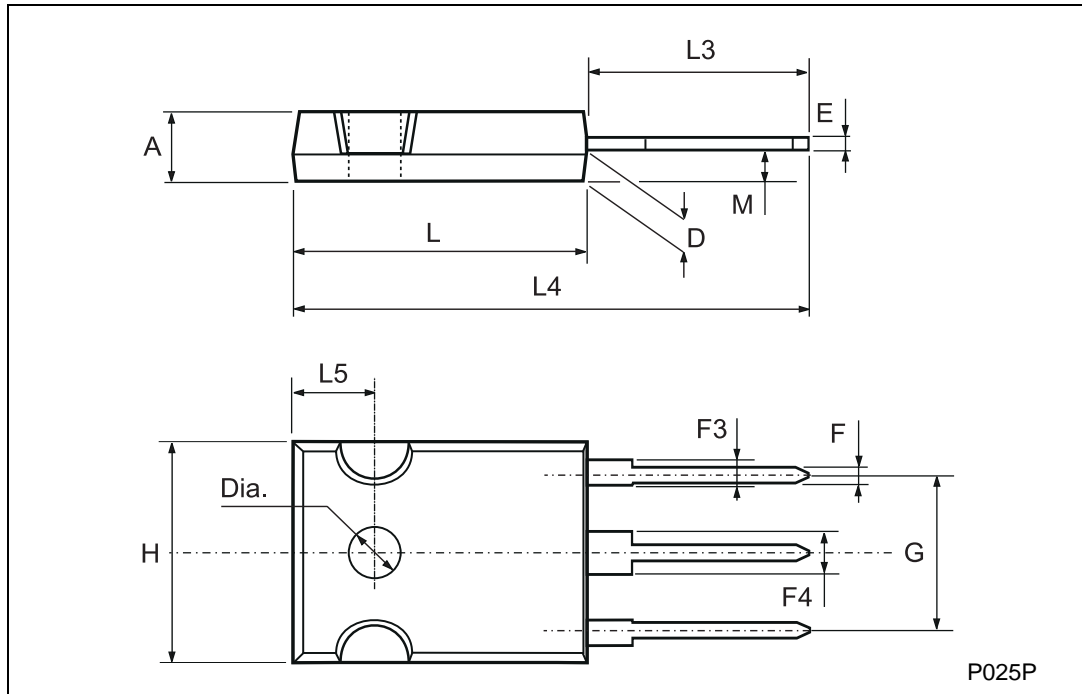


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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