



# STW48NM60N

## N-channel 600 V, 0.055 $\Omega$ typ., 44 A MDmesh™ II Power MOSFET in a TO-247 package

Datasheet — production data

### Features

Order codes	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STW48NM60N	650 V	< 0.07 $\Omega$	44 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

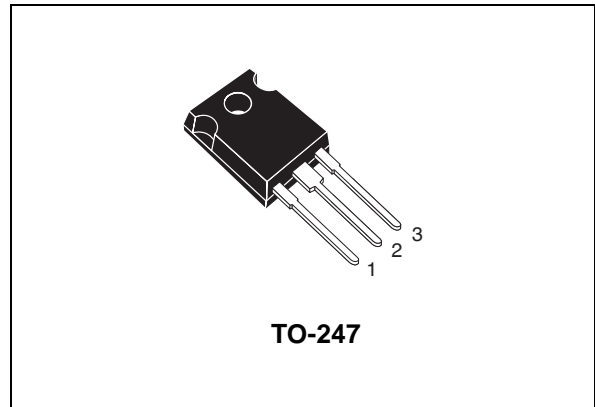


Figure 1. Internal schematic diagram

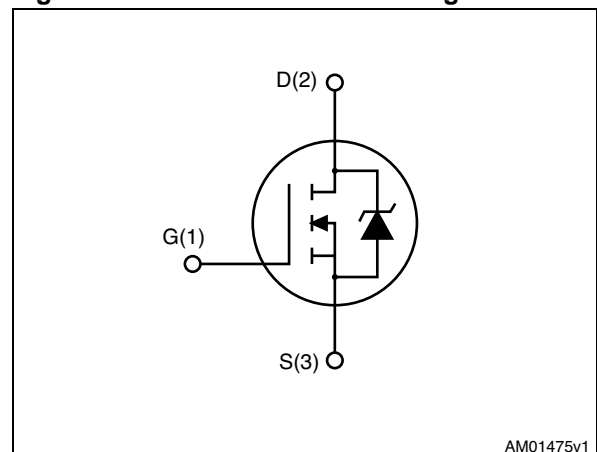


Table 1. Device summary

Order code	Marking	Package	Packaging
STW48NM60N	48NM60N	TO-247	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	44	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	28	A
$I_{DM}^{(1)}$	Drain current (pulsed)	176	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	330	W
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	457	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 44\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.38	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}, T_c = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.055	0.07	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	4285	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			212		pF
$C_{rss}$	Reverse transfer capacitance			9.5		pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	600	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}, V_{GS} = 0$		1.6		$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 44\text{ A},$ $V_{GS} = 10\text{ V},$ (see Figure 15)	-	124	-	nC
$Q_{gs}$	Gate-source charge			20		nC
$Q_{gd}$	Gate-drain charge			61.5		nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}, I_D = 20\text{ A}$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 14)	-	99	-	ns
$t_r$	Rise time			18		ns
$t_{d(off)}$	Turn-off delay time			214		ns
$t_f$	Fall time			25.5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		44	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		176	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 44 \text{ A}, V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 44 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	472		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$	-	10.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)	-	44.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 44 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	568		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$	-	14		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)	-	50		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

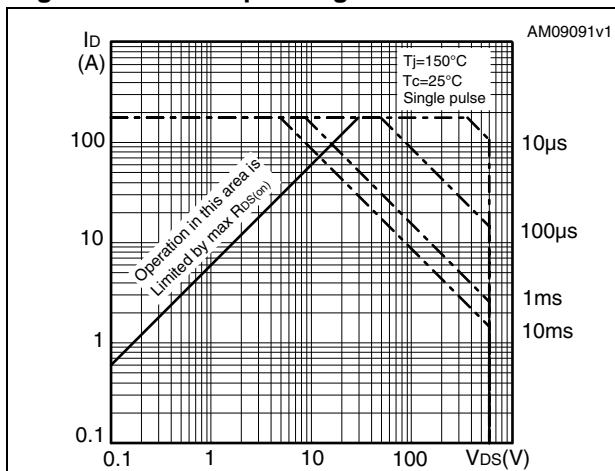


Figure 3. Thermal impedance

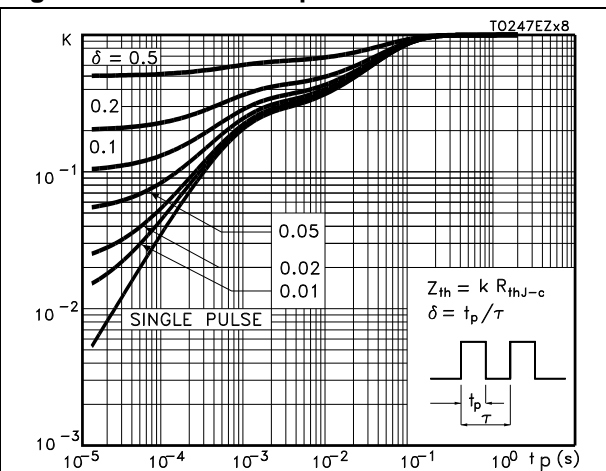


Figure 4. Output characteristics

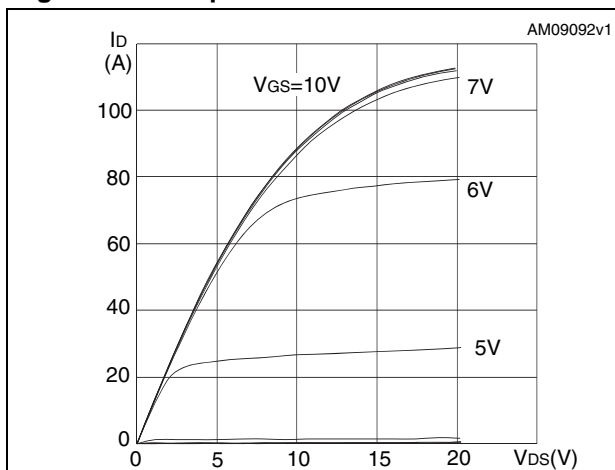


Figure 5. Transfer characteristics

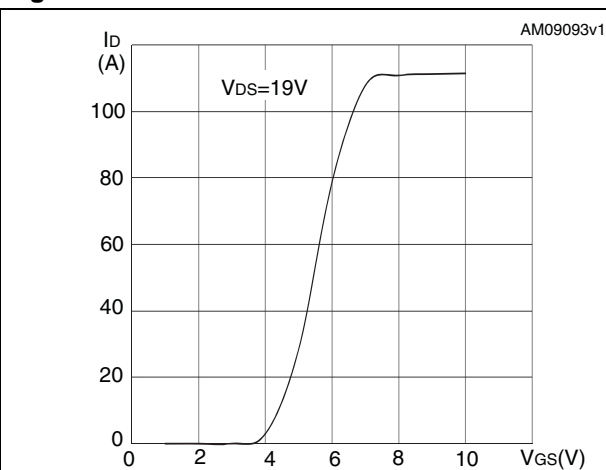


Figure 6. Normalized  $BV_{DSS}$  vs temperature

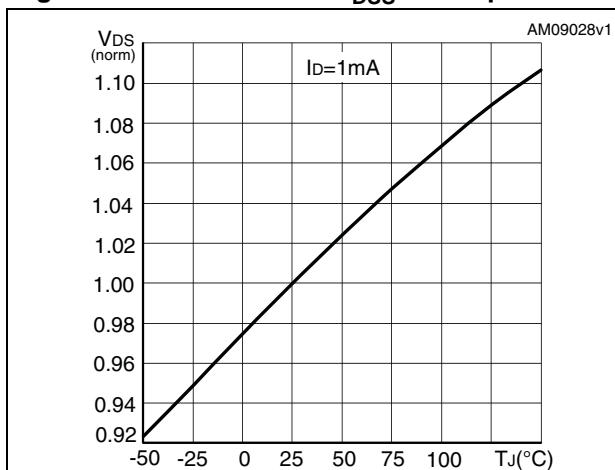


Figure 7. Static drain-source on-resistance

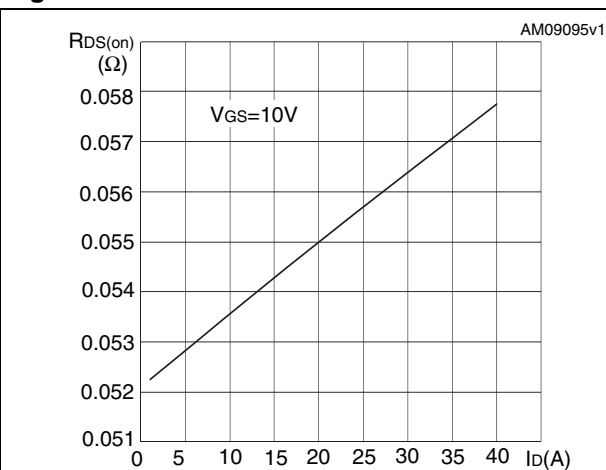


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

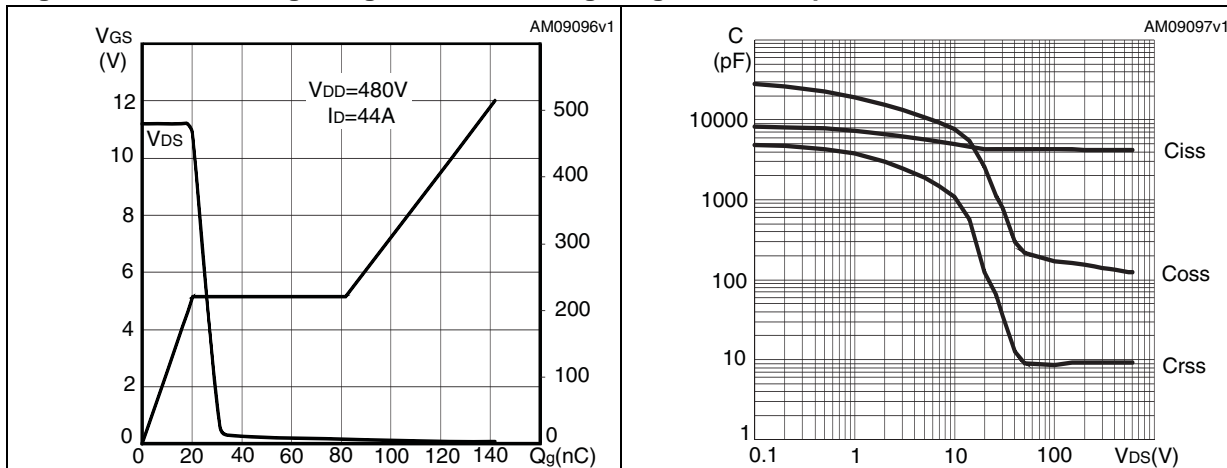


Figure 10. Output capacitance stored energy Figure 11. Normalized gate threshold voltage vs temperature

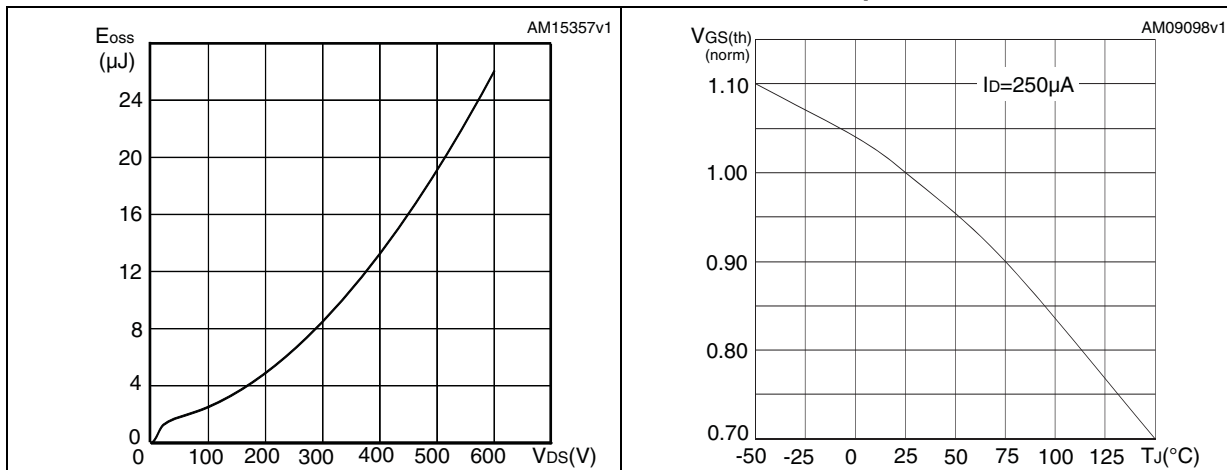
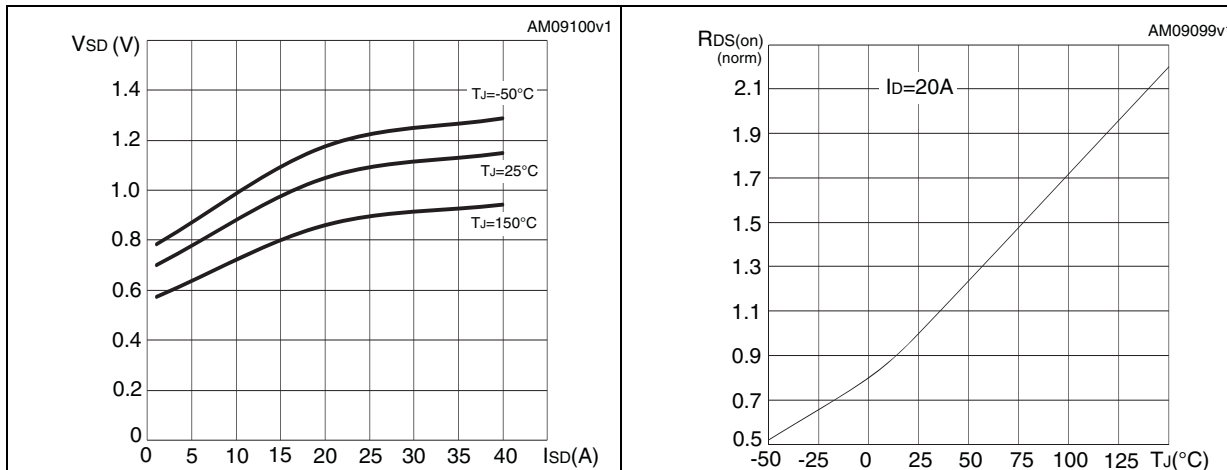


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized on-resistance vs temperature

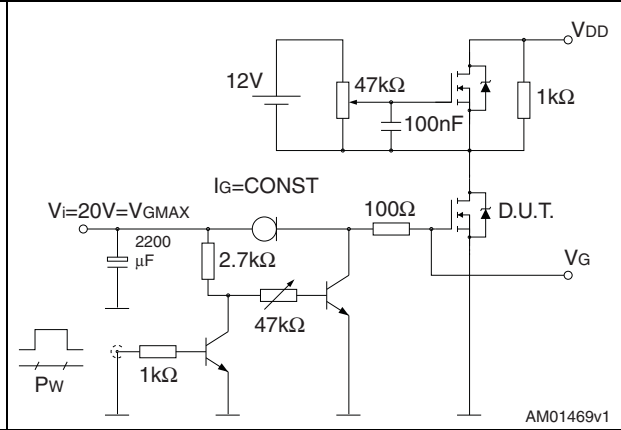


### 3 Test circuits

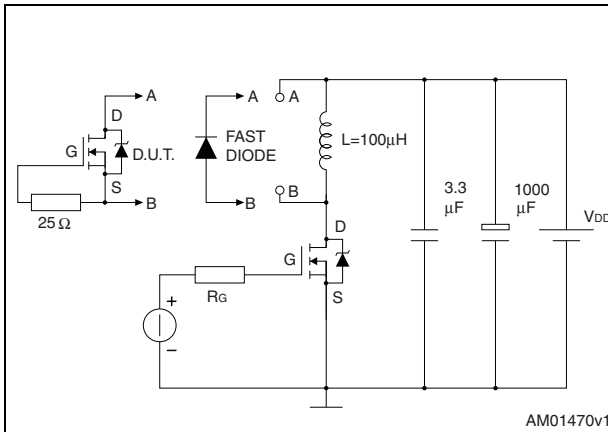
**Figure 14. Switching times test circuit for resistive load**



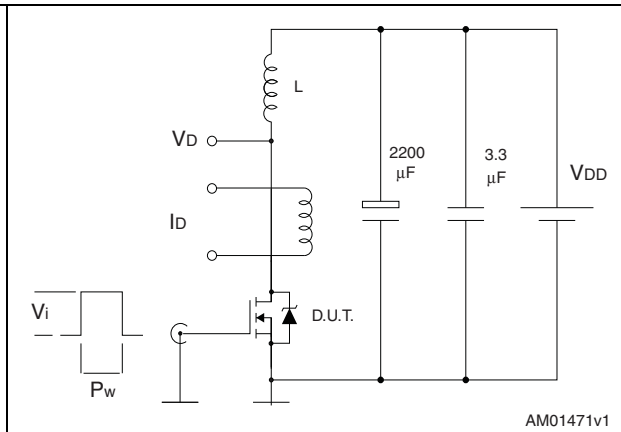
**Figure 15. Gate charge test circuit**



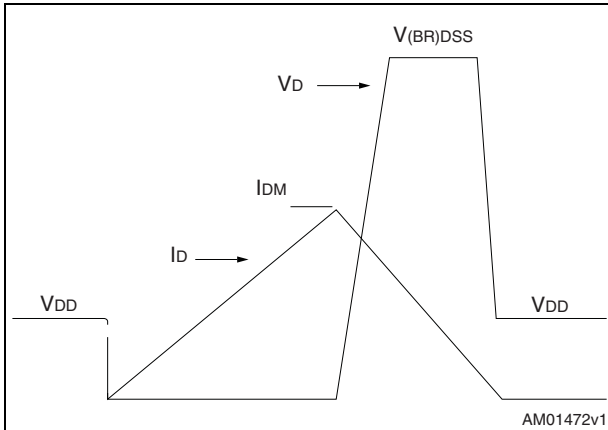
**Figure 16. Test circuit for inductive load switching and diode recovery times**



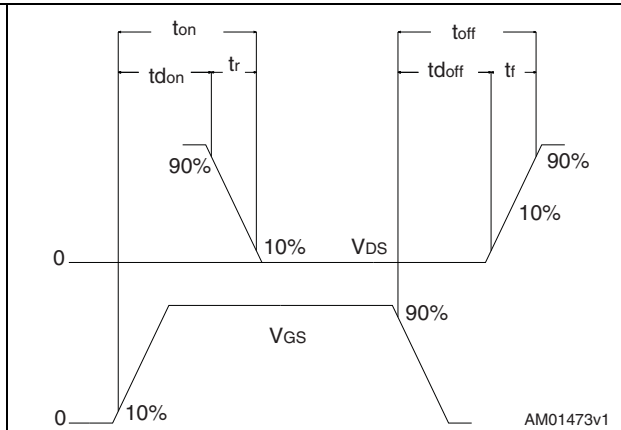
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**





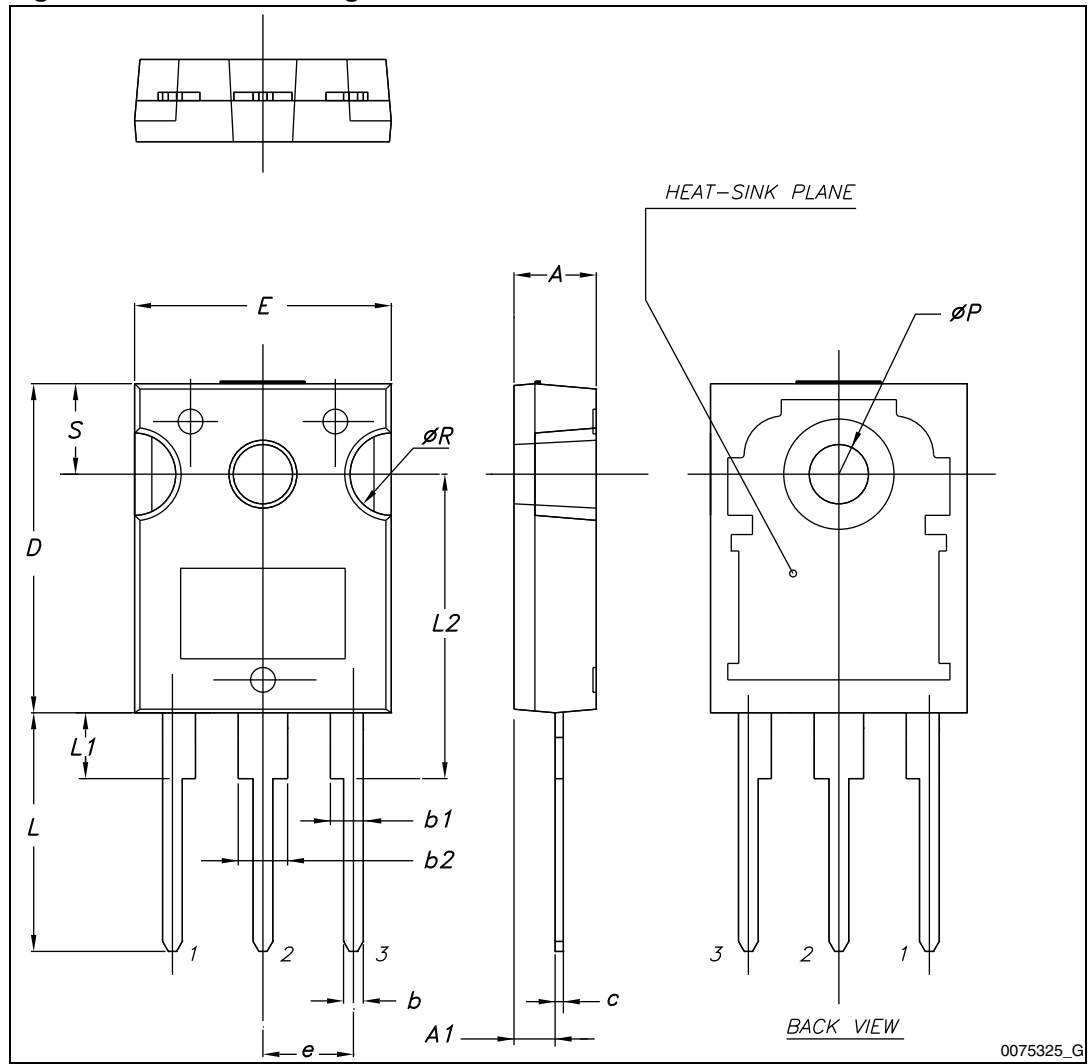
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 20. TO-247 drawing



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
06-Dec-2010	1	First release.
15-Apr-2011	2	Document status promoted from preliminary data to datasheet.
04-Jul-2011	3	Updated <a href="#">Figure 7</a> .
10-Oct-2012	4	– Modified: <a href="#">Figure 2</a> – Added: <a href="#">Figure 10</a> – Updated: <a href="#">Section 4: Package mechanical data</a>
19-Feb-2013	5	Updated <a href="#">Table 7: Source drain diode</a> .

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