GreenSIDE STW51000

SUPER INTEGRATED DSP ENGINE

DATA BRIEF

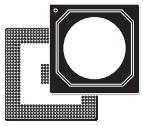
1 Product Features

- Super Integrated SoC including 2 x ST140 quad MAC DSP engines running at 600MHz and 1 x ARM926 Micro Controller running at 300MHz
- Double Quad-MAC units
- Double Quad-ALU (32 and 40-bit)
- 4800 MMacs/s - 29000 Mops - 7500 Mips
- Convolutional Decoder Engine:
  - 256 x 12.2 kpbs AMR voice users
  - Programmable Code Parameters to support multi-standards (W-CDMA, TD-SCDMA, CDMA2000 and EDGE)
- Turbo Decoder Engine:
  - 28 x 384 kbps (8 iterations)
  - Programmable Code Parameters to support multi-standards (W-CDMA, TD-SCDMA and CDMA2000)
  - Includes CRC Processing
  - Hardware Interleaver with multi-standard support
- Two 32-channel DMA Engines
- 16Mbit Central Memory shared among DSPs, µC and DMA Engines
- One 32-bit External Memory Controller
- One external Master Interface
- One 32-bit Communication Interface
- Two Multi-Channel Serial Ports
- Two Ethernet MAC
- One 16-bit UTOPIA Level 2 Interface
- 32-bit General Purpose I/Os
- Two 32-bit Timers
- Programmable PLL Clock Generator
- IEEE-1149.1 (JTAG)
- Development tools available
- Baseband modem SW deliverables available

2 ST140 Features

- 32-bit Load/Store Architecture
- 16-bit, 32-bit or 128-bit (SLIW) Instruction Set for high performance / high code density trade off

Figure 1. Package



PBGA/HSP-569

Table 1. Order Codes

Part Number	Package
STW51000AT	PBGA/HSP-569

- Conditional Instructions to reduce code size and overhead
- Built-in Coprocessor Interfaces for highly optimized Instruction Definition
- Compiler Friendly Instruction Set for high performance critical DSP Routines directly from C
- 8, 16, 32 and 40-bit Data Support
- Circular and bit-reversed Data addressing modes
- 32x16 bit Multiplier eases floating point to fixed point conversion
- 8-bit Overflow protection
- Bit Manipulation
- Normalization, Saturation
- Zero Overhead Loops
- 32Kbytes L1 Program Cache and 64Kbytes L1 Data Cache

3 ARM926 Features

- 32/16-bit RISC Architecture
- 32-bit ARM Instruction Set for maximum performance and flexibility
- 16-bit Thumb Instruction set for high code density
- Built-in Memory Management Unit for OS Support
- 32Kbytes L1 Program Cache
- 16KBytes L1 Data Cache

This is preliminary information on a new product now in development. Details are subject to change without notice.

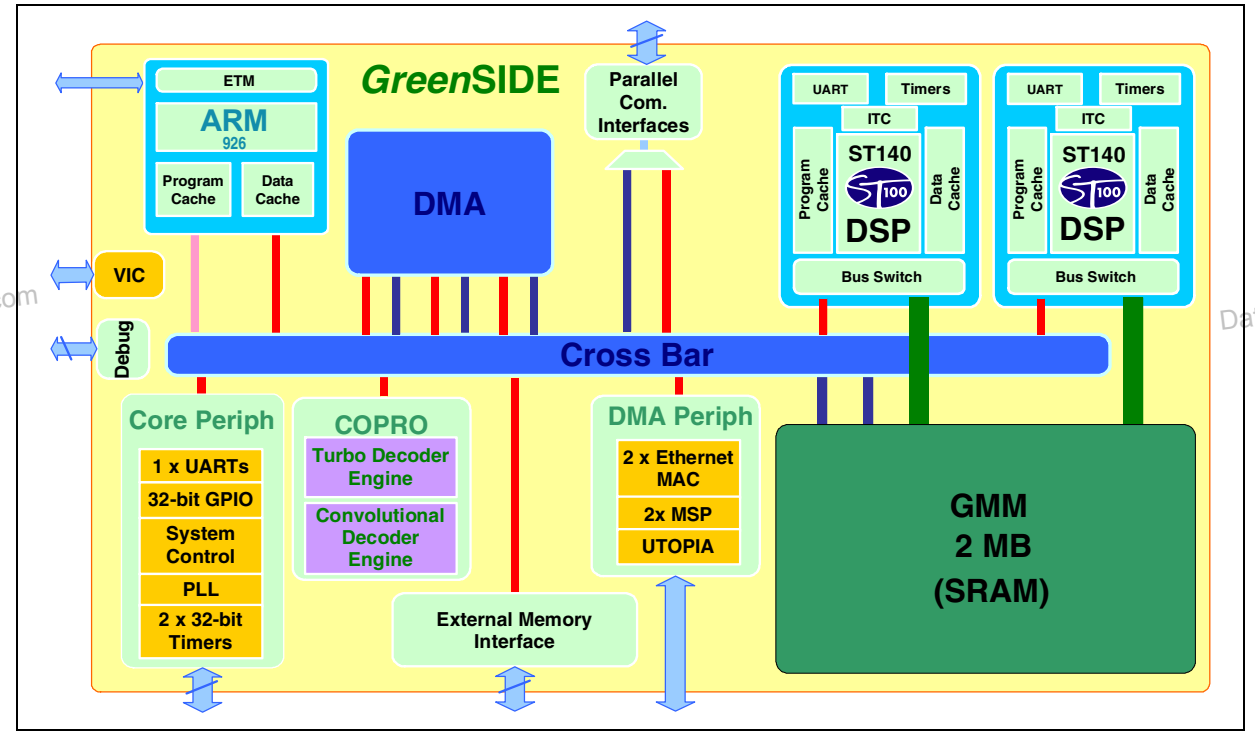
4 Overview/Description

GreenSIDE is a cost-effective, System-on-Chip device that targets applications in wireless infrastructure equipment. The device combines two quad-MAC ST140 DSP cores, a standard ARM926-EJS RISC processor core providing a total of 29000 Mops, 7500 Mips, 4800MMacs/s, 16Mb of embedded SRAM memory, dedicated Turbo Decoding Engine (TDE) for Data error correction, and Convolutional Decoding Engine (CDE) for Voice error correction for 2.5G and 3G standards, with a complete set of high-performance peripherals. As a highly-integrated baseband modem solution, GreenSIDE offers a unique opportunity to significantly reduce the overall cost/channel and cost/MIPS.

The GreenSIDE Super Integrated DSP Engine is based on the ST Open Wireless Infrastructure Platform. This is an extendable solution comprising hardware, software and integration tools used to develop a cost effective Wireless Infrastructure silicon solutions in a very short time.

The GreenSIDE ASSP is designed to be extremely flexible to suit all leading-edge wireless standards such as W-CDMA, CDMA2000, TD-SCDMA and EDGE. GreenSIDE is a step forward in the System Integration race. It offers a true System-on-Chip solution, including multiple embedded cores, and infrastructure application specific IP elements.

Figure 2. GreenSIDE ASSP Block Diagram



5 Architecture Overview

The GreenSIDE architecture is designed using ASIC Methodology. It employs re-usable embeddable cores as well as application specific IP blocks such as a Turbo Decoder Engine, Convolution Decoder Engine, UTOPIA Interface, Multi-channel Serial Ports, Ethernet MAC, etc.

The GreenSIDE Super Integrated DSP Engine includes two ST140 Digital Signal Processing CPUs. Each ST140 is a Quad-MAC DSP engine, able to process up to 24 complete W-CDMA modems for 12.2 kbps voice users. Having two ST140 instances provides the support of 48 above defined voice users processing capability.

GreenSIDE also includes an ARM926 micro-controller, used as a master for the complete system. It allows the setup of peripherals within the system, and schedules the DSP task execution.

The GreenSIDE bus architecture is based on the Multi-Layer AHB (Transfer Cross Bar). This bus architecture provides a large amount of bandwidth in the system, and prevents the bus architecture from being a bottleneck.

A 16Mbit memory provides a data exchange capability between CPUs. It allows storage of a collection of data coming from Fast Serial Ports or other DMA-based peripherals.

6 ST140 Overview

The ST140 is a 32-bit MCU/16-bit DSP Load/Store architecture, which provides full DSP-MCU capability. This capability is hosted by a comprehensive 32-bit Instruction set plus a 16-bit Instruction set for high code density, and a specific instruction mode offering an increased level of parallelism suitable for high performance DSP operations. The ST140 architecture is designed for maximum code efficiency for both micro-controller code and vector DSP code, even when programmed with "C" Language. The 32 x 40-bit data registers correspond to "C" data types and allow high precision results. The 17 x 32-bit Pointer / Index registers provide easy data access and the 3 hardware loop controllers are managed using C. The ST140 Compiler checks for parallel arguments at the instruction level, checks blocks of code, determines critical paths and dependencies and re-orders instructions to benefit from the predication and to maximize speed. The ST140 is fully pipelined for maximum efficiency; while data accesses are access decoupled for minimum access latency and reduced need to use the Data Registers. ST140 includes a 32Kbytes Program and 64 Kbytes Data Cache for high performance execution.

Table 2. ST140 Benchmarks

Functions	Formula	N	B	T	M	Cycles
Real Block IFR	(T+1) x N/4 + 24	40		16		194
Simple-Sample FIR	T/4 + 14	1		16		18
Complex Block FIR	(T + 0.5) x N + 13	40		16		673
LMS	T/2 + 16	1		16		28
IIR	N/A	1	2			8
Vector Dot Product	N/4 + 11	40				21
Vector Add	N / 2 + 11	40				31
Vector Maximum	N/4+10	40			5	20
FFT Radix-4	-	256				1380

N : Nb of Points - B: Nb of Sections - T: Nb of Taps - M: Nb of New Relative Maxima

7 ARM Sub-System Overview

The GreenSIDE ASSP is based on the open ARM PrimeXSys™ platform built around the ARM926 core and includes a set of Peripherals and an AMBA Multi-Layer AHB system bus for maximized throughput.

The ARM Sub System contains a set of standard Peripherals including Timers, Watchdog, 32-bit GPIOs, and Clock/System Controller.

Beside the standard peripherals the ARM Sub system also contains a set of high-speed DMA Peripherals including Multi-Channel Serial Ports, UTOPIA interface, Turbo Decoder Engine and Convolutional Decoder Engine.

Three DMA Engine manage all DMA operations over the System. An Interrupt Controller with 32 standard interrupts and 16-vectored interrupts provides a simple software interface to the interrupt system. For expansion purpose, two External Memory Controllers can address SRAM, Flash, ROM or I/O Devices. Those External Devices can be accessed by either DSPs or MCU.

8 Wireless Development Library

STMicroelectronics provides a complete set of libraries that implement complete Layer 1 of wireless standards such as EDGE, WCDMA FDD Release 4, 5, 6, TD-SCDMA, CDMA2000 1xEV-DO, 1xEV-DV, optimized for the GreenSIDE device and platform.

9 NODE B - GreenSIDE Implementation Examples

Figure 3. W-CDMA Node-B (1-Carrier, 96 voice users) - 2 chip-based

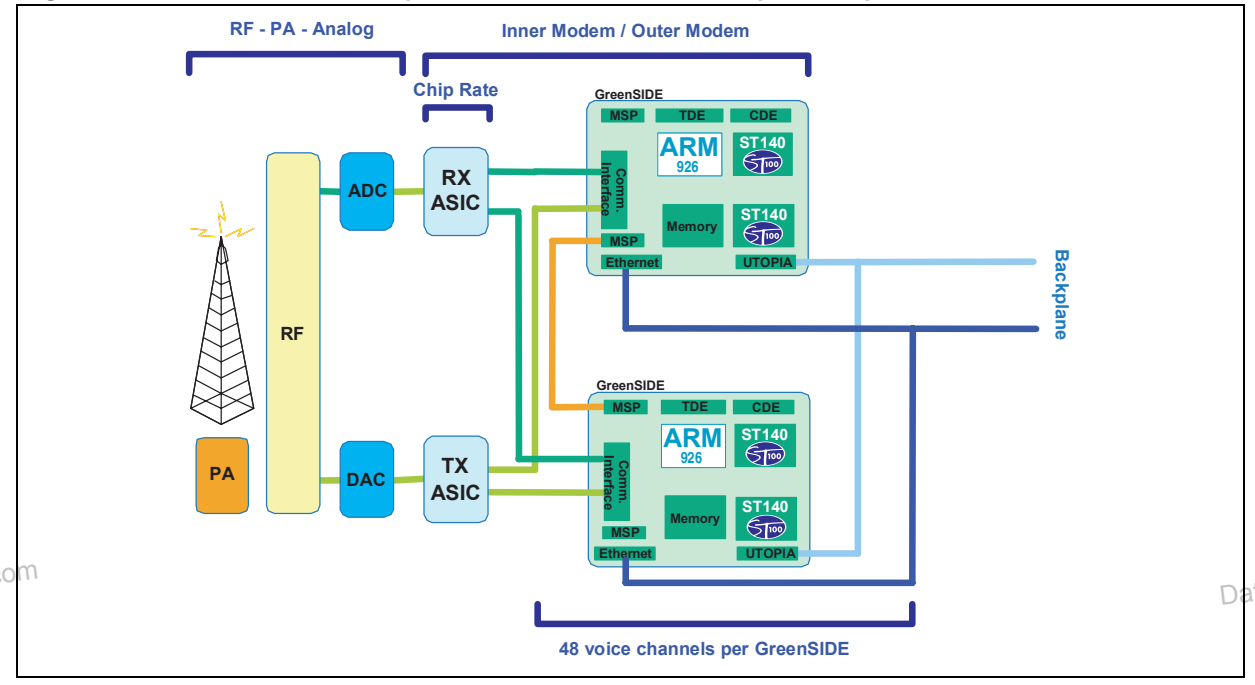
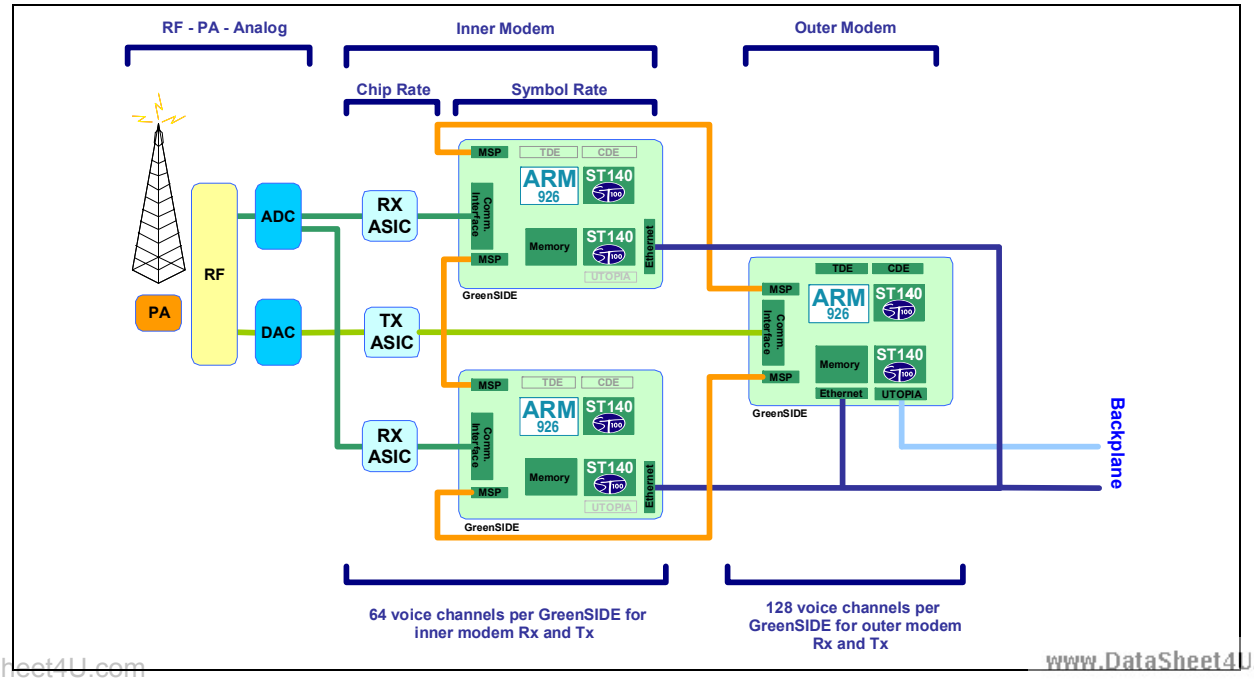


Figure 4. W-CDMA Node-B (1-Carrier, 128 voice users) - 3 chip-based



10 Development Support

STMicroelectronics provides a complete set of development tools around the GreenSIDE Super Integrated DSP Engine, to evaluate the performance, and to develop, debug, and integrate Application Code on the chip via an ARM/DSP environment, providing multi-Core Development/Debug capabilities.

10.1 Software Development Tools:

Software Development Tools for ARM and ST140 include an Integrated Development Environment tool, the C/C++ Compiler, Assembler and Linker Code Generation, the Instruction Set Simulator and the OS-aware Debugger application for Simulation and Emulation Debug. Beside standard Software Development Tools, RTOS dedicated tools for application-level debugging and analysis of embedded applications are available. It includes Runtime Debugging, System and Process information viewing, Manual Process Control, System Event Tracing and Monitoring, Memory Analysis and Message Search, CPU usage analysis and more.

10.2 Software Libraries

GreenSIDE silicon comes along with a Chip Support Package, which includes low level driver software (to configure and use GreenSIDE peripherals), RTOS Support (commercial OS porting to GreenSIDE platform) and application specific libraries (ATM, TCP/IP, ...).

10.3 Hardware development tools

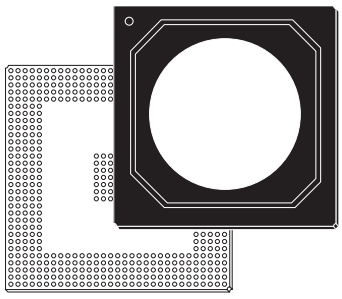
In addition to Software Development Tools, a complete set of Hardware tools help GreenSIDE users to speed-up the development of new applications. The GreenSIDE Evaluation Board is used to evaluate GreenSIDE performance, as well as to develop Software Application. It offers a basic set of peripherals in addition to the GreenSIDE built-in peripherals.

11 Package Information

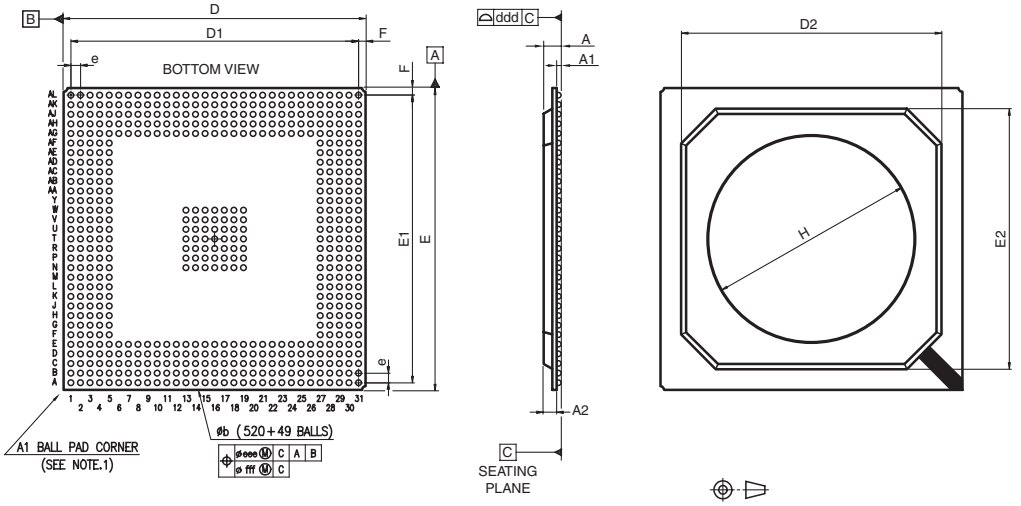
Figure 5. PBGA/HSP-569 (40x40x2.46mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.46			0.097
A1	0.36			0.142		
A2		1.73			0.068	
b	0.60	0.75	0.90	0.024	0.029	0.035
D	39.80	40.00	40.20	1.567	1.575	1.583
D1		38.10			1.500	
D2		34.50			1.358	
E	39.80	40.00	40.20	1.567	1.575	1.583
E1		38.10			1.500	
E2		34.50			1.358	
e		1.27			0.05	
F		0.95			0.037	
H		27.00			1.062	
ddd			0.20			0.008
eee			0.30			0.012
fff			0.15			0.006

OUTLINE AND MECHANICAL DATA



PBGA/HSp-569 (40x40x2.46mm)
Heat Spreader Plastic Ball Grid Array



(1) - The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug
- A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner.
- Exact shape of each corner is optional.

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12 Revision History

Table 3. Revision History

Date	Revision	Description of Changes
22-mar-2005	1	First Issue.
04-apr-2005	2	Updated the Section 1 first point “Micro Controller”. Updated the Section 7 “PrimeXSys™”.