STW56NM60N

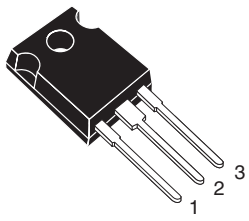
N-channel 600 V, 0.05 Ω, 45 A TO-247 MDmesh™ II Power MOSFET

Preliminary data

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STW56NM60N	600 V	< 0.06 Ω	45 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



TO-247

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Figure 1. Internal schematic diagram

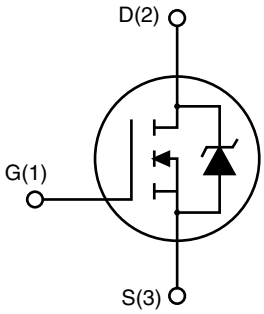


Table 1. Device summary

Order code	Marking	Package	Packaging
STW56NM60N	56NM60N	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	45	A
I_D	Drain current (continuous) at T_C = 100 °C	28	A
I_{DM} (1)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	TBD	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}=50 V)	TBD	mJ
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤11 A, di/dt ≤400 A/µs, V_{DS} peak ≤$V_{(BR)DSS}$, VDD = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.42	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA,	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C = 125 °C			1 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 22.5 A		0.05	0.06	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	4800 320 4.5	-	pF pF pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	TBD	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 45 A, V_{GS} = 10 V, *(see Figure 3)*	-	150 TBD TBD	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 22 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 2)*	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		45 180	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 45 A, di/dt = 100 A/µs V_{DD} = 100 V *(see Figure 4)*	-	TBD TBD TBD		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 45 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *(see Figure 4)*	-	TBD TBD TBD		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

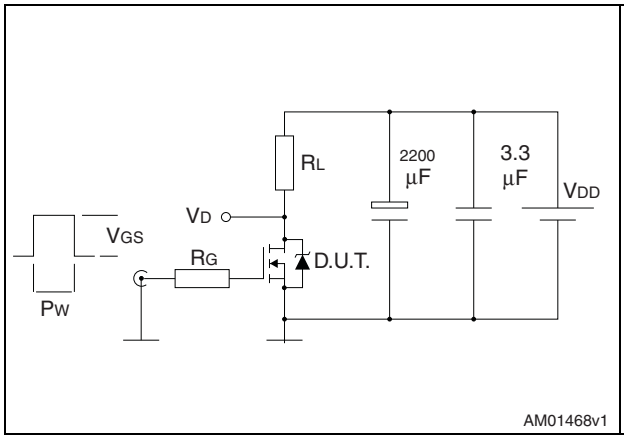


Figure 3. Gate charge test circuit

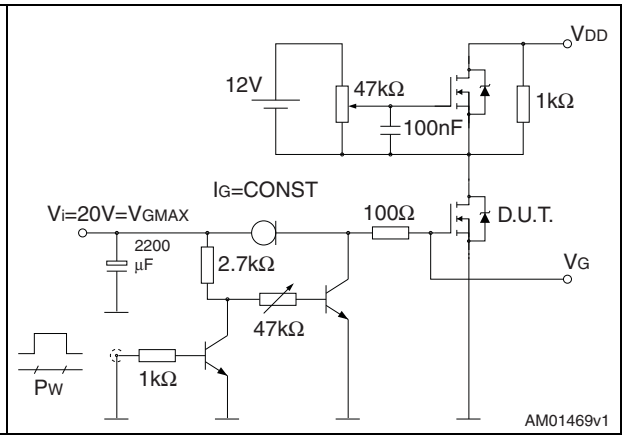


Figure 4. Test circuit for inductive load switching and diode recovery times

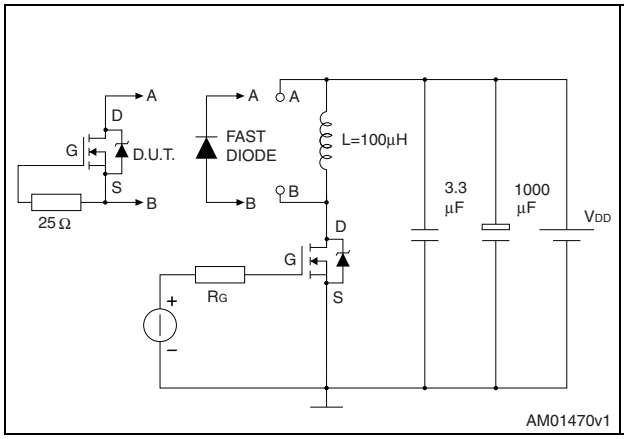


Figure 5. Unclamped inductive load test circuit

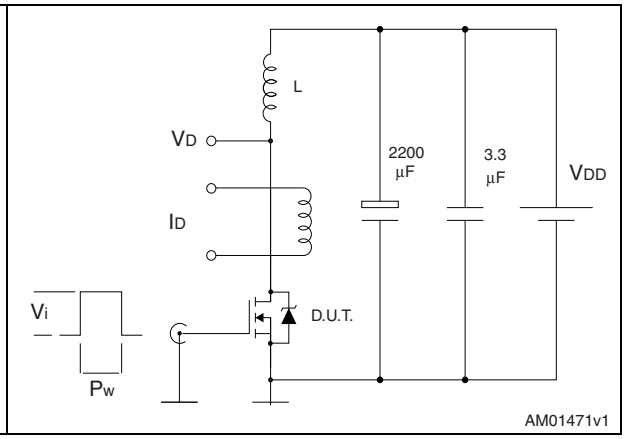


Figure 6. Unclamped inductive waveform

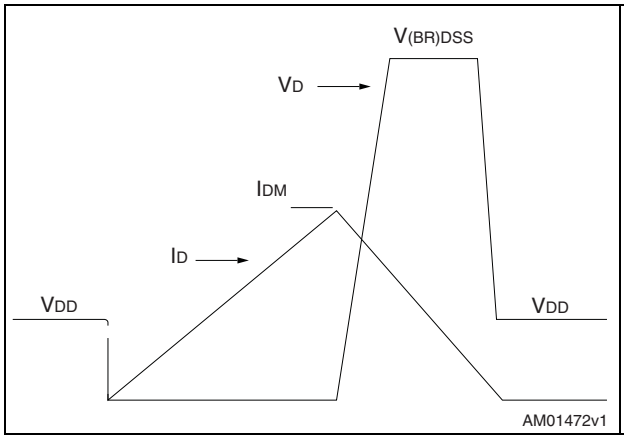
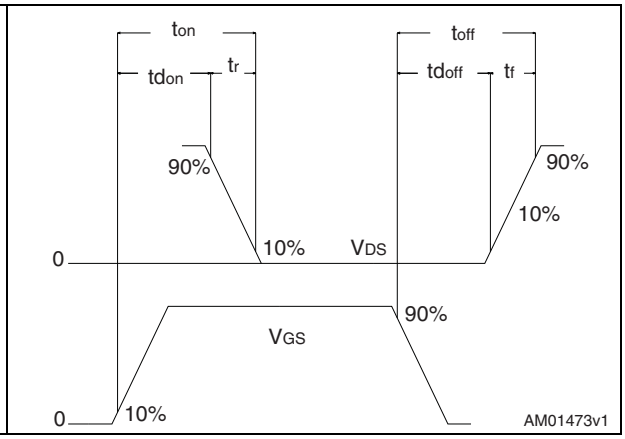


Figure 7. Switching time waveform



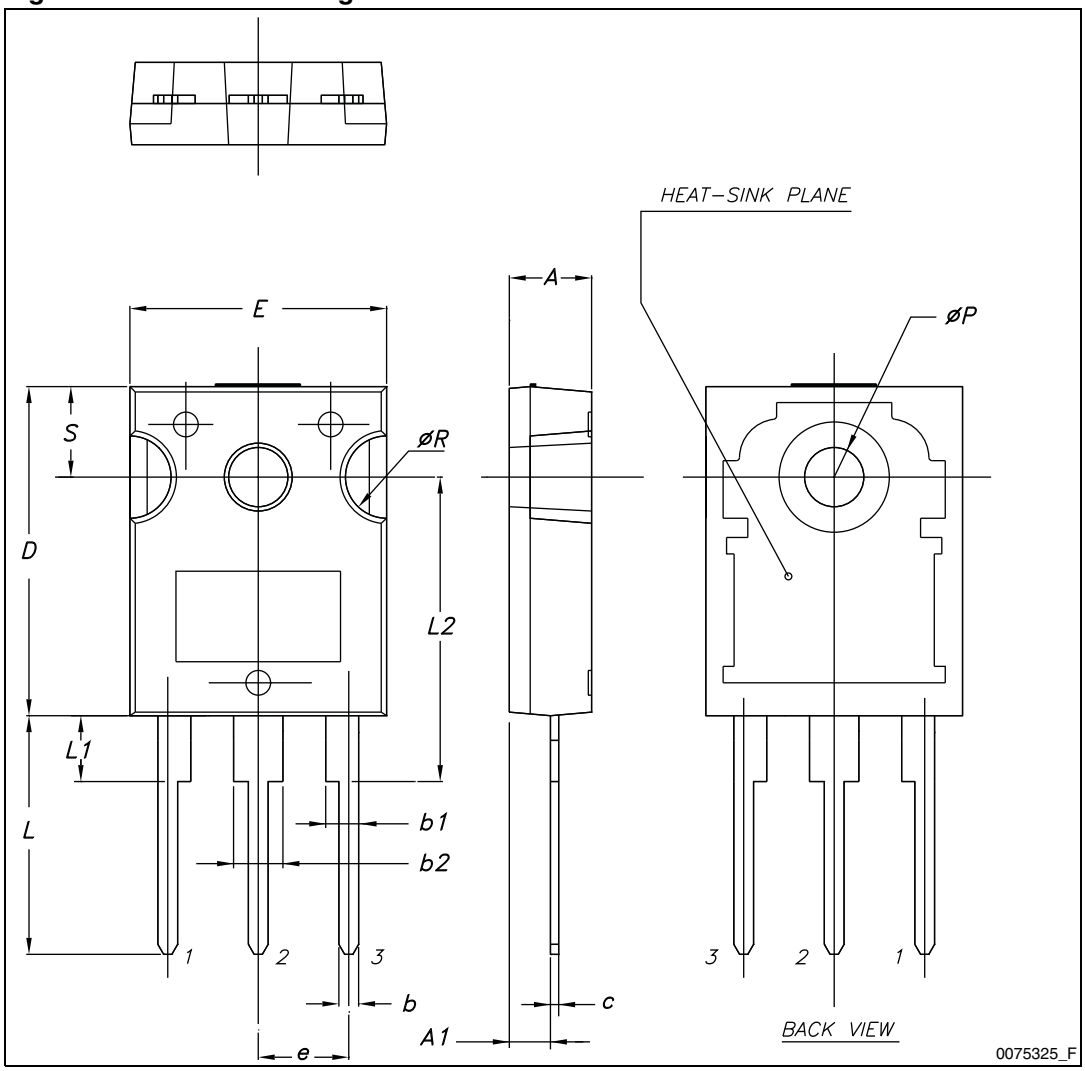
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 8. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Nov-2010	1	First release
18-Jul-2011	2	*Section 4: Package mechanical data* has been updated. Minor text changes.

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