

Automotive-grade N-channel 600 V, 0.052 Ω typ., 50 A MDmesh™ DM2 Power MOSFET in a TO-247 package

Datasheet - production data

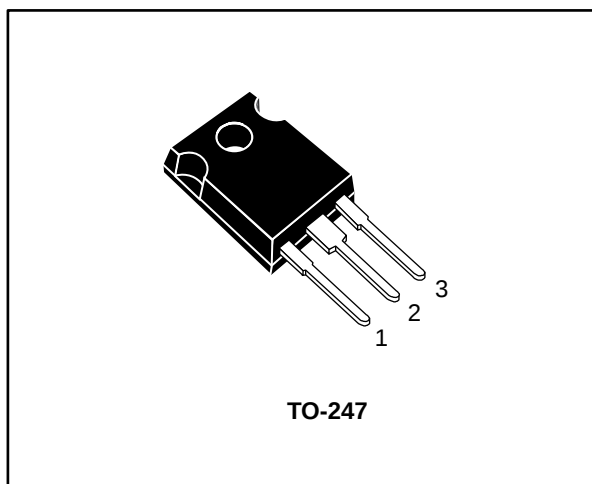
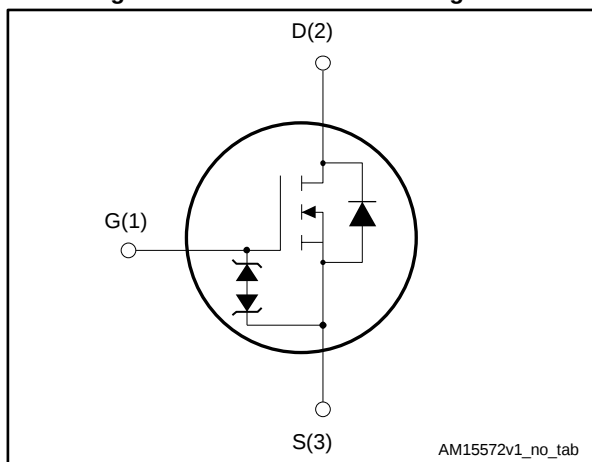


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW58N60DM2AG	600 V	0.060 Ω	50 A	360 W

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STW58N60DM2AG	58N60DM2	TO-247	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	50	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	31	
$I_{DM}^{(1)}$	Drain current (pulsed)	200	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	360	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ $I_{SD} \leq 50\text{ A}$, $di/dt=800\text{ A}/\mu\text{s}$; $V_{DS}\text{ peak} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

⁽³⁾ $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.35	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AS}^{(1)}$	Avalanche current, repetitive or not repetitive	12	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	800	mJ

Notes:

⁽¹⁾ Pulse width limited by T_{jmax} .

⁽²⁾ starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 5	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 25\text{ A}$		0.052	0.060	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	4100	-	pF
C_{OSS}	Output capacitance		-	190	-	
C_{RSS}	Reverse transfer capacitance		-	3.2	-	
$C_{\text{OSS eq.}}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	325	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	4.2	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 50\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Gate charge test circuit")	-	90	-	nC
Q_{gs}	Gate-source charge		-	18	-	
Q_{gd}	Gate-drain charge		-	44	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 25\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$ (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform")	-	24	-	ns
t_{r}	Rise time		-	60	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	130	-	
t_{f}	Fall time		-	12	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		50	A
I_{SDM}	Source-drain current (pulsed)		-		200	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 50\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 50\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.7		μC
I_{RRM}	Reverse recovery current		-	10.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 50\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	245		ns
Q_{rr}	Reverse recovery charge		-	2.6		μC
I_{RRM}	Reverse recovery current		-	21		A

Notes:

⁽¹⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

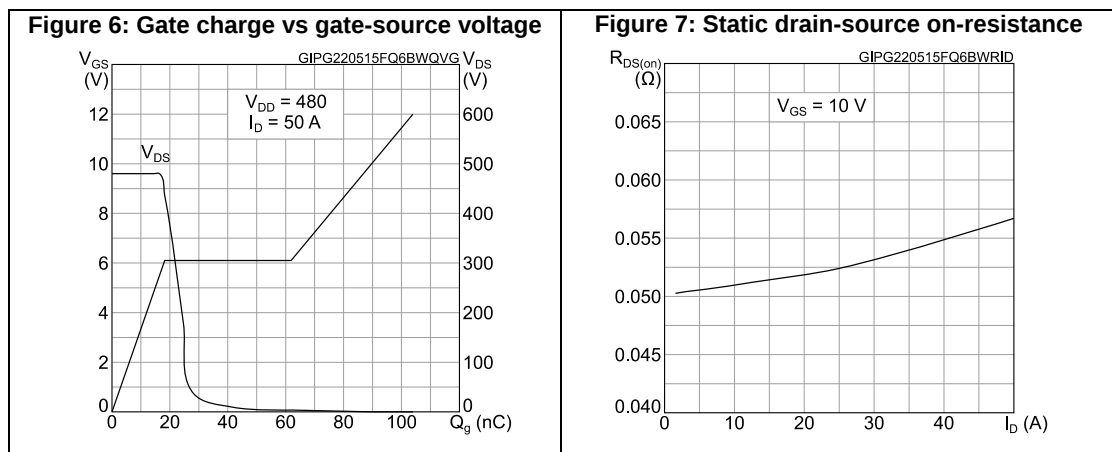
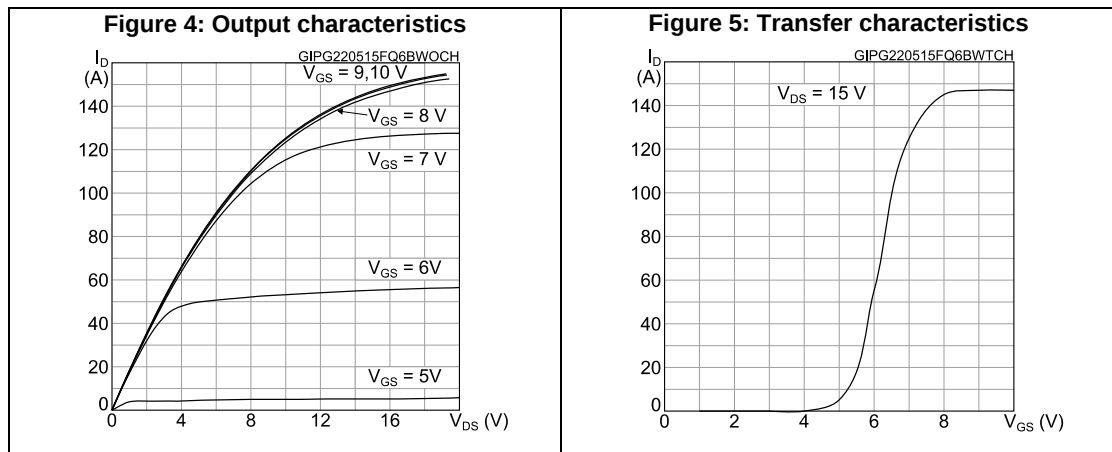
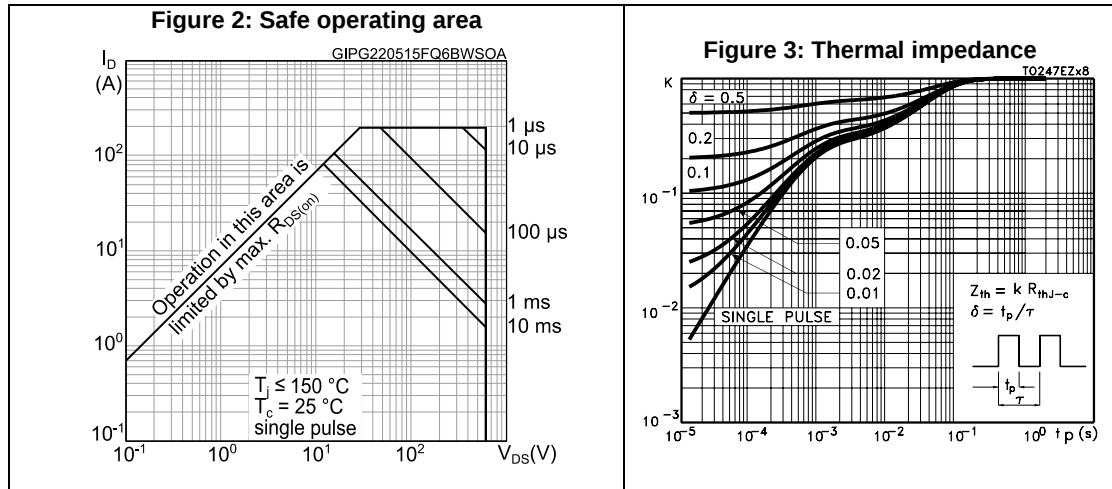


Figure 8: Capacitance variations

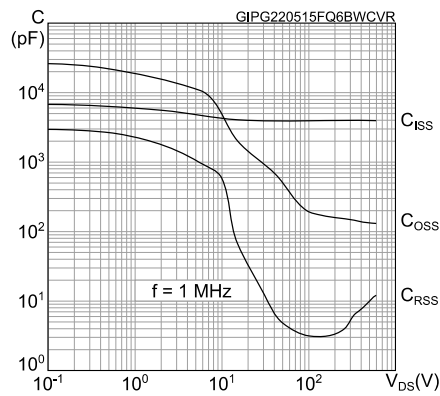


Figure 9: Normalized gate threshold voltage vs temperature

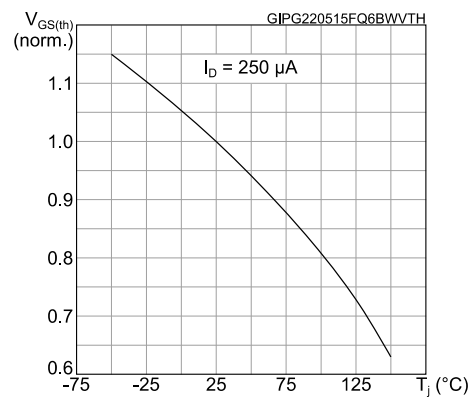


Figure 10: Normalized on-resistance vs temperature

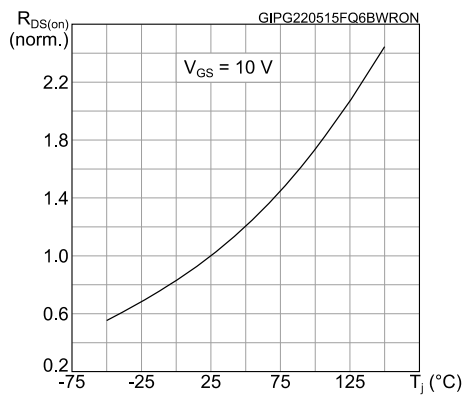


Figure 11: Normalized V(BR)DSS vs temperature

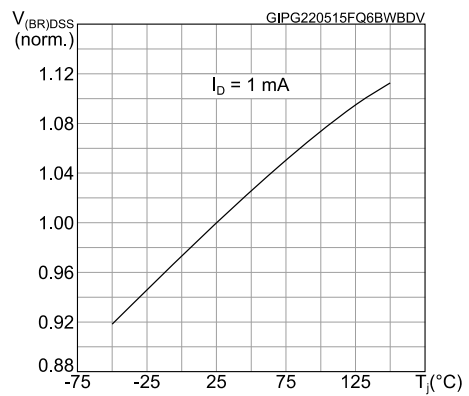


Figure 12: Output capacitance stored energy

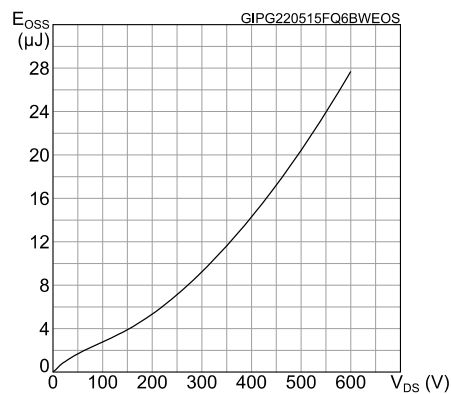


Figure 13: Source-drain diode forward characteristics

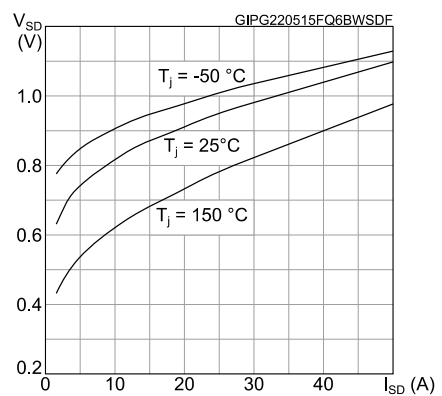


Figure 14: Switching times test circuit for resistive load



The schematic diagram illustrates the experimental setup for characterizing the D.U.T. (Device Under Test). The circuit is powered by a 12V source. A 47kΩ resistor is connected to the gate of the D.U.T. through a 100nF capacitor. A 1kΩ resistor is connected to the drain of the D.U.T. and to the V_{DD} supply. The gate voltage V_i is controlled by a pulse source V_i ≤ V_{GS}. The drain current I_G is constant. The power dissipation P_W is indicated by a pulse waveform. The D.U.T. is connected to a 100Ω resistor, which is in turn connected to a 2.7kΩ resistor and a 47kΩ resistor. The gate of the D.U.T. is also connected to a 2200μF capacitor and a 1kΩ resistor. The drain of the D.U.T. is connected to a 47kΩ resistor and a 1kΩ resistor. The gate voltage V_G is controlled by a pulse source V_i ≤ V_{GS}.

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The diagram shows a circuit for testing a Device Under Test (D.U.T.). An input voltage V_i with a pulse width P_w is applied to the D.U.T. The D.U.T. is represented by a diode symbol. The output of the D.U.T. is connected to a node labeled V_d and I_d . This node is also connected to a resistor L and a $2200 \mu F$ capacitor. The other end of the resistor L and the $2200 \mu F$ capacitor is connected to a $3.3 \mu F$ capacitor, which is then connected to a V_{DD} supply. The D.U.T. is also connected to ground.

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

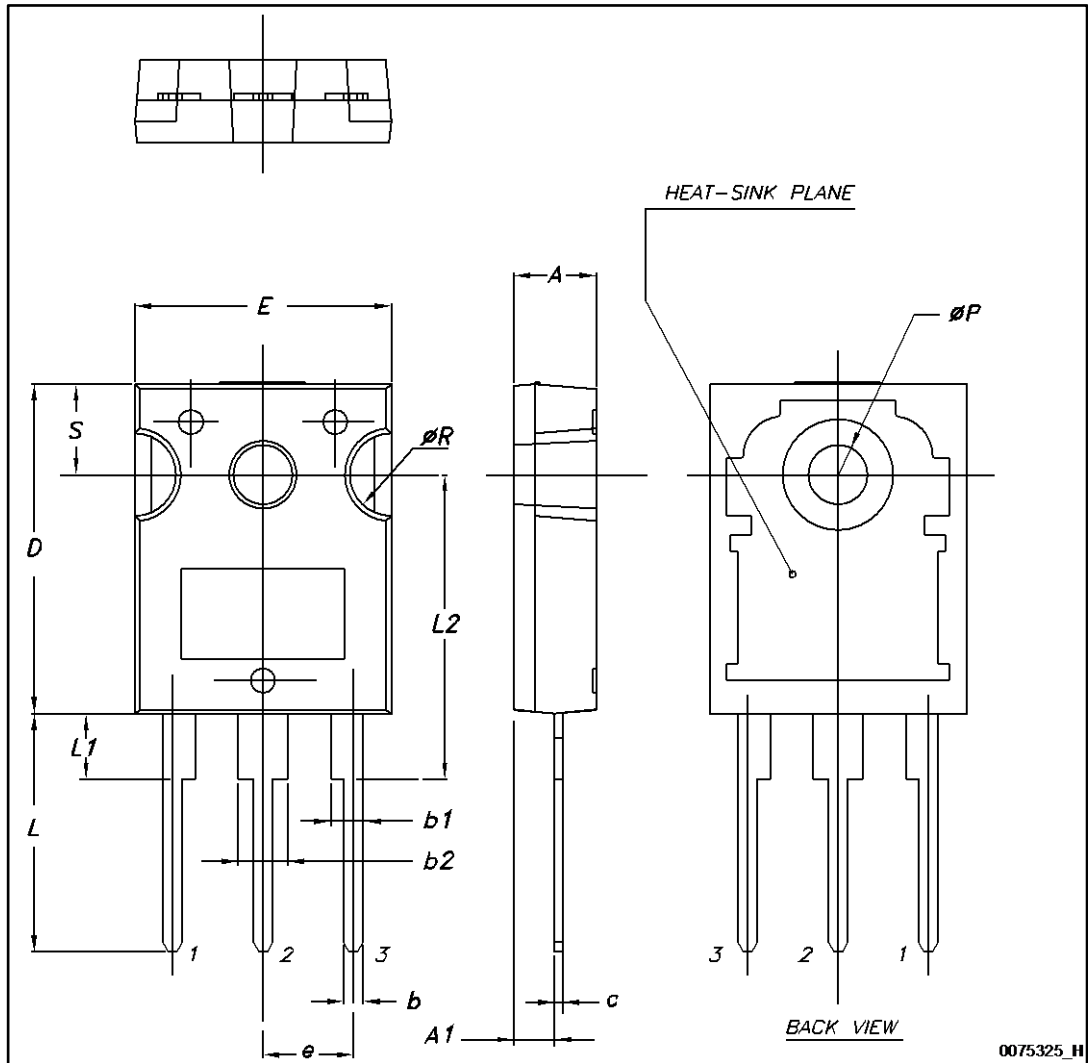


Table 9: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
12-Jun-2015	1	First release.
20-Jul-2015	2	Updated title and features. Minor text changes.

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