



STW80NF55-06

N-CHANNEL 55V - 0.005Ω - 80A TO-247 STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW80NF55-06	55 V	< 0.0065 Ω	80 A

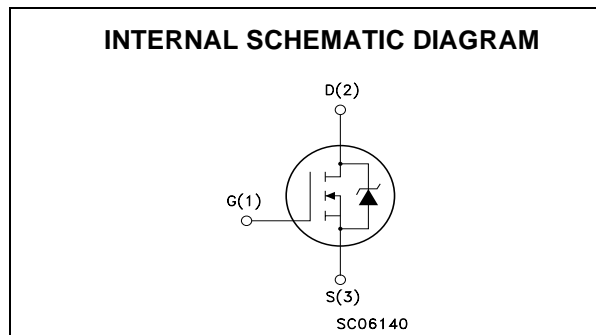
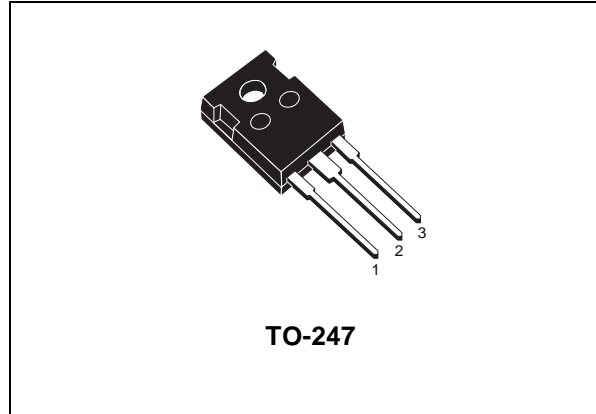
- TYPICAL R_{DS(on)} = 0.005Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC-AC & DC-DC CONVERTERS
- AUTOMOTIVE ENVIRONMENT
- SOLENOID AND RELAY DRIVERS
- MOTOR CONTROL, AUDIO AMPLIFIERS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	55	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	55	V
V _{GS}	Gate- source Voltage	±20	V
I _D (*)	Drain Current (continuous) at T _C = 25°C	80	A
I _D	Drain Current (continuous) at T _C = 100°C	80	A
I _{DM} (●)	Drain Current (pulsed)	320	A
P _{TOT}	Total Dissipation at T _C = 25°C	300	W
	Derating Factor	2	W/°C
E _{AS} (1)	Single Pulse Avalanche Energy	1	J
T _{stg}	Storage Temperature	- 55 to 175	°C
T _j	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area

(1) Starting T_j = 25°C, I_D = 40A, V_{DD} = 40V
(*) Current Limited by wire bonding

STW80NF55-06

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0	55			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10V, I _D = 40 A		0.005	0.0065	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > 15 V, I _D = 40 A		50		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		7300		pF
C _{oss}	Output Capacitance			980		pF
C _{rss}	Reverse Transfer Capacitance			250		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 27.5\text{ V}$, $I_D = 40\text{ A}$		40		ns
t_r	Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		240		ns
Q_g	Total Gate Charge	$V_{DD} = 44\text{ V}$, $I_D = 80\text{ A}$,		190	230	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = 10\text{ V}$		40		nC
Q_{gd}	Gate-Drain Charge			65		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	$V_{DD} = 27.5\text{ V}$, $I_D = 40\text{ A}$,		260		ns
t_f	Fall Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$ (see test circuit, Figure 3)		75		ns
$t_{d(off)}$	Off-voltage Rise Time	$V_{clamp} = 44\text{ V}$, $I_D = 80\text{ A}$		70		ns
$t_{r(Voff)}$	Off-voltage Rise Time	$R_G = 4.7\Omega$, $V_{GS} = 10\text{ V}$		185		ns
t_f	Fall Time	(see test circuit, Figure 5)		240		ns
t_c	Cross-over Time			110		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				80	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				320	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,		90		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 20\text{ V}$, $T_j = 150^\circ\text{C}$		0.295		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		6.5		A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Fig. 1: Unclamped Inductive Load Test Circuit

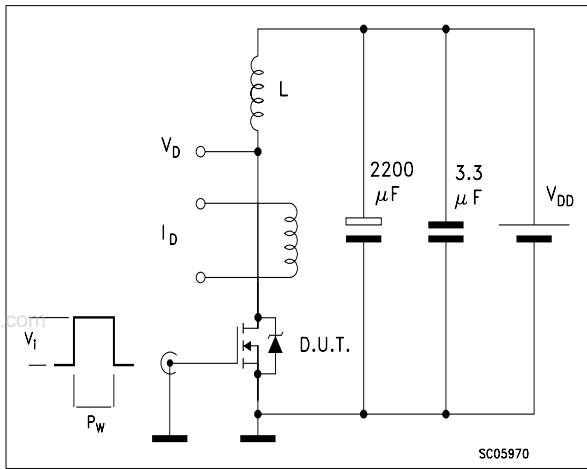


Fig. 2: Unclamped Inductive Waveform

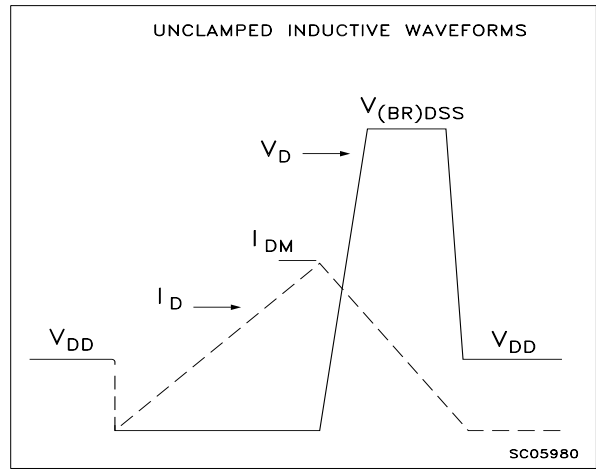


Fig. 3: Switching Times Test Circuit For Resistive Load

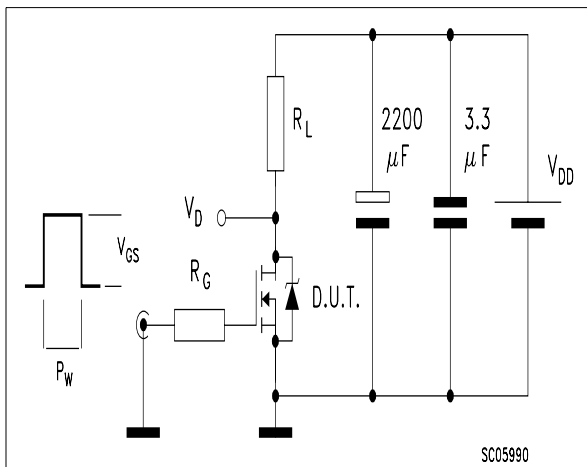


Fig. 4: Gate Charge test Circuit

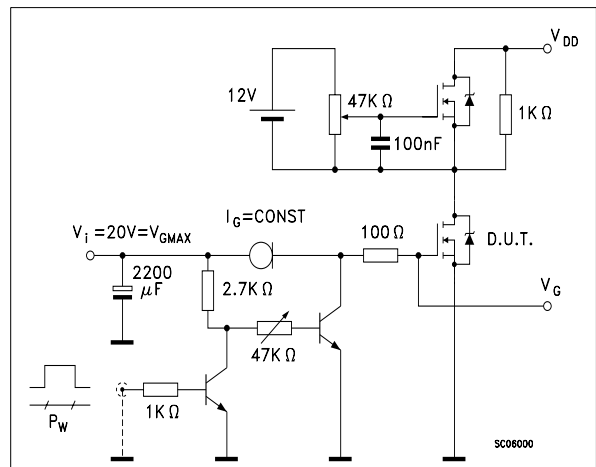
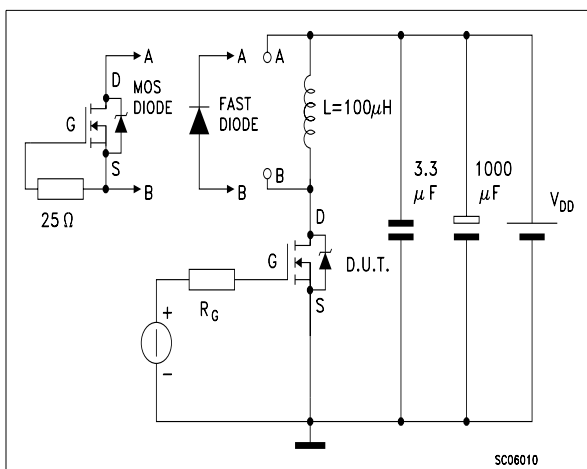
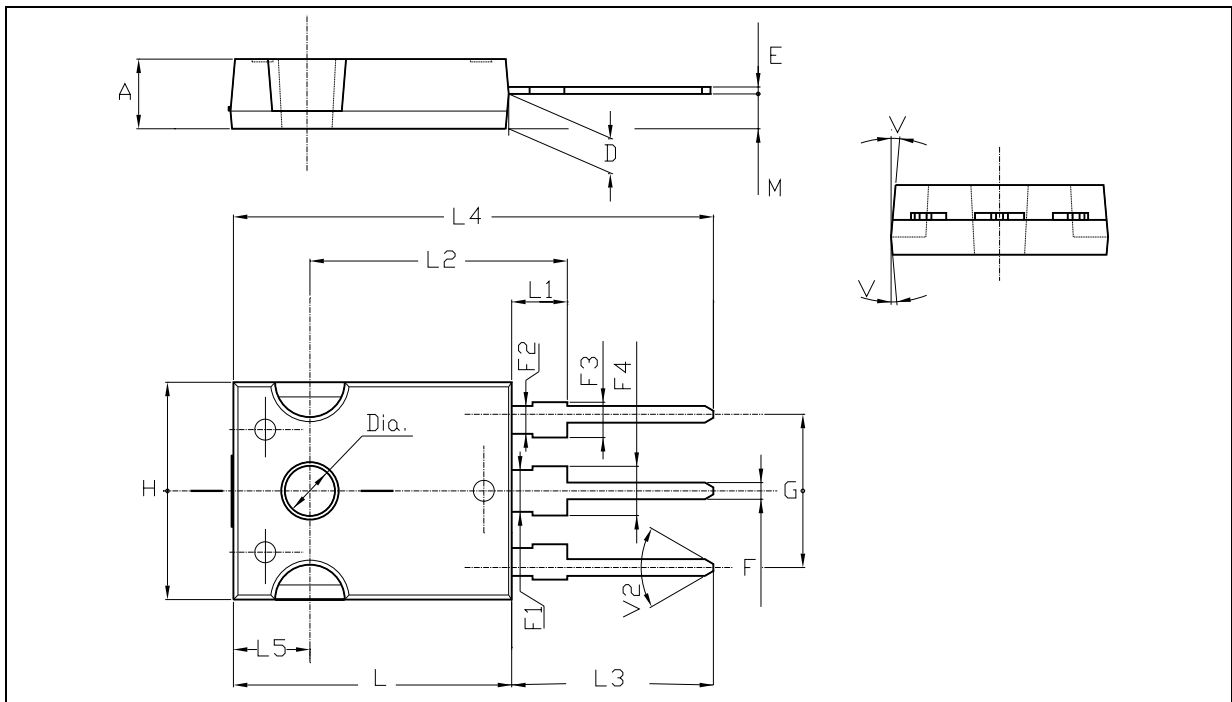


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
D	2.20		2.60	0.08		0.10
E	0.40		0.80	0.015		0.03
F	1		1.40	0.04		0.05
F1		3			0.11	
F2		2			0.07	
F3	2		2.40	0.07		0.09
F4	3		3.40	0.11		0.13
G		10.90			0.43	
H	15.45		15.75	0.60		0.62
L	19.85		20.15	0.78		0.79
L1	3.70		4.30	0.14		0.17
L2		18.50			0.72	
L3	14.20		14.80	0.56		0.58
L4		34.60			1.36	
L5		5.50			0.21	
M	2		3	0.07		0.11
V		5°			5°	
V2		60°			60°	
Dia	3.55		3.65	0.14		0.143



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 2001 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - China - Finland - France - Germany - Hong Kong - India - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - U.S.A.

<http://www.st.com>