



STW8NC90Z

N-CHANNEL 900V - 1.1 Ω - 7.6A TO-247 Zener-Protected PowerMESH™III MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW8NC90Z	900 V	< 1.38 Ω	7.6 A

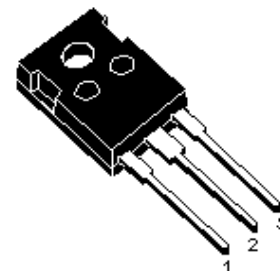
- TYPICAL R_{DS(on)} = 1.1 Ω
- EXTREMELY HIGH dv/dt CAPABILITY GATE-TO-SOURCE ZENER DIODES
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

The third generation of MESH OVERLAY™ Power MOSFETs for very high voltage exhibits unsurpassed on-resistance per unit area while integrating back-to-back Zener diodes between gate and source. Such arrangement gives extra ESD capability with higher ruggedness performance as requested by a large variety of single-switch applications.

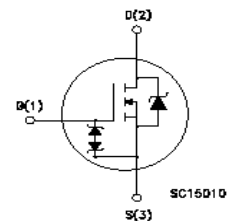
APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT



TO-247

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	900	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 k Ω)	900	V
V _{GS}	Gate- source Voltage	± 25	V
I _D	Drain Current (continuous) at T _C = 25°C	7.6	A
I _D	Drain Current (continuous) at T _C = 100°C	4.8	A
I _{DM} (•)	Drain Current (pulsed)	30	A
P _{TOT}	Total Dissipation at T _C = 25°C	190	W
	Derating Factor	1.51	W/°C
I _{GS}	Gate-source Current (*)	± 50	mA
V _{ESD(G-S)}	Gate source ESD(HBM-C=100pF, R=15K Ω)	4	KV
dv/dt (1)	Peak Diode Recovery voltage slope	3	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(•)Pulse width limited by safe operating area

(1)I_{SD} $\leq$ 7.6A, di/dt $\leq$ 100A/ μ s, V_{DD} $\leq$ V_{(BR)DSS}, T_j $\leq$ T_{JMAX}.

(*)Limited only by maximum temperature allowed

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THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	0.66	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	30	°C/W
Rthc-sink	Thermal Resistance Case-sink Typ	0.1	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	7.6	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	430	mJ

ELECTRICAL CHARACTERISTICS (TCASE = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 µA, V _{GS} = 0	900			V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temp. Coefficient	I _D = 1 mA, V _{GS} = 0		1		V/°C
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating, T _C = 125 °C			1 50	µA µA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±10	µA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 µA	3	4	5	V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V, I _D = 3.8 A		1.1	1.38	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{DS(on)} max, V _{GS} = 10V	7.6			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (1)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{DS(on)} max, I _D = 3.8A		9		S
C _{iss}	Input Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		3550		pF
C _{oss}	Output Capacitance			205		pF
C _{rss}	Reverse Transfer Capacitance			25		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON (RESISTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 450V, I_D = 4A$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		36		ns
t_r	Rise Time			12		ns
Q_g	Total Gate Charge	$V_{DD} = 720V, I_D = 8A,$ $V_{GS} = 10V$		73	102	nC
Q_{gs}	Gate-Source Charge			18		nC
Q_{gd}	Gate-Drain Charge			27		nC

SWITCHING OFF (INDUCTIVE LOAD)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 720V, I_D = 8A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		36		ns
t_f	Fall Time			45		ns
t_c	Cross-over Time			77		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				7.6	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				30	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 7.6A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 8A, di/dt = 100A/\mu s,$ $V_{DD} = 50V, T_j = 150^\circ C$ (see test circuit, Figure 5)		860		ns
Q_{rr}	Reverse Recovery Charge			10		μC
I_{RRM}	Reverse Recovery Current			24		A

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1mA$ (Open Drain)	25			V
α_T	Voltage Thermal Coefficient	$T = 25^\circ C$ Note(3)		1.3		$10^{-4}/^\circ C$
R_z	Dynamic Resistance	$I_{GS} = 50mA$		90		Ω

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

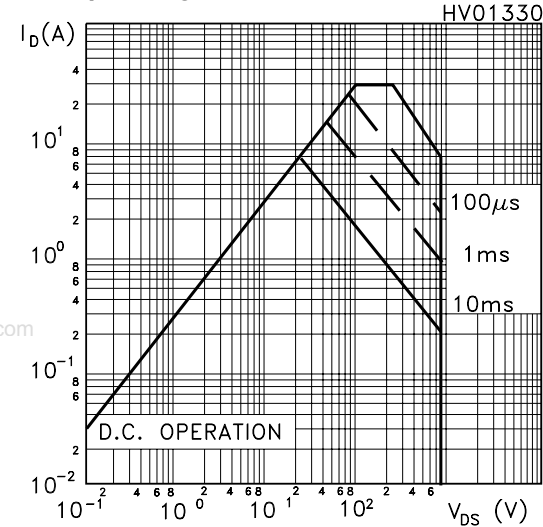
2. Pulse width limited by safe operating area.

3. $\Delta V_{BV} = \alpha_T (25^\circ - T) BV_{GSO}(25^\circ)$

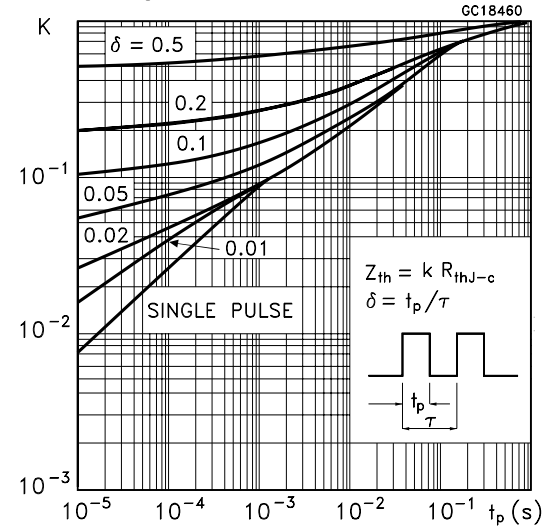
PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the 25V Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

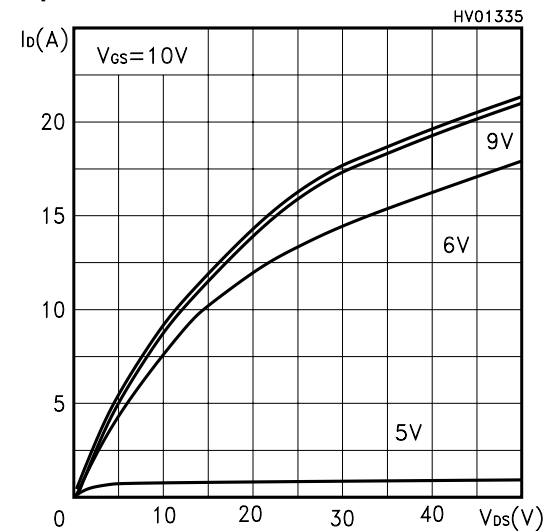
Safe Operating Area



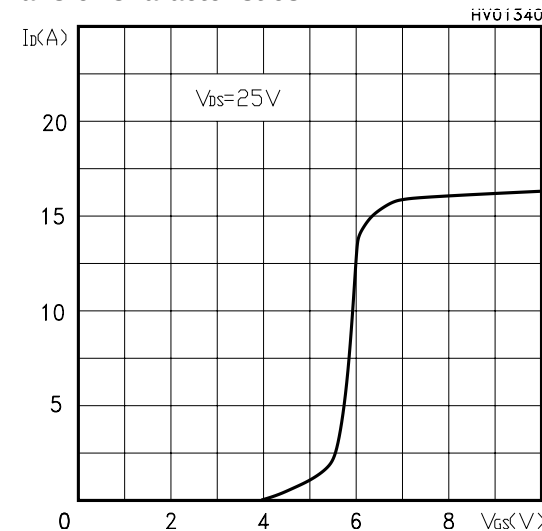
Thermal Impedance



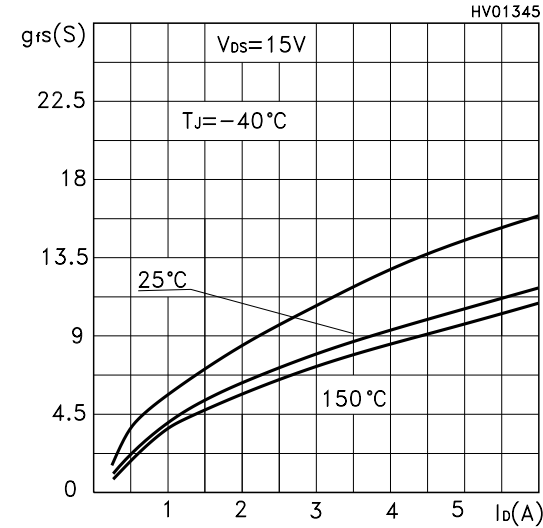
Output Characteristics



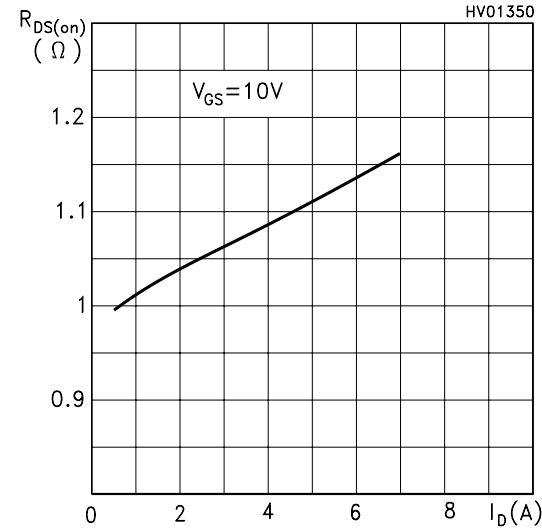
Transfer Characteristics



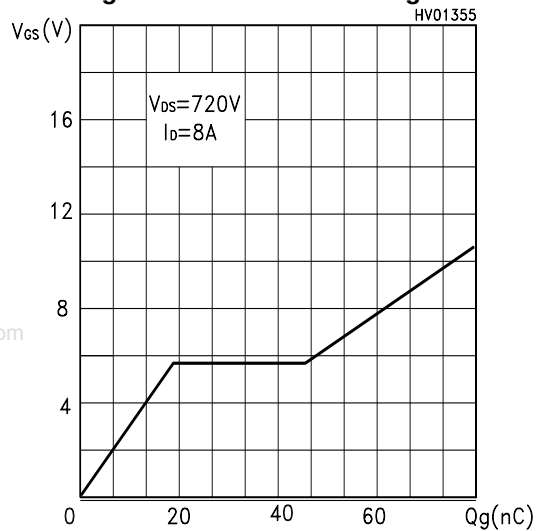
Transconductance



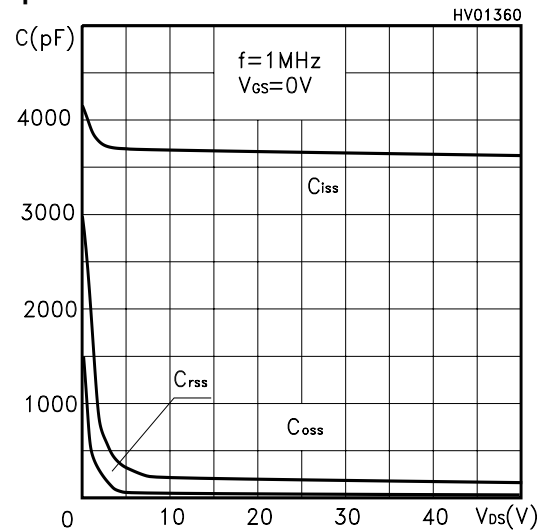
Static Drain-source On Resistance



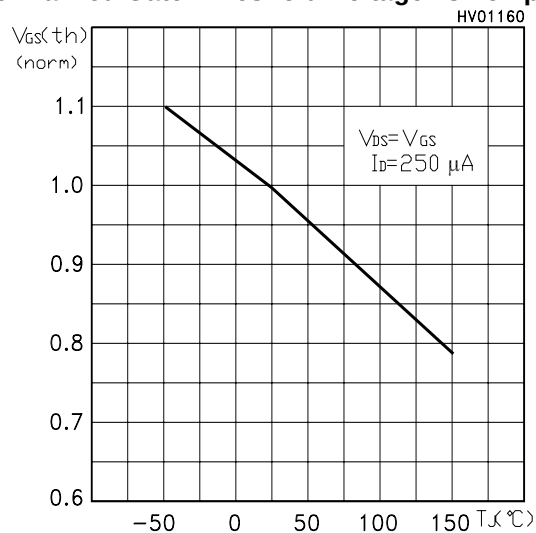
Gate Charge vs Gate-source Voltage



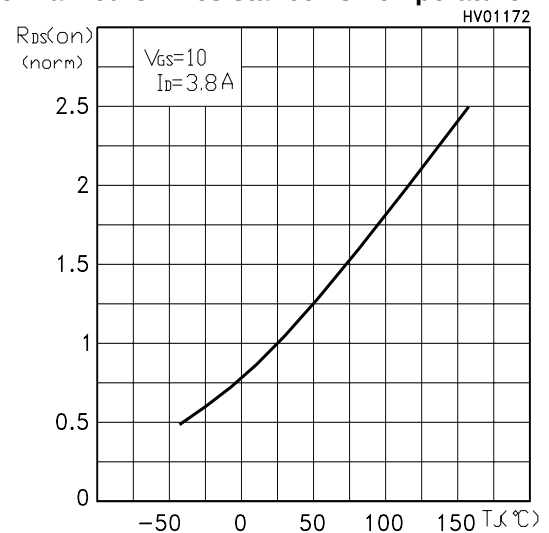
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

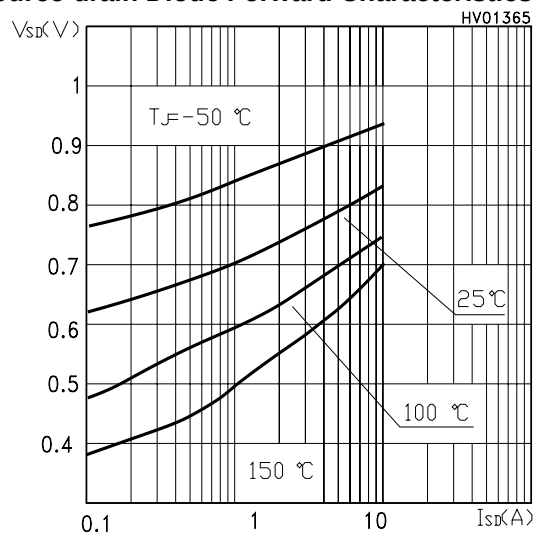


Fig. 1: Unclamped Inductive Load Test Circuit

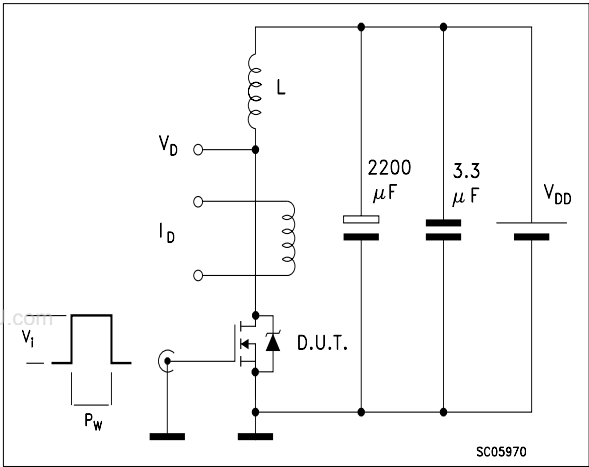


Fig. 2: Unclamped Inductive Waveform

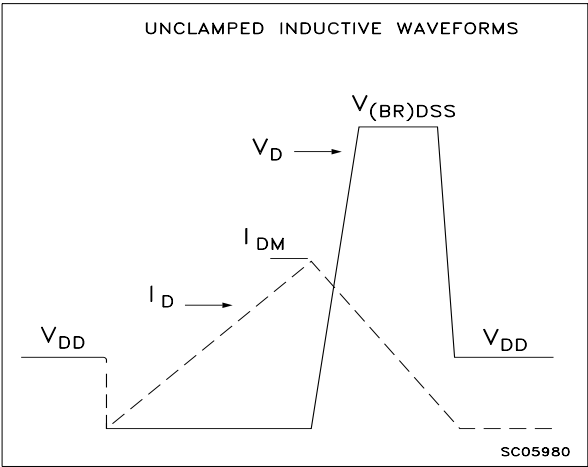


Fig. 3: Switching Times Test Circuits For Resistive Load

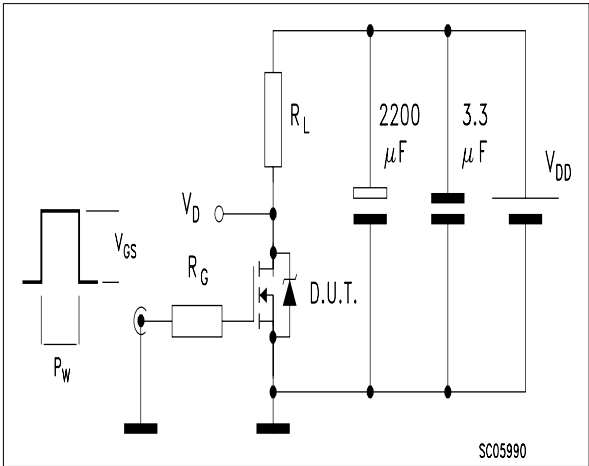


Fig. 4: Gate Charge test Circuit

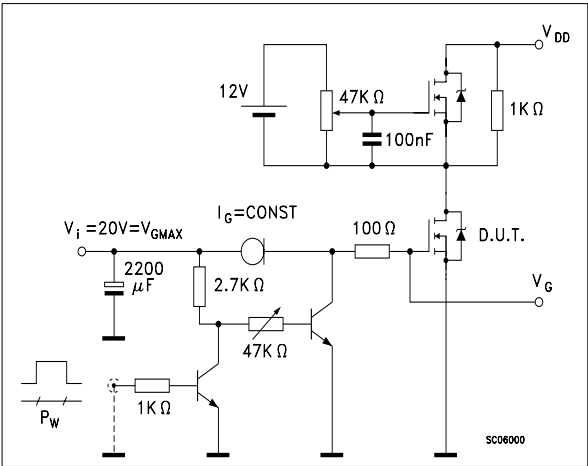
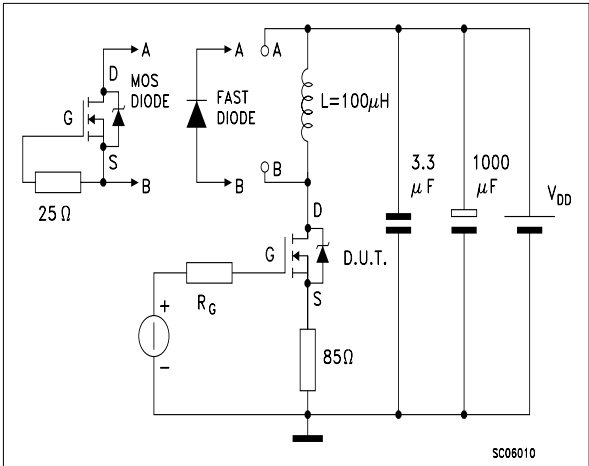
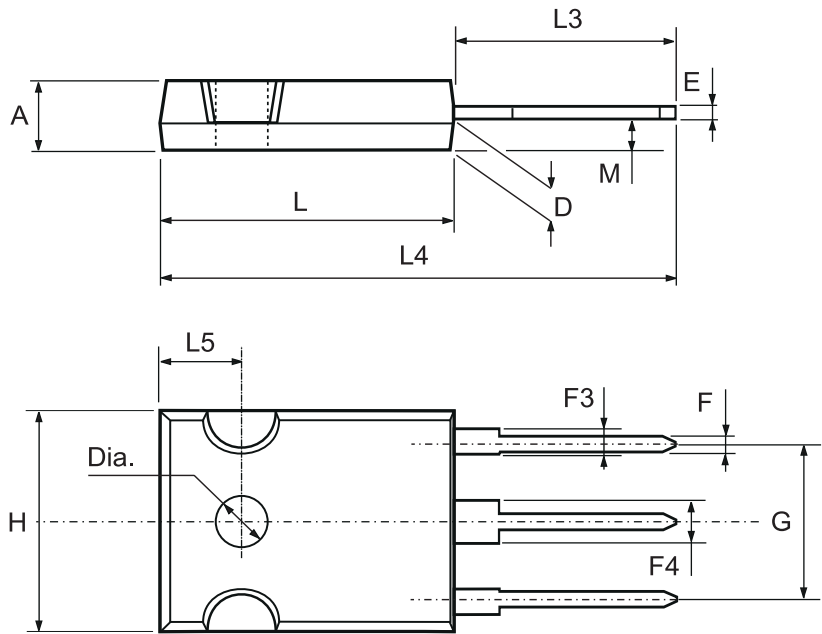


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559		0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118



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