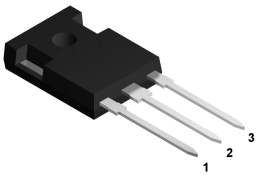
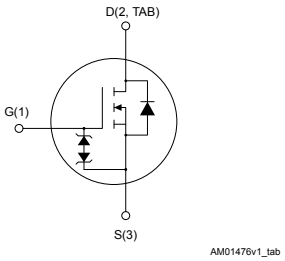
# STWA68N65DM6AG

Datasheet

## Automotive-grade N-channel 650 V, 33 mΩ typ., 72 A MDmesh DM6 Power MOSFET in a TO-247 long leads package




TO-247 long leads




## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STWA68N65DM6AG | 650 V | 39 mΩ | 72 A |

- AEC-Q101 qualified
- Fast-recovery body diode
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

## Applications

- Switching applications

## Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge ($Q_{rr}$), recovery time ($t_{rr}$) and excellent improvement in $R_{DS(on)}$ per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

| Product status link |
|---|
| STWA68N65DM6AG |

| Product summary | |
|---|---|
| **Order code** | STWA68N65DM6AG |
| **Marking** | 68N65DM6AG |
| **Package** | TO-247 long leads |
| **Packing** | Tube |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 72 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 46 | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 280 | A |
| $P_{TOT}$ | Total power dissipation at $T_C$ = 25 °C | 480 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 100 | V/ns |
| di/dt (2) | Peak diode recovery current slope | 1000 | A/µs |
| dv/dt (3) | MOSFET dv/dt ruggedness | 100 | V/ns |
| $T_{STG}$ | Storage temperature range | -55 to 150 | °C |
| $T_J$ | Operating junction temperature range | | °C |

1. *Pulse width limited by safe operating area.*
2. *$I_{SD}$ ≤ 72 A, $V_{DS}$ (peak) < $V_{(BR)DSS}$, $V_{DD}$ = 400 V.*
3. *$V_{DS}$ ≤ 520 V.*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.26 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | 50 | °C/W |

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive ($t_p$ limited by $T_J$ max) | 9 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$) | 1.9 | J |

# 2 Electrical characteristics

$T_C$ = 25 °C unless otherwise specified

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | | 10 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_C$ = 125 °C (1) | | | 300 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±5 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3.25 | 4 | 4.75 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10 V, $I_D$ = 36 A | | 33 | 39 | mΩ |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 5900 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 260 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 2.6 | - | |
| $C_{oss\ eq.}$ (1) | Equivalent output capacitance | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 V | - | 867 | - | |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 1.4 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 72 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 118 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 37 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 48 | - | |

1. *$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 325 V, $I_D$ = 36 A, $R_G$ = 4.7 Ω , $V_{GS}$ = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 34 | - | ns |
| $t_r$ | Rise time | | - | 53 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 92 | - | ns |
| $t_f$ | Fall time | | - | 10 | - | ns |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 72 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 280 | A |
| $V_{SD}$(2) | Forward on voltage | $V_{GS}$ = 0 V, $I_{SD}$ = 72 A | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 72 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 142 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 0.9 | - | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 10.6 | - | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 72 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_J$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 310 | - | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 4.5 | - | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 26 | - | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

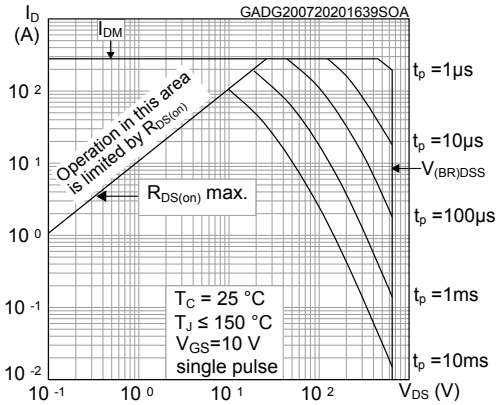



**Figure 2. Maximum transient thermal impedance**

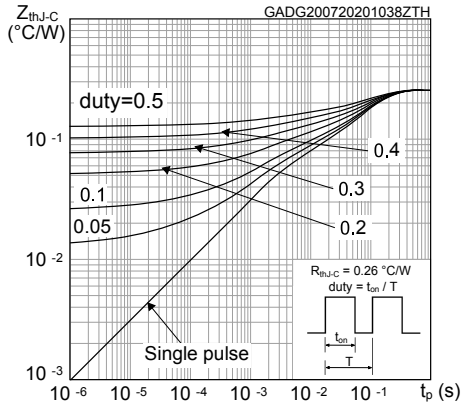



**Figure 3. Typical output characteristics**

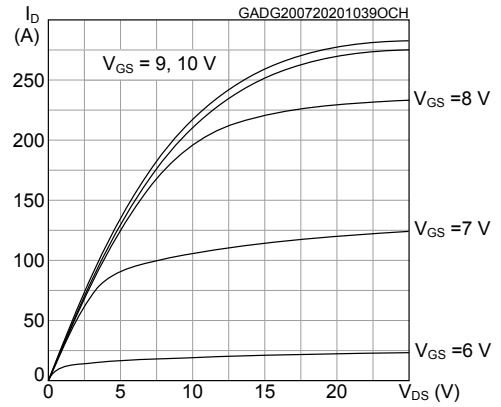



**Figure 4. Typical transfer characteristics**

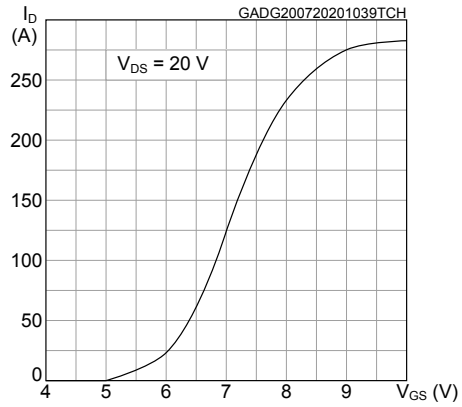



**Figure 5. Typical gate charge characteristics**

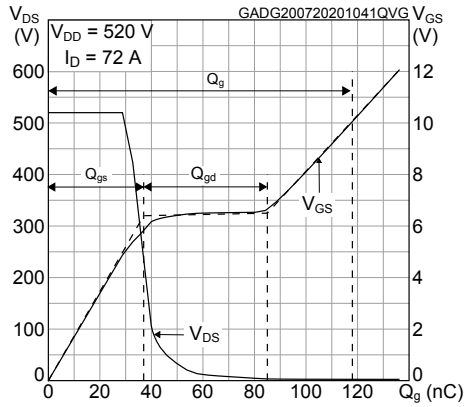



**Figure 6. Typical drain-source on-resistance**

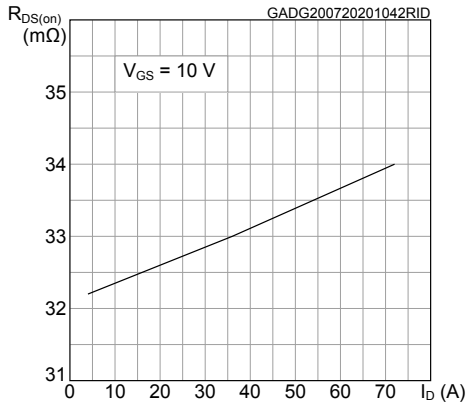


**Figure 7. Typical capacitance characteristics**

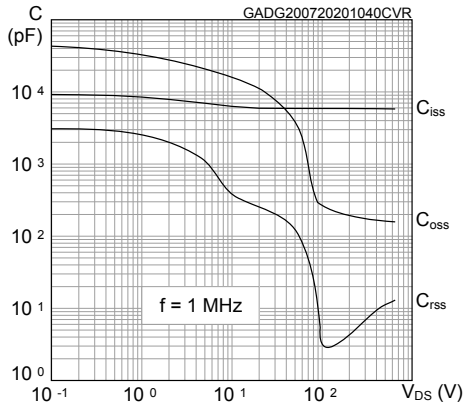



**Figure 8. Typical output capacitance stored energy**

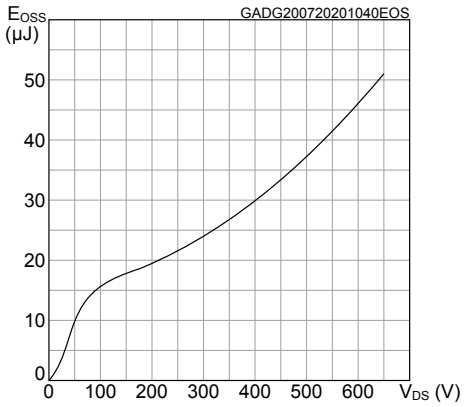



**Figure 9. Normalized gate threshold vs temperature**

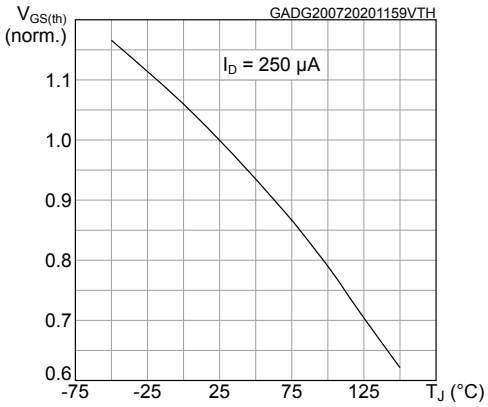



**Figure 10. Normalized on-resistance vs temperature**

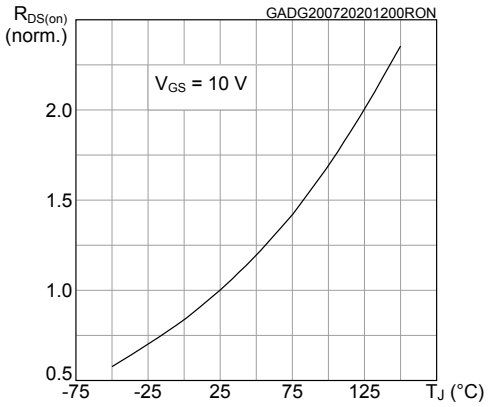



**Figure 11. Normalized breakdown voltage vs temperature**

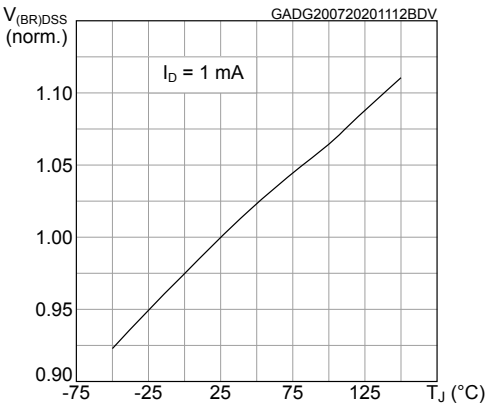
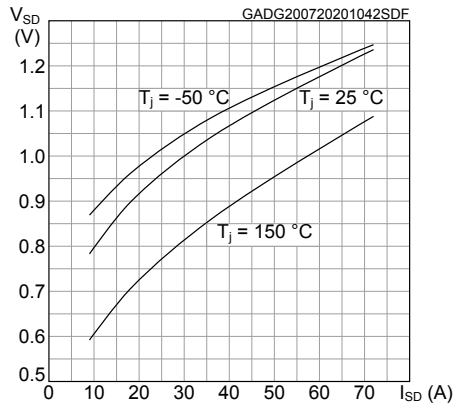



**Figure 12. Typical reverse diode forward characteristics**



# 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**

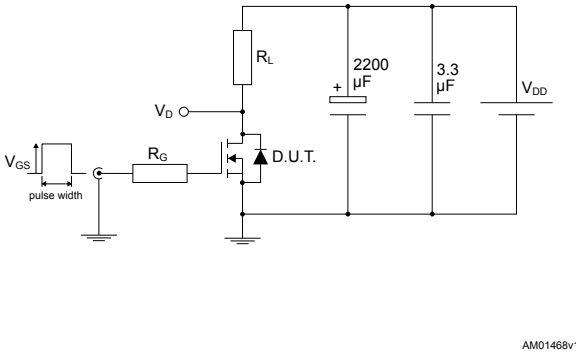



**Figure 14. Test circuit for gate charge behavior**

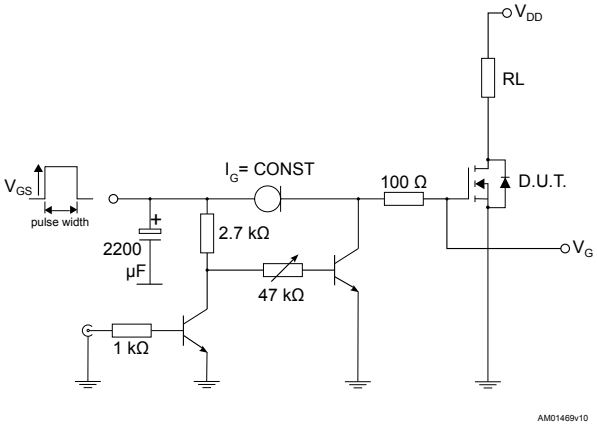



**Figure 15. Test circuit for inductive load switching and diode recovery times**

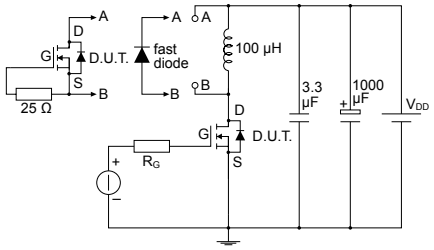



**Figure 16. Unclamped inductive load test circuit**

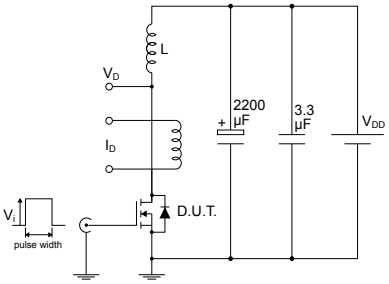



**Figure 17. Unclamped inductive waveform**

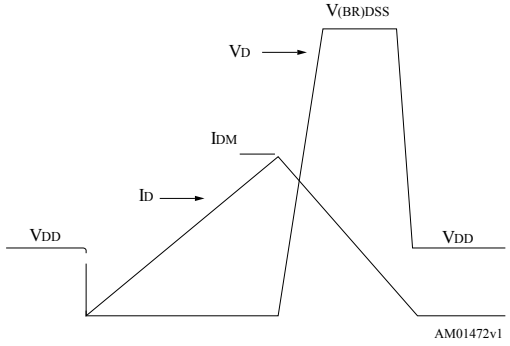
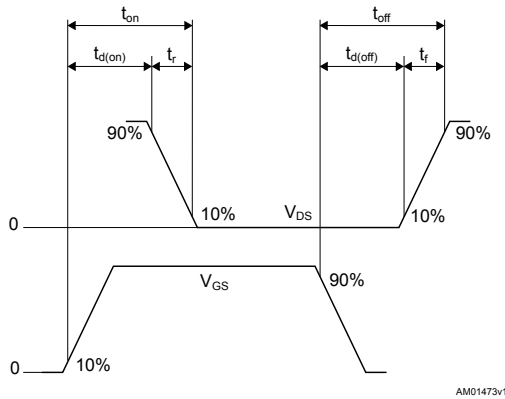



**Figure 18. Switching time waveform**

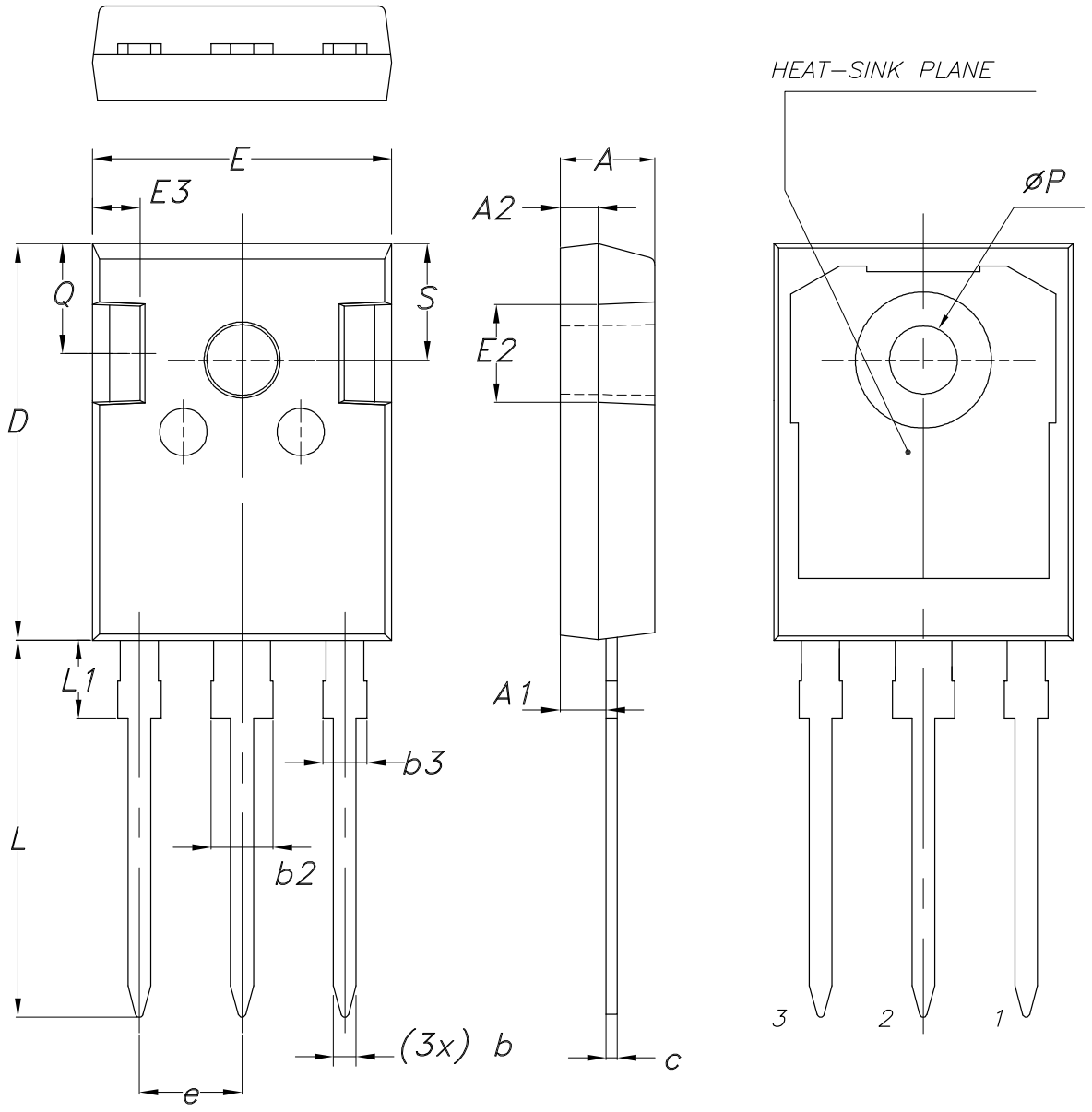


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 4.1 TO-247 long leads package information

**Figure 19. TO-247 long leads package outline**




8463846_2_F

Table 8. **TO-247 long leads package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.90 | 5.00 | 5.10 |
| A1 | 2.31 | 2.41 | 2.51 |
| A2 | 1.90 | 2.00 | 2.10 |
| b | 1.16 | | 1.26 |
| b2 | | | 3.25 |
| b3 | | | 2.25 |
| c | 0.59 | | 0.66 |
| D | 20.90 | 21.00 | 21.10 |
| E | 15.70 | 15.80 | 15.90 |
| E2 | 4.90 | 5.00 | 5.10 |
| E3 | 2.40 | 2.50 | 2.60 |
| e | 5.34 | 5.44 | 5.54 |
| L | 19.80 | 19.92 | 20.10 |
| L1 | | | 4.30 |
| P | 3.50 | 3.60 | 3.70 |
| Q | 5.60 | | 6.00 |
| S | 6.05 | 6.15 | 6.25 |

## Revision history

Table 9. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 27-Jul-2020 | 1 | First release. |

# Contents

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