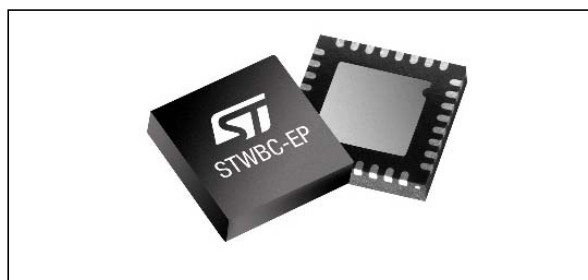# Digital controller for wireless battery chargers transmitters for Qi 15 W applications

Datasheet - production data

Features

- Digital controller for wireless battery charger transmitter
- 15 W single coil inductive transmitters optimized for:
  - Cell phones and smartphones
  - Tablets and phablets
  - Charging accessories
- Support for Wireless Power Consortium (WPC) 1.2 EPP 15 W certified applications
  - Backward compatible with 5 W WPC 1.1 applications
- Support for half bridge topology with DC/DC
- VIN range: 3 V to 5.5 V
  - Supports USB Vin
- Active presence detector
- Foreign object detection
- Q-factor measurement
- Parametric customization via GUI
- Turnkey firmware solution
- Peripherals
  - 10-bit ADC
  - UART interface
  - I^2C master fast/slow speed rate
  - GPIOs

- Memory
  - Flash and EEPROM with read-while-write (RWW) and Error Correction Code (ECC)
  - Program memory: 32-Kbyte Flash; data retention: 20 years at 55 °C after 1000 cycles at 55 °C
  - Data memory: 1 Kbyte true data EEPROM; data retention: 20 years at 55 °C after 1000 cycles at 85 °C
  - RAM: 6 Kbytes
- Transmitter reference design:
  - WPC Qi 1.2.3 certified
  - MP-A10 single coil 15 W topology
  - Evaluation board order code: STEVAL-ISB044V1
  - 2-layer PCBs
  - Active object detection
  - Graphical User Interface for application monitoring
- Operating temperature: -40 °C up to 105 °C
- Package: VFQFPN32 - 5 x 5mm

Table 1. Device summary

Order code	Type
STWBC-EP	VFQFPN32 , tube
STWBC-EPTR	VFQFPN32 tape and reel

Contents

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1   Description

The STWBC-EP is the digital controller for the wireless battery charger (WBC) transmitters (TX) from STMicroelectronics optimized for Extended Power Profile (EPP) Wireless Power Consortium (WPC) 1.2 certified applications up to 15 W.

It offers the most flexible and efficient solution for controlling the power transfer to a receiver (RX) in WBC-enabled applications such as smartphones, tablets and other battery-powered devices that use the electromagnetic induction for recharging.

The TX is responsible for controlling the transmitting coil and generating the correct amount of power requested by the RX. The RX continuously provides the transmitter with the correct power level requested, by modulating the transmitter carrier through the controlled resistive or capacitive load. Generating the correct amount of power ensures the highest level of end-to-end efficiency due to reduced energy losses. It also helps maintaining a lower operational temperature.

The TX can adapt to the amount of energy transferred by the coil by modulating the frequency, duty cycle or amplitude of the PWM voltage on the transmitting coil.

The STWBC-EP is capable of bidirectional communication with the RX as specified by the WPC 1.2 protocol.

Figure 1. Wireless charging system description
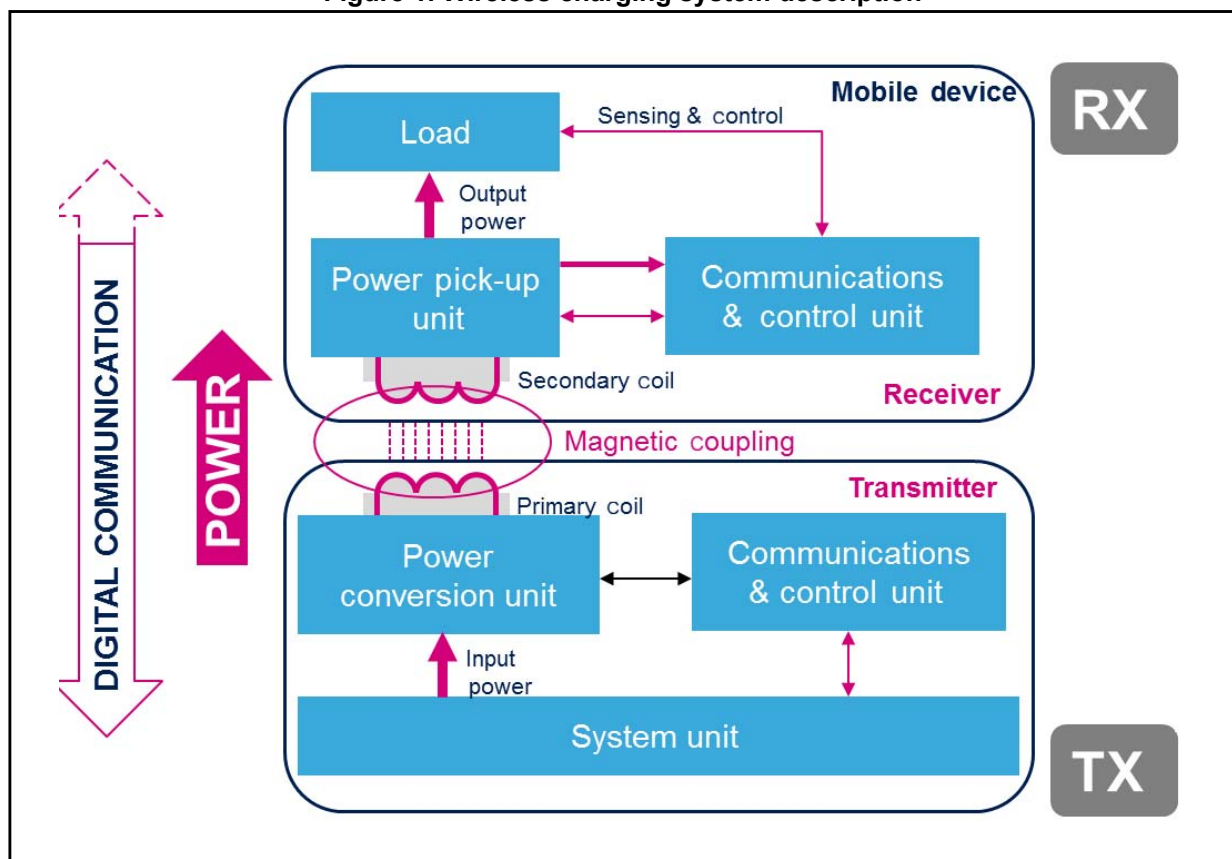
The STWBC-EP firmware is specifically designed to take advantage of the hardware to monitor and control the correct wireless charging operations.

2   STWBC-EP system architecture

Figure 2 illustrates the overall system blocks implemented in the STWBC-EP architecture.

The STWBC-EP is a flexible controller that supports a half bridge coil driver together with a DC/DC controller, which regulates the input voltage of the bridge in order to control the amount of the power transmitter to the receiver.

The digital controller also regulates the half bridge operating frequency and duty cycle to further adjust the amount of power increasing the overall efficiency at the light load.

It implements the WPC 1.2 protocol, including foreign object detection (FOD) extensions. An accurate Q-factor measurement provides enhanced FOD.

The STWBC-EP is able to manage both WPC Baseline Power Profile (up to 5 W) and Extended Power Profile (EPP).

Figure 2. STWBC-EP device architecture
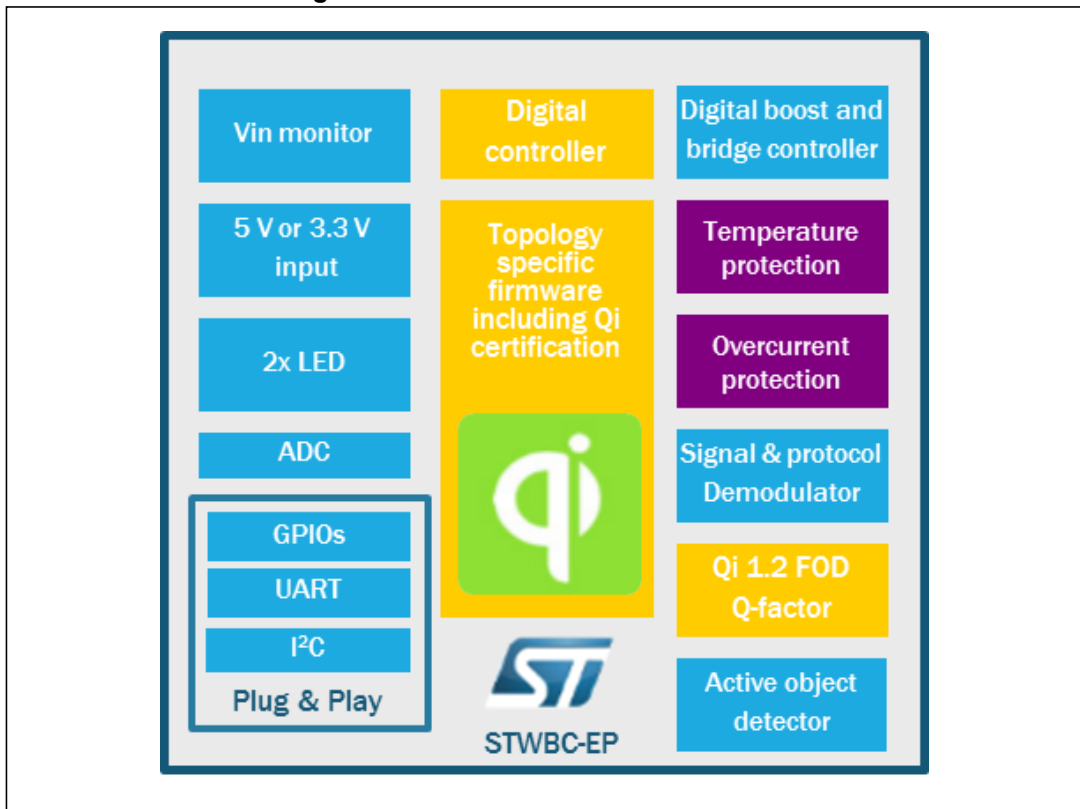
Firmware

The STWBC-EP firmware is available in a turnkey software package distributed as a binary file.

The STWBC-EP provides UART communication interface, for external programming of parameters and STWBC-EP control.

3 Reference design

The STWBC-EP is available with the STEVAL-ISB044V1 reference design. The certification and interoperability tests are based on the Qi standard version 1.2.3 and supports FOD extensions.

The STEVAL-ISB044V1 reference design provides a complete kit which includes the STWBC-EP IC, firmware, layout, graphical interfaces and tools. The layout is based on a cost-effective 2-layer PCB.

Figure 3. STEVAL-ISB044V1 evaluation board

4   STWBC-EP pinout and pin description

This section shows the pinout used by the STWBC-EP.

Figure 4. STWBC-EP configuration
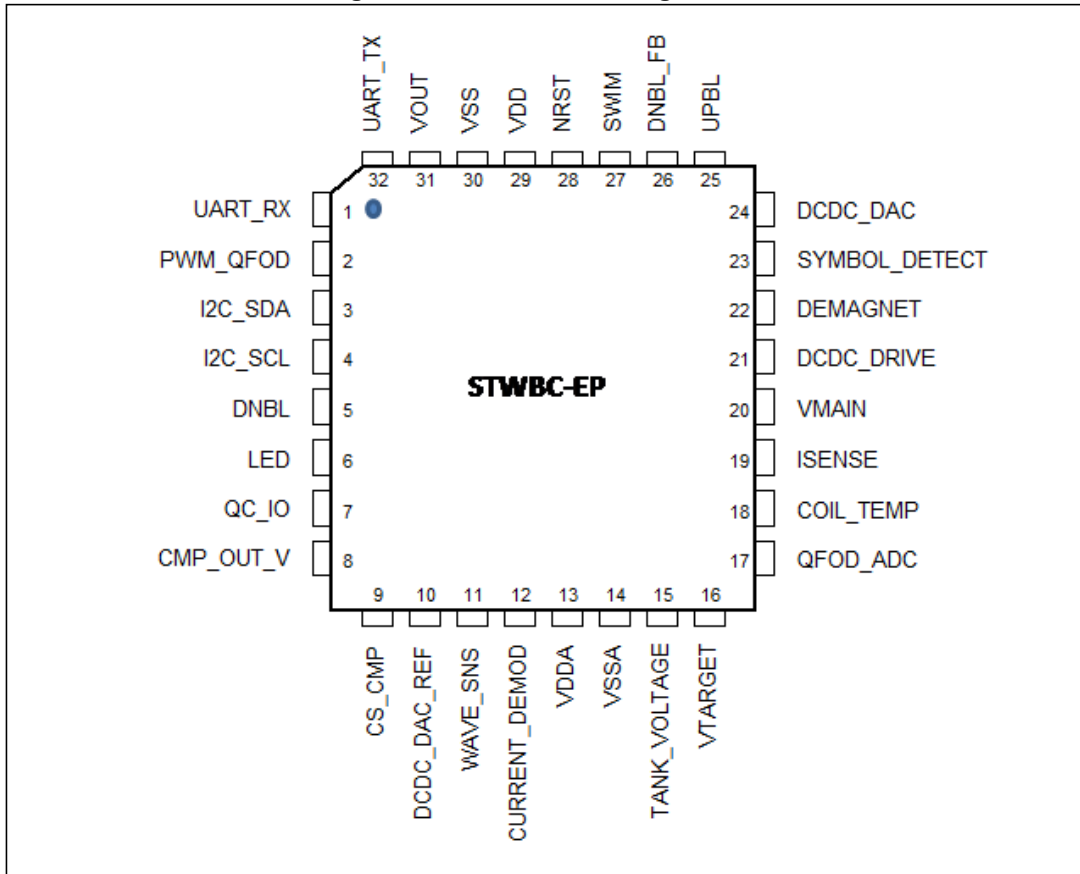
Table 2. Pinout description

Pin number	Pin name	Pin type	Description
1	UART_RX	DI	UART RX link on USB debug connector
2	PWM_QFOD	DO	PWM dedicated to QFOD circuit
3	I2C_SDA	DI	I2C_SDA
4	I2C_SCL	DI	I2C_SCL
5	DNBL	DO	Output signal for HB low-side driver
6	LED	DO	Digital output for green and red LEDs indicators
7	QC_IO	DO	Quick Charge™ circuit signal
8	CMP_OUT_V	AI	Boost output voltage sensing
9	CS_CMP	AI	Boost current sensing
10	DCDC_DAC_REF	AI	DAC reference value for boost output voltage

Table 2. Pinout description (continued)

Pin number	Pin name	Pin type	Description
11	WAVE_SNS	AI	Symbol detector based on delta frequency
12	CURRENT_DEMOD	AI	Current demodulation
13	VDDA	PS	Analog power supply
14	VSSA	PS	Analog ground
15	TANK_VOLTAGE	AI	Analog input to measure the LC voltage (power calculation)
16	VTARGET	AI	Boost voltage measurement
17	QFOD_ADC	AI	High sensitivity peak voltage detector used for quality factor measurement
18	COIL_TEMP	AI	Analog input for temperature measurement. The input is connected to external NTC biased to the VDD_STWBC
19	ISENSE	AI	Analog input to measure the current flowing into the power bridge
20	VMAIN	AI	Analog input to measure the main power supply
21	DCDC_DRV	DO	DCDC Boost PWM drive
22	DEMAGNET	DI	Transformer demagnetization sensing
23	SYMBOL_DETECT	DI	Voltage demodulation
24	DCDC_DAC	DO	Boost PWM output DAC (setting the CPP3 comparator voltage reference)
25	UPBL	DO	Output signal for HB high-side driver
26	DNBL_FB	DI	Hardware PWM feedback
27	SWIM	DIO	Digital I/O for Debug interface
28	NRST	DI	Reset input monitoring
29	VDD	PS	Digital and I/O power supply
30	VSS	PS	Digital and I/O ground
31	VOUT	Supply	Internal LDO output
32	UART_TX	DO	UART TX link on USB debug connector

Note: *The operative voltage of analog inputs (AI) ranges from 0 V to 1.2 V.*

5 Pins functional description

This section describes the functions related to the pins of the device.

5.1 Power supplies: VDD, VDDA, VSS, VSSA, VOUT

The digital portion of the STWBC-EP is powered using VDD and VSS (typically 4.5 V).

The analog portion of the STWBC-EP is powered using VDDA and VSSA (typically 4.5 V).

VDD and VDDA should be correctly filtered to allow the correct operation of the device.

The STWBC-EP generates its own internal power supply which needs a filter capacitor of 1 μF on the VOUT pin.

5.2 DC/DC converter: DCDC_DRV, DCDC_DAC, CMP_OUT_V, CS_CMP, DCDC_DAC_REF, DEMAGNET, VTARGET

The STWBC-EP is designed to drive a DC/DC boost converter placed in front of the half bridge coil driver. The DC/DC power switch (external NMOS) is driven by the DCDC_DRV pin through an output buffer.

The DC/DC inductor charging current is monitored using a sense resistor. The sense resistor has to be connected to the CS_CMP pin so that the STWBC-EP can detect the current flowing into the inductor.

The DC/DC converter loop compares a reference target voltage applied on the DCDC_DAC_REF pin with the feedback voltage connected to the CMP_OUT_V pin. The CMP_OUT_V signal is a partition of the DC/DC output voltage.

The DCDC_DAC_REF reference voltage is variable in order to adjust the DC/DC output voltage depending on wireless power solution requirements. The DCDC_DAC_REF is generated by filtering the PWM signal present on the DCDC_DAC pin. A second order passive filter is required.

The DC/DC output voltage is monitored by the STWBC-EP using the VTARGET pin. The VTARGET should be generated as a partition of the DCDC output voltage.

In order to enhance the efficiency at the medium and low load, the DC/DC converter can operate in the quasi-resonant mode. To do so, the STWBC-EP monitors the demagnetization of the inductor using the DEMAGNET pin.

5.3 Half bridge driver: UPBL, DNBL, PWM_QFOD, WAVE_SNS

The power half bridge is driven using the UPBL and DNBL pins. The UPBL pin has to be connected to a high-side gate driver, while the DNBL pin has to be connected to a low-side gate driver for the power switches.

The UPBL and DNBL pins are active-high: when 1, the corresponding power switch has to be ON.

The STWBC-EP integrates programmable dead time between the active states of the UPBL and DNBL avoiding simultaneous conduction of power switches. The external gate driver doesn't need to manage dead time.

The STWBC-EP requires the following capability to be supported by the gate driver:

- UPBL = 0, DNBL = 0: in such case, the power half bridge must be in the high impedance state.
- UPBL = 1, DNBL = 0: high-side power switch must be ON.
- UPBL = 0, DNBL = 1: low-side power switch must be ON.
- UPBL = 1, DNBL = 1: optional mode where both high and low-side power switches must be ON (simultaneous conduction).

While the power half bridge is driven with UPBL and DNBL signals, a low energy drive is needed to run the coil quality factor estimation. For this function, the bridge is driven by using the PWM_QFOD pin instead of the UPBL (UPBL is 0 during this operation). The PWM_QFOD has to be connected to the low energy high-side switch while the DNBL is still used for the low-side low impedance switch drive.

In many situation the STWBC-EP requires ¼ wave synchronization with the LC tank connected to the half bridge. A simple passive detector must be connected to the LC tank and the WAVE_SNS pin. The WAVE_SNS pin should be limited to a ± 0.6 V swing.

5.4 Wireless power functions: TANK_VOLTAGE, ISENSE, COIL_TEMP, SYMBOL_DETECT, CURRENT_DEMOD, CS_CMP_AVG

The STWBC-EP requires monitoring the peak voltage on the LC tank as well as the rectified current circulating in the tank. To do so, a peak voltage detector of the LC tank must be connected to the TANK_VOLTAGE pin and a filtered current sensor must be connected to the ISENSE pin .

For quality factor measurement, a high sensitivity peak voltage detector of the LC tank must be connected to the CS_CMP_AVG pin.

The STWBC-EP requires external signal conditioning blocks to pre-demodulate the WPC Qi messages. One of this blocks detects the effect of modulation on the LC tank voltage and it must be connected to the SYMBOL_DETECT pin. Another block is required to detect the effect of modulation on the LC tank current and it must be connected to the CURRENT_DEMOD pin.

For safety reason the STWBC is capable of monitoring the temperature of the transmitting coil. In order to do so, a NTC thermistor must be connected to the COIL_TEMP pin.

5.5 Input power supply management: VMAIN, QC_IO

The STWBC-EP monitors the input power supply voltage using the VMAIN pin. This voltage is used for optimum programming of the DC-DC converter but also for the wireless power mode of the operation.

The STWBC-EP is capable of requesting 12 V output voltage available from some USB wall adaptors. While the USB wall adaptor provides 5 V by default, using a specific signaling on the D+ and D- signals of the USB interface, 12 V can be obtained if supported. When 12 V is available, the STWBC-EP can provide up to 15 W to a receiver load. The QC_IO pin has to be connected to a simple interfacing circuit with the USB connector. When QC_IO is 0, 5 V is requested to the USB wall adaptor. When QC_IO is 1, 12 V is requested to the USB wall adaptor.

5.6 External digital interface: UART_TX, UART_RX

The STWBC-EP can be programmed and/or controlled using a 57600 bps 8-bit 1start 1stop no-parity UART interface. The STWBC-EP UART TX output is present on the UART_TX pin and the UART RX input is present on the UART_RX pin.

5.7 End user signaling: LED

The STWBC-EP manages 2 LEDs (red and green typically) using a single LED pin. The pin is the output 0 to drive the first LED, the output 1 to drive the second LED and high impedance to not drive any LED. A simple circuit can be used to interface the LEDs with this LED pin.

5.8 Expansion interface: I2C_SDA, I2C_SCL

The STWBC-EP embeds an I²C master interface on the I2C_SDA and I2C_SCL pins. This interface is typically inactive and reserved for future use.

5.9 Debug: SWIM, NRST

The SWIM pin may be used to interface with the STLINK/V2 debugger. The STWBC-EP can be reset using the active-low NRST pin.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referred to VSS. VDDA and VDD must be connected to the same voltage value. VSS and VSSA must be connected to together with the shortest wire loop.

6.2 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with the ambient temperature at T_A = 25 °C and T_A = T_A max. (given by the selected temperature range).

6.3 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} and V_{DDA} = 5 V. They are given only as design guidelines and are not tested. Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range.

6.4 Typical curves

Unless otherwise specified, all typical curves are given as design guidelines only and are not tested.

6.5 Typical current consumption

For typical current consumption measurements, V_{DD} and V_{DDA} are connected together as shown in *Figure 5*.

Figure 5. Supply current measurement conditions
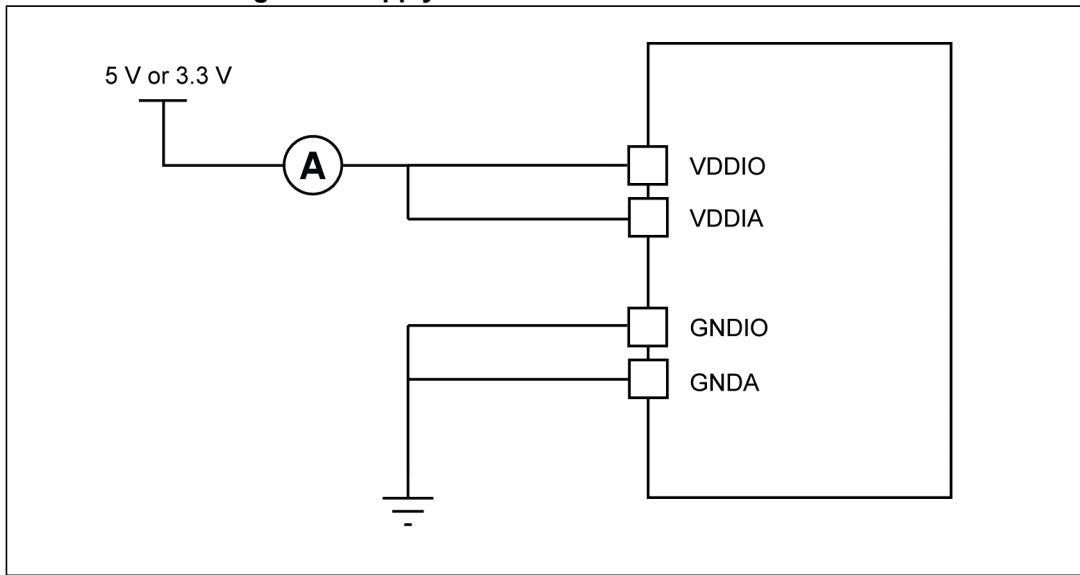
6.6 Loading capacitors

The loading conditions used for the pin parameter measurement are shown in *Figure 6*.

Figure 6. Pin loading conditions
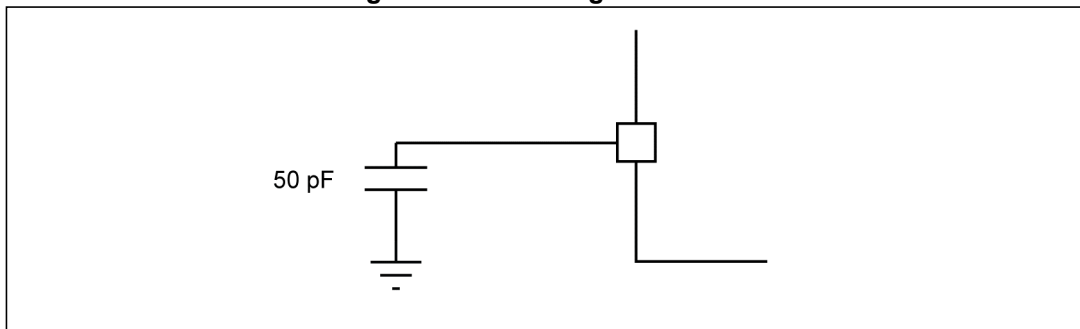
6.7 Pin output voltage

The input voltage measurement on a pin is described in *Figure 7*.

Figure 7. Pin input voltage
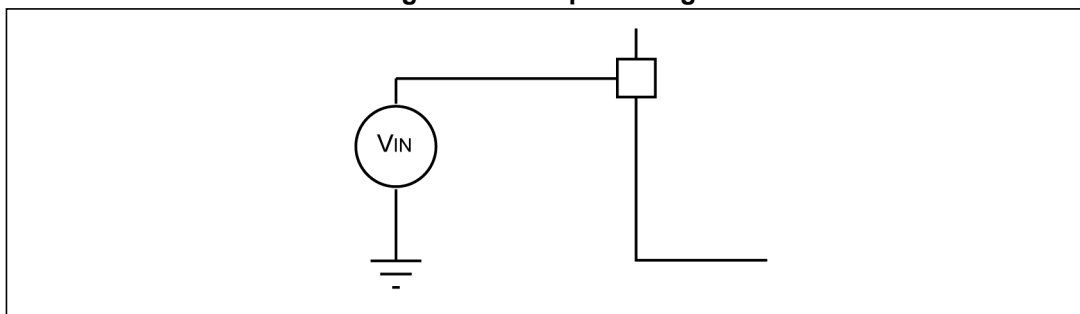
6.8 Absolute maximum ratings

Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

Table 3. Voltage characteristics

| Symbol	Ratings	Min.	Max.	Unit
V_{DDX} - V_{SSX}	Supply voltage[1]	-0.3	6.5	V
V_{IN}	Input voltage on any other pin[2]	V_{SS} -0.3	V_{DD} +0.3	
V_{DD} - V_{DDA}	Variation between different power pins	-	50	mV
V_{SS} - V_{SSA}	Variation between all the different ground pins[3]	-	50	mV

1. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.

2. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$ value. A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS}.

3. V_{SS} and V_{SSA} signals must be interconnected together with a short wire loop.

Table 4. Current characteristics

Symbol	Ratings	Max.[1]	Unit
I_{VDDX}	Total current into VDDX power lines[2]	100	mA
I_{VSSX}	Total current out of VSSX power lines[2]	100	
I_{IO}	Output current sunk by any I/Os and control pin	Ref. to *Table 10 on page 21*	
	Output current source by any I/Os and control pin	-	
$I_{INJ(PIN)}$ [3], [4]	Injected current on any pin	±4	
$I_{INJ(TOT)}$ [3],[4], [5]	Sum of injected currents	±20	

1. Data based on characterization results, not tested in production.

2. All power V_{DDX} (V_{DD}, V_{DDA}) and ground V_{SSX} (V_{SS}, V_{SSA}) pins must always be connected to the external power supply.

3. $I_{INJ(PIN)}$ must never be exceeded. This is implicitly insured if V_{IN} maximum is respected. If V_{IN} maximum cannot be respected, the injection current must be limited externally to the $I_{INJ(PIN)}$) value. A positive injection is induced by V_{IN} > V_{DD} while a negative injection is induced by V_{IN} < V_{SS}.

4. Negative injection disturbs the analog performance of the device.

5. When several inputs are submitted to a current injection, the maximum $\Sigma_{IINJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $\Sigma_{IINJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 5. Thermal characteristics

Symbol	Ratings	Max.	Unit
T_{STG}	Storage temperature range	-65 to 150	°C
TJ	Maximum junction temperature	150	

6.9 Operating conditions

The device must be used in operating conditions that comply with the parameters in *Table 6*. In addition, a full account must be taken for all physical capacitor characteristics and tolerances.

Table 6. General operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{CPU}	Internal CPU clock frequency	-	-	16	-	MHz
V_{DD1}, V_{DDA1}	Operating voltages	-	$3^{(1)}$	5	$5.5^{(1)}$	
V_{DD}, V_{DDA}	Nominal operating voltages	-	$3.3^{(1)}$	5	$5^{(1)}$	V
V_{OUT}	Core digital power supply	-	-	$1.8^{(2)}$	-	
	CVOUT: capacitance of external capacitor$^{(3)}$	at 1 MHz	470	-	3300	nF
	ESR of external capacitor	-	0.05	-	0.2	Ω
	ESL of external capacitor	-	-	-	15	nH
$\Theta_{JA}^{(4)}$	FR4 multilayer PCB	VFQFPN32	-	26	-	°C/W
T_A	Ambient temperature	Pd = 100 mW	-40	-	105	°C

1. The external power supply can range from 3 V to 5.5 V although IC performances are optimized for power supply equal to 5 V.

2. Internal core power supply voltage.

3. Care should be taken when the capacitor is selected due to its tolerance, its dependency on temperature, DC bias and frequency.

4. To calculate P_{Dmax} (T_A), use the formula $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$.

Table 7. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$V_{IT}+$	Power-on reset threshold	-	2.65	2.8	$2.98^{(1)}$	V
$V_{IT}-$	Brownout reset threshold	-	2.58	2.73	$2.88^{(1)}$	
$V_{HYS(BOR)}$	Brownout reset hysteresis	-	-	70	-	mV

1. VDD rise must be monotone. The slew rate should be between 1 μV/μs to 0.5 V/μs.

6.9.1 VOUT external capacitor

The stabilization of the main regulator is achieved by connecting an external capacitor C_{VOUT}[a] to the VOUT pin. The C_{VOUT} is specified in *Section 6.9: Operating conditions*. Care should be taken to limit the series inductance to less than 15 nH.

Figure 8. External capacitor C$_{VOUT}$

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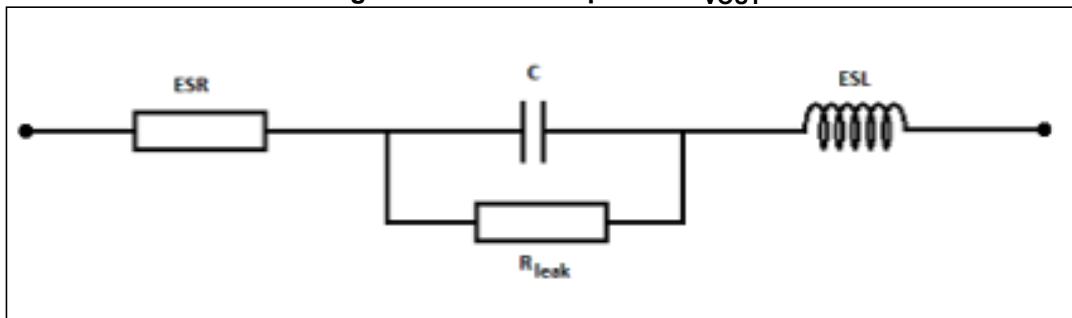
a. ESR is the equivalent series resistance and ESL is the equivalent inductance.

6.9.2 Memory characteristics

Flash program and memory/data EEPROM memory

General conditions: T_A = -40 °C to 105 °C.

Table 8. Flash program memory/data EEPROM memory

Symbol	Parameter	Conditions	Min.[1]	Typ.[1]	Max. [1]	Unit
t_{PROG}	Standard programming time	-	-	6	6.6	ms
	(including erase) for byte/word/block	-	-	-	-	
	(1 byte/4 bytes/128 bytes)	-	-	-	-	
	Fast programming time for 1 block (128 bytes)	-	-	3	3.3	
t_{ERASE}	Erase time for 1 block (128 bytes)	-	-	3	3.3	ms
N_{WE}	Erase/write cycles[2] (program memory)	T_A = 25 °C	10 K	-	-	Cycles
	Erase/write cycles[2] (data memory)	T_A = 85 °C	100 K	-	-	
		T_A = 105 °C	35 K	-	-	
t_{RET}	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 85 °C	15	-	-	Years
	Data retention (program memory) after 10 K erase/write cycles at T_A= 25 °C	T_{RET} = 105 °C	11	-	-	
	Data retention (data memory) after 100 K erase/write cycles at T_A= 85 °C	T_{RET} = 85 °C	15	-	-	
	Data retention (data memory) after 35 K erase/write cycles at T_A= 105 °C	T_{RET} = 105 °C	6	-	-	
I_{DDPRG}	Supply current during program and erase cycles	-40 ºC $\leq T_A \leq$ 105 ºC	-	2	-	mA

1. Data based on characterization results, not tested in production.

2. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.

6.9.3 I/O port pin characteristics

The I/O port pin parameters are specified under general operating conditions for V_{DD} and T_A unless otherwise specified. Unused input pins should not be left floating.

Table 9. Voltage DC characteristics

Symbol	Description	Min.[1]	Typ.	Max[1]	Unit
V_{IL}	Input low voltage	-0.3	-	0.3 * V_{DD}	V
V_{IH}	Input high voltage[2]	0.7 * V_{DD}	-	V_{DD}	
V_{OL1}	Output low voltage at 3.3 V[3]	-	-	0.4[4]	
V_{OL2}	Output low voltage at 5 V[3]	-	-	0.5	
V_{OL3}	Output low voltage high sink at 3.3 V / 5 V[2], [5]	-	0.6[4]	-	
V_{OH1}	Output high voltage at 3.3 V[3]	V_{DD} -0.4[4]	-	-	
V_{OH2}	Output high voltage at 5 V[3]	V_{DD} -0.5	-	-	
V_{OH3}	Output high voltage high sink at 3.3 V / 5 V[2], [5]	V_{DD} -0.6[4]	-	-	
H_{VS}	Hysteresis input voltage[6]	-	0.1 * V_{DD}	-	
R_{PU}	Pull-up resistor	30	45	60	kΩ

1. Data based on characterization result, not tested in production.

2. Input signals cannot exceed V_{DDX} (V_{DDX} = V_{DD}, V_{DDA}).

3. Parameter applicable to signals: PWM_QFOD, DNBL, LED, QC_IO, DCDC_DRV, DCDC_DAC, UPBL, UART_TX.

4. Electrical threshold voltage not characterized at -40 ºC.

5. Parameter applicable to the signals: SWIM, DEMAGNET.

6. Applicable to any digital inputs.

Table 10. Current DC characteristics

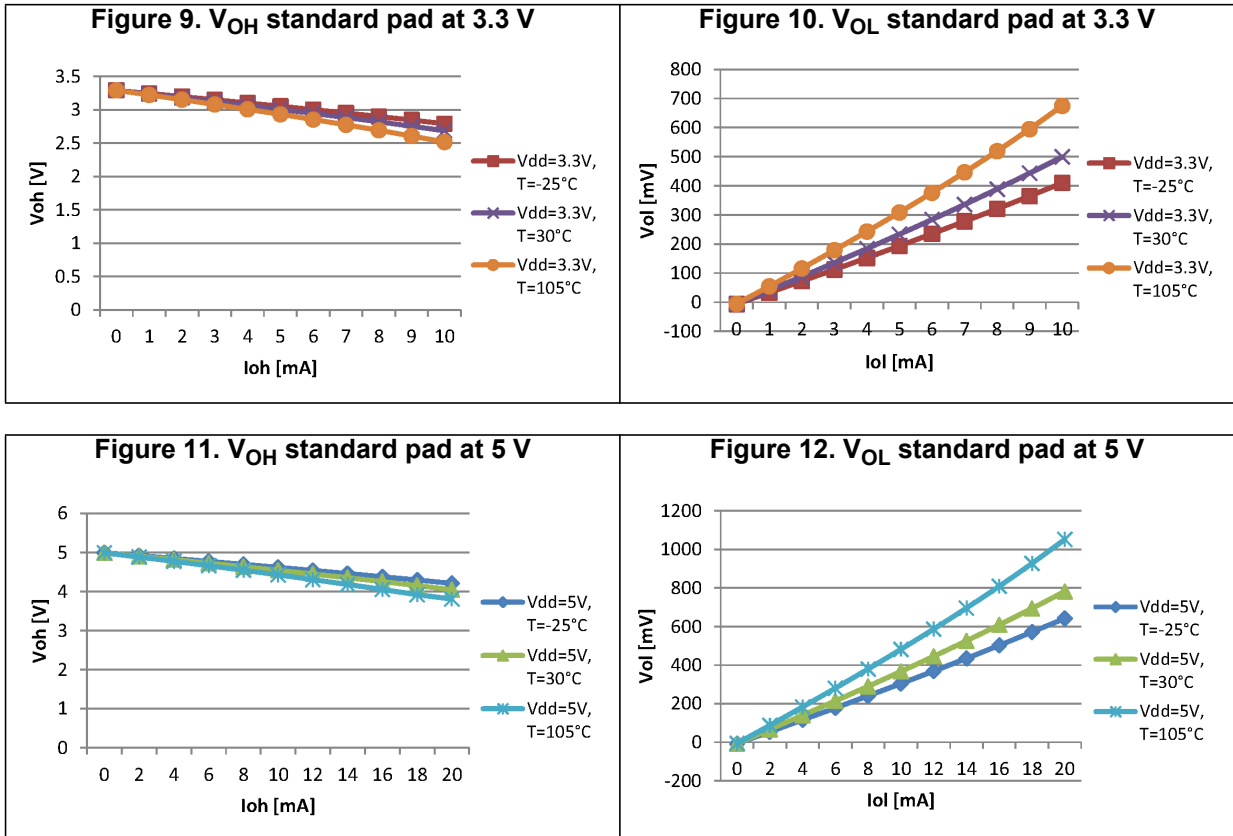| Symbol	Description	Min.	Typ.	Max.[1]	Unit
I_{OL1}	Standard output low level current at 3.3 V and VOL1[2]	-	-	1.5	mA
I_{OL2}	Standard output low level current at 5 V and VOL2[2]	-	-	3	
I_{OLhs1}	High sink output low level current at 3.3 V and VOL3[3]	-	-	5	
I_{OLhs2}	High sink output low level current at 5 V and VOL3[3]	-	-	7.75	
I_{OH1}	Standard output high level current at 3.3 V and VOH1[2]	-	-	1.5	
I_{OH2}	Standard output high level current at 5 V and VOLH2[2]	-	-	3	
I_{OHhs1}	High sink output high level current at 3.3 V and VOH3[3]	-	-	5	
I_{OHhs2}	High sink output high level current at 5 V and VOH3[3]	-	-	7.75	
I_{LKg}	Input leakage current digital - analog VSS $\leq$ VIN $\leq$ VDD[4]	-	-	± 1	µA
$I_{\_Inj}$	Injection current[5], [6]	-	-	± 4	mA
$\Sigma I_{\_Inj}$	Total injection current (sum of all I/O and control pins)[5]	-	-	± 20	

1. Data based on characterization result, not tested in production.

2. Parameter applicable to signals: PWM_QFOD, DNBL, LED, QC_IO, DCDC_DRV, DCDC_DAC, UPBL, UART_TX.

3. Parameter applicable to the signals: SWIM, DEMAGNET.

4. Applicable to any digital inputs.

5. The maximum value must never be exceeded.

6. The negative injection current on the TANK_VOLTAGE, VTARGET, QFOD_ADC, COIL_TEMP, ISENSE, VMAIN pins have to be avoided since it affects ADC conversion accuracy.

6.9.4 Typical output level curves

This section shows the typical output level curves measured on a single output pin for the three pad family present in the STWBC-EP device.
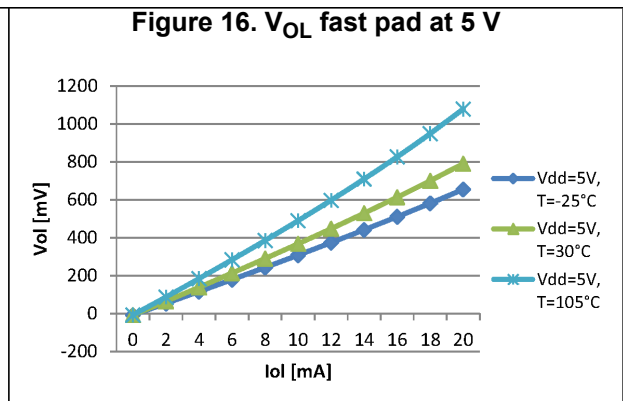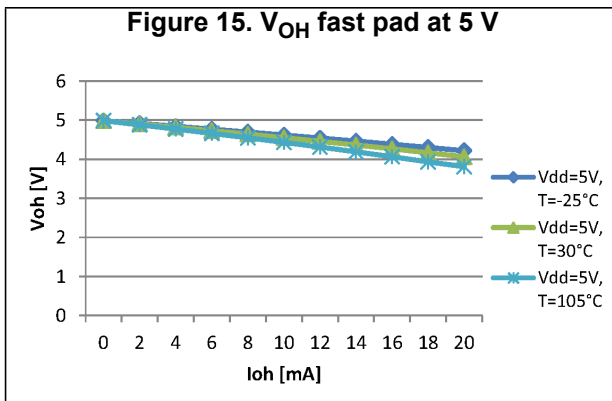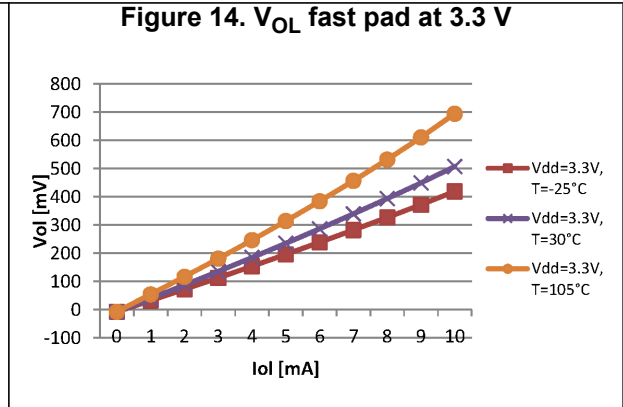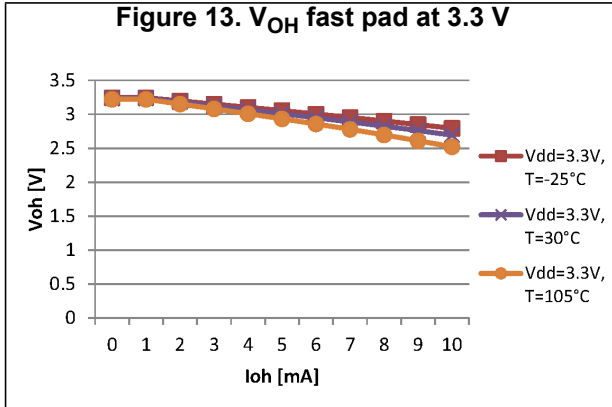
Standard pad

This pad class is associated to the following pins: I2C_SDA, I2C_SCL, LED, QC_IO, SYMBOL_DETECT, SWIM, UART_TX.

Figure 9. V_{OH} standard pad at 3.3 V

Figure 10. V_{OL} standard pad at 3.3 V

Figure 11. V_{OH} standard pad at 5 V

Figure 12. V_{OL} standard pad at 5 V

Fast pad

This pad class is associated to the PWM_QFOD, DNBL, DCDC_DRV, DCDC_DAC, UPBL pins.

Figure 13. V_{OH} fast pad at 3.3 V

Figure 14. V_{OL} fast pad at 3.3 V

Figure 15. V_{OH} fast pad at 5 V

Figure 16. V_{OL} fast pad at 5 V

6.9.5 Reset pin characteristics

The following data are specified under general operating conditions for V_{DD} and T_A defined in *Table 6 on page 17* unless otherwise specified.

Table 11. NRST pin characteristics

Symbol	Parameter	Conditions	Min.[1]	Typ.	Max.[1]	Unit
$V_{IL(NRST)}$	NRST input low level voltage[1]	-	-0.3	-	0.3 x V_{DD}	
$V_{IH(NRST)}$	NRST input high level voltage[1]	-	0.7 x V_{DD}	-	V_{DD} + 0.3	V
$V_{OL(NRST)}$	NRST output low level voltage[1]	I_{OL} = 2 mA	-	-	0.5	
$R_{PU(NRST)}$	NRST pull-up resistor[2]	-	30	40	60	kΩ
$t_{IFP(NRST)}$	NRST input filtered pulse[3]	-		-	75	
$t_{INFP(NRST)}$	NRST not input filtered pulse[3]	-	500	-	-	ns
$t_{OP(NRST)}$	NRST output filtered pulse[3]	-	15	-	-	µs

1. Data based on characterization results, not tested in production.
2. The RPU pull-up equivalent resistor is based on a resistive transistor.
3. Data guaranteed by design, not tested in production.

6.9.6 I^{2}C interface characteristics

Table 12. I^{2}C interface characteristics

Symbol	Parameter	Standard mode		Fast mode		Unit
		Min.[1]	Max.[1]	Min.[1]	Max.[1]	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	
$t_{h(SDA)}$	SDA data hold time	0[2]	-	0[2]	900[2]	
$t_{r(SDA)} t_{r(SCL)}$	SDA and SCL rise time (V_{DD} = 3.3 to 5 V)[3]	-	1000	-	300	ns
$t_{f(SDA)} t_{f(SCL)}$	SDA and SCL fall time (V_{DD} = 3.3 to 5 V)[3]	-	300	-	300	
$t_{h(STA)}$	START condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated START condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	STOP condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	STOP to START condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line[4]	-	50	-	50	pF

1. Data based on the standard I^{2}C protocol requirement, not tested in production.
2. The maximum hold time of the start condition has only to be met if the interface does not stretch the low time.
3. I^{2}C multifunction signals require the high sink pad configuration and the interconnection of 1 kΩ pull-up resistances.
4. 50 pF is the maximum load capacitance value to meet the I^{2}C std. timing specifications.

6.9.7   10-bit SAR ADC characteristics

The 10-bit SAR ADC parameters are specified under general operating conditions for V_{DDA} and T_A unless otherwise specified.

Table 13. ADC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution	-	10	-	bit
R_{ADCIN}	ADC input impedance[1]	1	-	-	MΩ
V_{IN}	Input conversion voltage range	0	-	1.25[1],[2]	V
V_{ref}	ADC main reference voltage[3]	-	1.250	-	

1. Maximum input analog voltage cannot exceed V_{DD}/V_{DDA}.

2. Exceeding the maximum voltage on the TANK_VOLTAGE, VTARGET, COIL_TEMP, ISENSE, QFOD_ADC signals has to be avoided since it may impact the ADC conversion accuracy defined in *Table 14*.

3. ADC reference voltage at T_A = 25 °C.

ADC accuracy characteristics

See *Figure 18* for more details about the ADC accuracy parameter definition.

Table 14. ADC accuracy characteristic at V_{DD}/V_{DDA} = 5 V

Symbol	Parameter	Min.[1]	Typ.[2]	Max.[1]	Unit
$|E_O|$	Offset error[3], [4]	-	0.5	-	
$|E_G|$	Gain error[3], [4], [5]	-	0.4	-	
E_{OG}	Offset + Gain error [5], [6]	-8.3	-	8.9	
E_{OG}	Offset + Gain error[5], [7]	-10.9	-	10.9	LSB
E_{OG}	Offset + Gain error[5], [8]	-13.8	-	10.9	
$|E_D|$	Differential linearity error[1], [2], [3]	-	0.8	-	
$|E_L|$	Integral linearity error[3], [4]	-	2.0	-	

1. Data based on characterization results, not tested in production.

2. Operating temperature: T_A = 25 °C.

3. ADC accuracy vs. negative injection current. The injecting negative current on any of the analog input pins should be avoided as this reduces the accuracy of the conversion being performed on another analog input. It is recommended that a Schottky diode (pin to ground) has to be added to standard analog pins which may potentially inject a negative current. Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in the I/O port pin characteristics section does not affect the ADC accuracy. The ADC accuracy parameters may be also impacted exceeding the ADC maximum input voltage V_{IN}.

4. Results in manufacturing test mode.

5. Gain error evaluated with the two-point method.

6. Temperature operating range: 0 ºC $\leq T_A \leq$ 85 ºC.

7. Temperature operating range: -25 ºC $\leq T_A \leq$ 105 ºC.

8. Temperature operating range: -40 ºC $\leq T_A \leq$ 105 ºC.

ADC equivalent input circuit

Figure 17 shows the ADC equivalent input circuit.

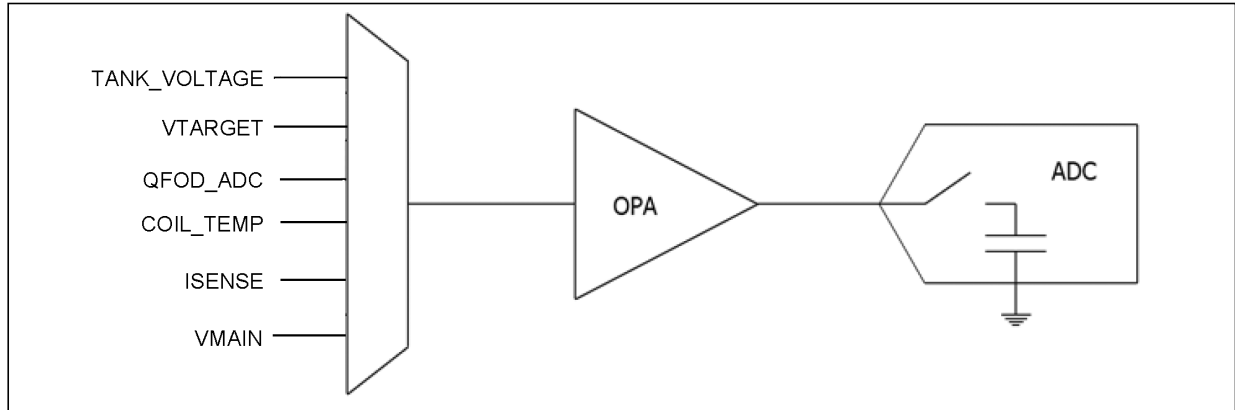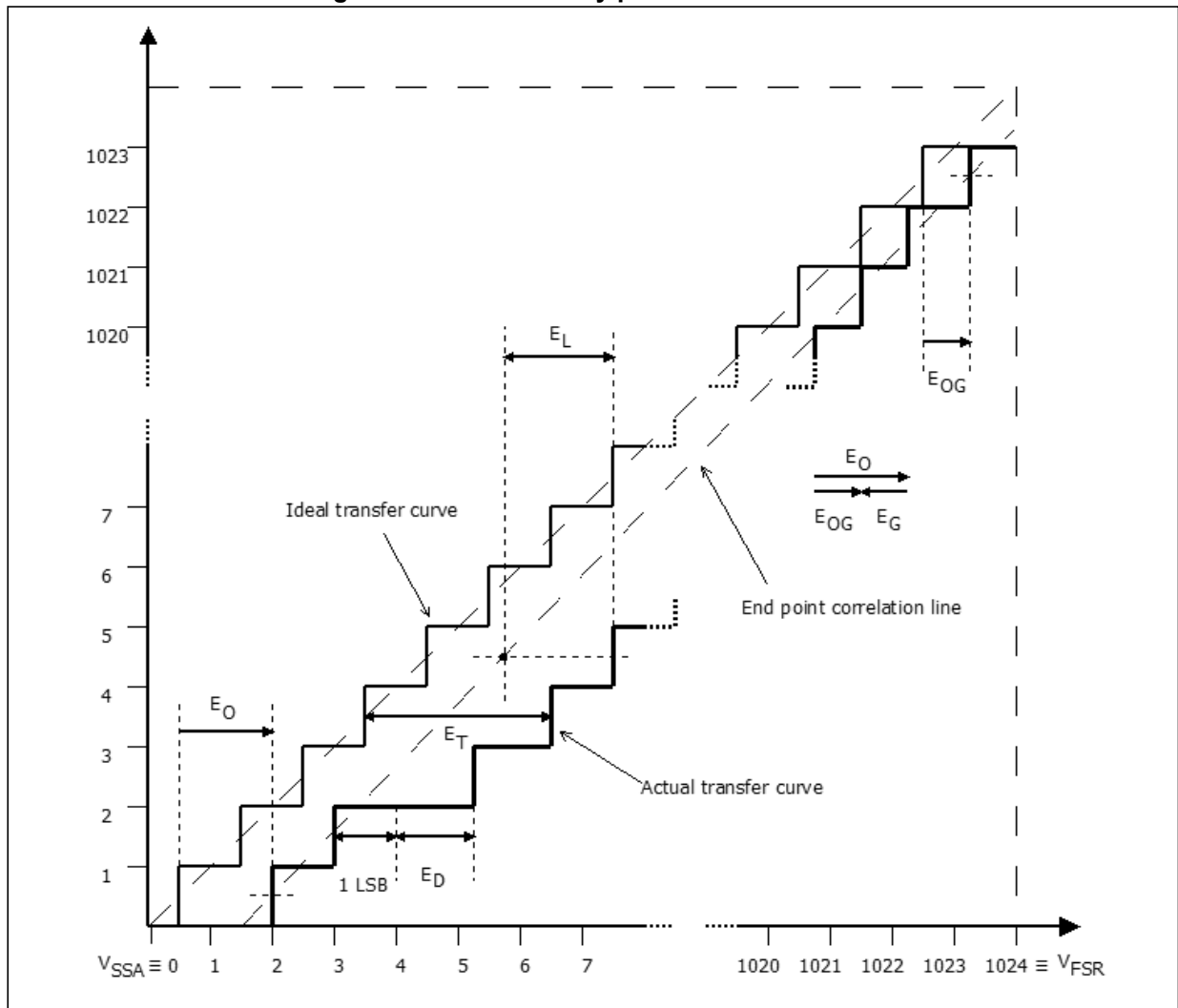**Figure 17. ADC equivalent input circuit**

Figure 18. ADC accuracy parameter definitions

E_T = total unadjusted error: maximum deviation between the actual and the ideal transfer curves.

E_O = offset error: deviation between the first actual transition and the first ideal one.

E_{OG} = offset + gain error (1-point gain): deviation between the last ideal transition and the last actual one.

E_G = gain error (2-point gain): defined so that $E_{OG} = E_O + E_G$ (parameter correlated to the deviation of the characteristic slope).

E_D = differential linearity error: maximum deviation between actual steps and the ideal one.

E_L = integral linearity error: maximum deviation between any actual transition and the end point correlation line.

7 Thermal characteristics

The STWBC-EP functionality cannot be guaranteed when the device is operating under the maximum chip junction temperature (T_{Jmax}).

T_{Jmax}, in degrees Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (PD_{max} \times \Theta_{JA})$$

where:

T_{Amax} is the maximum ambient temperature in °C.

Θ_{JA} is the package junction to ambient thermal resistance in °C/W.

PD_{max} is the sum of $PINT_{max}$ and PI/O_{max} ($PD_{max} = PINT_{max} + PI/O_{max}$).

$PINT_{max}$ is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

PI/O_{max} represents the maximum power dissipation on output pins where:
$PI/O_{max} = \Sigma (V_{OL} * I_{OL}) + \Sigma [(V_{DD} - V_{OH}) * I_{OH}]$, taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at the low and high level.

Table 15. Thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction ambient[1]	26	°C/W

1. Thermal resistances are based on JEDEC JESD51-2 with the 4-layer PCB in a natural convection environment.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 VFQFPN32 package information
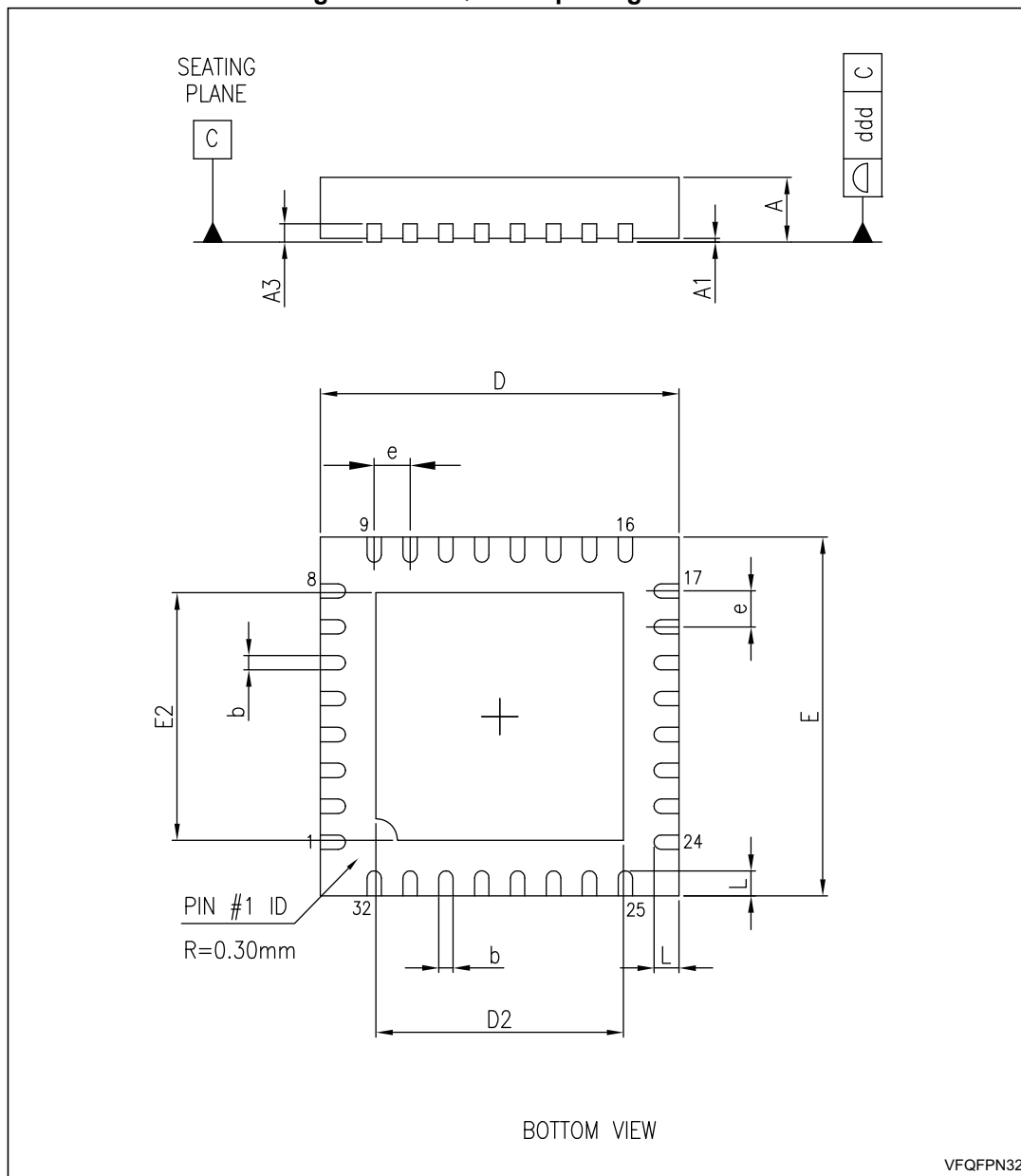
Figure 19. VFQFPN32 package outline

Table 16. VFQFPN32 package mechanical data

Symbol	Dimensions (mm)		
	Min.	**Typ.**	**Max.**
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20	-
b	0.18	0.25	0.30
D	4.85	5.00	5.15
D2	3.40	3.45	3.50
E	4.85	5.00	5.15
E2	3.40	3.45	3.50
e	-	0.50	0.55
L	0.30	0.40	0.50
ddd	-	-	0.08

Note: *1. VFQFPN stands for "Thermally Enhanced Very thin Fine pitch Quad Flat Package No lead".*

2. Very thin profile: 0.80 < A ≤ 1.00 mm.

3. Details of the terminal 1 are optional, but must be located on the top surface of the package by using either a mold or marked features.

4. Package outline exclusive of any mold flashes dimensions and metal burrs.

9 Revision history

Table 17. Document revision history

Date	Revision	Changes
10-Oct-2017	1	Initial release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY