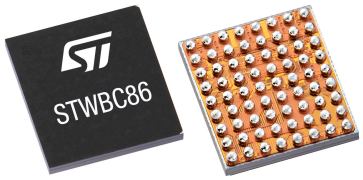
STWBC86

Datasheet

Qi compatible wireless power transmitter for 5W applications with integrated full bridge



Product status link
STWBC86

Product summary	
Order code	STWBC86JR
Package	WLCSP72
Packing	Tape and reel

Features

- WPC Qi 1.2.4 compatible Power Class 0 BPP
- Power Tx reference design based on A11a topology
- Up to 5W output power transfer on the receiver side
- Wide input voltage range 4.75V to 20V
- Monolithic solution with integrated Half-bridge/Full-bridge inverter and drivers for high efficiency and low BOM
- 32-bit, 64MHz ARM Cortex micro controller with 8KB SRAM
- FTP (Few Times Programmable) for Firmware patching and advanced features
- On-chip current sense
- 10-bit A/D converter
- I^2C interface
- Fully Configurable GPIOs
- Accurate voltage/current measurements for FOD
- Current limit and Thermal protection
- Robust ASK,FSK communication
- Flip chip 72 bumps (3.26mm x 3.67mm)

Application

- Smartphone charging
- Medical electronics
- Smart Wearable, Hearable Charging

Description

The STWBC86 is a highly integrated monolithic wireless power transmitter solution suitable for applications up to 5W.

This solution requires low external BOM count. Because of the integrated low impedance Full/Half bridge inverter, STWBC86 achieves high efficiency and low power dissipation.

I^2C interface allows firmware and platform parameters to be customized and the device can be configured using the embedded FTP.

Additional firmware patching also improves application flexibility of STWBC86.

The Flip Chip package and low BOM count make the device suitable for very compact applications.

1 Introduction

STWBC86 is primarily a wireless power transmitter that provides up to 5W of power.

It offers the most flexible and efficient solution for controlling the power transfer to a receiver (RX) in applications such as smart phones, smart wearable, hearable devices that use electromagnetic induction for recharging.

The 32-bit core MCU is the supervisor of the whole device and manages all the functional blocks to

- establish and maintain communication with the receiver,
- optimize the efficiency by properly adjusting the operating point
- guarantee reliability by monitoring and protecting both the load and the device itself.

The Tx is responsible for controlling the transmitting coil and generating correct amount of power requested by the Rx.

Transferring a correct amount of power ensures the highest level of end to-end efficiency due to reduced energy losses. It also helps maintaining a lower operational temperature.

The I^2C interface provides access to the internal registers of the STWBC86 for applications in which the host system directly monitors or controls the power transfer.

The Tx can adapt to the amount of energy transferred by the coil by adjusting the frequency, duty cycle of the PWM voltage on the transmitting coil.

The power transmitter firmware is placed in ROM and is able to operate fully autonomously. This firmware is patchable with 8kB on-board FTP.

STWBC86 comes with a current limit and over-temperature protections to ensure safety of the device.

Figure below shows a block diagram of the device with simplified interconnections among the functional blocks.

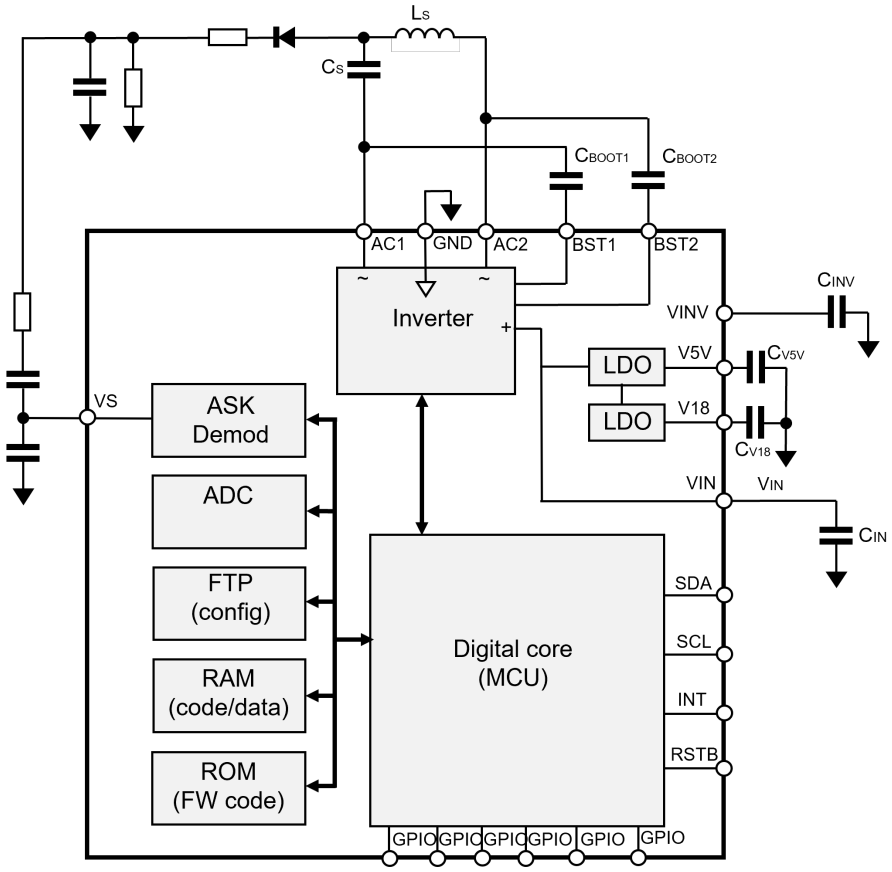
The inverter converts the DC input voltage into an AC voltage, which is used to drive the coil. The four switches of the inverter (essentially an H-bridge) are controlled by the digital core in order to minimize both conduction and switching losses.

Two bootstrap capacitors are externally connected to the BOOT1-BOOT2 pins to correctly drive the high-side switches of the inverter.

VIN power supply is also the input rail for auxiliary linear regulators in charge of deriving the 5 V and 1.8 V supply voltages.

2 Block Diagram

Figure 1. **Simplified block diagram**



3 Device pinout

Figure 2. **Pin assignment (through top view)**

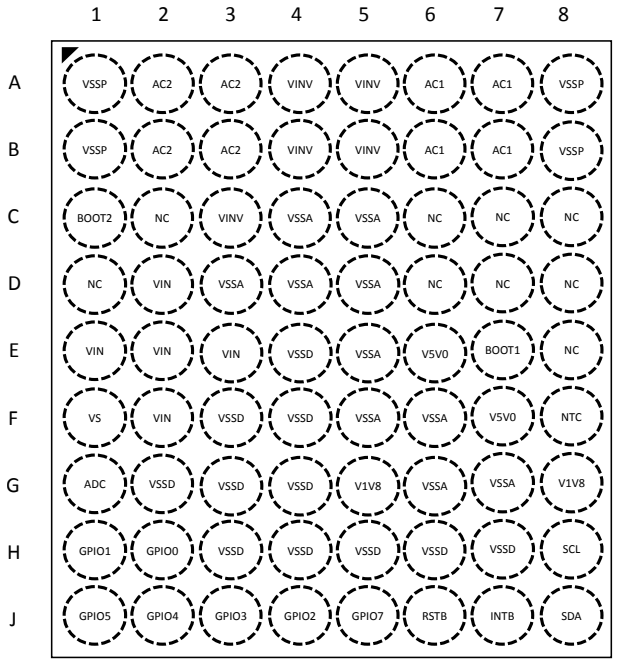


Table 1. **Pin description**

Pin name	Pin location	Pin function
VSSA	C4,C5,D3,D4, D5,E5,F5,F6, G6,G7	Analog ground.
VSSD	E4, F3, F4, G2, G3, G4, H3, H4, H5, H6, H7	Digital ground. Reference for digital input and output signals.
VSSP	A1, A8, B1, B8	Power ground. Power return for the inverter.
AC1	A6, A7, B6, B7	AC power input: Output of the inverter. Connect to the Tx series resonant circuit.
AC2	A2, A3, B2, B3	AC power input: Output of the inverter. Connect to the Tx series resonant circuit.
BOOT1	E7	Inverter bootstrap capacitor, connect a 47 nF (typical) ceramic capacitor between this pin and AC1.
BOOT2	C1	Inverter bootstrap capacitor, connect a 47 nF (typical) ceramic capacitor between this pin and AC2.
VINV	A4, A5, B4, B5, C3	Inverter input supply. A suitable capacitor between these pins and VSSP ensures residual AC ripple filtering.
VS	F1	ASK demodulation input. (optional) ADC in: Ring node voltage input used for FOD
ADC	G1	
NTC	F8	Coil temperature sensing input: connect to the center tap of a resistor divider having an NTC in the low-side position. If this function is not used, the pin must be pulled-up to V1V8 through a 10 kΩ resistor to prevent triggering the coil over-temperature protection.
VIN	D2, E1, E2, E3, F2	Power supply input. Connect a suitable filtering capacitor between these pins and ground to ensure stable operation and proper load transient response in all operating conditions.

Pin name	Pin location	Pin function
V1V8	G5, G8	1.8V LDO output and supply rail for the digital core, the ADC and the analog circuitry. Connect a 1 µF filtering capacitor between this pin and ground.
V5V0	F7, E6	5V LDO output and supply rail for the auxiliary circuitry. Connect a 4.7 µF filtering capacitor between this pin and ground.
RSTB	J6	Chip-reset input. If set low, the internal digital core is reset. This pin can also be used by the host controller to control the power transfer process.
SCL	H8	I2C bus, clock line input. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels. I2C bus, data line I/O. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels.
SDA	J8	
GPIO0	H2	Programmable general-purpose I/Os: the function of these pins depends on the configuration of the device.
GPIO1	H1	
GPIO2	J4	
GPIO3	J3	
GPIO4	J2	
GPIO5	J1	
GPIO7	J5	
INTB/GPIO6	J7	Interrupt output (active low). Programmable open-drain output used to generate an interrupt on specific events for the host controller.
NC	C2,C6,C7,C8, D1,D6,D7,D8,E8	Not connected pins , to be left floating.

4 Electrical and thermal specifications

4.1 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in Table 2 is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Parameter	Pin(s)	Min.	Max.	Unit
Pin voltage range	AC1, AC2 respect to ground (VSSA, VSSD and VSSP pins)	-0.9	27	V
	BOOT1 to AC1	-0.3	5.5	
	BOOT2 to AC2			
	BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins)	-0.3	27	
	VINV, VIN respect to ground (VSSA, VSSD and VSSP pins)	-0.7	27	
	V1V8, NTC, VS and ADC respect to ground (VSSA, VSSD and VSSP pins)	-0.3	1.98	
	V5V0 respect to ground (VSSA, VSSD and VSSP pins)	-0.7	5.5	
	GPIO0 through GPIO5,GPIO7, INTB, RSTB, SDA, SCL respect to ground (VSSA, VSSD and VSSP pins)	-0.7	5.5	
	Relative voltage between any ground pin (VSSA, VSSD, VSSP)	-0.3	0.3	
RMS Current	AC1,AC2,VINV		2.0	A
HBM ESD susceptibility JEDEC JS001-2012	All pins		2000	V
CDM ESD susceptibility JEDEC JS002-2012			500	
Latch-Up EIA/JESD78E		-200	200	mA

4.2 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{A,OP}$(1)	Operating ambient temperature		-40		85	°C
$T_{J,OP}$	Operating junction temperature		0		125	
$R_{\Theta JA}$(2)	Junction to ambient thermal resistance	2s2p		47		°C/W

1. *Ta -40°C to 85°C , limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization,if not otherwise specified.*
2. *Device mounted on a standard JESD51-5 test board*

4.3 Electrical characteristics

0 °C < T_A < 85 °C; V_{VINPUT} = 5 V to 10 V. Typical values are at T_J = 25 °C, if not otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply section						
$V_{VIN,UVLO}$	VIN Under-Voltage Lock-Out upper (turn-on) threshold	VIN pin voltage, rising edge		3.0	3.3	V
$V_{VIN,MAX}$	VIN maximum operating supply voltage	Voltage on VIN pin			20	V
$I_{VIN,Q}$	VIN current consumption in shut-down mode	RSTB low for more than 1 ms, supply voltage (5 V) applied to VIN		400	750	µA
$I_{VIN,OP}$	Operating current consumption	RSTB high, supply voltage applied to VIN		14.7		mA
1.8V supply voltage LDO linear regulator						
V_{V1V8}	LDO output voltage	I_{V1V8} = 5 mA	1.79	1.8	1.81	V
	LDO load regulation	0 mA < I_{V1V8} < 10 mA		5	20	mV
5V supply voltage LDO linear regulator						
V_{V5V0}	LDO output voltage	I_{V5V0} = 5 mA	4.8	5	5.2	V
	LDO load regulation	0 mA <I_{V5V0} = 0 mA <10 mA		2	20	mV
	LDO UVLO upper threshold		2.8	3	3.2	V
$I_{V5V0,EXT}$	Maximum current with external load				15	mA
Inverter						
Efficiency	Target rectifier efficiency	I_{VINV} = 1 A, V_{VIN}= 5.2 V, f_{AC} = 100 kHz to 250 kHz		97		%
		I_{VIN} = 1 A, V_{VIN} = 9.2 V, f_{AC} = 100 kHz to 250 kHz		97		
F_{FREQ}	Inverter frequency range		100		500	KHZ
V_{IN}	Input voltage range	VIN	4.95		20	V
I_{SENSE}	Input current sense range		0		2500	mA
Micro controller						
Architecture	Arm® Cortex®			32		bit
RAM	RAM Size			8		KB
Few Times Programmability						
FTP	Memory size for configuration and firmware patch			8		KB
Clock generator						
F_{OSC}	Clock generator & PWM timer frequency			64		
F_{OSC_TOL}	Tolerance of the clock generator frequency		-4		+4	%
Digital signals						
V_{IL}	Low level input voltage				0.55	V
V_{IH}	High level input voltage		1.14			
V_{OH}	GPIOx high level output voltage	Output high, I_{SOURCE} = 3mA	1.25			

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	GPIOx pin current capability	Output high	3			mA
V_{OL}	Low level output voltage	Output low, I_{SINK}=3mA			0.4	V

5 Device description

5.1 Wireless power interface

Wireless charging system diagram is shown below. The key blocks are Inverter (Power conversion unit), Communications and Control unit.

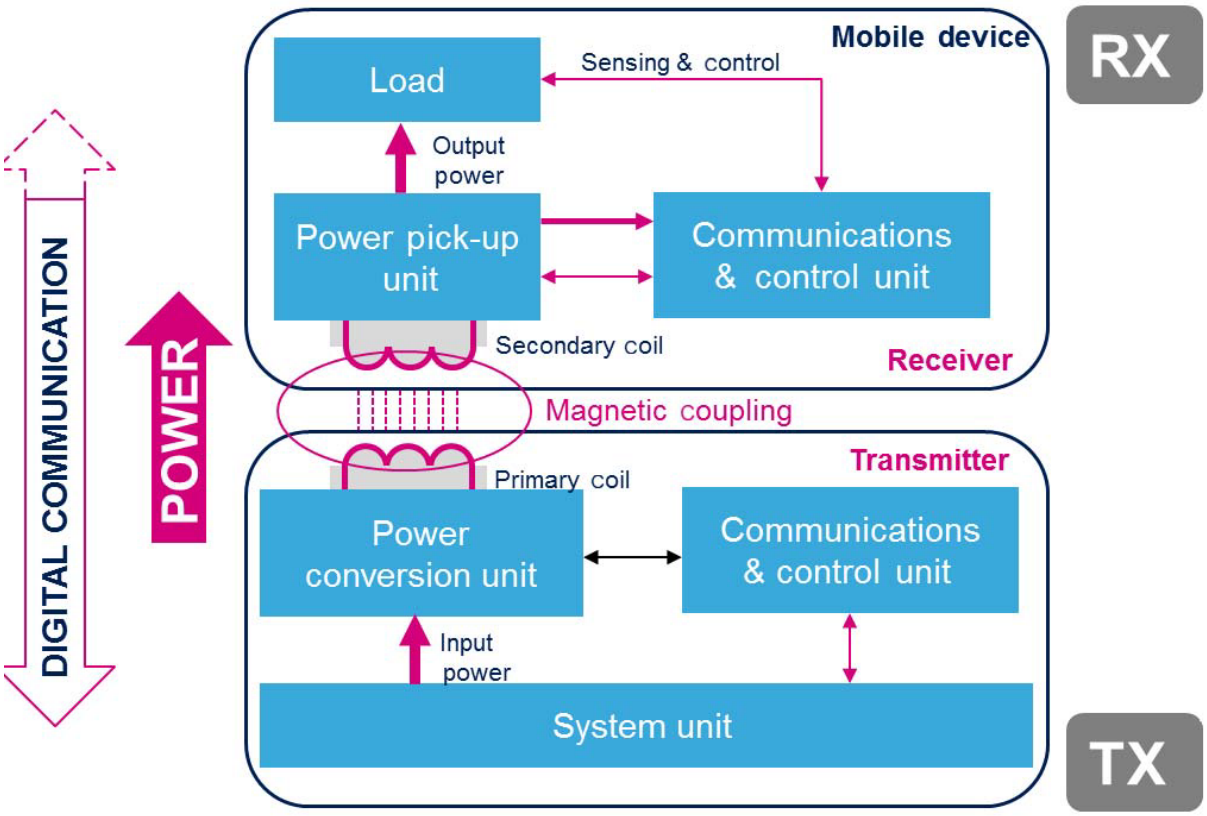
The Tx is responsible for controlling the transmitting coil and transferring the correct amount of power requested by the Rx.

The Rx modulates the power signal using resistive and capacitive load to communicate to the Tx requested power level.

Transferring the correct amount of power ensures the highest level of end to-end efficiency due to reduced energy losses. It also helps maintaining a lower operational temperature.

The Tx can adapt to the amount of energy transferred by the coil by adjusting the frequency, duty cycle of the PWM voltage on the transmitting coil.

Figure 3. Wireless charging system



5.2 Inverter

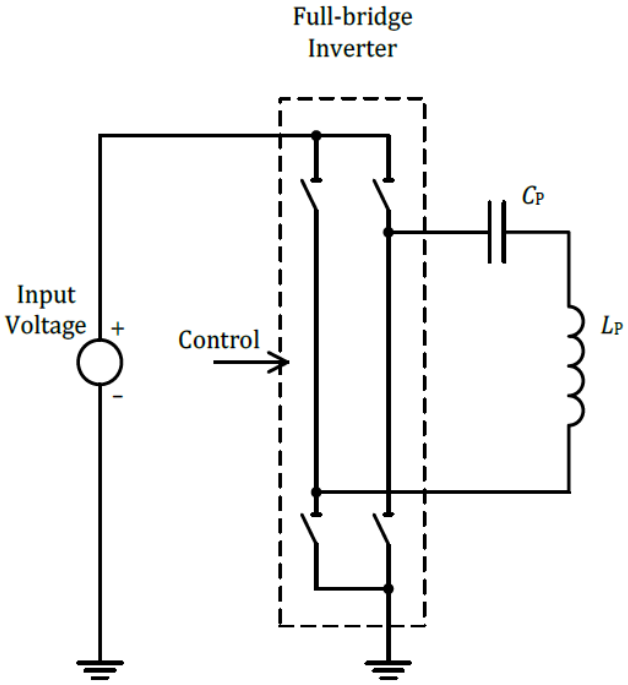
The power transmitter design uses a Full bridge inverter to drive the primary coil and series capacitance. The power transmitted to the coil is regulated by varying switching frequency and/or duty cycle of the bridge.

A higher operating frequency (for example 200kHz) leads to lower transmitted power, while a lower frequency (for example 110kHz) leads to higher transmitted power.

The LC resonant circuit optimization to be done based on power transfer requirements.

Full bridge inverter circuit is shown below.

Figure 4. **Full bridge inverter**



Typical Operating Frequency range of the full-bridge inverter is op = 120 … 148 kHz , duty cycle range 10% to 50%.

Primary Coil and Shielding has a self-inductance P = 6.3±10% µH.

The value of the series capacitance is P =0.4±5% µF.

The input voltage to the full-bridge inverter is 5±5% V.

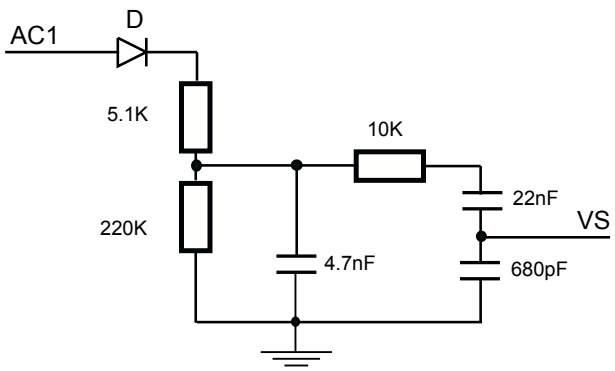
5.3 ASK communication

Robust and reliable in-band ASK communication is critical to the operation of any Qi compliant devices.

Using ASK modulation, the receiver sends Control Error Packets (CEP) to tune the operating point to match load requirements.

The coil signal is demodulated using a circuit shown below and fed to the VS pin of STWBC86.

Figure 5. **ASK demodulation filter circuit**



5.4 Chip reset pin

The RSTB pin, active low, can block operation of the device by forcing the digital core in reset state.

After releasing the reset pin, STWBC86 can resume normal operation mode.

5.5 GPIOx and INTB pins

The GPIO0 through GPIO7 pins are programmable general-purpose I/O pins. These pins can be configured as inputs or outputs (push-pull or open-drain) according to the selected function.

The INTB(GPIO6) pin is an interrupt output line that can be associated to any internal interrupt condition and used to inform the host system about specific events.

5.6 Device protections

Input voltage and input current are monitored by an internal ADC.

Both input voltage and input current can be limited by setting OVP and OCP thresholds.

Exceeding either threshold triggers a corresponding protection.

Internal temperature is also measured using the internal ADC and it's threshold can be set in °C.

When the internal temperature exceeds the set threshold, the OTP protection is triggered.

6 I2C interface

The STWBC86 can operate fully independently, i.e. without being interfaced with a host system.

In applications in which the STWBC86 has to be a part of peripherals managed by the host system, the two SDA and SCL pins could be connected to the existing I²C bus.

The device works as an I²C slave and supports standard (100 kbps) fast (400 kbps) data transfer modes.

The STWBC86 has been assigned 0x61, a 7-bit hardware address. The pull-up resistors should be selected as a trade-off between communication speed (lower resistors lead to faster edges) and data integrity (the input logic levels have to be guaranteed to preserve communication reliability).

When the bus is idle, both SDA and SCL lines are pulled HIGH.

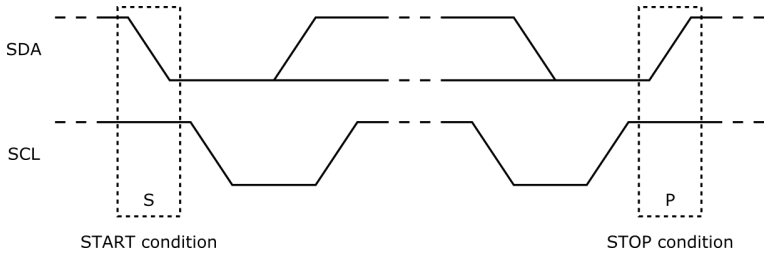
Data Validity

The data on the SDA line must be stable during the high period of the clock. The high and low states of the SDA line can only change when the SCL clock signal is low.

Start and Stop Conditions

Both the SDA and the SCL lines remain high when the I^{2}C bus is not busy. A START condition is a high-to-low transition of the SDA line when SCL is HIGH, while the STOP condition is a low-to-high transition of the SDA line when SCL is HIGH. A STOP condition must be sent before each START condition.

Figure 6. Start and Stop Condition on the I2C Bus



Byte format

Every byte transferred over the SDA line must contain 8 bits. Each byte received by the STWBC86 generally is followed by an acknowledge (ACK) bit. The MSB is transferred first. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high state of each SCL clock pulse.

The device generates the ACK pulse (by pulling-down the SDA line during the acknowledge clock pulse) to confirm the correct device address or received data bytes.

Interface protocol

The interface protocol consists of

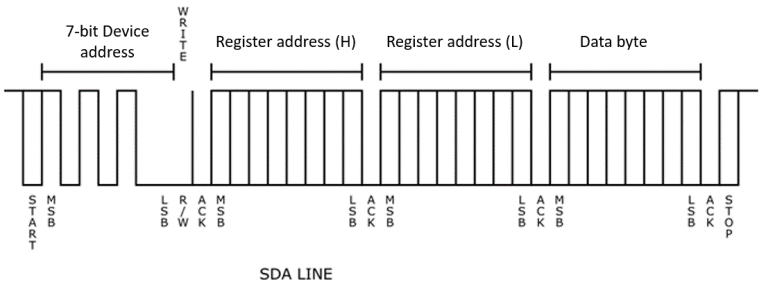
- Start condition (START)
- 7-bit device address (0x61) + R/W bit (read = 1 / write = 0)
- Register pointer, high-byte
- Register pointer, low-byte
- Data sequence: N x (data byte + ACK)
- Stop condition (STOP)

The register pointer (or address) byte defines the destination register to which the read or write operation applies. When the read or write operation is finished, the register pointer is automatically incremented.

Writing to a single register

Writing to a single register begins with a START condition followed by device address 0xC2 (7-bit device address plus R/W bit cleared), two bytes of the register pointer and the data byte to be written in the destination register. Each transmitted byte is acknowledged by the STWBC86 through an ACK pulse.

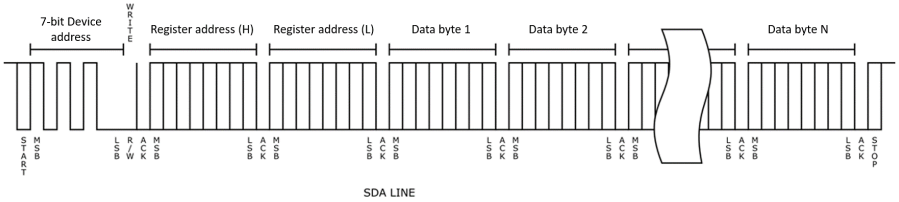
Figure 7. Writing to single register byte



Writing to multiple registers (page write)

The STWBC86 supports writing to multiple registers with auto-incremental addressing. When data is written into a register, the register pointer is automatically incremented, therefore transferring data to a set of subsequent registers (also know as page write) is a straightforward operation.

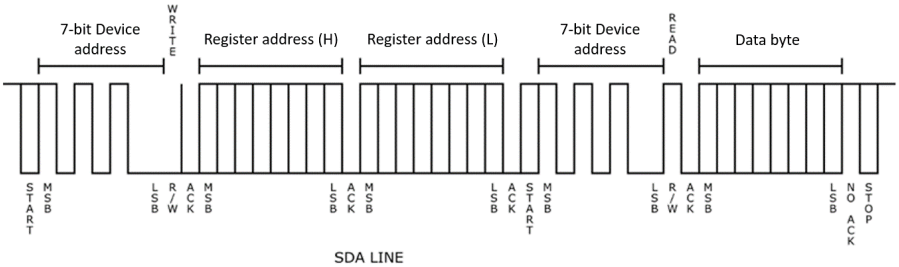
Figure 8. Writing multiple register bytes



Reading from a single register

Reading from a single register begins with a START condition followed by the device address byte 0xC2 (7-bit device address plus R/W bit cleared) and two bytes of register pointer, then a re-START condition is generated and the device address 0xC3 (7-bit device address plus R/W bit asserted) is sent, followed by data reading. ACK pulse is generated by the STWBC86 at the end of each byte, but not for data bytes retrieved from the register. A STOP condition is finally generated to terminate the operation.

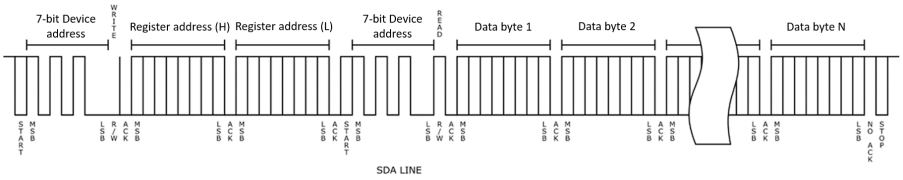
Figure 9. Reading single register byte



Reading from multiple registers (page reading)

Similarly to multiple (page) writing, reading from subsequent registers relies on an auto-increment of the register: the master can extend data reading to the following registers by generating and an ACK pulse at the end of each byte. Data reading starts immediately and the stream is terminated by a NMAK pulse at the end of the last data byte, followed by a STOP condition.

Figure 10. Reading multiple bytes



7 I²C register map

The STWBC86 can be monitored and controlled by accessing the internal registers via I²C interface. The following registers map reports the accessible addresses. Addresses not shown in the map and blank bits have to be considered reserved and not altered as well.

Table 5. Register abbreviations

Register type	Description
R/W	can read and write the bits
R	can read only
W	can write only

Table 6. Chip information

Address	Register name	R/W	Default	Description
0x0000	Chip ID Low	R	0x56	Chip ID [7..0]
0x0001	Chip ID High	R	0x00	Chip ID [15..8]
0x0002	Chip revision	R	0x02	Chip revision [7..0]
0x0003	Customer ID	R	0x00	Customer ID [7..0]
0x0004	ROM ID	R	0x18	ROM ID [7..0]
0x0005	ROM ID	R	0x01	ROM ID [15..8]
0x0006	NVM Patch ID	R	-	NVM patch ID [7..0]
0x0007	NVM Patch ID	R	-	NVM patch ID [15..8]
0x000A	Configuration ID	R	-	Configuration ID [7..0]
0x000B	Configuration ID	R	-	Configuration ID [15..8]
0x000C	Production ID	R	0x07	PE ID [7..0]
0x000E	Operation mode	R	0x03	0x1: Standalone (debug) mode ; 0x3: Qi TX mode
0x0010 ..0 x001F	Device ID	R	-	Device ID Bytes 0 ...15

Table 7. System information

Address	Register name	R/W	Default	Description
0x0020	System command	RW	-	Bit 0: Switch to TX command Write 1 to switch to Qi TX mode
				Bit 1..7 Reserved
0x002C	System error	R	-	Bit 0: Core hard fault error 0: No hard fault error detected 1: Hard fault error detected
		R	-	Bit 1: HW WDT trigger latch 0: HW WDT not triggered 1: HW WDT triggered
		R	-	Bit 2: FTP IP error 0: No FTP IP error detected

Address	Register name	R/W	Default	Description
0x002C	System error			1: FTP IP error detected
		R	-	Bit 4: FTP Boot error
		R	-	Bit [9..8] FTP PE error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [11..10] FTP Configuration error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [13..12] FTP Patch error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit[15..14]FTP Production Information error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved

Table 8. Commands

Address	Register name	R/W	Default	Description
0x0020	TX EN	RW	-	Bit 0: Switch to TX command Write 1 to switch to Qi TX mode

Table 9. Mode monitor

Address	Register name	R/W	Default	Description
0x0040	VINV Byte 0..1	R	-	Inverter voltage in mV [7..0]
0x0041				[15..8]
0x0042	VIN Byte 0..1	R	-	Main Voltage input in mV [7..0]
0x0043				Main Voltage input in mV [15..8]
0x0044	TX ICUR Byte 0..1	R	-	Input current in mA [7..0]
0x0045				[15..8]
0x0046	TMEAS Byte 0..1	R	-	Chip temperature in deg C [7..0]
0xx0047				[15..8]
0x0048	NTC Byte 0..1	R	-	NTC measurement [7..0]
0x0049				[15..8]
0x004A	ADC IN Byte 0..1	R	-	ADC IN Measurement [7..0]

Address	Register name	R/W	Default	Description
0x004B	ADC IN Byte 0..1	R	-	[15..8]
0x004C	OP FREQ	R	-	Operating frequency specified in units of 4kHz [7..0]
0x004D				[15..8]
0x006E	POWER RX Byte 0..1	R	-	RX received power in mW [7..0]
0x006F				[15..8]
0x0070	POWER TX Byte 0..1	R	-	Power transmitted to RX [7..0]
0x0071				[15..8]
0x0072	POWER RPP	R	-	Last value sent in received power packet [7..0]
0x0073				[15..8]
0x0074	RECENT CEP	R	-	Last CEP value received from RX [7..0]
0x0075				[15..8]
0x0076	SIG STREN	R	-	Signal strength measured in RX [7..0]
0x0077				[15..8]
0x00E9	OP DUTY	R	-	TX operating duty cycle in % [7..0]

Table 10. GPIO

Address	Register name	R/W	Default	Description
0x30	GPIO0 Fun	RW	-	Please refer to GPIO configuration description.
0x31	GPIO1 Fun	RW	-	
0x32	GPIO2Fun	RW	-	
0x33	GPIO03Fun	RW	-	
0x34	GPIO04Fun	RW	-	
0x35	GPIO05Fun	RW	-	
0x36	GPIO06Fun	RW	-	Configured as Interrupt - INTB Pin
0x37	GPIO07Fun	RW	-	

GPIO configuration - alternate functions

- 0x00: GPIO configured as Input , FLOATING (Default)
- 0x01: GPIO configured as Input , Pull up resistor to internal 1.8V.
- 0x02: GPIO configured as Input ,Pull down resistor to Internal Ground.
- 0x03: GPIO configured as Output , Open Drain (Active High)
- 0x04: GPIO configured as Output , Open Drain (Active Low)
- 0x05:GPIO configured as Interrupt pin , Open Drain output.
- 0x06: Initialization complete, FW ready.

Table 11. TX Commands

Address	Register name	R/W	Default	Description
0x00D0		RW	-	Bit0: TX EN Enable the TX. Write 1 to start Ping
		RW	-	Bit1:TX DIS Disable the TX. Write 1 to stop the inverter and cut the power to Rx

Table 12. **TX Interrupt enable**

Address	Register name	R/W	Default	Description
0x00C0	TX interrupt enable Byte0	RW	-	Bit 0: TX OVTP EN Over temperature protection enable 0: disable 1: enable
		RW	-	Bit 1: TX OCP EN Over current protection enable 0: disable 1: enable
		RW	-	Bit 2:TX OVP EN Over voltage protection enable 0: disable 1: enable
		RW	-	Bit 3:TX SYS ERR EN System error enable 0: disable 1: enable
		RW	-	Bit4: TX RP PKT RCVD EN RP packet received interrupt enable 0: disable 1: enable
		RW	-	Bit5: TX CE PKT RCVD EN CE packet received interrupt enable 0: disable 1: enable
		RW	-	Bit6: TX SEND PKT SUC EN Packet sent interrupt enable 0: disable 1: enable
		RW	-	Bit7: TX EXT MON EN Ext TX Detect interrupt enable 0: disable 1: enable
0x00C1	TX interrupt enable Byte1	RW	-	Bit0: TX CEP TO EN CEP Timeout interrupt enable 0: disable 1: enable
		RW	-	Bit1: TX RPP TO EN RPP Timeout interrupt enable 0: disable 1: enable
		RW	-	Bit2: TX EPT EN AC powered down interrupt enable

Address	Register name	R/W	Default	Description
0x00C1	TX interrupt enable Byte1			0: disable 1: enable
		RW	-	Bit3: TX START PING EN Ping started interrupt enable 0: disable 1: enable
		RW	-	Bit4:TX SS PKT RCVD EN SS ID packet received interrupt enable 0: disable 1: enable
		RW	-	Bit5: TX ID PKT RCVD EN ID packet received interrupt enable 0: disable 1: enable
		RW	-	Bit6: TX CFG PKT RCVD EN Configuration packet received interrupt 0: disable 1: enable
		RW	-	Bit7: TX PP PKT RCVD EN PP packet received interrupt enable 0: disable 1: enable
0x00C2	TX interrupt enable Byte2	RW	-	Bit0:TX BRIDGE MD EN Bridge mode (half/full) changed interrupt 0: disable 1: enable
		RW	-	Bit1: TX FOD DET EN TX FOD detect interrupt enable 0: disable 1: enable
		RW	-	Bit2:TX PTC UPDATE EN The power transfer contract is successfully updated after negotiation/renegotiation 0: disable 1: enable
		RW	-	Bit 3: TX DTS SUCC EN DTS send data stream successfully 0: disable 1: enable
		RW	-	Bit 4: TX DTS SEND END TO EN DTS stopped sending due to time out 0: disable 1: enable
		RW	-	Bit 5: TX DTS SEND END RST EN

Address	Register name	R/W	Default	Description
0x00C2	TX interrupt enable Byte2			DTS stopped sending due to reset 0: disable 1: enable
		RW	-	Bit 6: TX DTS RCVD SUCC EN DTS received data successfully 0: disable 1: enable
		RW	-	Bit7: TX DTS RCVD END TO EN DTS stopped receiving due to time out 0: disable 1: enable
0x00C3	TX interrupt enable Byte3			Reserved

Table 13. TX Interrupt clear

Address	Register name	R/W	Default	Description
0x00C4	TX interrupt clear Byte0	R	-	Bit 0:TX OVTP CLR Over temperature protection clear 1: clear
		R	-	Bit 1:TX OCP CLR Over current protection clear 1: clear
		R	-	Bit 2:TX OVP CLR Over voltage protection clear 1: clear
		R	-	Bit 3:TX SYS ERR CLR System error clear 1: clear
		R	-	Bit4: TX RP PKT RCVD CLR RP packet received interrupt clear 1: clear
		R	-	Bit5:TX CE PKT RCVD CLR CE packet received interrupt clear 1: clear
		R	-	Bit6: TX SCLRD PKT SUC CLR Packet sent interrupt clear 1: clear
		R	-	Bit7:TX EXT MON CLR Ext TX Detect interrupt clear 1: clear
0x00C5	TX interrupt clear Byte1	R	-	Bit0:TX CEP TO CLR CEP Timeout interrupt clear 1: clear

Address	Register name	R/W	Default	Description
0x00C5	TX interrupt clear Byte1	R	-	Bit1: TX RPP TO CLR RPP Timeout interrupt clear 1: clear
		R	-	Bit2: TX EPT CLR AC powered down interrupt clear 1: clear
		R	-	Bit3: TX START PING CLR Ping started interrupt clear 1: clear
		R	-	Bit4:TX SS PKT RCVD CLR SS ID packet received interrupt clear 1: clear
		R	-	Bit5:TX ID PKT RCVD CLR ID packet received interrupt clear 1: clear
		R	-	Bit6: TX CFG PKT RCVD CLR Configuration packet received interrupt clear 1: clear
		R	-	Bit7: TX PP PKT RCVD CLR PP packet received interrupt clear 1: clear
0x00C6	TX interrupt clear Byte2	R	-	Bit0: TX BRIDGE MD CLR Bridge mode (half/full) changed interrupt clear 1: clear
		R	-	Bit1: TX FOD DET CLR TX FOD detect interrupt clear 1: clear
		R	-	Bit2:TX PTC UPDATE CLR the power transfer contract is successfully updated after negotiation/renegotiation clear 1: clear
		R	-	Bit 3: TX DTS SUCC CLR DTS send data stream successfully clear 1: clear
		R	-	Bit 4: TX DTS SEND END TO CLR DTS stopped sending due to time out clear 1: clear
		R	-	Bit 5: TX DTS SEND END RST CLR DTS stopped sending due to reset clear 1: clear
		R	-	Bit 6: TX DTS RCVD SUCC CLR DTS received data successfully clear 1: clear
		R	-	Bit7: TX DTS RCVD END TO CLR

Address	Register name	R/W	Default	Description
0x00C6	TX interrupt clear Byte2			DTS stopped receiving due to time out clear 1: clear
0x00C7	TX interrupt clear Byte3			Reserved

Table 14. TX interrupt latch

Address	Register name	R/W	Default	Description
0x00C8	TX interrupt latch Byte 0	R	-	Bit 0: TX OVTP LTCH Over temperature protection latch 1: latch
		R	-	Bit 1: TX OCP LTCH Over current protection latch 1: latch
		R	-	Bit 2:TX OVP LTCH Over voltage protection latch 1: latch
		R	-	Bit 3: TX SYS ERR LTCH System error latch 1: latch
		R	-	Bit4: TX RP PKT RCVD LTCH RP packet received interrupt latch 1: latch
		R	-	Bit5:TX CE PKT RCVD LTCH CE packet received interrupt latch 1: latch
		R	-	Bit6: TX SLTCHD PKT SUC LTCH Packet sent interrupt latch 1: latch
		R	-	Bit7: TX EXT MON LTCH Ext TX Detect interrupt latch 1: latch
0x00C9	TX interrupt latch Byte 1	R	-	Bit0: TX CEP TO LTCH CEP Timeout interrupt latch 1: latch
		R	-	Bit1:TX RPP TO LTCH RPP Timeout interrupt latch 1: latch
		R	-	Bit2: TX EPT LTCH AC Powered down interrupt latch 1: latch
		R	--	Bit3: TX START PING LTCH Ping started interrupt latch 1: latch
		R	-	Bit4: TX SS PKT RCVD LTCH SS ID packet received interrupt latch

Address	Register name	R/W	Default	Description
				1: latch
0x00C9	TX interrupt latch Byte 1	R	-	Bit5: TX ID PKT RCVD LTCH ID packet received interrupt latch 1: latch
		R	-	Bit6: TX CFG PKT RCVD LTCH Configuration packet received interrupt latch 1: latch
		R	-	Bit7: TX PP PKT RCVD LTCH PP packet received interrupt latch 1: latch
0x00CA	TX interrupt latch Byte 2	R	-	Bit0: TX BRIDGE MD LTCH Bridge mode (half/full) changed interrupt latch 1: latch
		R	-	Bit1: TX FOD DET LTCH TX FOD detect interrupt latch 1: latch
		R	-	Bit2: TX PPTC UPDATE LTCH The power transfer contract is successfully updated after negotiation/renegotiation 1: latch
		R	-	Bit 3: TX DTS SUCC LTCH DTS Send data stream successfully latch 1: latch
		R	-	Bit 4: TX DTS SEND END TO LTCH DTS stopped sending due to time out latch 1: latch
		R	-	Bit 5: TX DTS SEND END RST LTCH DTS stopped sending due to reset latch 1: latch
		R	-	Bit 6: TX DTS RCVD SUCC LTCH DTS received data successfully latch 1: latch
		R	-	Bit7: TX DTS RCVD END TO LTCH DTS stopped receiving due to time out latch 1: latch
0x00CB	TX interrupt latch Byte 3			Reserved

Table 15. TX Interrupt status

Address	Register name	R/W	Default	Description
0x00CC	TX interrupt status Byte 0	R	-	Bit 0: TX OVTP STAT Over temperature protection status
		R	-	Bit 1: TX OCP STAT

Address	Register name	R/W	Default	Description
0x00CC	TX interrupt status Byte 0			Over current protection status
		R	-	Bit 2: TX OVP STAT Over voltage protection status
		R	-	Bit 3:TX SYS ERR STAT System error status
		R	-	Bit4: TX RP PKT RCVD STAT RP packet received interrupt status
		R	-	Bit5: TX CE PKT RCVD STAT CE packet received interrupt status
		R	-	Bit6: TX SSTATD PKT SUC STAT Packet sent interrupt status
		R	-	Bit7:TX EXT MON STAT Ext TX Detect interrupt status
0x00CD	TX interrupt status Byte 1	R	-	Bit0: TX CEP TO STAT CEP Timeout interrupt status
		R	-	Bit1:TX RPP TO STAT RPP Timeout interrupt status
		R	-	Bit2: TX EPT STAT AC powered down interrupt status
		R	-	Bit3: TX START PING STAT Ping started interrupt status
		R	-	Bit4:TX SS PKT RCVD STAT SS ID packet received interrupt status
		R	-	Bit5:TX ID PKT RCVD STAT ID packet received interrupt status
		R	-	Bit6:TX CFG PKT RCVD STAT Configuration packet received interrupt status
		R	-	Bit7: TX PP PKT RCVD STAT PP packet received interrupt status
0x00CE	TX interrupt status Byte 2	R	-	Bit0: TX BRIDGE MD STAT Bridge mode (half/full) changed interrupt status
		R	-	Bit1:TX FOD DET STAT TX FOD detect interrupt status
		R	-	Bit2: TX PTC UPDATE STAT The power transfer contract is successfully updated after negotiation/renegotiation
		R	-	Bit 3: TX DTS SUCC STAT DTS Send data stream successfully status
		R	-	Bit 4: TX DTS SEND END TO STAT DTS stopped sending due to time out status
		R	-	Bit 5: TX DTS SEND END RST STAT DTS stopped sending due to reset status

Address	Register name	R/W	Default	Description
0x00CE	TX interrupt status Byte 2	R	-	Bit 6: TX DTS RCVD SUCC STAT DTS received data successfully status
		R	-	Bit7: TX DTS RCVD END TO STAT DTS stopped receiving due to time out status
0x00CF	TX interrupt status Byte 3			Reserved

The status bits are updated at run time and they are temporarily set when corresponding interrupt event occurs.

Table 16. TX Configuration

Address	Register name	R/W	Default	Description
0x00D2	TX configuration	RW	0x2422 (148kHz)	Bits [7…0] : TX FREQ MAX Max frequency specified in units of 16Hz
0x00D3				Bits [15..8]
0x00D4		RW	0x1ADB (110kHz)	Bits [7…0] :TX FREQ MIN Min frequency specified in units of 16Hz
0x00D5				Bits [15…8]
0x00D6		RW	0x23A5 (146kHz)	Bits [7…0] : TX FREQ PING Ping frequency specified in units of 16Hz
0x00D7				Bits [15…8]
0x00D8		RW	0x32 (50%)	Bits [7…0] : TX DC MAX Max TX duty cycle %. Max value is 50. Must be >= TX_MIN_DC
0x00D9		RW	0x14 (10%)	Bits [7…0] : TX DC MIN Min TX duty cycle %. Must be <= TX_MAX_DC In full bridge mode the set value is 2 times the duty cycle.
0x00DA		RW	0x32 (50%)	Bits [7…0] :TX DC PING Ping duty cycle in percentage
0x00DB		RW	0xC8 (2000 ms)	Bits [7…0]:TX PING INTERVAL Interval between ping (in 10ms)
0x00DC		RW	0x50 (80 ms)	Bits [7…0] : TX PING DURATION TX ping duration in ms.
0x00DD		RW	0x28 (20V)	Bits[7..0] : TX OVP THR TX OVP threshold in 500mV units.
0x00DE		RW	0x14 (2A)	Bits[7..0] : TX OCP THR TX OCP current in 100mA units.
0x00DF		RW	0x64 (100 C)	Bits[7..0]: TX OVTP THR Over temperature protection threshold in degree C.
0x00E0		RW	0x03(96mW)	Bits [7…0]: TX PLOSS FOD THR TX PLOSS FOD detection threshold in 32mW units. 0 - Disable 1 - 32mW … 255 - 8160mW .
0x00E1		RW	0x04	Bits [7…0] :TX FOD DBNC CNT Continuous PLOSS based RP de bounce count before FOD EPT. 0 - EPT immediately.

Address	Register name	R/W	Default	Description
0x00E2	TX configuration	RW	0x03	Bits [7…0] :TX CE TO MAX Max count TX retries with different frequency after failing to listen to CE packet within time frame.
0x00E3		RW	0x0F(1920Hz)	Bits [7…0] : TX FHOP Define the step size (in Hz) for every frequency hop. Internally it is multiplied with 128 1: 128Hz step size 2: 256Hz step size 3: 384Hz step size ….
0x00E4		RW	0x00	Bits [7…0]:TX PID MAX CURR TX max current for PID control target in units of 16mA. 0 - not limited 1 - 16mA ... 255 - 4080mA

Table 17. TX EPT reason

Address	Register name	R/W	Default	Description
0x00E6	TX EPT reason Byte 0	R	-	Bit 0:TX OVP over voltage triggered
		R	-	Bit 1: TX OCP over current protection triggered
		R	-	Bit 2: TX OVTP over temperature protection triggered
		R	-	Bit 3: TX FOD Foreign object detected
		R	-	Bit4: TX HOST Host issued EPT command
		R	-	Bit5: TX RX EPT EPT Source Rx EPT packet
		R	-	Bit6: TX CEP TO Control error packet timeout
		R	-	Bit7: TX RPP TO Received power packet timeout
0x00E7	TX EPT reason Byte 1	R	-	Bit0: TX RX RST Rx send SS/ID/CFG at wrong time , probably because of RX RESET
		R	-	Bit1:TX SYS ERR System error
		R	-	Bit2: TX SS TO Signal strength timeout , Ping time out.
		R	-	Bit3: TX SS ERR Signal strength packet error
		R	-	Bit4: TX ID ERR Identification packet error
		R	-	Bit 5: TX CFG

Address	Register name	R/W	Default	Description
0x00E7	TX EPT reason Byte 1			Error in configuration packet
		R	-	Bit 6: TX CFG CNT Number optional packets received doesn't match with number in configuration packet
		R	-	Bit 7: TX PCH ERR Power control hold-off packet error
0x00E8	TX EPT reason Byte 2	R	-	Bit 0: TX XID ERR Extended identification packet error
		R	-	Bit 0 : TX NEG ERR Negotiation error
		R	-	Bit1: TX NEGO TO Negotiation Time out
				Bits[2..7] Reserved

Table 18. TX protections

Address	Register name	R/W	Default	Description
0x00DD	TX OVP THRES	RW	0x28 (20V)	Bit [7…0] Specify TX OVP threshold in 500mV units.
0x00DE	TX OCP THRES	RW	0x14 (2A)	Bit [7…0] Specify TX OCP current in 100mA units.0 - Disable1 - 100mA…
0x00DF	TX OVTP THRES	RW	0x64(100°C)	Bit [7 …0] Over temperature protection threshold in °C. If transmitter die temperature rises above this value, then OTP triggered.

8 Application information

This chapter is aimed to provide some application hints such as a reference schematic, PCB layout guidelines, minimum components to properly run an application and other aspects.

8.1 Reference application

A typical STWBC86 application schematic is shown below.

Typical component values for a power transmitter capable of 5W output power are listed in the tables below.

Figure 11. STWBC86 basic application diagram

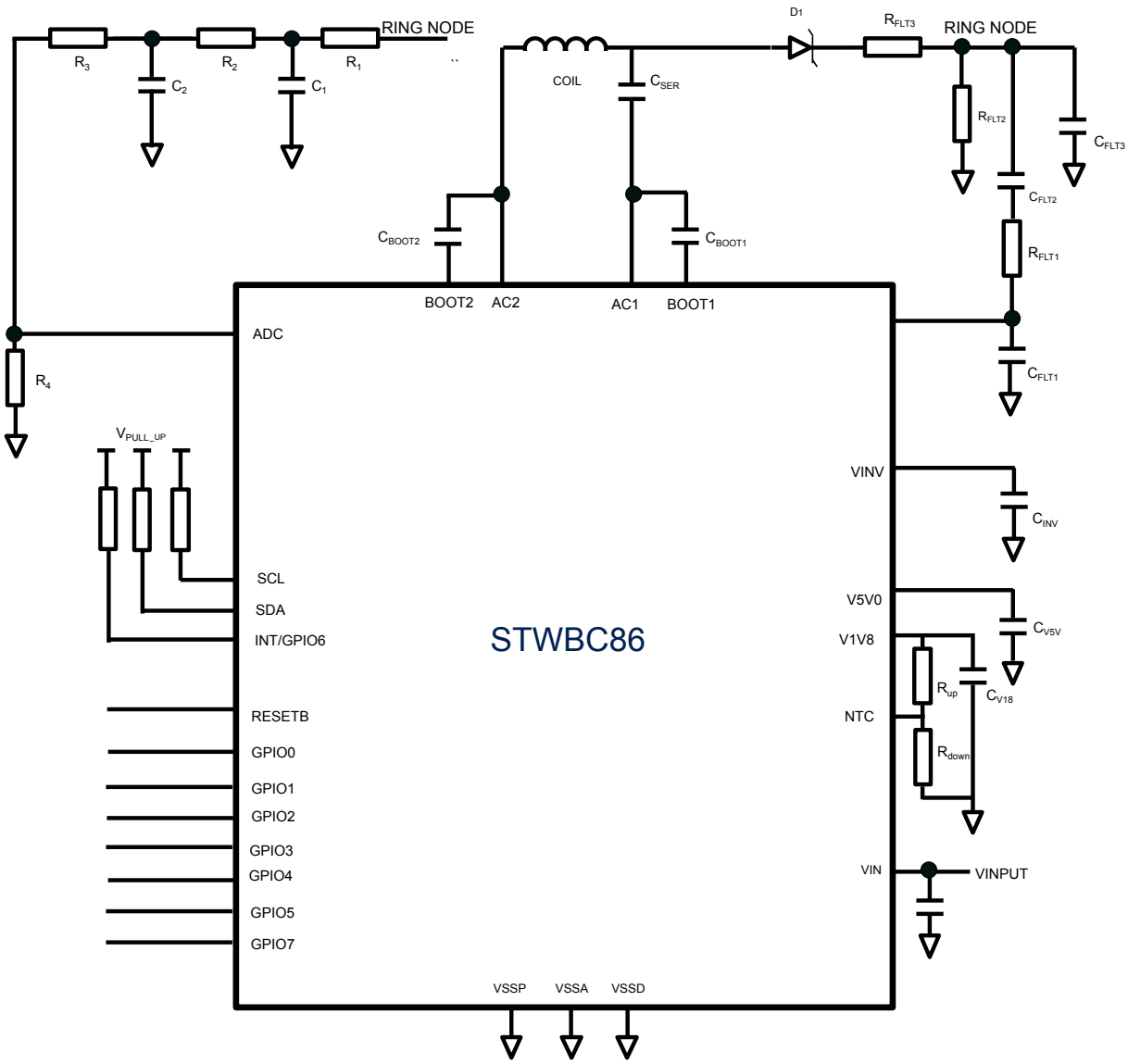


Table 19. Typical components list for a 5 W Tx application

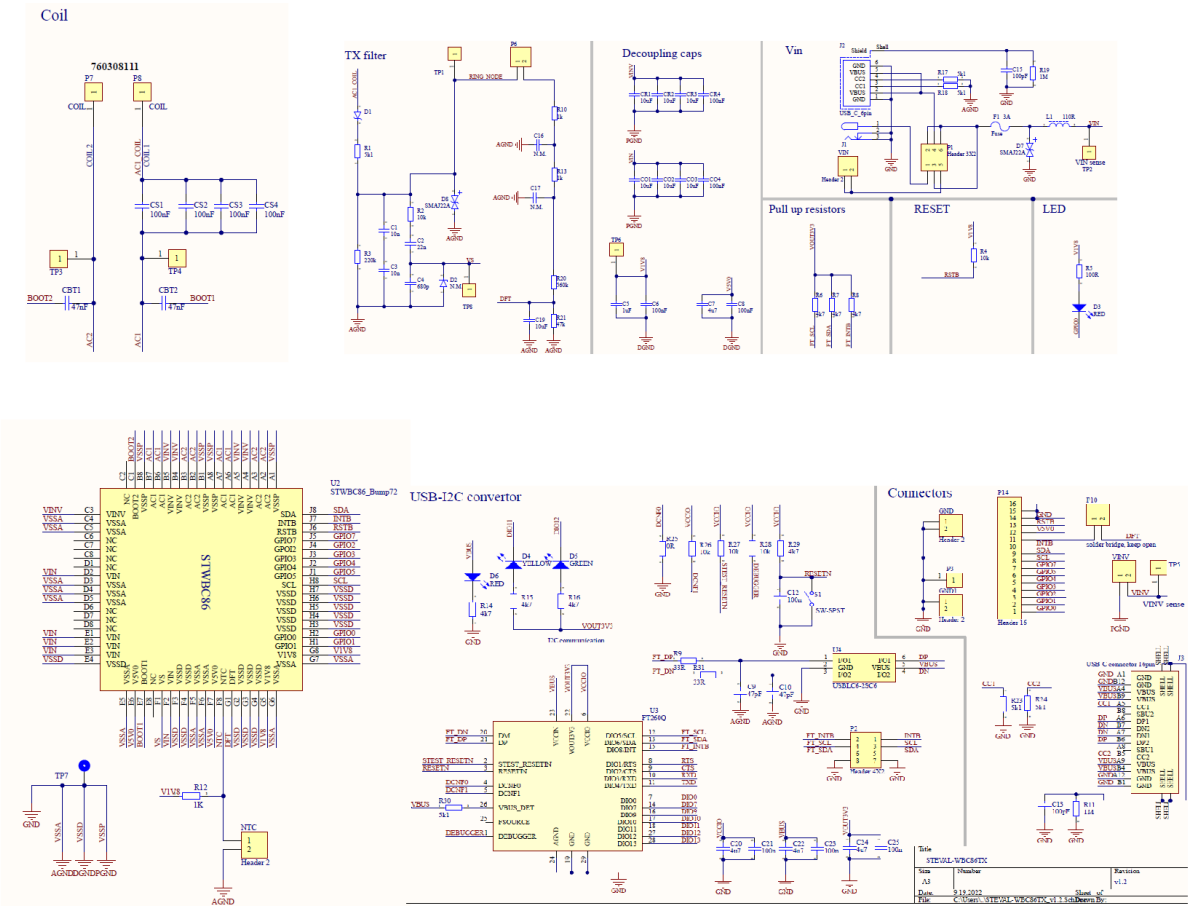
Component	Value	Manufacturer	Part Number	Notes
L1	6.3µH	Wurth	760308111	Primary coil

Component	Value	Manufacturer	Part Number	Notes
CSER	100nF/50V		4x GRM31C5C1H104JA01L	Series resonant capacitor
CBOOT1, CBOOT2	47nF/50V	Murata	GRM155R61H473JA01D	Boot strap capacitor
CV5V0	4.7uF/50V	Murata	GRM155R61A475KE15	V5V0 filtering capacitor
CV18	1µF/25V	Murata	GRM155R61E105KE11D	V1V8 filtering capacitor
CINV	10µF/25V	Murata	3x GRM188R61E106MA73D	VINV filter capacitor, rating depending on application
CIN	10µF/25V	Murata	2x GRM188R61E106MA73D	INPUT filter capacitor, rating depending on application
Z1,2	TVS	Littlefuse	SMAJ22CA	TVS protection diodes
RHS,RNTC	30K,100K			Optional
RFLT1,2,3			5K1,220K,10K	ASK demod filter resistors
D1		Rohm	1N4448HLP	ASK demod circuit
CFLT1,2,3			2x10nF,22nF,680pF	ASK demod filter capacitors
R1,R2,R3,R4			10K,10K,560K,47K	Ring node detection circuit
C1,C2			-	Ring node detection circuit

Note: All of the components listed above refer to a typical application. Operation in the application may be limited by a choice of these external components (voltage ratings, current and power dissipation capability, etc.)

8.2 Reference schematic

A typical schematic of STWBC86 in a 5W BPP application is shown below.



8.3 PCB routing guidelines

1. Auxiliary 1V8 and 5V0 LDO filtering capacitors should be placed as close to the STWBC86 as possible. Connection traces should be short and placed in top layer. Capacitors connected directly to a GND plane.
2. Power ground(VSSP) will carry the sum of ripple current from VINV/CINV and DC current from VIN, return paths from LDO caps should avoid these high currents.
3. C_{INV} and C_{IN} capacitors should be placed close to STWBC86.
4. Power traces (AC1, AC2, VINV, VIN) should be kept wide enough to a sustain high current. Duplicating these traces in inner layers is advisable wherever possible.
5. AC1 and AC2 tracks should be routed close to each other to minimize the area of the resulting loop.
6. Communication signals (I2C), Sensing and Input monitoring signals to be routed away from High di/dt (AC1,AC2)switching signals , to Minimize interference.
7. Thermal performance and grounding should be always optimized by preserving bottom layer (usually assigned to ground) integrity.

8.4 External components selection

TX series resonant circuit components

The series capacitance Cser is an essential part of the series resonant circuit, therefore, it should show an excellent quality factor, relatively high RMS current capability and superior capacitance stability in the frequency range of interest.

Capacitance tolerance and stability strongly depend on the dielectric type used. COG type capacitors are recommended for their stable performance across various temperatures and voltage levels.

ESD protection diodes

Since the transmitting coil is a easy entry point for ESD (relatively large area with remarkable capacitive coupling),a good application design should consider protections for the most exposed pins: AC1 and AC2.

Uni-directional Transient Voltage Suppression (TVS) diodes at both pins are recommended.

ESDs have essentially a common mode nature and, although the receiving coil has low DC-resistance, its AC impedance may appear quite high to fast voltage spikes: independent clamping at AC1 and AC2 pins is thus mandatory.

The knee-voltage of the TVS diodes should be selected considering the maximum VINV voltage plus some margin to avoid non-negligible leakage current at higher temperature, while their energy dissipation capability should be maximized considering the size of the package.

9 Glossary

- ASK: Amplitude Shift Keying
- BPP : Baseline Power Profile
- CEP: Control Error Packets
- EPP: Extended Power Profile
- EPT: End Power Transfer
- FOD : Foreign Object Detection
- FSK: Frequency Shift Keying
- ID: Identification
- PP: Proprietary Packet
- RPP: Received Power Packet
- SS : Signal Strength Packet
- XID : Extended Identification

10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 WLCSP72 package information

Figure 12. **WLCSP72 3.264x3.674x0.6 0.4 Pitch 0.25 Ball package outline**

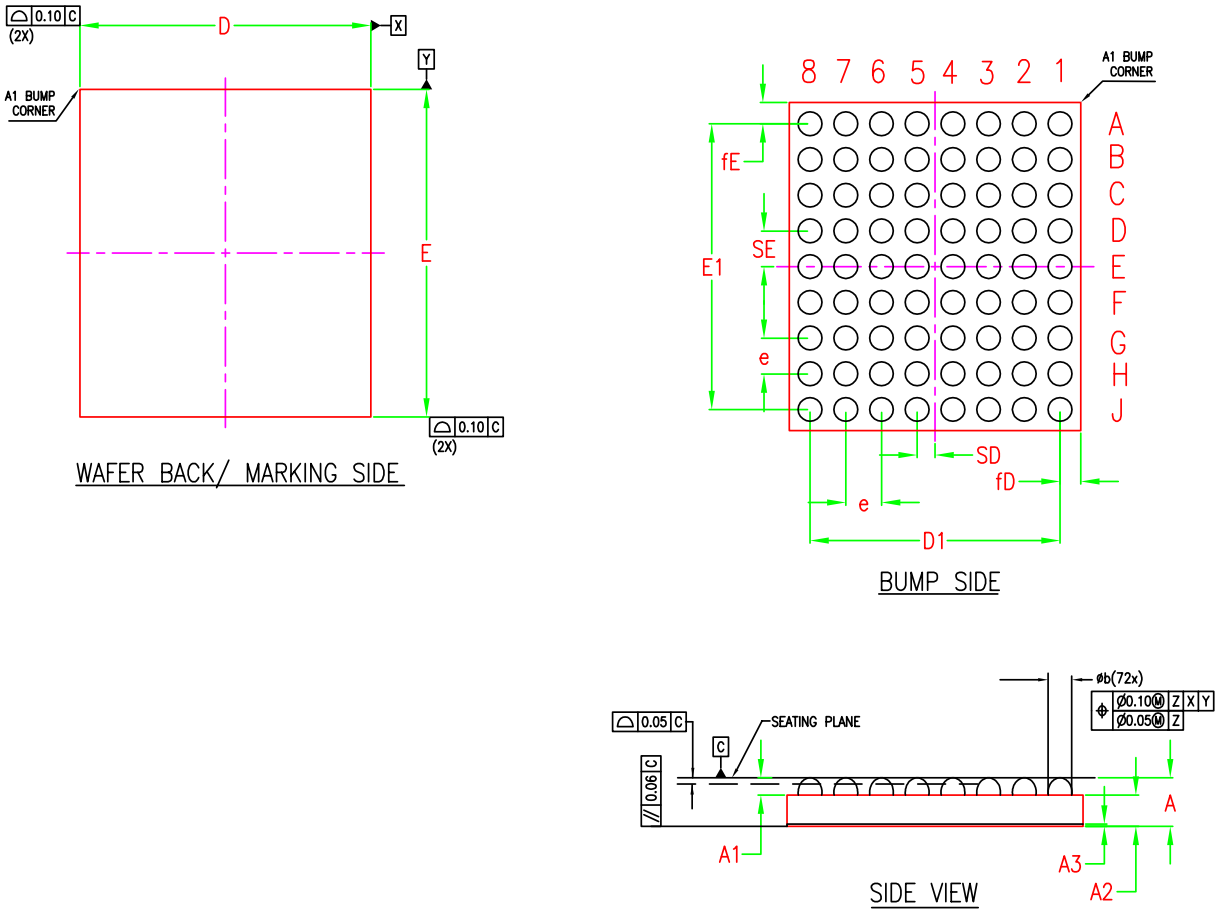


Table 20. **WLCSP72 3.264x3.674x0.6 0.4 Pitch 0.25 Ball mechanical data**

Ref	Data range (mm)		
	Min	Typ	Max
A	0.522	0.548	0.574
A1	0.182	0.198	0.214
A2	0.33	0.35	0.37
A3	-	-	-
b	0.245	0.270	0.295
D	3.244	3.264	3.284
D1		2.80	
E	3.653	3.673	3.693
E1		3.20	
e		0.400	
SE		0.400	
SD		0.200	
fD		0.232	
fE		0.237	
ccc		0.03	

Figure 13. **Recommended footprint**

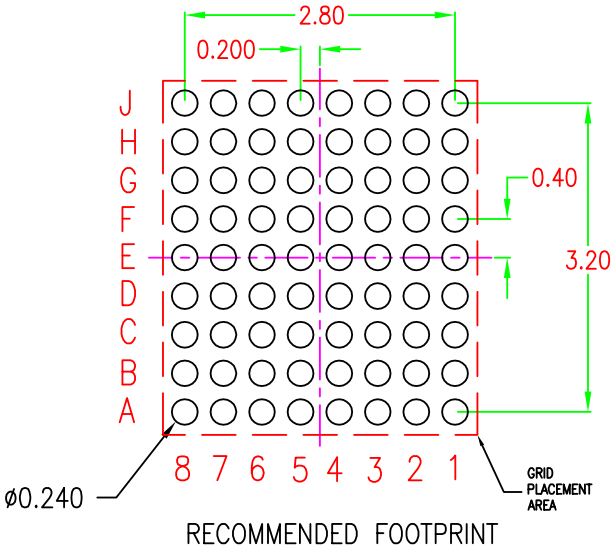
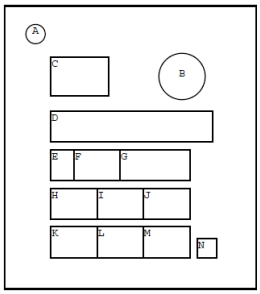


Figure 14. **Tape and Reel information**

PACKAGE FACE : TOP



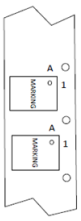
LEGEND

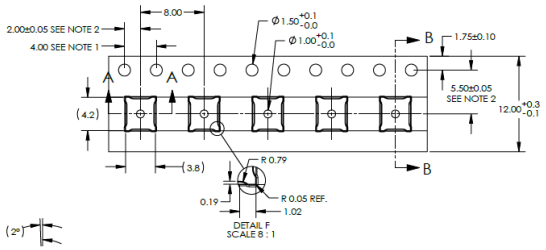
Unmarkable Surface

Marking Composition Field

A - 96349 - STRIPE (PIN 1 IDENT)
B - 96350 - Second_lvl_intct
C - 96337 - STANDARD ST LOGO
(0000093)
D - 96348 - MARKING AREA
E - 96347 - Assy Year
(Y)
F - 96346 - Assy Week
(WW)

Carrier Tape Top View





Revision history

Table 21. **Document revision history**

Date	Version	Changes
20-Sept-2022	1	Initial release.

Contents

List of tables

List of figures