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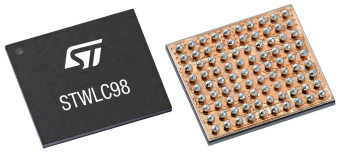
STWLC98

Datasheet

Qi-compliant inductive wireless power receiver for 70W applications



Product status link
STWLC98

Product summary	
Order code	STWLC98JR
Package	WLCSP90
Packing	Tape and reel

Features

- Up to 70W output power
- Up to 15W output power in Tx mode
- Qi 1.3 compliant
- Integrated 27 V synchronous rectifier with ≥ 98% efficiency
- ARC(Adaptive Rectifier Configuration) mode for enhanced spatial freedom
- Low drop-out linear regulator with output current and input voltage loops
- Programmable output voltage up to 20V
- 32bit, 64MHz ARM®Cortex® M3 core with 16KB FTP, 16KB RAM,80KB ROM
- 10-bit A/D converter
- 6 configurable GPIOs
- I^2C Slave, Master interface
- 8-levels ASK modulator, enhanced FSK demodulator
- Foreign Object Detection (FOD)
- Coil Q-factor measurement for FOD in Tx mode
- Over voltage, over current and thermal protection
- Flip chip 90 bumps (4.3 mm x 3.9 mm)

Application

- Smartphones,tablets, laptops
- Power banks,cordless power tools
- Medical devices

Description

The STWLC98 is a highly integrated wireless power receiver suitable for applications delivering an output power up to 70W.The chip has been designed to support Qi 1.3 specifications for inductive communication protocol with extended power profile (EPP) and proprietary ST Super Charge(STSC) protocol for fast charging.

With integrated low-loss synchronous rectifier and low drop-out linear regulator, STWLC98 achieves high efficiency with low power dissipation.

Through I^2C interface the user can access and modify the configuration parameters for customized applications. The final configuration parameters are stored in embedded Few Times Programmable(FTP) non-volatile memory and automatically retrieved at power-up.

The device can also operate as a wireless transmitter, capable of transmitting up to 15W of power (depending on the coil used)

Chip-Scale Package and low bill of materials (BOM) count make it very suitable for compact applications.

1 Introduction

The STWLC98 is primarily wireless power receiver, but it can also reverse its operation and act as a wireless power transmitter in the same application.

When configured as wireless power receiver (Rx mode), it rectifies the AC voltage induced across the receiving coil and provides a regulated DC voltage at the output.

The 32-bit core MCU is the supervisor of the whole device and manages all the functional blocks to

- establish and maintain communication with the transmitter,
- ensure adherence to Qi standard specifications (where necessary),
- optimize the efficiency by properly adjusting the operating point
- guarantee reliability by monitoring and protecting both the load and the device itself.

In order to execute the above mentioned (and many others) tasks, the MCU core relies on a resident firmware stored in ROM . In addition, some configuration parameters (e.g. output voltage, FOD tuning parameters, etc.) can be saved in the internal Few Times Programmable memory (FTP) and retrieved at power-up, allowing the STWLC98 to operate as a fully autonomous stand-alone chip.

For applications in which the host system directly monitors or controls the power transfer, the I^2C interface provides access to the internal registers of the STWLC98.

The device is also equipped with

- Six programmable general-purpose I/O pins (GPIOs) to implement specific functions (e.g. driving status LEDs, enabling the output on request, informing the host system about faulty conditions, etc.),
- Analog inputs to monitor voltages and signals (for example, the temperature of the coil),
- Master I²C interface to manage external devices.

Figure below shows the block diagram of the device with simplified interconnections among the functional blocks. The synchronous rectifier converts the AC voltage from the receiving coil into a DC voltage at the VRECT pin. The four switches of the rectifier (that is basically an H-bridge) are controlled by the digital core, to minimize both conduction and switching losses as a function of the output voltage and current, both monitored by ADC channels. Two bootstrap capacitors are externally connected to the BOOT1-BOOT2 pins to correctly drive the high-side switches of the rectifier.

The output of the rectifier, filtered by an external capacitor, is also the input rail for the main LDO linear regulator and for the auxiliary linear regulators in charge of deriving the 5V,1.8V,1.2V supply voltages.

The digital core has full control of the main LDO linear regulator in order to manage the output voltage, the output current, and the dropout voltage.

The minimization of the dropout voltage requires a closed loop regulation of the voltage at the VRECT pin, i.e. a feedback information that is sent to the transmitter (via ASK modulation) which, in turn, adjusts the delivered power by acting on the supply voltage, the switching frequency or the switching duty-cycle (or a combination of the three) of its own power stage, depending on the chosen method.

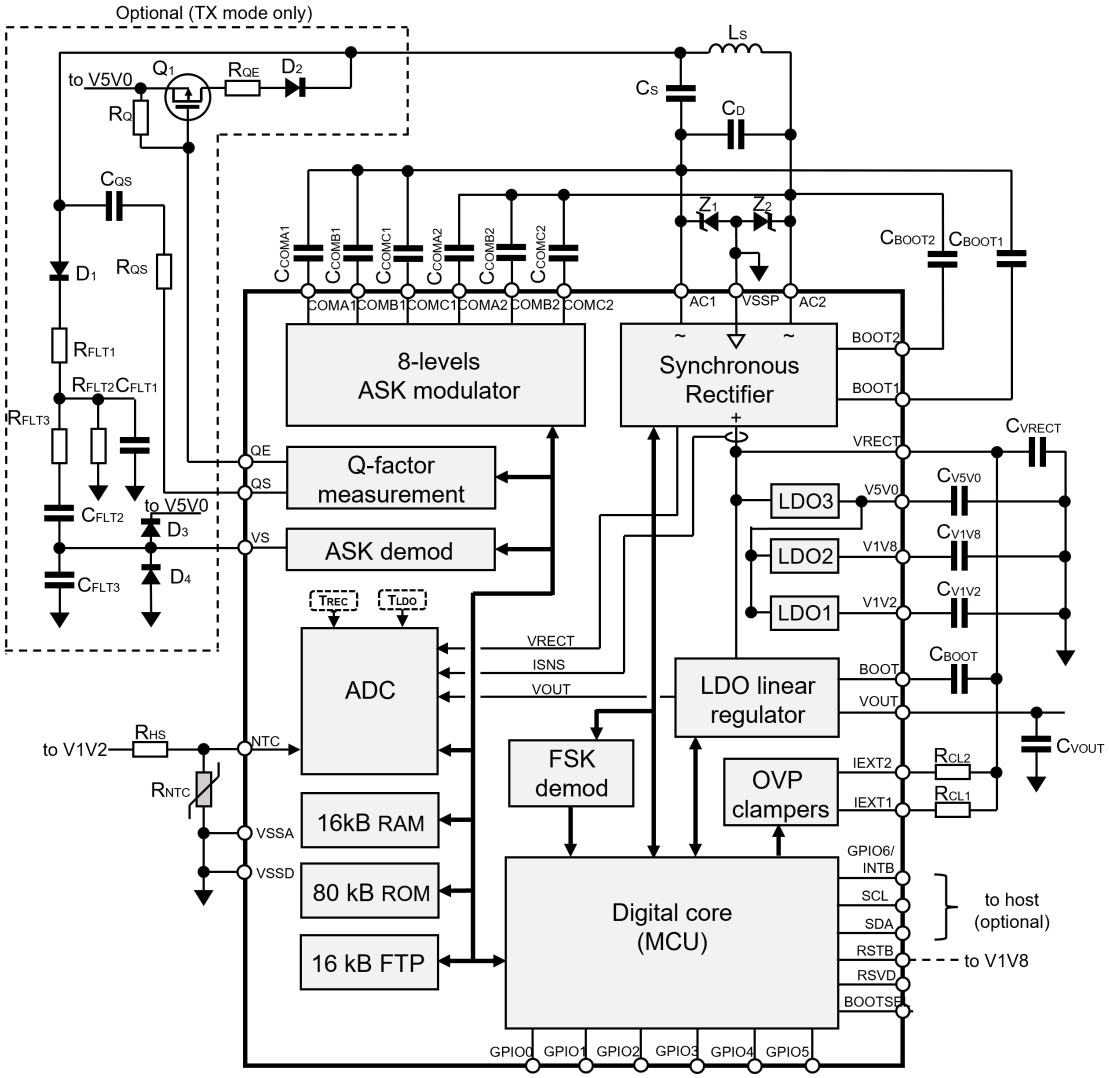
This regulation loop involving the transmitter is an essential part of the wireless power transmission and is extensively described in Qi specifications.

The STWLC98 is equipped with an enhanced and robust FSK/ASK communication circuit.

Regarding the safety precautions for the user, the STWLC98 provides over-temperature protection (OTP) and two programmable, independent over-voltage protection (OVP) mechanisms.

STWLC98 is also capable to function as a transmitter to provide power up to 15W, depending on the characteristics of the coil. In this operating mode, a dedicated Q-factor measurement circuit is used to determine the quality factor of the coil for accurate foreign object detection (FOD) prior to initiating a power transfer negotiation.

2 Typical application diagram



3 Device pin out

Figure 1. **Pin assignment (through top view)**

Table 1. **Pin description**

Pin name	Pin location	Pin function
VSSA	C5, C6, D5, D6, E6, F6, F7, G7, G8	Analog ground. Power return for the main LDO and the analog circuitry.
VSSD	E5,F4, F5, F10, G3, G4, G5, H4, H5, H6, H8, J1	Digital ground. Reference for digital input and output signals.
VSSP	A2, A9, B1, B2, B9, B10, C1, C10	Power ground. Power return for the synchronous rectifier.
AC1	A7, A8, A10, B7, B8	AC power input: input of the synchronous rectifier. Connect to Rx series resonant circuit.
AC2	A1, A3, A4, B3, B4	AC power input: input of the synchronous rectifier. Connect to Rx series resonant circuit.
BOOT1	E8	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC1.
BOOT2	C2	Synchronous rectifier bootstrap capacitor connection: a 47 nF (typ.) ceramic capacitor is connected between this pin and AC2.
BOOT	E9	Main LDO power transistor bootstrap capacitor. Connect a 4.7 nF (typ.) ceramic capacitor between this pin and VRECT.
COMA1	D9	Modulation switches connection: capacitors between COMA1 and AC1 pin and between COMA2 and AC2 pin are used to implement ASK modulation.
COMA2	D8	
COMB1	C9	Auxiliary modulation switches connection: the two COMB1-COMB2 and COMC1-COMC2 pairs are dynamically managed, in conjunction with COMA1-COMA2 pair, to modify the ASK modulation index in specific operating conditions. Two sets of capacitors are connected between these pins and AC1-AC2 (similarly to COMA1 and COMA2 pins, see reference schematic).
COMB2	C8	
COMC1	D10	
COMC2	E10	
VRECT	A5, A6, B5, B6, C4, C7, D4, D7	Synchronous rectifier output and input for the main LDO linear regulator. A suitable capacitor between these pins and VSSP ensures residual AC ripple filtering and energy storage for proper load transient response.

Pin name	Pin location	Pin function
VOUT	E1, E2, E3, E4, F1, F3	Main LDO linear regulator power output. Connect a suitable filter capacitor between these pins and VSSA to ensure stable operation and proper load transient response in all operating conditions.
V1V2	G6, G9, G10	1.2 V LDO output and supply rail for the digital core. Connect a 1 µF (typ.) filtering capacitor between this rail and ground (VSSD).
V1V8	J10	1.8 V LDO output and supply rail for the ADC and the analog circuitry. Connect a 1 µF (typ.) filtering capacitor between this pin and ground (VSSA).
V5V0	E7, F8	5V LDO output and supply rail for the auxiliary circuitry. Connect a 4.7 µF (typ.) filtering capacitor between this pin and ground (VSSA).
RSVD	H7	Reserved , this pin is to be **left floating**
BOOTSEL	J6	Boot-up memory selector, this pin is to be **left floating**
VS	F2	ASK de-modulation input.
IEXT1	C3	Internal pull-down switches for active (dissipative) two-levels over-voltage clamper: a resistor with adequate power dissipation capability must be connected between each pin and VRECT to damp excessive voltage developing at the output of the rectifier.
IEXT2	D2	
QE	H1	Coil quality-factor measurement, excitation output. This pin is used to drive an external transistor to inject excitation pulses into the resonant circuit. Used in conjunction with QS pin to measure the quality factor of the coil.
QS	D1	Coil quality-factor measurement, sensing input. This pin is used to sense the ringing developing across the resonant circuit after an excitation pulse is applied via QE pin.
NTC	F9	Coil temperature sensing input: this pin is connected to the center tap of a resistor divider having an NTC in the low-side position. If this function is not used, the pin must be pulled-up to V1V2 through a 10 kΩ resistor to prevent triggering the coil over-temperature protection.
RSTB	J7	Chip-reset input. If set low, the internal digital core is reset. This pin is eventually used by the host controller to control the power transfer process. Connect to V1V8 pin if not used.
SCL	H9	I^2C bus, clock line input. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels.
SDA	J9	I^2C bus, data line I/O. A pull-up resistor to the supply rail of the host controller is required to ensure correct digital levels.
RSVD	D3	Reserved: No connection, this pin must be **left floating**.
GPIO0	H3	Programmable general-purpose I/Os: the function of these pins depends on the configuration of the device.
GPIO1	H2	
GPIO2	J5	
GPIO3	J4	
GPIO4	J3	
GPIO5	J2	
INTB	J8	Interrupt output (active low). Programmable open-drain output used to generate an interrupt on specific events for the host controller. Also used as auxiliary control signal during flash.
ADCIN1	G2	Analog inputs. These pins can be used to monitor external signals. The maximum voltage at these pins cannot exceed 1.8 V.
ADCIN2	G1	
ADCIN3	H10	

4 Electrical and thermal specifications

4.1 Absolute maximum ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in Table 2 is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Parameter	Pin(s)	Min.	Max.	Unit
Pin voltage range	AC1, AC2, COMA1, COMA2, COMB1,COMB2,COMC1 and COMC2 respect to ground (VSSA, VSSD and VSSP pins)	-0.9	31.5	V
	BOOT1 to AC1	-0.3	6.5	
	BOOT2 to AC2			
	BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins)	-0.3	35	
	BOOT respect to VRECT	-0.3	6.5	
	VRECT, VOUT and IEXT1,IEXT2 and QS respect to ground (VSSA, VSSD and VSSP pins)	-0.3	31.5	
	V1V8, GPIO0 through GPIO5,INTB,RSTB,SDA,SCL and BOOTSEL respect to ground (VSSA, VSSD and VSSP pins) if V5V0 >4V	-0.3	2.4	
	V5V0, VS, QE respect to ground (VSSA, VSSD and VSSP pins)	-0.7	5.5	
	Relative voltage between any ground pin (VSSA, VSSD, VSSP)	-0.3	0.3	
RMS pin current	AC1,AC2		4	A
	VRECT,VOUT		3.5	
	COMA1,COMA2,COMB1,COMB2,COMC1,COMC2		0.6	
	IEXT1,IEXT2		0.5	
HBM ESD susceptibility JEDEC JS001-2012	All pins		2000	V
CDM ESD susceptibility JEDEC JS002-2012			500	
Latch-Up EIA/JESD78E			200	mA

4.2 Maximum Operating Voltages

Table 3. Maximum Operating Voltage

Parameter	Pin(s)	Min.	Max.	Unit
Pin voltage range	AC1, AC2, COMA1, COMA2, COMB1,COMB2,COMC1 and COMC2 respect to ground (VSSA, VSSD and VSSP pins)	-0.9	27	V
	BOOT1 to AC1	-0.3	5	
	BOOT2 to AC2			
	BOOT1 and BOOT2 respect to ground (VSSA, VSSD and VSSP pins)	-0.3	32	
	BOOT respect to VRECT	-0.3	5	
	VRECT, VOUT and IEXT1,IEXT2 and QS respect to ground (VSSA, VSSD and VSSP pins)	-0.3	27	
	V1V8, GPIO0 through GPIO5,INTB,RSTB,SDA,SCL and BOOTSEL respect to ground (VSSA, VSSD and VSSP pins) if V5V0 >4V	-0.3	1.98	
	V5V0, VS, QE respect to ground (VSSA, VSSD and VSSP pins)	-0.7	5.25	
	Relative voltage between any ground pin (VSSA, VSSD, VSSP)	-0.3	0.3	

4.3 Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{A,OP}$(1)	Operating ambient temperature		-40		85	°C
$T_{J,OP}$	Operating junction temperature		0		125	
$R_{\Theta JA}$(2)	Junction to ambient thermal resistance	2s2p		47		°C/W
T_{SHDN}	Thermal shutdown threshold	Default Programmable 105,115,125,135		115		°C
$T_{SHDN,HYST}$	Thermal shutdown hysteresis			10		

1. *Ta -40°C to 85°C , limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization,if not otherwise specified.*
2. *Device mounted on a standard JESD51-5 test board*

4.4 Electrical characteristics

0 °C < T_A < 85 °C; V_{VRECT} = 5 V to 10 V. Typical values are at T_J = 25 °C, if not otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply section						
$V_{VRECT,UVLO}$	VRECT Under-Voltage Lock-Out upper (turn-on) threshold	VRECT pin voltage, rising edge in RX mode		3.0	3.3	V
$V_{VOUT,UVLO}$	VOUT Under-Voltage Lock-Out upper (turn-on) threshold	VOUT pin voltage, rising edge in TX mode		3.0	3.3	
$V_{VRECT,MAX}$	VRECT maximum operating supply voltage	Voltage on VRECT pin		27		V
$I_{VOUT,Q}$	VOUT current consumption in shut-down mode	RSTB low for more than 1 ms, supply voltage (5 V) applied to VOUT		1.2		mA
$I_{VRECT,OP}$	Operating current consumption (not considering the programmed dummy-load current)	RSTB high, supply voltage applied to VRECT		12		mA
$I_{VOUT,OP}$		RSTB high, supply voltage applied to VOUT		12		
I_{DMYL}	Dummy load current (internally drawn from VRECT when enabled)	V_{VRECT} = 5 V to 20 V		50		
1.2V supply voltage LDO linear regulator						
V_{V1V2}	LDO1 output voltage	I_{V1V2} = 5 mA	1.08	1.2	1.32	V
1.8V supply voltage LDO linear regulator						
V_{V1V8}	LDO2 output voltage	I_{V1V8} = 5 mA	1.71	1.8	1.89	V
5V supply voltage LDO linear regulator						
V_{V5V0}	LDO3 output voltage	I_{V5V0} = 5 mA	4.8	5	5.2	V
	LDO3 load regulation	0 mA <I_{V5V0} = 0 mA <10 mA		2	20	mV
	LDO3 under-voltage lock-out upper threshold		2.8	3	3.2	V
$I_{V5V0,EXT}$	Maximum current allowed for external load				10	mA
Synchronous rectifier						
$f_{AC\ RX}$	Synchronous rectifier operating frequency range		50		400	KHz
Efficiency	Target rectifier efficiency	I_{VRECT} = 1 A, V_{VRECT}= 5.2 V, f_{AC} = 100 kHz to 200 kHz		94		%
		I_{VRECT} = 1 A, V_{VRECT} = 20 V, f_{AC} = 100 kHz to 200 kHz		98		
$f_{AC\ TX}$	Inverter operating frequency range		100		400	KHz
ASK modulator						
$R_{DSON,COMMx}$	COMA1,COMA2,COMB1,COMB2,COMC1,COMC2modulation switches on-resistance	V_{VRECT} = 5 V		1	2	Ω
$I_{COMxx\ MAX}$	COMA1,COMA2,COMB1,COMB2,COMC1,COMC2 modulation switches current capability	RMS value		0.25		A
Main LDO linear regulator						
VOUT	Output voltage range	VOUT_SET = 0x00C8	4.90	5.0	5.10	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
VOUT	Output voltage range	VOUT_SET = 0x0320	19.9	20	20.1	V
	VOUT Line regulation	I_{VOUT} = 0.1 A, VOUT = 5 V, 6 V < V_{VRECT} < 15 V		3	15	mV
	VOUT Load regulation	V_{VRECT} = 5.5 V, VOUT = 5 V, 1 mA < I_{VOUT} < 800mA		30	70	mV
V_{OUT_STEP}	Programmable step size			25		mV
V_{DROP}	Linear regulator drop-out voltage	I_{OUT} = 1 A		100	200	mV
TX Mode						
VIN-Tx	VOUT input operating voltage in Tx mode		4.95		20	V
Thermal protection (external NTC)						
$V_{NTC,OTP}$	External over-temperature NTC pin upper threshold		0.55	0.59	0.65	V
	External over-temperature NTC pin hysteresis		50	125	150	mV
$I_{NTC,BIAS}$	NTC pin bias current	V_{NTC} = 1.5 V		1	2	µA
Over-Voltage Protection						
V_{OVPH}	Hard OVP (AC1-AC2 short to VSSP) upper threshold	Default: 26V Programmable 26.5V,26V,25.5V,25V		26		V
	Hard OVP release voltage	Default:19V Programmable 19V,16V,13V,10V		19		
V_{OVPS1}	Soft OVP1 (IEXT1 clamper intervention) upper threshold at VRECT	Default: 23V Programmable 24V,23.5V,23V,22.5V		23		V
V_{OVPS2}	Soft OVP2 (IEXT2 clamper intervention) upper threshold at VRECT	Default: 24.5V Programmable 25V,24.5V,24V,23.5V		24.5		
V_{OVPSL}	Soft OVP1 and soft OVP2 release threshold at VRECT			$V_{OVPS1-1V}$		
$I_{IEXT,MAX}$	IEXT clamping switch current capability	Non-repetitive 100 ms rectangular pulse			0.3	A
$R_{IEXT,ON}$	IEXT switch on-resistance	I_{IEXT} = 250 mA		1		Ω
Current sensor						
I_{SNS}	Current sensing range	RX mode	0		3.5	A
	Overall absolute accuracy			1	3	%
Digital signals						
V_{IL}	Low level input voltage	VDDE: IO supply voltage 1.8V			0.3*VDDE	V
V_{IH}	High level input voltage	VDDE: IO supply voltage 1.8V	0.7*VDDE			
V_{OH}	GPIOx high level output voltage	Output high, I_{SOURCE} = 3mA VDDE: IO supply voltage 1.8V	VDDE-0.2			
I_{OH}	GPIOx pin current capability	Output high	3			mA
V_{OL}	Low level output voltage	Output low, I_{SINK}=3mA			0.4	V

5 Device description

5.1 Chip reset pin

The RSTB pin, active low, can block the operation of the device by forcing the digital core in reset state. Both rectifier low-side switches are turned-on while high-side switches are turned-off to protect the device.

After releasing the RSTB pin, the STWLC98 re-starts and retrieves the default configuration data from the FTP.

If not used, the RSTB pin should be connected to the V1V8.

5.2 Synchronous rectifier

The synchronous rectifier of the STWLC98 is a key block in charge of converting the AC input power from the receiving coil into a DC supply rail for the following linear regulator.

In principle it consists of four N-channel MOSFETs arranged in a H-bridge, conveniently driven by a control block that monitors the voltage at the AC1 and AC2 pins to optimize the commutations and to charge the external bootstrap capacitors for the high-side switches.

When designing the filtering capacitor at the output of the synchronous rectifier, it must be taken into account that it has to minimize the AC residual ripple and to provide energy storage to sustain load transients, without impacting on the ASK communication with the transmitter.

5.3 Main linear regulator

The main linear regulator of the STWLC98 ensures a constant output voltage with minimum power loss. Excellent line and load regulation is demanded of the analog circuitry of this block, while the optimal operating point is managed by the MCU core.

The minimization of the power loss is achieved by adjusting the drop-out voltage according to a programmed target curve. To do so, the MCU core handles the communication with the transmitter to get the desired VRECT rail voltage.

Key voltages and currents in the block are constantly monitored to optimize the performance of the linear regulator and provide multiple protection levels (see related section).

The main linear regulator has independent control loops acting on the power pass element:

- Output voltage regulation loop: this loop regulates the output voltage at the nominal value set in the dedicated register;
- Input current regulation loop: in order to prevent a collapse at the output of the synchronous rectifier, the current through the linear regulator is limited to a programmed threshold.
- Input voltage regulation loop: this loop works in conjunction with the input current one and avoids that the VRECT rail drops (VOUT LDO input) below a programmable value.

Regulation loops play an important role: since the output of the rectifier is a highly variable voltage source (especially because of unpredictable changes in coil coupling), extra care is needed to avoid voltage drops that could lead to an undesirable MCU core reset.

The pass transistor is an N-channel MOSFET, and the BOOT pin is dedicated to its bootstrap capacitor, ensuring correct driving and lower on-resistance also in the case of drop-out condition.

A filtering capacitance higher than 20 µF has to be connected to the output rail (VOUT) to ensure stable operation of the linear regulator.

5.4 ASK , FSK communication

Robust and reliable in-band amplitude shift keying (ASK) modulation is critical to the operation of any Qi-compliant device. STWLC98 has dedicated hardware, in addition to the firmware algorithm, to improve the performance of in-band communication.

STWLC98 allows for three sets of modulation capacitors, namely COMA1/2, COMB1/2, and COMC1/2. These three sets of ASK communication capacitors can be used in parallel or individually, depending on the load condition of the device.

This allows for a high level of flexibility to accommodate a wide range of wireless transmitters. The modulation control can be set by the firmware.

STWLC98 comes with an advanced frequency-shift keying (FSK) demodulation filter that is able to remove any glitches present in the rectifier output.

5.5 ARC (Adaptive Rectifier Configuration) Mode

ARC (Adaptive Rectifier Configuration) mode improves the ping up and power transfer spatial freedom of the system in both X and Y direction.

Without any change in hardware or optimization of the coil, the ping up distance is enhanced by up to 50% in all directions by enabling ARC mode. This transforms the whole surface of the Tx to a usable area. Further enhancement is possible by customization of the coil.

Coil parameter tolerance requirements are widely relaxed due to ARC mode ping up feature. This is critical to applications where coils are of smaller and thinner dimensions, and it is relatively costlier to keep coil parameters within tight tolerances.

5.6 GPIOx and INTB pins

The GPIO0 through GPIO5 pins are programmable general-purpose I/O pins whose functions can be assigned in NVM memory. These pins can be configured both as inputs and outputs (either push-pull or open-drain) according to the selected function.

The INTB (GPIO6) pin is an interrupt output line that can be associated to any internal interrupt condition and used to inform the host system about specific events. The INTB pin can be programmed to be push-pull or open-drain type as well.

5.7 Protections

Over-voltage protection

The STWLC98 integrates different Over-Voltage Protection circuits to protect itself, the load connected to its output rail and the external components from damage due to overheating and/or exceeding AMR condition.

Any protection can trigger interrupt , it can be configured to automatically disable main voltage regulator and/or send an EPT.

Under normal operating conditions the voltage at the output of the synchronous rectifier is slightly higher than the output one thanks to the communication with the transmitter.

A sudden change in the coupling factor between transmitting and receiving coils, for example due to abrupt reciprocal repositioning of the coils, easily leads to unpredictable voltage peaks at the AC input terminals: the TX-RX regulation loop is not fast enough to prevent such an event and additional precautions must be taken.

Both the VRECT and VOUT outputs are constantly monitored.

The VRECT rail has three OVP mechanisms: Hard OVP , Soft OVP1, Soft OVP2.

Hard OVP (Hard Over Voltage Protection)

In the event of VRECT pin ≥ 26V (programmable 25V, 25.5V, 26V, 26.5V),Hard OVP protection circuit is triggered. the protection circuit immediately shorts both AC1 and AC2 pins to ground. HOVP condition releases when VRECT falls below certain voltage, depending on the VOUT set.

Table 6. HOVP release settings

VOUT target voltage(V)	HOVP release when VRECT less than (V)
< 12	10
12 ≤ VOUT < 15	13
15 ≤ VOUT < 18	16
≥ 18	19

SOVP Soft Over Voltage Protections

Two SOVP protections implemented in STWLC98

SOVP1 : In the event of VRECT pin ≥ 24V (Programmable 24V, 24.5V, 25V, 25.5V with 1V hysteresis) during power up, IEXT1 switch will be turned-on.

SOVP2: In the event of VRECT pin ≥ 24.5V (Programmable 24.5V, 25V, 25.5V 26V with 1V hysteresis) during power up, IEXT2 switch will be turned-on.

SOVP1 and SOVP2 are released when VRECT<(SOVP1 threshold -1V).

SOVP would interrupt Firmware to issue EPT and provide the time needed for the ASK modulation.

Over-temperature protection

The STWLC98 is equipped with three over-temperature detection circuits based on different sources:

1) Internal temperature sensor

2) External NTC temperature sensor

3) TSHUT (hardware)

Over temperature protection (software); the signals coming from the internal temperature sensors are conditioned and routed to the ADC.

The temperature can be monitored in a dedicated register. When the temperature exceeds the set threshold level, it can turn off the Main voltage regulator (VOUT), EPT can be sent to Tx to stop power transfer.

The external sensor (ADC NTC) typically placed very close to the coil to detect the over temperature of the coil, the low-sided NTC of a resistor divider whose center tap is connected to the NTC pin (analog input), while the high-side resistor is connected to the V1V2 pin. The temperature threshold is programmable by GUI. If this function is not used, the pin must be pulled-up to V1V2 through a 10 kΩ resistor to prevent triggering the coil over-temperature protection.

TSHUT comparator monitors the die temperature and turns off the Main voltage regulator (VOUT) when temperature exceeds set threshold level.

The temperature threshold is programmable by GUI from 105°C to 135°C with 10°C step (10 °C hysteresis).

When TSHUT is triggered both rectifier low-side switches are turned on while high-side switches are turned-off.

Over-current protection

HW OCP : when the output current exceed the HW set over current threshold (maximum 2.5A),it will turn-off Main Voltage regulator (VOUT), EPT can be sent to TX to stop power transfer.

ADC OCP : FW is periodically monitoring ADC data and once the current value exceeds set ADC OCP threshold, OCP INT can be triggered , and can turn-off VOUT and EPT can be sent to TX to stop power transfer.

5.8 TX Mode

STWLC98 can be configured to transmit (Tx) mode, and it is capable of delivering output power up to 15W, depending on the coil used.

Input Voltage

The device can support wide range of input voltage of 5V up to 20V.

Power is applied to the VOUT pin (VIN), which is the same VOUT pin used in Receiver Mode.

Tx Inverter

The power transmitter uses a Full Bridge inverter, with four N-channel MOSFETs arranged in an H-bridge configuration. The inverter converts the DC input into an AC waveform that drives a resonant circuit, consisting of a primary coil and series capacitor.

The power transmitted to the coil is regulated by varying the switching frequency of the bridge.

A higher operating frequency, such as 200kHz, results in lower transmitted power, while a lower operating frequency, such as 110kHz, results in higher transmitted power.

Q Factor detection

The Q factor feature in STWLC98 is enabled to detect the presence of a receiver (RX) or a non-RX electromagnetic object by comparing amplitudes at two different frequencies: the Q-factor and resonance frequency.

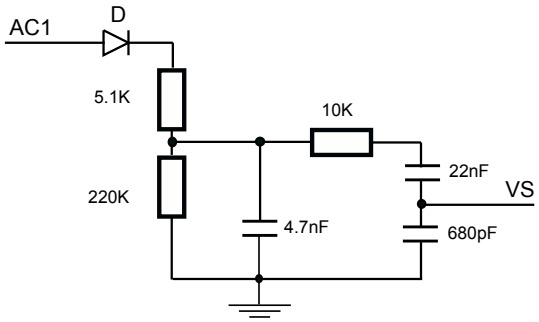
The Q-factor is measured at the coil, and the excitation signal must be controlled to avoid waking up a RX, if present.

ASK Demodulation

Using amplitude-shift keying (ASK) modulation, the power receiver regularly sends control error packets to tune the operating point and match load requirements.

The transmitter (Tx) receives this modulated signal from the AC1 input. The coil signal is conditioned using a discrete filter circuit, as shown below, and fed into the VS pin for demodulation.

Figure 2. ASK Demodulator Circuit



5.9 Wireless power interface

The blocks that refer to the wireless power interface include the synchronous rectifier, the main low-dropout (LDO) linear regulator, the amplitude-shift keying (ASK) modulator, and the digital core as supervisor.

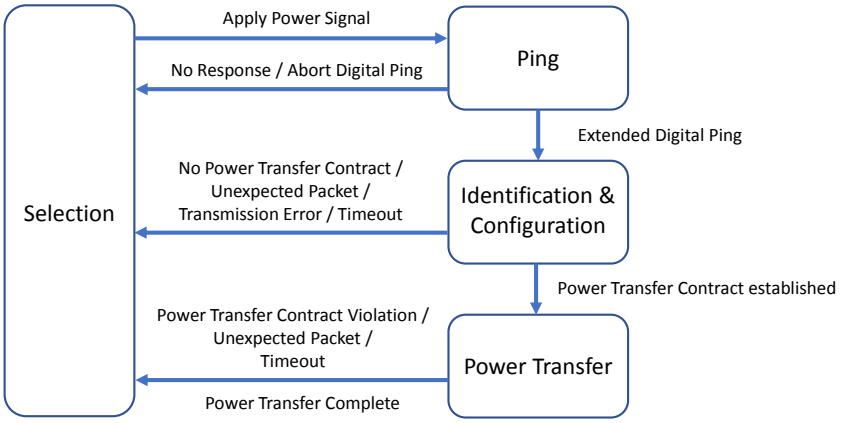
The power transfer from the transmitter to the receiver is established through a procedure consisting of several distinct stages.

The power transfer begins after the transmitter has properly detected a valid receiver and a specific communication has been established between the two parts.

BPP

The flow-chart in below reports the whole process of power transfer in Baseline Power Profile (BPP up to 1A@5V)

Figure 3. Power transfer phases for Baseline Power Profile



- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal Strength packet.
- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver.

EPP

The flow-chart in below shows the whole process leading to a power transfer in Extended Power Profile (EPP) up to 1.25A@12V

Figure 4. Power transfer phases for Extended Power Profile

Without entering the details of the different phases, the basic sequence of events taking place when a receiver is properly placed on the transmitting coil are summarized as:

- Digital ping: this phase is an interrogation session based on a more energetic AC burst during which the potential receiver is expected to reply through amplitude shift-keying (ASK) modulation, the receiver device sends Signal strength packet.

- Identification & configuration: this phase is aiming to identify the receiver and to gather information about its power transfer capability. The transmitter generates a so-called “Power Transfer Contract” tailoring some parameters that will characterize the following power transfer phase.
- Negotiation: in this phase the Power Receiver negotiates with the Power Transmitter to fine tune the Power Transfer Contract.
- Power transfer: this is the final step, where the transmitter initially increases and subsequently modulates the transmitted power in response to the control (feedback) data from the receiver

STWLC98 goes autonomously through Selection, Ping, Identification & Configuration phases, entering Power Transfer phase if no error occurs.

During the Power Transfer phase, the device sends Received-Power and Control-Error packets periodically as feedback information for the transmitter.

If a critical event like over-voltage, over-current or over-temperature occurs, the STWLC98 automatically sends the End-Power-Transfer packet.

When the Power Transfer is up and running, the End-Power-Transfer packet (with any response value) or any custom packet (e.g. Proprietary packet or Charge-Status packet) can be sent to the transmitter simply through commands via I^2C interface.

Sending a custom packet may result in a reply (either a data packet or a pattern response from the transmitter) or no reply at all: if a response is received, the content is captured and stored in specific I^2C registers.

Important notes:

- Changing the output voltage must respect the overall system design (selected coil, transmitter type, etc.).
- Output load transient response strongly depends on a correct design of the output capacitors. Severe load transients may lead to temporary output voltage collapse due to the overall TX-RX response time.
- A minimal output load significantly helps in increasing the signal-to-noise ratio during digital ping and is advisable to ensure interoperability with all transmitters.
- The initial load at power-up should not exceed 2.5W, smoothly ramping-up to full power subsequently.

6 I2C interface

The STWLC98 can operate fully independently, i.e. without being interfaced with a host system.

In applications in which the STWLC98 has to be a part of peripherals managed by the host system, the two SDA and SCL pins could be connected to the existing I²C bus.

The device works as an I²C slave and supports standard (100 kbps) and fast (400 kbps) data transfer modes.

The STWLC98 has been assigned 0x61 7-bit hardware address. The pins are tolerant up to 1.8V and the pull-up resistors should be selected as a trade-off between communication speed (lower resistors lead to faster edges) and data integrity (The guaranteed input logic levels ensure communication reliability).

When the bus is idle, both SDA and SCL lines are pulled HIGH.

Data Validity

The data on the SDA line must be stable during the high period of the clock. The high and low states of the SDA line can only change when the SCL clock signal is low.

Start and Stop Conditions

Both the SDA and the SCL lines remain high when the I^2C bus is not busy. A START condition is a high-to-low transition of the SDA line when SCL is HIGH, while the STOP condition is a low-to-high transition of the SDA line when SCL is HIGH. A STOP condition must be sent before each START condition.

Interface protocol

The interface protocol consists of

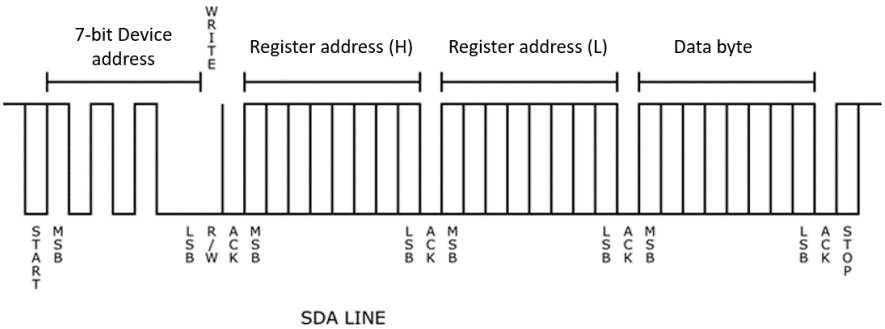
- Start condition (START)
- 7-bit device address (0x61) + R/W bit (read = 1 / write = 0)
- Register pointer, high-byte
- Register pointer, low-byte
- Data sequence: N x (data byte + ACK)
- Stop condition (STOP)

The register pointer (or address) byte defines the destination register to which the read or write operation applies. When the read or write operation is finished, the register pointer is automatically incremented.

Writing to a single register

Writing to a single register begins with a START condition followed by device address 0xC2 (7-bit device address plus R/W bit cleared), two bytes of the register pointer and the data byte to be written in the destination register. Each transmitted byte is acknowledged by the STWLC98 through an ACKnowledgment (ACK) signal.

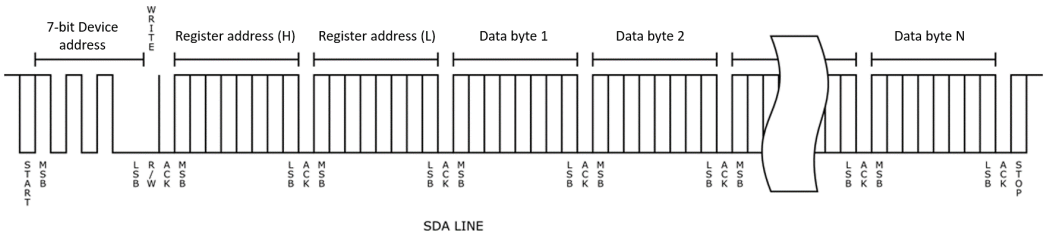
Figure 5. Writing to single register byte



Writing to multiple registers (page write)

The STWLC98 supports writing to multiple registers with auto-incremental addressing. When data is written into a register, the register pointer is automatically incremented, therefore transferring data to a set of subsequent registers (also know as page write) is a straightforward operation.

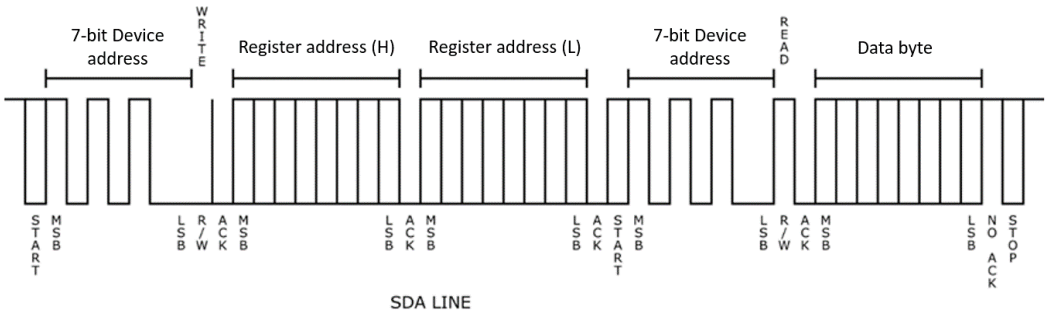
Figure 6. Writing multiple register bytes



Reading from a single register

Reading from a single register begins with a START condition followed by the device address byte 0xC2 (7-bit device address plus R/W bit cleared) and two bytes of register pointer, then a re-START condition is generated and the device address 0xC3 (7-bit device address plus R/W bit asserted) is sent, followed by data reading. ACKnowledgment (ACK) signal is generated by the STWLC98 at the end of each byte, but not for data bytes retrieved from the register. A STOP condition is finally generated to terminate the operation.

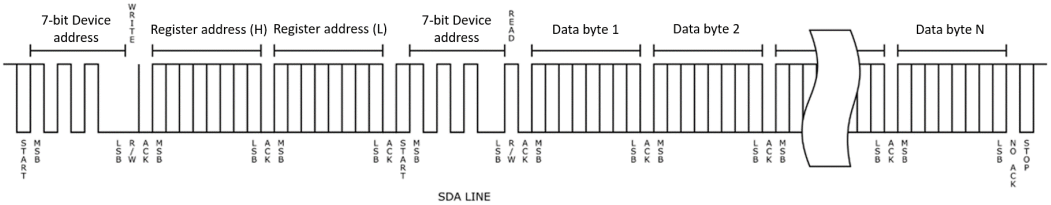
Figure 7. Reading single register byte



Reading from multiple registers (page reading)

Similarly to multiple (page) writing, reading from subsequent registers relies on an auto-increment of the register: the master can extend data reading to the following registers by generating an ACKnowledgment (ACK) signal at the end of each byte. Data reading starts immediately and the stream is terminated by a NACK pulse at the end of the last data byte, followed by a STOP condition.

Figure 8. Reading multiple bytes



7 I2C register map

The STWLC98 can be monitored and controlled by accessing the internal registers via I2C interface. The following registers map reports the accessible addresses. Addresses not shown in the map and blank bits have to be considered Reserved and not altered as well.

Table 7. Register abbreviations

Register type	Description
R/W	can read and write the Bits
R	can read only
W	can write only

Table 8. Chip information

Register address	Register name	R/W	Default	Description
0x0000	Chip ID Low	R	0x62	Chip ID [7..0]
0x0001	Chip ID High	R	0x00	Chip ID [15..8]
0x0002	Chip revision	R	0x02	Chip revision [7..0]
0x0003	Customer ID	R	-	Customer ID [7..0]
0x0004	ROM ID	R	-	ROM ID [7..0]
0x0005	ROM ID	R	-	ROM ID [15..8]
0x0006	NVM Patch ID	R	-	NVM patch ID [7..0]
0x0007	NVM Patch ID	R	-	NVM patch ID [15..8]
0x0008	Patch ID	R	-	Patch ID [7..0]
0x0009	Patch ID	R	-	Patch ID [15..8]
0x000A	Configuration ID	R	-	Configuration ID [7..0]
0x000B	Configuration ID	R	-	Configuration ID [15..8]
0x000C	Production ID	R	-	PE ID [7..0]
0x000D	Production ID	R	-	PE ID [7..0]
0x000E	Operation mode	R	0x02	0x1: Standalone (debug) mode 0x2: Qi RX mode 0x3: Qi TX mode
0x0010 ..0 x001F	Device ID	R	-	Device ID Bytes 0 ...15

Table 9. System information

Register address	Register name	R/W	Default	Description
0x0020	System command	RW	-	Bit 0: Switch to TX command Write 1 to switch to Qi TX mode
		RW	-	Bit 1: Switch to RX command Write 1 to switch to Qi RX mode
		-	-	Bit 2..7 Reserved

Register address	Register name	R/W	Default	Description
0x002C	System error	R	-	Bit 0: Core hard fault error 0: No hard fault error detected 1: Hard fault error detected
		R	-	Bit 1: HW WDT trigger latch 0: HW WDT not triggered 1: HW WDT triggered
		R	-	Bit 2: FTP IP error 0: No FTP IP error detected 1: FTP IP error detected
		R	-	Bit 3: MI2C error 0: No MI2C error detected 1: MI2C error detected
		R	-	Bit 4: FTP Boot error
		-	-	Bit [7..5] Reserved
0x002D	System error	R	-	Bit [1..0] FTP PE error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [3..2] FTP Configuration error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit [5..4] FTP Patch error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved
		R	-	Bit[7..6] FTP Production Information error 0: No error 1: Section header error 2: Section CRC failed 3: Reserved

Table 10. Communication

Register address	Register name	R/W	Default	Description
0x00D8 ,0x00D9	DTS SEND LEN	RW	-	DTS ADS number of data bytes in stream
0x00DA	DTS SEND RQ	RW	-	send ADC request Bits [4..0]
0x00DC, 0x00DD	DTS RCV LEN	RW	-	DTS ADS number of bytes in stream received
0x00DE	DTS RCV RQ	RW	-	received ADC request Bits [4..0]

Table 11. **Mode monitor**

Register address	Register name	R/W	Default	Description
0x0092	VRECT	R	-	Rectifier voltage in mV [7..0]
0x0093				[15..8]
0x0094	VOUT	R	-	Main LDO Voltage output in mV [7..0]
0x0095				Main LDO Voltage output in mV [15..8]
0x0096	RX ICUR	R	-	Output current in mA [7..0]
0x0097				[15..8]
0x0098	TMEAS	R	-	Chip temperature in deg C [7..0]
0xx099				[15..8]
0x009A	OP FREQ	R	-	Operating frequency in kHz [7..0]
0x009B				[15..8]
0x009C	NTC	R	-	NTC temperature measurement [7..0]
0x009D				[15..8]
0x009E	ADC IN	R	-	ADC IN measurement [7..0]
0x009F				[15..8]
0x00A4	POWER RX	R	-	RX received power in mW [7..0]
0x00A5				[15..8]
0x00A6	POWER RPP	R	-	Last RP value sent [7..0]
0x00A7				[15..8]
0x00A8	RX VOLT DIFF	R	-	Rx voltage difference between target and measured VRECT in mV [7..0]
0x00A9				[15..8]
0x00AA	RECENT CEP	R	-	Last CE value sent [7..0]
0x00AB	SIG STREN	R	-	Signal strength measured in Rx [7..0]

Table 12. **GPIO**

Register address	Register name	R/W	Default	Description
0x0030	GPIO0 Function	RW	-	Please refer to user manual for detailed description .
0x0031	GPIO1 Function	RW	-	
0x0032	GPIO2 Function	RW	-	
0x0033	GPIO3 Function	RW	-	
0x0034	GPIO4 Function	RW	-	
0x0035	GPIO5 Function	RW	-	
0x0036	GPIO6 Function	RW	-	used for INTB function

Receiver mode (Rx) registers

Table 13. RX interrupts enable

Register address	Register name	R/W	Default	Description
0x0080	RX OVTP EN	RW	-	Bit 0: over temperature protection enable 0: disable 1: enable
	RX OCP EN	RW	-	Bit 1: over current protection enable 0: disable 1: enable
	RX OVP EN	RW	-	Bit 2: over voltage protection 0: disable 1: enable
	RX SYS ERROR EN	RW	-	Bit 3: system error enable 0: disable 1: enable
	RX TX REMOVAL EN	RW	-	Bit 4 : When using external 5V, TX removal is detected. I2C master should power down ext 5V upon interrupt. 0: disable 1: enable
	RX MSG RCVD EN	RW	-	Bit 5: message received from TX 0: disable 1: enable
	RX OUTPUT ON EN	RW	-	Bit 6: output on interrupt enable 0: disable 1: enable
	RX OUTPUT OFF EN	RW	-	Bit 7: Output off interrupt enable 0: disable 1: enable
0x0081	RX SENT PACKET EN	RW	-	Bit 0: Packet sent interrupt enable 0: disable 1: enable
	RX SENT PKT TO EN	RW	-	Bit 1: Packet sending timeout interrupt enable 0: disable 1: enable
	RX SIG STR EN	RW	-	Bit 2: Signal Strength sent interrupt enable 0: disable 1: enable
	RX VRECT RDY EN	RW	-	Bit 3: VRECT ready interrupt enable 0: disable 1: enable
	RX SCP EN	RW	-	Bit 4: Short circuit protection enable 0: disable

Register address	Register name	R/W	Default	Description
0x0081				1: enable
		-	-	Bits 5,6,7: Reserved
0x0082	RX DTS SEND SUCCESS EN	RW	-	Bit0: DTS sending data stream successfully interrupt enable 0: disable 1: enable
	RX DTS SEND TO END EN	RW	-	Bit 1: DTS stopped sending due to timeout error interrupt enable 0: disable 1: enable
	RX DTS RCVD RESET END EN	RW	-	Bit 2: DTS stopped sending due to reset interrupt enable 0: disable 1: enable
		RW	-	Bit 3: Reserved
	RX DTS RCVD SUCCESS EN	RW	-	Bit 4: DTS received data stream successful interrupt enable 0: disable 1: enable
	RX DTS RCVD TO END EN	RW	-	Bit 5: DTS stopped receiving due to timeout error interrupt enable 0: disable 1: enable
	RX DTS RCVD RESET END EN			Bit 6: DTS stopped receiving due to reset 0: disable 1: enable
		-	-	Bit7: Reserved

Table 14. RX interrupts Clear

Register address	Register name	R/W	Default	Description
0x0084	RX OVTP CLR	R	-	Bit 0: over temperature protection clear 1: clear
	RX OCP CLR	R	-	Bit 1: over current protection clear 1: clear
	RX OVP CLR	R	-	Bit 2: over voltage protection clear 1: clear
	RX SYS ERROR CLR	R	-	Bit 3: system error clear 1: clear
		-	-	Bit 4: Reserved
	RX MSG RCVD CLR	R	-	Bit 5: message received from TX clear 1: clear
	RX OUTPUT ON CLR	R	-	Bit 6: Output on interrupt clear

Register address	Register name	R/W	Default	Description
0x0084				1: clear
	RX OUTPUT OFF CLR	R	-	Bit 7: Output off interrupt clear 1: clear
0x0085	RX SENT PACKET CLR	R	-	Bit 0: Packet sent interrupt clear 1: clear
	RX SENT PKT TO CLR	R	-	Bit 1: Packet sending timeout interrupt clear 1: clear
	RX SIG STR CLR	R	-	Bit 2: Signal Strength sent interrupt clear 1: clear
	RX VRECT RDY CLR	R	-	Bit 3: VRECT ready interrupt clear 1: clear
	RX DTS RCVD SECCESS CLR	R	-	Bit4:DTS received data stream successfully 1: clear
		R	-	Bit 5,6,7: Reserved
0x0086	RX DTS SEND SUCCESS CLR	R	-	Bit1: DTS sending data stream successfully interrupt clear 1: clear
	RX DTS SEND TO END CLR	R	-	Bit 2: DTS stopped sending due to timeout error interrupt clear 1: clear
	RX DTS RCVD RESET END CLR	R	-	Bit 3: DTS stopped sending due to reset interrupt clear 1: clear
		-	-	Bit 4: Reserved
	RX DTS RCVD SUCCESS CLR	R	-	Bit 5: DTS received data stream successful interrupt clear 1: clear
	RX DTS RCVD TO END CLR	R	-	Bit 6: DTS stopped receiving due to timeout error interrupt clear 1: clear

Table 15. RX interrupts latch

Register address	Register name	R/W	Default	Description
0x0088	RX OVTP LTCH	R	-	Bit 0: over temperature protection latch
	RX OCP LTCH	R	-	Bit 1: over current protection latch
	RX OVP LTCH	R	-	Bit 2: over voltage protection latch
	RX SYS ERROR LTCH	R	-	Bit 3: system error latch
		-	-	Bit 4: Reserved
	RX MSG RCVD LTCH	R	-	Bit 5: message received from TX latch
	RX OUTPUT ON LTCH	R	-	Bit 6: Output on interrupt latch
	RX OUTPUT OFF LTCH	R	-	Bit 7: Output off interrupt latch
0x0089	RX SENT PACKET LTCH	R	-	Bit 0: Packet sent interrupt latch
	RX SENT PKT TO LTCH	R	-	Bit 1: Packet sending timeout interrupt latch

Register address	Register name	R/W	Default	Description
0x0089	RX SIG STR LTCH	R	-	Bit 2: Signal Strength sent interrupt latch
	RX VRECT RDY LTCH	R	-	Bit 3: VRECT ready interrupt latch
	RX DTS RCVD SUCCESS LTCH	R	-	Bit 4:DTS received data stream successfully latch
	RX UVLO LTCH	R	-	Bit 5: under voltage protection interrupt latch
		-	-	Bit 6..7: Reserved
0x008A	RX DTS SEND SUCCESS LTCH	R	-	Bit 1: DTS sending data stream successfully interrupt latch
	RX DTS SEND TO END LTCH	R	-	Bit 2: DTS stopped sending due to timeout error interrupt latch
	RX DTS RCVD RESET END LTCH	R	-	Bit 3: DTS stopped sending due to reset interrupt latch
		R	-	Bit 4: Reserved
	RX DTS RCVD SUCCESS LTCH	R	-	Bit 5: DTS received data stream successful interrupt latch
	RX DTS RCVD TO END LTCH	R	-	Bit 6: DTS stopped receiving due to timeout error interrupt latch

Table 16. RX interrupts status

Register address	Register name	R/W	Default	Description
0x008C	RX OVTP STAT	R	-	Bit 0: over temperature protection status
	RX OCP STAT	R	-	Bit 1: over current protection status
	RX OVP STAT	R	-	Bit 2: over voltage protection status
	RX SYS ERROR STAT	R	-	Bit 3: system error status
		-	-	But 4: Reserved
	RX MSG RCVD STAT	R	-	Bit 5: message received from TX status
	RX OUTPUT ON STAT	R	-	Bit 6: Output on interrupt status
	RX OUTPUT OFF STAT	R	-	Bit 7: Output off interrupt status
0x008D	RX SENT PACKET STAT	R	-	Bit 0: Packet sent interrupt status
	RX SENT PKT TO STAT	R		Bit 1: Packet sending timeout interrupt status
	RX SIG STR STAT	R	-	Bit 2: Signal Strength sent interrupt status
	RX VRECT RDY STAT	R	-	Bit 3: VRECT ready interrupt status
	RX DTS RCVD SUCCESS STAT	R	-	Bit 4: DTS received data stream successfully interrupt status
	RX UVLO STAT	R	-	Bit 5: under voltage protection interrupt status
		-	-	Bit 6,7: Reserved
0x008E		-	-	Bit 0: Reserved
	RX DTS SEND SUCCESS STAT	R	-	Bit 1: DTS sending data stream successfully interrupt status
	RX DTS SEND TO END STAT	R	-	Bit 2: DTS stopped sending due to timeout error interrupt status
	RX DTS RCVD RESET END STAT	R	-	Bit 3: DTS stopped sending due to reset interrupt status

Register address	Register name	R/W	Default	Description
0x008E		-	-	Bit 4: Reserved
	RX DTS RCVD SUCCESS STAT	R	-	Bit 5: DTS received data stream successful interrupt status
	RX DTS RCVD TO END CLR	R	-	Bit 6: DTS stopped receiving due to timeout error interrupt status

Table 17. RX commands

Register address	Register name	R/W	Default	Description
0x0090	RX VOUT ON	RW	-	Bit 0: Turn on the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.
	RX VOUT OFF	RW	-	Bit 1: Turn off the VOUT. If both VOUT_ON and VOUT_OFF are set to 1, this command is ignored and both requests are cleared.

Table 18. RX configuration

Register address	Register name	R/W	Default	Description
0x00B4	RX VOUT SET	RW	-	VOUT_SET [7:0] Byte 0
0x00B5				VOUT_SET[15:8] Byte 1 Step size 25mV
0x00B3	RX ILIM SET	RW	-	Program current limit and regulation from 100mA to 2.5A Step size 100mA Set to "0" disable current limit and regulation loop

Table 19. RX LDO configuration

Register address	Register name	R/W	Default	Description
0x00C8	LDO DROP 0	RW	-	LDO target voltage drop at 0mA IOUT. Specified in 16mV units. Set point 0
0x00C9	LDO DROP 1	RW	-	LDO target voltage drop at ldo_cur_thres1 IOUT. Specified in 16mV units. Set point 1
0x00CA	LDO DROP 2	RW	-	LDO target voltage drop at ldo_cur_thres2 IOUT. Specified in 16mV units. set point 2
0x00CB	LDO DROP 3	RW	-	LDO target voltage drop at ldo_cur_thres3 IOUT. Specified in 16mV units. set point 3
0x00CC	LDO CUR TH1	RW	-	LDO voltage drop IOUT current threshold 1. Specified in 8mA units.
0x00CD	LDO CUR TH2	RW	-	LDO voltage drop IOUT current threshold 2. Specified in 8mA units.

Register address	Register name	R/W	Default	Description
0x00CE	LDO CUR TH3	RW	-	LDO voltage drop IOUT current threshold 3. Specified in 8mA units.

Table 20. RX FOD configuration

Register address	Register name	R/W	Default	Description
0x00B6	FOD CUR THR1	RW	-	FOD current threshold 1, in units of 8mA
0x00B7	FOD CUR THR2	RW	-	FOD current threshold 2, in units of 8mA
0x00B8	FOD CUR THR3	RW	-	FOD current threshold 3, in units of 8mA
0x00B9	FOD CUR THR4	RW	-	FOD current threshold 4, in units of 8mA
0x00BA	FOD CUR THR5	RW	-	FOD current threshold 5, in units of 8mA
0x00BB	FOD GAIN OFFS0	RW	-	FOD Gain scaler offset 0, at current 0, base is 512, default scaler is 512. Specify this value as signed (2'complement) offset. 0 - 512/512;1 - 513/512; -1 - 511/512
0x00BC	FOD GAIN OFFS1	RW	-	FOD Gain scaler offset 1, at current 1
0x00BD	FOD GAIN OFFS2	RW	-	FOD Gain scaler offset 2, at current 2
0x00BE	FOD GAIN OFFS3	RW	-	FOD Gain scaler offset 3, at current 3
0x00BF	FOD GAIN OFFS4	RW	-	FOD Gain scaler offset 4, at current 4
0x00C0	FOD GAIN OFFS5	RW	-	FOD Gain scaler offset 5, at current 5
0x00C1	FOD OFFSET 0	RW	-	FOD offset at current 0, specified in units of 8mW
0x00C2	FOD OFFSET 1	RW	-	FOD offset at current 1, specified in units of 8mW
0x00C3	FOD OFFSET 2	RW	-	FOD offset at current 2, specified in units of 8mW
0x00C4	FOD OFFSET 3	RW	-	FOD offset at current 3, specified in units of 8mW
0x00C5	FOD OFFSET 4	RW	-	FOD offset at current 4, specified in units of 8mW
0x00C6	FOD OFFSET 5	RW	-	FOD offset at current 5, specified in units of 8mW
0x00C7	FOD RSER	RW	-	Coil series resistance, specified in units of 4mΩ

Table 21. RX EPP FOD configuration

Register address	Register name	R/W	Default	Description
0x00E4	EPP FOD CUR THR1	RW	-	EPP FOD current threshold 1, in units of 8mA.
0x00E5	EPP FOD CUR THR2	RW	-	EPP FOD current threshold 2, in units of 8mA.
0x00E6	EPP FOD CUR THR3	RW	-	EPP FOD current threshold 3, in units of 8mA.
0x00E7	EPP FOD CUR THR4	RW	-	EPP FOD current threshold 4, in units of 8mA.
0x00E8	EPP FOD CUR THR5	RW	-	EPP FOD current threshold 5, in units of 8mA.
0x00E9	EPP FOD GAIN OFFS0	RW	-	EPP FOD Gain scaler offset 0, at current 0, base is 512, default scaler is 512. Specify this value as signed (2'complement) offset. 0 - 512/512;1 - 513/512; -1 - 511/512
0x00EA	EPP FOD GAIN OFFS1	RW	-	EPP FOD Gain scaler offset 1, at current 1
0x00EB	EPP FOD GAIN OFFS2	RW	-	EPP FOD Gain scaler offset 2, at current 2
0x00EC	EPP FOD GAIN OFFS3	RW	-	EPP FOD Gain scaler offset 3, at current 3

Register address	Register name	R/W	Default	Description
0x00ED	EPP FOD GAIN OFFS4	RW	-	EPP FOD Gain scaler offset 4, at current 4
0x00EE	EPP FOD GAIN OFFS5	RW	-	EPP FOD Gain scaler offset 5, at current 5
0x00EF	EPP FOD OFFSET 0	RW	-	EPP FOD offset at current 0, specified in units of 8mW
0x00F0	EPP FOD OFFSET 1	RW	-	EPP FOD offset at current 1, specified in units of 8mW
0x00F1	EPP FOD OFFSET 2	RW	-	EPP FOD offset at current 2, specified in units of 8mW
0x00F2	EPP FOD OFFSET 3	RW	-	EPP FOD offset at current 3, specified in units of 8mW
0x00F3	EPP FOD OFFSET 4	RW	-	EPP FOD offset at current 4, specified in units of 8mW
0x00F4	EPP FOD OFFSET 5	RW	-	EPP FOD offset at current 5, specified in units of 8mW
0x00F5	EPP FOD RSER	RW	-	EPP Coil series resistance, specified in units of 4mΩ

Table 22. TX Interrupt enable

Register address	Register name	R/W	Default	Description
0x0100	TX OVTP EN	RW	-	Bit 0: over temperature protection enable 0: disable 1: enable
	TX OCP EN	RW	-	Bit 1: over current protection enable 0: disable 1: enable
	TX OVP EN	RW	-	Bit 2: over voltage protection enable 0: disable 1: enable
	TX SYS ERR EN	RW	-	Bit 3: system error enable 0: disable 1: enable
	TX RP PKT RCVD EN	RW	-	Bit 4: RP packet received interrupt enable 0: disable 1: enable
	TX CE PKT RCVD EN	RW	-	Bit 5: CE packet received interrupt enable 0: disable 1: enable
	TX SEND PKT SUC EN	RW	-	Bit 6: Packet sent interrupt enable 0: disable 1: enable
	TX EXT MON EN	RW	-	Bit 7: Ext Tx Detect interrupt enable 0: disable 1: enable
0x0101	TX CEP TO EN	RW	-	Bit 0: CEP Timeout interrupt enable 0: disable 1: enable
	TX RPP TO EN	RW	-	Bit 1: RPP Timeout interrupt enable 0: disable

Register address	Register name	R/W	Default	Description
0x0101				1: enable
	TX EPT EN	RW	-	Bit 2: AC powered down interrupt enable 0: disable 1: enable
	TX START PING EN	RW	-	Bit 3: Ping started interrupt enable 0: disable 1: enable
	TX SS PKT RCVD EN	RW	-	Bit 4: SS ID packet received interrupt enable 0: disable 1: enable
	TX ID PKT RCVD EN	RW	-	Bit 5: ID packet received interrupt enable 0: disable 1: enable
	TX CFG PKT RCVD EN	RW	-	Bit 6: Configuration packet received interrupt 0: disable 1: enable
	TX PP PKT RCVD EN	RW	-	Bit 7: PP packet received interrupt enable 0: disable 1: enable

Table 23. TX Interrupt clear

Register address	Register name	R/W	Default	Description
0x0104	TX OVTP CLR	R	-	Bit 0: over temperature protection clear 1: clear
	TX OCP CLR	R	-	Bit 1: over current protection clear 1: clear
	TX OVP CLR	R	-	Bit 2: over voltage protection clear 1: clear
	TX SYS ERR CLR	R	-	Bit 3: system error clear 1: clear
	TX RP PKT RCVD CLR	R	-	Bit 4: RP packet received interrupt clear 1: clear
	TX CE PKT RCVD CLR	R	-	Bit 5: CE packet received interrupt clear 1: clear
	TX SCLRD PKT SUC CLR	R	-	Bit 6: Packet sent interrupt clear 1: clear
	TX EXT MON CLR	R	-	Bit 7: Ext Tx Detect interrupt clear 1: clear
0x0105	TX CEP TO CLR	R	-	Bit 8: CEP Timeout interrupt clear 1: clear
	TX RPP TO CLR	R	-	Bit 9: RPP Timeout interrupt clear

Register address	Register name	R/W	Default	Description
0x0105				1: clear
	TX EPT CLR	R	-	Bit 10: AC powered down interrupt clear 1: clear
	TX START PING CLR	R	-	Bit11: Ping started interrupt clear 1: clear
	TX SS PKT RCVD CLR	R	-	Bit 12: SS ID packet received interrupt clear 1: clear
	TX ID PKT RCVD CLR	R	-	Bit 13: ID packet received interrupt clear 1: clear
	TX CFG PKT RCVD CLR	R	-	Bit 14: Configuration packet received interrupt clear 1: clear
	TX PP PKT RCVD CLR	R	-	Bit 15: PP packet received interrupt clear 1: clear

Table 24. TX interrupt latch

Register address	Register name	R/W	Default	Description
0x0108	TX OVTP LTCH	R	-	Bit 0: over temperature protection latch 1: latch
	TX OCP LTCH	R	-	Bit 1: over current protection latch 1: latch
	TX OVP LTCH	R	-	Bit 2: over voltage protection latch 1: latch
	TX SYS ERR LTCH	R	-	Bit 3: system error latch 1: latch
	TX RP PKT RCVD LTCH	R	-	Bit 4: RP packet received interrupt latch 1: latch
	TX CE PKT RCVD LTCH	R	-	Bit 5: CE packet received interrupt latch 1: latch
	TX SLTCHD PKT SUC LTCH	R	-	Bit 6: Packet sent interrupt latch 1: latch
	TX EXT MON LTCH	R	-	Bit 7: Ext Tx Detect interrupt latch 1: latch
0x0109	TX CEP TO LTCH	R	-	Bit 0: CEP Timeout interrupt latch 1: latch
	TX RPP TO LTCH	R	-	Bit 1: RPP Timeout interrupt latch 1: latch
	TX EPT LTCH	R	-	Bit 2: AC powered down interrupt latch 1: latch
	TX START PING LTCH	R	--	Bit 3: Ping started interrupt latch 1: latch

Register address	Register name	R/W	Default	Description
0x0109	TX SS PKT RCVD LTCH	R	-	Bit 4: SS ID packet received interrupt latch 1: latch
	TX ID PKT RCVD LTCH	R	-	Bit 5: ID packet received interrupt latch 1: latch
	TX CFG PKT RCVD LTCH	R	-	Bit 6: Configuration packet received interrupt latch 1: latch
	TX PP PKT RCVD LTCH	R	-	Bit 7: PP packet received interrupt latch 1: latch

Table 25. TX Interrupt status

Register address	Register name	R/W	Default	Description
0x010C	TX OVTP STAT	R	-	Bit 0: over temperature protection status
	TX OCP STAT	R	-	Bit 1: over current protection status
	TX OVP STAT	R	-	Bit 2: over voltage protection status
	TX SYS ERR STAT	R	-	Bit 3: system error status
	TX RP PKT RCVD STAT	R	-	Bit 4: RP packet received interrupt status
	TX CE PKT RCVD STAT	R	-	Bit 5: CE packet received interrupt status
	TX SSTATD PKT SUC STAT	R	-	Bit 6: Packet sent interrupt status
	TX EXT MON STAT	R	-	Bit 7: Ext Tx Detect interrupt status
0x010D	TX CEP TO STAT	R	-	Bit 0: CEP Timeout interrupt status
	TX RPP TO STAT	R	-	Bit 1: RPP Timeout interrupt status
	TX EPT STAT	R	-	Bit 2: AC powered down interrupt status
	TX START PING STAT	R	-	Bit 3: Ping started interrupt status
	TX SS PKT RCVD STAT	R	-	Bit 4: SS ID packet received interrupt status
	TX ID PKT RCVD STAT	R	-	Bit 5: ID packet received interrupt status
	TX CFG PKT RCVD STAT	R	-	Bit 6: Configuration packet received interrupt status
	TX PP PKT RCVD STAT	R	-	Bit 7: PP packet received interrupt status

Table 26. TX configuration

Register address	Register name	R/W	Default	Description
0x0144	TX FREQ MAX	RW	-	Bits [7…0] Max frequency specified in units of KHz
0x0145	TX FREQ MIN	RW	-	Bits [7…0] Min frequency specified in units of KHz
0x0146	TX FREQ PING	RW	-	Bits [7…0] Ping frequency specified in units of KHz
0x0147	TX PING INTERVAL	RW	-	Bits [7…0] Interval between ping (in 10ms)

Register address	Register name	R/W	Default	Description
0x0148	TX DC MAX	RW	-	Bits [7…0] Max Tx duty cycle %. Max value is 50. Must be >= TX_MIN_DC
0x0149	TX DC MIN	RW	-	Bits [7…0] Min Tx duty cycle %. Must be <= TX_MAX_DC
0x014E	TX DC PING	RW	-	Bits [7…0] Ping duty cycle in percentage
0x014A	TX PLOSS FOD THR	RW	-	Bits [7…0] Tx PLOSS FOD detection threshold in 32mW units. 0 - Disable 1 - 32mW … 255 - 8160mW
0x014B	TX FOD DBNC CNT	RW	-	Bits [7…0] Continuous PLOSS based RP de bounce count before FOD EPT. 0 - EPT immediately
0x014C	TX CE TO MAX	RW	-	Bits [7…0] Max count TX retries with different frequency after failing to listen to CE packet within time frame.
0x014D	TX FHOP	RW	-	Bits [7…0] Define the step size (in Hz) for every frequency hop. Internally it is multiplied with 128 1: 128Hz step size 2: 256Hz step size 3: 384Hz step size ….
0x0134	TX BRDG MODE	RW	-	Bits [1...0] Tx power transfer half bridge / full bridge mode control. 0 - No change (same as ping) 1 - Manual half bridge mode 2 - Manual full bridge mode 3 - Auto switch
	TX PING HALF BRDG	RW	-	Bit 2: Tx ping in half bridge mode. 0 - Disable (Start ping in full bridge mode) 1 - Enable (Start ping in half bridge mode)

Table 27. TX EPT reason

Register address	Register name	R/W	Default	Description
0x0112	TX OVTP	RW	-	Bit 0: over temperature triggered
	TX OCP	RW	-	Bit 1: over current protection triggered
	TX OVP	RW	-	Bit 2: over voltage protection triggered
	TX FOD	RW	-	Bit 3: Foreign object detected
	TX HOST	RW	-	Bit4: Host issued EPT command
	TX RX EPT	RW	-	Bit 5: EPT Source Rx EPT packet
	TX CEP TO	RW	-	Bit 6: Control error packet timeout
	TX RPP TO	RW	-	Bit 7: Received power packet timeout
0x0113	TX RX RST	RW	-	Bit 0: Rx send SS/ID/CFG at wrong time , probably because of RX RESET
	TX SYS ERR	RW	-	Bit 1: System error
	TX SS TO	RW	-	Bit 2: Signal strength timeout
	TX SS ERR	RW	-	Bit 3: Signal strength packet error
	TX ID ERR	RW	-	Bit 4: Identification packet error
	TX CFG	RW	-	Bit 5: Error in configuration packet
	TX CFG CNT	RW	-	Bit 6: Number optional packets received doesn't match with number in configuration packet
	TX PCH ERR	RW	-	Bit 7: Power control hold-off packet error

Register address	Register name	R/W	Default	Description
0x0114	TX XID ERR	RW	-	Bit 0: Extended identification packet error
	TX NEG ERR	RW	-	Bit 1: Negotiation error
	TX NEGO TO	RW	-	Bit 2: Negotiation time out error

Table 28. TX protections

Register address	Register name	R/W	Default	Description
0x0140	TX OVP THRES	RW	-	Bit [7…0] Specify Tx OVP threshold in 500mV units.
0x0141	TX OCP THRES	RW	-	Bit [7…0] Specify Tx OCP current in 100mA units.0 - Disable1 - 100mA…
0x0142	TX OVTP THRES	RW	-	Bit [7 …0] Over temperature protection threshold in degree C. If transmitter die temperature rises above this value, then OTP triggered.

Table 29. Auxiliary Data

Register address	Register name	R/W	Default	Description
0x0180	AUX DATA 00	RW	-	auxiliary data 000 / send msg 00
…..				
0x018F	AUX DATA 15	RW	-	auxiliary data 15 / send msg 15
0x0190	AUX DATA 16	R	-	auxiliary data 16 / receive msg 00
….				
0x019F	AUX DATA 31	R	-	auxiliary data 31 / receive msg 15
0x01A0	AUX DATA 32	RW	-	auxiliary data 32 / mi2c write buf 00
….				
0x01AF	AUX DATA 47	RW	-	auxiliary data 47 / mi2c write buf 15
0x01B0	AUX DATA 48	R	-	auxiliary data 48/ mi2c read buf 00
….				
0x1BF	AUX DATA 63	R	-	auxiliary data 63 / mi2c read buf 15
0x01C0	AUX DATA 64	RW	-	auxiliary data 64
….				
0x01FF	AUX DATA 127	RW	-	auxiliary data 127
0x0200	AUX DATA 128	RW	-	auxiliary data 128/ dts send msg 000
….				
0x027F	AUX DATA 255	RW	-	auxiliary data 255 / dts send msg 127
0x0280	AUX DATA 256	R	-	auxiliary data 256 / dts receive msg 000
….				
0x02FF	AUX DATA 383	R	-	auxiliary data 383 / dts receive msg 127

8 Application information

This chapter is aimed at providing some application hints, including the reference schematic, PCB layout guidelines, minimum components required to properly run the application, and other aspects.

8.1 Reference application

The STWLC98 typical application schematic for receiver (Rx) and transmitter (Tx) modes are shown below. The typical component values for a power receiver capable of 50W output power are listed in the tables below.

Figure 9. STWLC98 basic application diagram in Rx mode

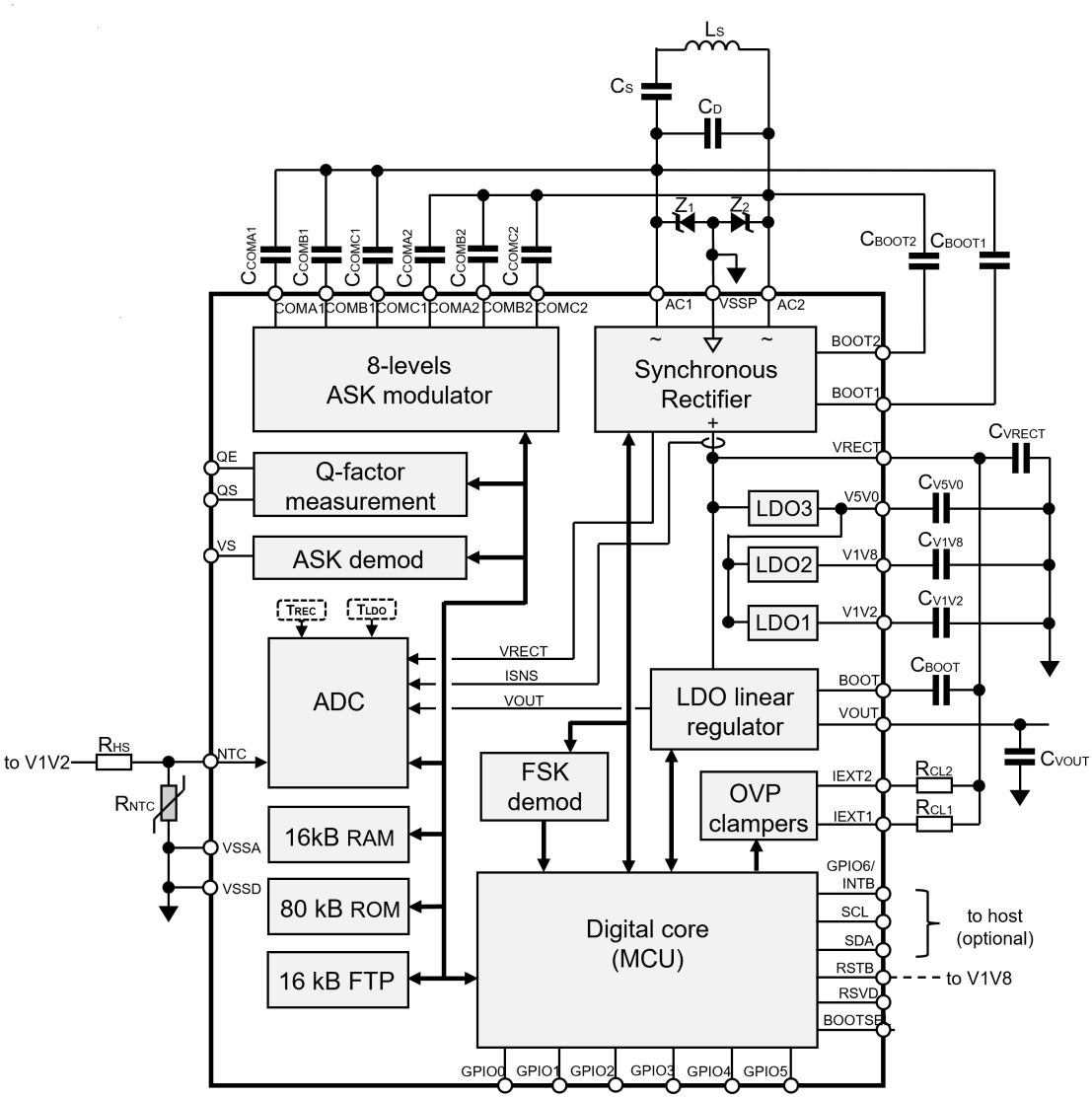


Figure 10. **STWLC98 basic application diagram in RTx mode**

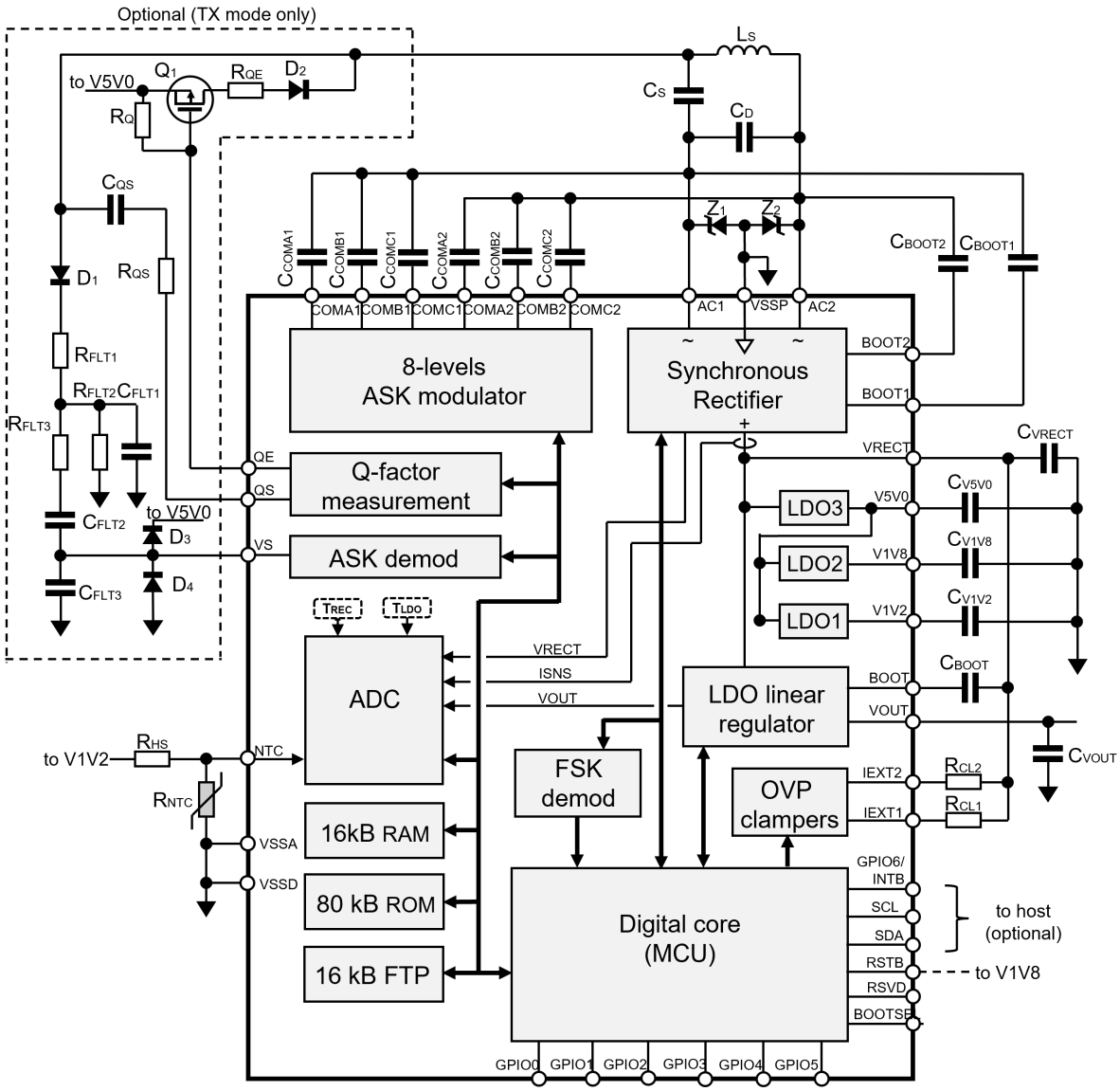


Table 30. **Typical components list for a 50 W RTx application**

Component	Value	Manufacturer	Part Number	Notes
LS	8µH	LUXSHARE	LD81FP008-1H	Receiving coil
CS	100nF/50V	WURTH	4x 885012206095	Series resonant capacitor
CD	3.3nF/50V	WURTH	885012206086	Parallel resonant capacitor
CBOOT1, CBOOT2	47nF/50V	WURTH	885012206093	Bootstrap capacitor
CBOOT	4.7nF/50V	WURTH	885012206087	Bootstrap capacitor
CCOMA1,CCOMA2	22nF/50V	WURTH	885012206091	ASK modulation capacitors
CCOMB1,CCOMB2	10nF/50V	WURTH	885012206089	ASK modulation capacitors
CCOMC1,CCOMC2	4.7nF/50V	WURTH	885012206087	ASK modulation capacitors

Component	Value	Manufacturer	Part Number	Notes
CV5V0	4.7uF/50V	WURTH	885012106012	V5V0 filtering capacitor
CV1V8,C1V2	1µF/25V	WURTH	2x 885012206052	V1V8,V1V2 filtering capacitors
CVRECT	10µF/50V	MURATA	4x GRM21BR61H106KE43L	VRECT filter capacitor, rating depending on application
CVOUT	10µF/50V	MURATA	1xGRM21BR61H106KE43L	OUT filter capacitor, rating depending on application
Z1,2	TVS	LITTLEFUSE	SMJ22A	TVS protection diodes
RCL1	200R	PANASONIC	2xERJ-UP6J101V	clamping resistor
RCL2	91R	PANASONIC	2xERJ-UP6J470V	clamping resistor
RFLT1	5.1K	YAGEO	RC0603FR-075K1L	ASK demod filter resistors(optional TX only)
RFLT2	220K	YAGEO	RC0603FR-07220KL	ASK demod filter resistors(optional TX only)
RFLT3	10K	YAGEO	RC0603FR-0710KL	ASK demod filter resistors(optional TX only)
D1,D2,D3,D4		ROHM	1N4448HLP-7	ASK demod circuit(optional TX only)
CFLT1	5nF/50	WURTH	2x 885012206089	ASK demod filter capacitors(optional TX only)
CFLT2	22nF/50	WURTH	885012206091	ASK demod filter capacitors(optional TX only)
CFLT3	680pF/50V	WURTH	885012206082	ASK demod filter capacitors(optional TX only)
CQS	470pF/50V	WURTH	885012206081	Q factor circuit (Optional TX only)
RQS	10K	YAGEO	RC0603FR-0710KL	ASK demod filter resistors(optional TX only)
RQE	75R	YAGEO	RC0603FR-0775RL	ASK demod filter resistors(optional TX only)
RQ	100K	YAGEO	AC0603FR-07100KL	ASK demod filter resistors(optional TX only)

Note: All of the components listed above refer to a typical application. The operation of the application may be limited by the choice of these external components, such as voltage ratings, current and power dissipation capability, etc.

The basic application schematic is relatively simple since the STWLC98 does not require many external parts to operate. However, there are different aspects that must be carefully considered to properly design a customized application. In most cases, the main constraints are limited PCB size/room and thickness, which unavoidably lead to crowded solutions with far-from-optimal electrical and thermal performance.

8.2 External components selection

RX series resonant circuit components

Series resonant circuit, both Cs and Cd should show excellent quality factor, relatively high RMS current capability and superior capacitance stability in the frequency range of interest.

Multi-Layer Ceramic capacitors (MLCCs) are inherently good devices in terms of RMS current capability and quality factor. Capacitance tolerance and stability strongly depend on the dielectric type.

Dielectrics such as X5R ,X7R,COG are used to achieve higher capacitance per volume at the cost of lower accuracy and undesired dependencies (e.g. DC-biasing, temperature, etc.).

In practice, the C_S(most critical) usually consists of a few smaller, low-profile X5R/X7R capacitors connected in parallel. The parallel connection also helps to increase RMS current capability and mitigate the effect of capacitance tolerance due to production spread.

The voltage rating for these capacitors is usually maximized to take into account the voltage developed in proximity to resonance: 50V-rated capacitors are generally a good choice.

ASK modulation capacitors

The capacitors at the COMAx/COMBx/COMCx pins are connected to the AC1-AC2 terminals through controlled switches (ASK modulator): the de-tuning effect of closing these switches results in an amplitude modulation detected by the transmitter and also visible at the rectified voltage.

Positive or negative modulation may occur, depending on the operating frequency and other factors.

The ASK modulation index clearly depends on the capacitance value of these capacitors, whose value has to be adjusted in case of a heavy negative modulation at VRECT (that is generally undesirable).

The same considerations made above for the resonant capacitors is also applicable here, where capacitance tolerance is less critical: X5R dielectric-type are a good choice and an initial value of 22 nF is typically doing the job.

VRECT over-voltage clamping resistor

The voltage at the VRECT pin is primarily dictated by the transmitter, whose operating point is linked to the feedback information received via ASK modulation.

Unexpected conditions, however, may increase the VRECT voltage to dangerous values (close to AMR levels). A sudden change in relative alignment between the transmitting and receiving coils, for example, could result in a dramatic change in coupling factor and, in turn, a fast-rising voltage.

Since the reaction of the transmitter is relatively slow, the STWLC98 protects itself by closing the switch internally connected to the IEXT1,IEXT2 pins. The switch is externally connected to VRECT via a resistor (R_{CL}) to implement an active clamper.

The value of R_{CL} is selected so that most of the power is dissipated in the clamper circuit rather than inside of the chip. Special resistors (surge resistors) capable of withstanding higher energy pulses are recommended.

ESD protection diodes

Since the receiving coil is a easy entry point for ESD (relatively large area with remarkable capacitive coupling), a good application design should consider protections for the most exposed pins: AC1 and AC2.

Uni-directional Transient Voltage Suppression (TVS) diodes at both pins are recommended.

ESDs have essentially a common-mode nature and, although the receiving coil has low DC-resistance, its AC impedance may appear quite high to fast voltage spikes: independent clamping at AC1 and AC2 pins is thus mandatory.

The knee-voltage of the TVS diodes should be selected considering the maximum VRECT voltage plus some margin to avoid non-negligible leakage current at higher temperature, while their energy dissipation capability should be maximized considering the size of the package.

Coil thermal protection

Maximizing the amount of transferred power is ofter desirable, but also limited by operating conditions : applications in which the wireless power receiver has poor power dissipation capability and/or the power loss in the receiving coil is relevant (e.g. very tiny and slim coils with relatively high DC-resistance) may require some thermal protection.

This feature is implemented with STWLC98 thanks to its NTC pin. A channel of the internal ADC is routed to the NTC pin, allowing the user to read the voltage across an external NTC thermistor.

8.3 PCB routing guidelines

1. Power traces (AC1, AC2, VRECT, VOUT) and power ground traces should be kept wide enough to sustain high current. Duplicating these traces in inner layers , adding vias is advisable wherever possible to lower impedance as low as possible.
2. AC1, AC2, BOOT1, BOOT2, COMAx, COMBx and COMCx are some source of noise in the board Good Shielding of these traces (by running ground planes below).
3. Power ground(VSSP) will carry the sum of ripple current from V_{RECT}/$C_{RECT}$and DC current from VOUT/ Load, return paths from LDO caps should avoid these high currents.
4. AC1 and AC2 tracks should be routed closely to minimize the area of the resulting loop.
5. Communication signals (I2C), Sensing and Input monitoring signals to be routed away from High di/dt (AC1,AC2,COMAx,COMBx,COMCx,BOOT) switching signals , to Minimize interference.
6. COMM1,COMM2,BOOT1,BOOT2 capacitors should be placed close to the device.
7. CRECT and COUT capacitors should be placed close to device , to avoid large current loops.
8. Auxiliary LDO capacitors C5v0 ,C1v2 and Cv18 should be placed as close as possible to the device.
9. Tracks connection should be short and placed in top layer. Capacitors ground can be connected directly into GND plane.
10. Thermal performance and grounding should be optimized by preserving bottom layer (usually assigned to ground) integrity.

8.4 FTP (Few Times Programmable Memory)

STWLC98 has a 16kB FTP which allows for multiple erase/re-write cycles.

This provides flexibility for custom firmware needed for various applications like proprietary protocols or field firmware upgrades.

FTP also offers design in flexibility during preproduction optimization.

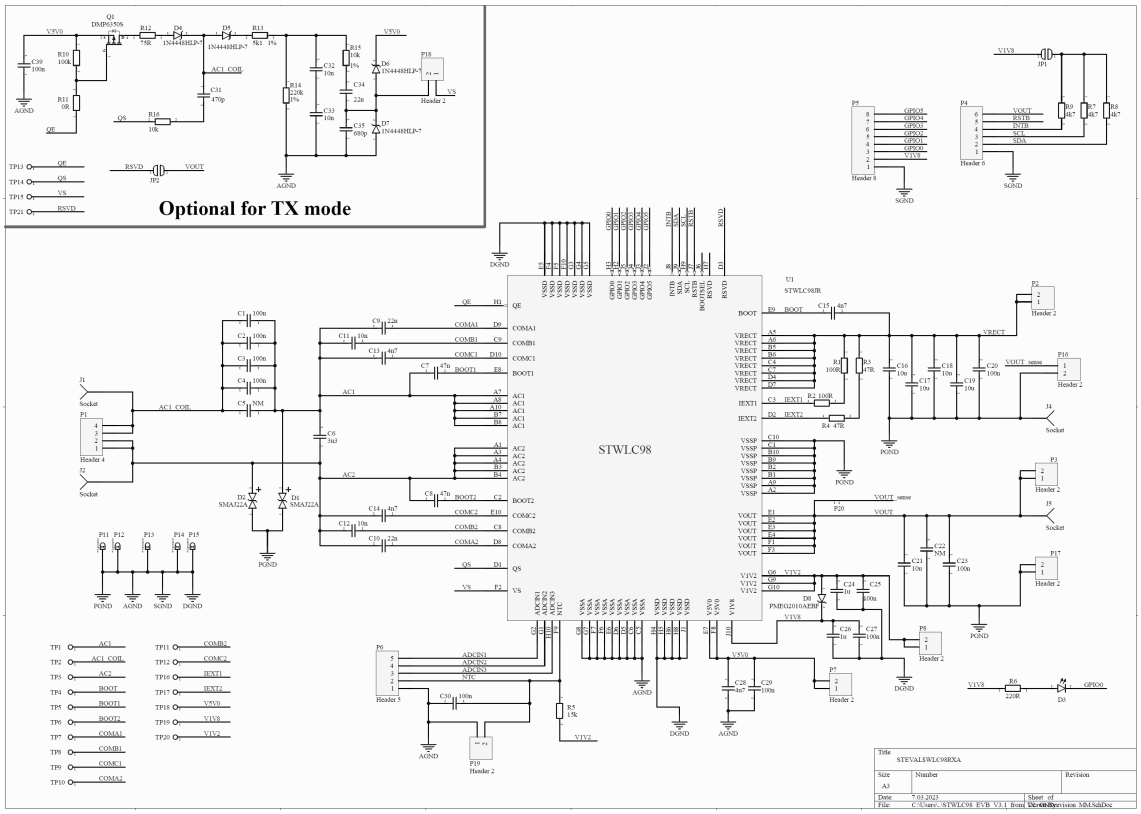
FTP programming can be done in standalone mode, applying 5V (USB-VBUS 5V) to VOUT pin.

Using USB-I2C interface to PC GUI tool.

9 Reference schematic

Typical application schematic for the STWLC98 is shown below. The values reported in and refer to typical Wireless Power Receiver applications capable of an output power of 50W.

Figure 11. STWLC98 50W schematic diagram



Note: All the above components refer to a typical application. Operation of the device in the application may be limited by the choice of these external components (voltage ratings, current and power dissipation capability, etc.).

10 Glossary/Abbreviations

- ADC: Auxiliary Data Control
- ADT : Auxiliary Data Transport
- ASK: Amplitude Shift Keying
- BPP : Baseline Power Profile
- CHS : Charge Status
- CEP: Control Error Packets
- CFG : Configuration
- DSR : Data Stream Response
- DTS : Data Transport Stream
- EPP: Extended Power Profile
- EPT: End Power Transfer
- FOD : Foreign Object Detection
- FSK: Frequency Shift Keying
- FTP: Few Times Programmable
- ID: Identification
- PCH: Power Control Hold-off
- PP: Proprietary Packet
- RP/RP8: Received Power Packet
- SRQ : Specific Request
- SS/SIG : Signal Strength Packet
- XID : Extended Identification

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 Package information

Figure 12. WLCSP90 4.289mmx3.869mm 0.4 Pitch 0.25 Ball package outline

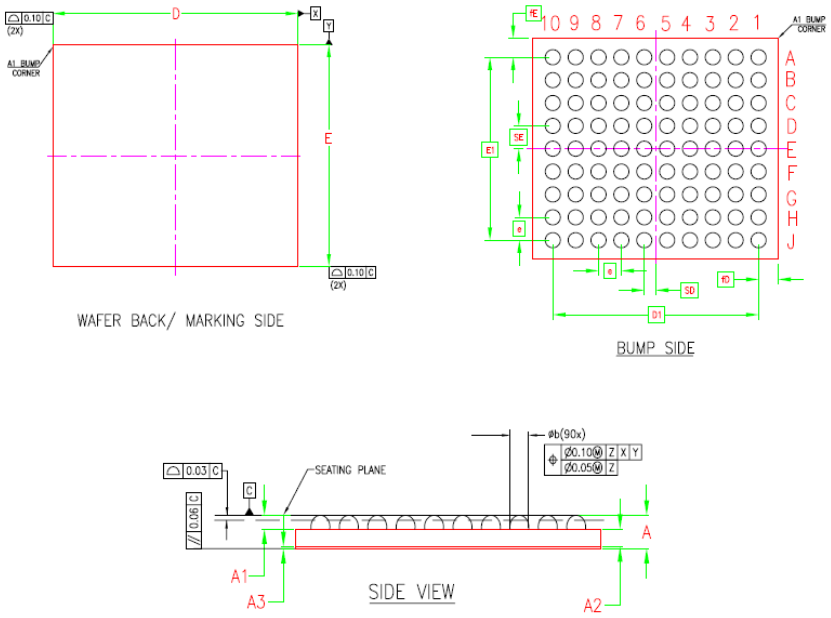


Table 31. **WLCSP90 4.289mmx3.869mm 0.4 Pitch 0.25 Ball mechanical data**

Ref	Data range (mm)		
	Min	Typ	Max
A	0.450	0.471	0.492
A1	0.181	0.196	0.211
A2	0.235	0.250	0.265
A3	0.022	0.025	0.028
b	0.243	0.268	0.293
D	4.269	4.289	4.309
D1		3.60	
E	3.849	3.869	3.889
E1		3.20	
e		0.400	
SE		0.400	
SD		0.200	
fD		0.345	
fE		0.334	
ccc		0.03	

Figure 13. **Recommended footprint**

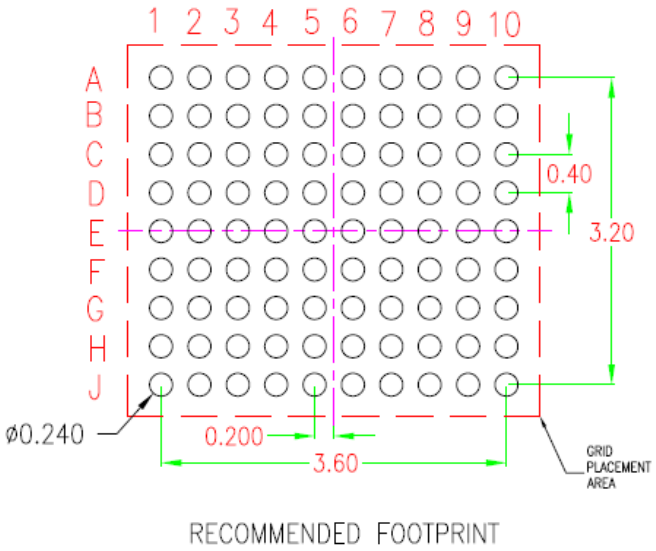
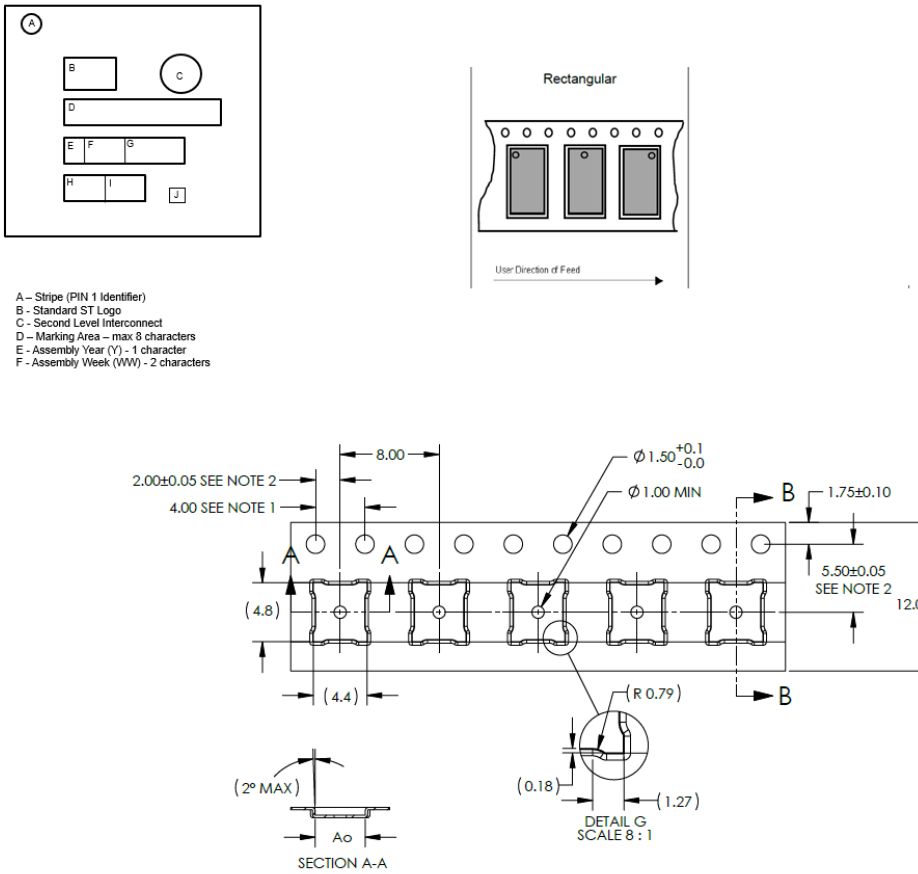


Figure 14. Device marking ,Tape and reel information



Revision history

Table 32. **Document revision history**

Date	Version	Changes
15-July-2023	1	Initial release.

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