STi7197

Advanced STB decoder with integrated QAM demodulator

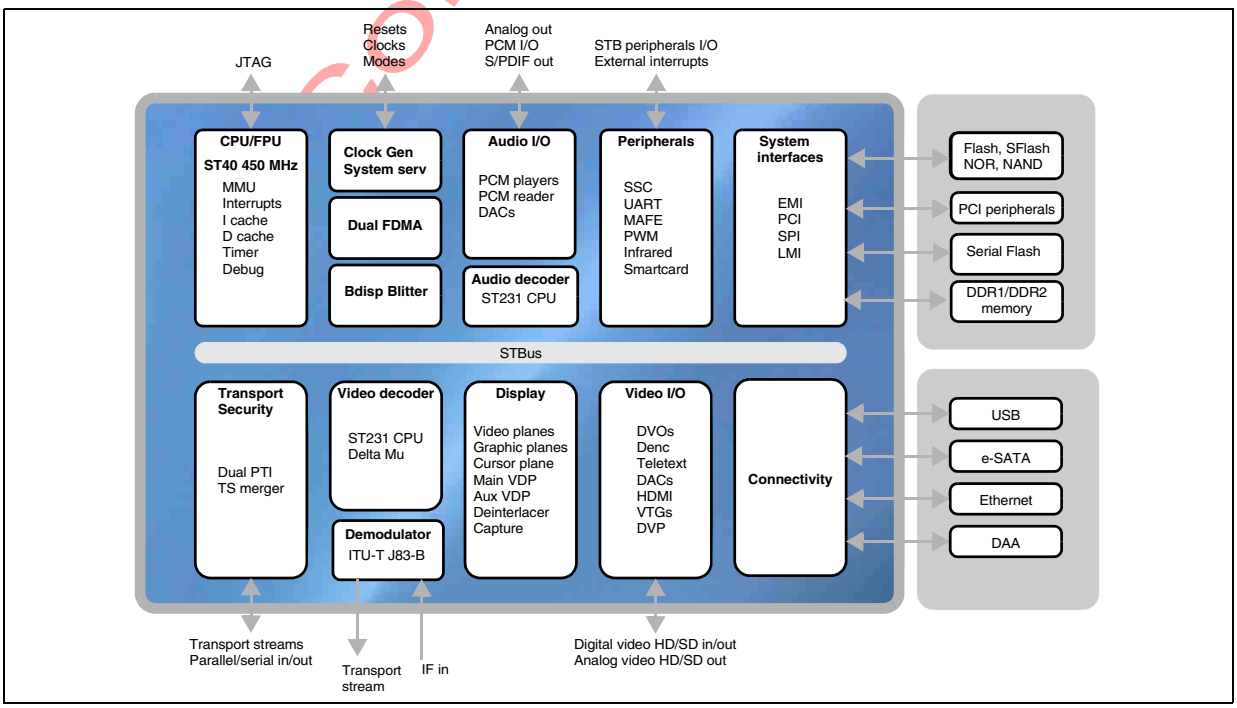
Features

- ITU-T J83 Annex B compliant
- 256 QAM (quadrature amplitude modulation) demodulation and FEC (forward error correction) sub-system
- Advanced high-definition video decoding (H.264/VC-1/MPEG2)
- Advanced standard-definition video decoding (H.264/VC-1/MPEG2/AVS)
- Advanced multi-channel audio decoding (MPEG 1, 2, MP3, DD/DD+, AAC/AAC+, WMA9/WMA9Pro)
- DVD data decryption
- Multi-stream, DVR capable transport stream processing
- Linux, Windows CE and OS21 compatible ST40 applications CPU (450 MHz)
- 32-bit DDR1/DDR2 compatible local memory interface
- Extensive connectivity (dual USB 2.0 host ports, e-SATA, Ethernet MAC/MII/RMII, and PCI)
- Advanced security and DRM support including SVP, MS-DRM, and DTCP-IP

Description

The STi7197 is an advanced STB decoder with an integrated QAM demodulator, suitable for cable networks conforming to the ITU-T J83-Annex B standard (for example, US cable).

The STi7197 integrates multi-stream transport demultiplexing, audio video decode, video processing, graphics and display handling, STB peripherals, audio video DACs, digital audio video outputs, PCI, e-SATA, dual USB ports, an Ethernet GMAC controller and ST40 applications CPU.



Contents

1 Related documents

This datasheet is part of the STi7197 documentation suite which forms a complete system description and programming guide. This datasheet is intended for hardware engineers, and describes the pins, package, electrical characteristics, and timing information for the STi7197 device.

To obtain an up-to-date specification of this product, this datasheet should be read in conjunction with the latest relevant product errata sheet (buglist). If an errata sheet for this product exists, it will be obtainable from your STMicroelectronics representative.

The documents related to this datasheet are described in the following sections.

1.1 STi7197 programming manual

The *STi7197 programming manual* describes how to program and configure the STi7197 device. It is intended for software and system engineers.

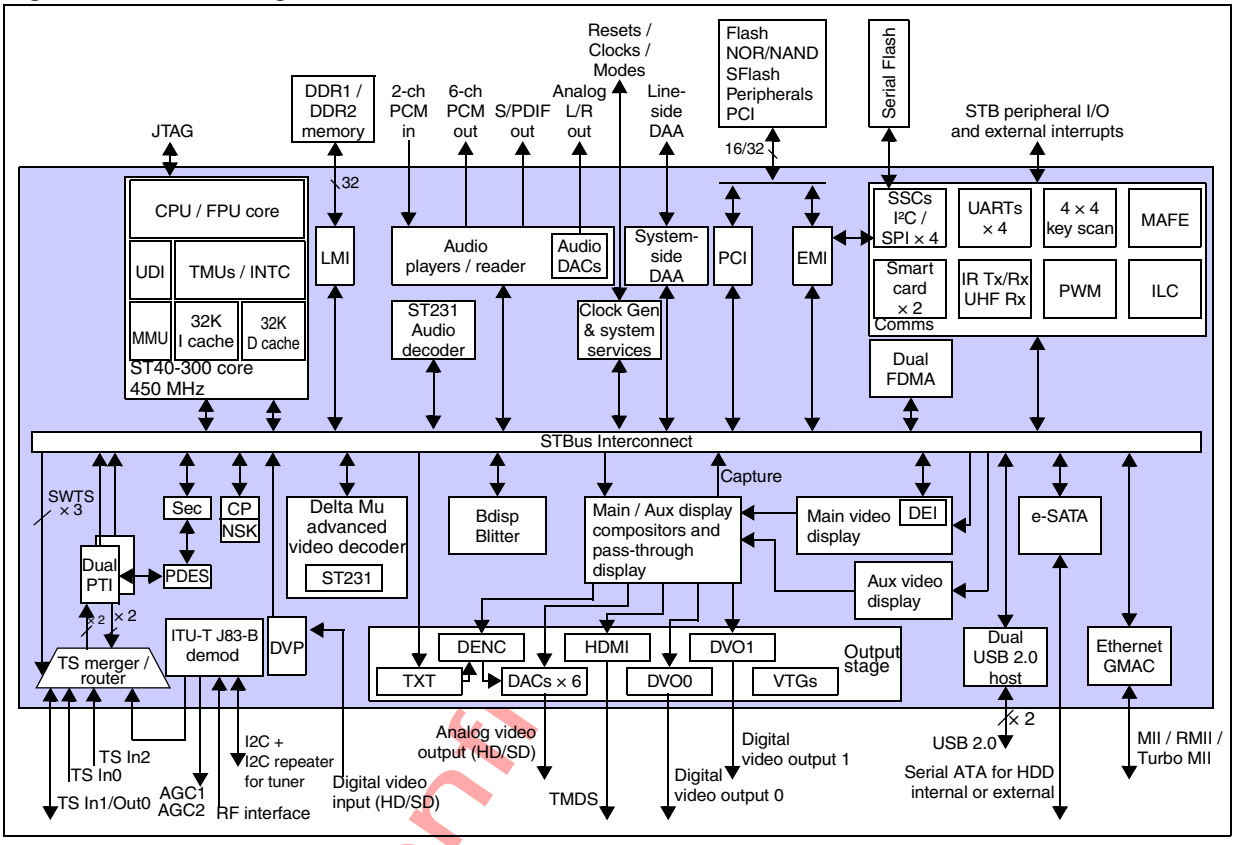
1.2 CPU documentation

The ST40 core and its instruction set are documented in the *ST40 32-bit CPU Core Architecture Manual.*

The ST231 core and its instruction set are documented in the *ST231 CPU Core and Instruction Set Architecture Manual.*

2 Functional overview

Figure 1. Block diagram of the STi7197



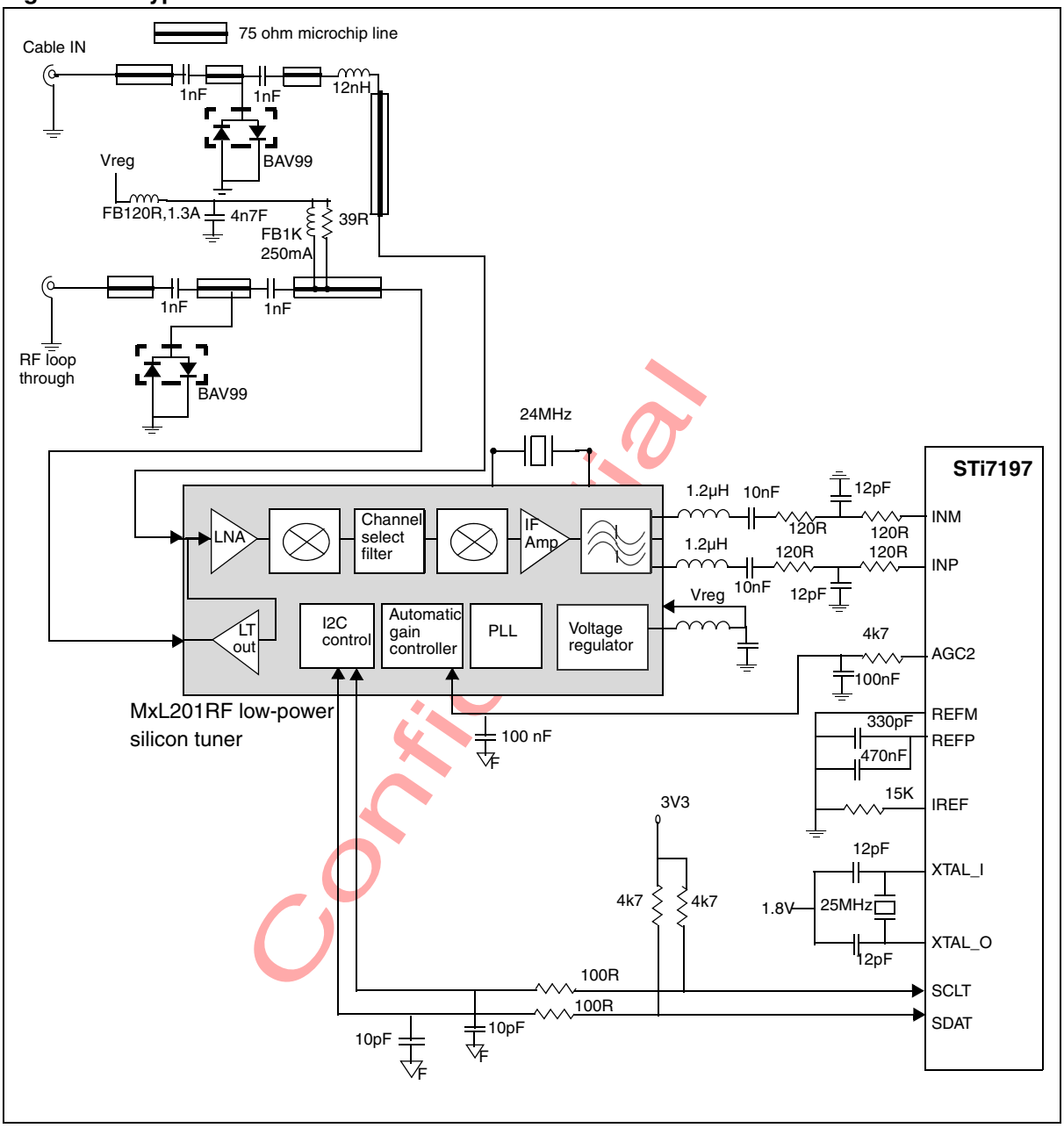
2.1 Front end

The STi7197 is designed to be optimized, both in cost and performance, with the most advanced Can and Silicon tuners available in the market and is compliant with the ITU-T J83 Annex B standard.

The STi7197 front end has one of the lowest power consumptions in the market today. This has been made possible because of technology and clock rate management. This also has the advantage of improving the channel acquisition and re-acquisition efficiency.

The *Figure 2* shows an application diagram for a typical front-end receiver circuit that can be used with the STi7197.

Figure 2. Typical front-end receiver circuit



2.2 QAM demodulator/FEC

The STi7197 front-end QAM section provides quadrature amplitude modulation (QAM) demodulation and forward error correction (FEC). The front end performs IF-to-MPEG2 block processing of QAM signals. It is intended for the digital transmission of compressed television, video, sound, and data services over cable, and is fully compliant with ITU-T J83 Annex B specification bitstreams. It can handle square (16, 64, 256-QAM) and non-square (32, 128-QAM) constellations.

The IF can be up to 57 MHz, and the sampling clock can be selected freely from a given range (constrained by the SAW filter and symbol rate characteristics). All further processing is fully digital, so no external feedback loop is required. The STi7197 handles a wide range of symbol rates, from the highest practical rates to rates as low as 0.87 Mbaud, even when there is a significant frequency offset.

The STi7197 provides all demodulation and FEC functions required for the recovery of QAM bitstreams with outstanding BER results. In addition, it includes several features that give simple and immediate access to various quality and status monitoring parameters.

The demodulator provides error-corrected MPEG transport stream outputs, which can be routed to the transport sub-system.

2.3 IF to MPEG2 TS block conversion

A high-performance 12-bit ADC samples, at sampling rates up to 60 MHz, and down-converts to baseband the intermediate frequency (IF) differential carrier signal produced by CATV tuners. The signal is then demodulated by the QAM demodulator to recover a byte stream. The FEC block then performs trellis decoding, convolutional de-interleaving, Reed–Solomon decoding, and de-randomizing to provide an MPEG2 transport stream. The QAM/FEC processing is fully compatible with ITU-T J83 Annex B streams up to 256 QAM.

2.4 Transport

The front-end demodulator outputs an error-corrected MPEG transport stream for routing to the transport subsystem. The STi7197 receives transport streams from broadcast networks through three parallel/serial transport stream inputs and one serial transport stream input. The fourth transport interface can be configured as a fourth input or as an output. Transport stream routing for DVB-CI+ (HD/SD profiles) modules can also be supported. One of the transport inputs is dedicated to the output of the internal QAM demodulator.

Transport streams are processed by two integrated programmable transport stream engines (PTIs). These perform demultiplexing, descrambling, and section filtering on multiple transport streams received from Broadcast, IP, and HDD sources.

2.5 Connectivity

The STi7197 has a wide range of options for connecting to external peripherals or IP network devices, such as wired Ethernet, xDSL, and Wi-Fi. These interfaces enable the delivery of IP streams received over broadband networks and support streaming over home networks. These interfaces include two USB host ports, a 32-bit PCI interface, and a high-speed Ethernet MAC/MII/RMII interface.

PCI uses the same physical interface as the EMI with dynamic interleaving of access types possible. Transport streams received through IP can be routed internally to the PTIs for demultiplexing and descrambling similar to the broadcast TS streams. The PTIs can concurrently process multiple TS streams from both sources.

2.6 Audio/video decoding

The STi7197 can decode H264, VC-1/WMV9, and MPEG2 HD and SD streams with concurrent decoding of one HD stream and one SD stream possible for PIP applications. AVS SD decoding is also supported. Multiple decoding of lower resolution streams can also be supported for Mosaic applications. The decoder is well proven in the industry and is powerful and flexible enough to decode other video formats, such as MPEG4 part2 and DivX (3.x, 4.x, and 5.x). It can also support concurrent H263 encode and decode for video conference applications.

A programmable ST231 CPU core provides the flexibility and performance for decoding multi-channel advanced audio streams. Concurrent decoding of an audio description channel is also supported.

2.7 Graphics and display

The STi7197 integrates a graphics and display sub-system that can deliver a high quality visual experience for applications. Graphics generation can use both the CPU and an independent multi-operator graphics accelerator that supports 2D graphics and 3D user interface effects. Graphics can be displayed on any one of three graphics planes. The graphics planes are combined, with video, using alpha blending and color keying. The graphics and video are combined by two independent display compositors, one for the Main TV and a second for output to a VCR or DVD-R. Two video planes are available for PIP on the main composition or downscaled video on the second composition. Video post-processing can be applied to resize, reformat, and de-interlace video between the encoded and intended display formats prior to composition. Advanced de-blocking and de-ringing processing can be applied to decoded MPEG2 SD video. With such capabilities, feature-rich displays can be generated including PIP, POP, Mosaics, animations, highlighting, blended overlays, scrolling subtitles, and so on.

2.8 Audio/video outputs

The STi7197 has both HDMI and analog interfaces for outputting video to the TV/panel. In addition to the standard 720p and 1080i HD formats, the STi7197 supports 1080p60 display output on the HDMI interface. The analog interface comprises six video DACs with CGMS-A, Rovi™, and Dwight-Cavendish copy protection, whilst the HDMI interface supports the HDCP copy protection. For more information on HDMI features supported, refer to *Section 2.13*.

Audio is output over HDMI, S/PDIF, stereo analog DACs, and a digital PCM output interface. It is possible to output both compressed and decoded audio streams at the same time over different interfaces (for example, Dolby Digital 5.1 over S/PDIF with decoded and downmixed AAC-plus audio through the analog output). A 2-channel PCM input is also available for inputting audio from external sources such as a microphone (for example, for VOIP telephony).

2.9 Processors

The STi7197 embeds the latest ST40 class applications processor, the ST40-300 with 2–way, set associative caches, a 32 K instruction cache, and a 32 K data cache. At an operating frequency of 450 MHz it can deliver > 800 DMIPs performance[(a)].

2.10 System interfaces

The STi7197 supports the latest DDR2 memory technology on its 32-bit local memory interface (LMI) providing a high bandwidth unified memory for code, data, audio and video buffers, graphics and so on. With two 2-Gbit devices in a ×16 configuration, up to 512 Mbytes capacity can be supported. The STi7197 also retains the ability to support DDR1 memory types.

A 16-bit external memory interface (EMI) is used for connecting to Flash and SRAM/peripherals supporting a standard 8/16-bit asynchronous read/write protocol. Synchronous or burst mode can also be supported. Both NOR and NAND Flash types can be used, with the ability to boot from, and perform code authentication checking from both types. Interfacing and authenticated booting from serial Flash attached through SPI is also supported.

2.11 DVR

The STi7197 supports attachment of an HDD through e-SATA, USB, or EIDE (PIO mode) allowing DVR STBs to be developed. The e-SATA interface can independently support either internal or external SATA drive attachment. The STi7197 can support recording of up to four HD streams with local playback of an HD stream with trick modes, as well as playback of additional streams for export to client STBs over a home network. Streams can be encrypted to/from the HDD and to/from a home network for copy protection using AES, T-DES, or DES ciphers.

2.12 STB peripherals

The STi7197 integrates a range of peripherals and interfaces to minimize or eliminate the external cost of implementing basic STB functions. These include UARTs and SSCs used for serial interfaces, I²C control buses, two smartcard controllers, a PWM module, IR receiver and transmitter, general-purpose programmable I/O, external interrupt inputs, and a controller for scanning/debouncing a 4 × 4 key matrix. There are also two options available for implementing a software modem on the STi7197; a MAFE interface to connect to an external modem codec and integration of a system-side DAA circuit to connect to an external line-side DAA device. For HDMI interfacing, a dedicated I²C port is available, together with a hardware CEC line controller.

a. An extended mode of STi7197 can enable the operation of ST40-300 at 600 MHz that can deliver > 1100 DMIPS performance. Contact customer support for application note and guidance.

2.13 HDMI interface

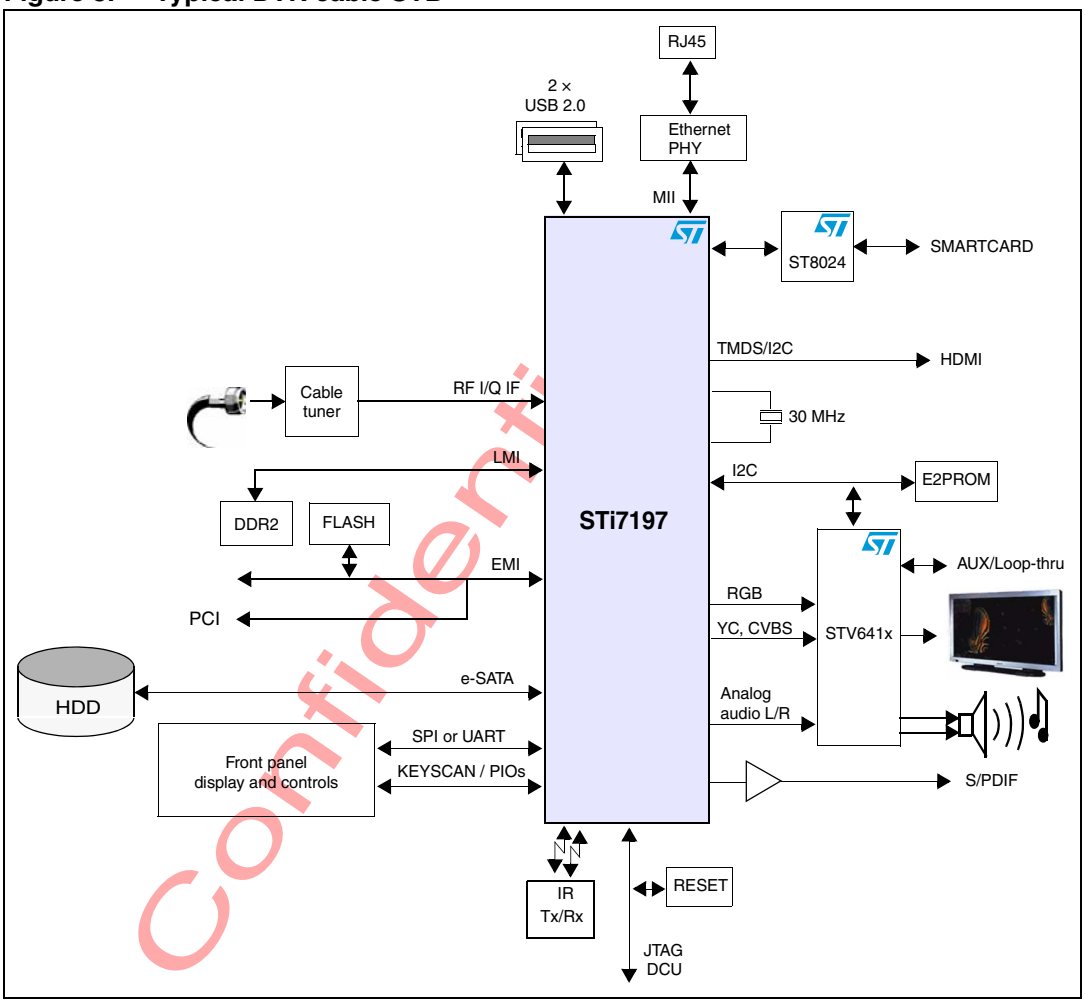
The STi7197 supports the following features compliant to HDMI 1.4a specification:

- 3D video
  - 3D video format timings — Video resolution up to 1920 x 1080p @60 Hz
  - 3D over HDMI — Side-by-side (Half) and Top-and-Bottom formats
- Content Type
- Audio formats — LPCM, Dolby Digital, and Dolby Digital Plus
- CEC
- HDCP

2.14 Target applications

2.14.1 Cable applications

Figure 3. Typical DVR cable STB



3 System on chip subsystem overview

This section gives a top-level overview of the device components.

3.1 ITU-T J83 Annex B demodulator/FEC

- High-performance integrated 12-bit A/D converter suitable for direct IF architecture in all quadrature amplitude modulation (QAM) modes
- Decodes ITU-T J83-Annex B bit streams
- Forward error correction (FEC) compliant with ITU-T J83-Annex B with integrated de-interleaving SRAM
- Supports 16, 32, 64, 128, and 256 point constellations
- Two automatic gain control (AGC) outputs suitable for delayed AGC applications (sigma-delta outputs)
- Integrated signal quality monitors, plus lock indicator and interrupt pins
- RF signal loss detection and automatic recovery
- Easy controlling and monitoring using two-wire fast I²C bus
- Additional I²C bus (I²C repeater) dedicated to tuner control for minimum tuner disturbance

3.2 STBus interconnect

The STBus multipath unified interconnect provides high on-chip bandwidth and low latency accesses between modules. The interconnect operates hierarchically, with latency-critical modules placed at the top level. The multipath router allows simultaneous access paths between modules, and simultaneous read and write phases from different transactions to and from the modules. Split transactions maximize the use of the available bandwidth.

3.3 Processor core

The STi7197 integrates a 450 MHz ST40-300 processor core that features a 32-bit superscalar RISC CPU and IEEE-754 compliant floating point unit (FPU). The ST40-300 includes 2-way, set-associative caches and an interrupt controller with 15 user interrupt sources and an interrupt expansion port.

3.4 External memory interface (EMI)

The EMI is a general-purpose interface for attaching Flash memory and peripherals. The EMI features are:

- Five banks
- Addressing up to at least 64 Mbytes of NOR Flash
- External bus master support through BUSREQ/BUSGNT signals
- Slave mode EMI support
- Single level cell (SLC) NAND Flash and boot from SLC NAND Flash
- Serial Flash support
- PCI interface, host and device selected on boot
- ATAPI PIO mode 4
- DVB-CI+

3.5 Local memory interface (LMI)

The STi7197 integrates one 32-bit DDR2-DDR1 interface. The interface can run up to 400 MHz when configured in DDR2 mode or up to 250 MHz when in DDR1 mode.

The LMI supports 32-bit configurations, including:

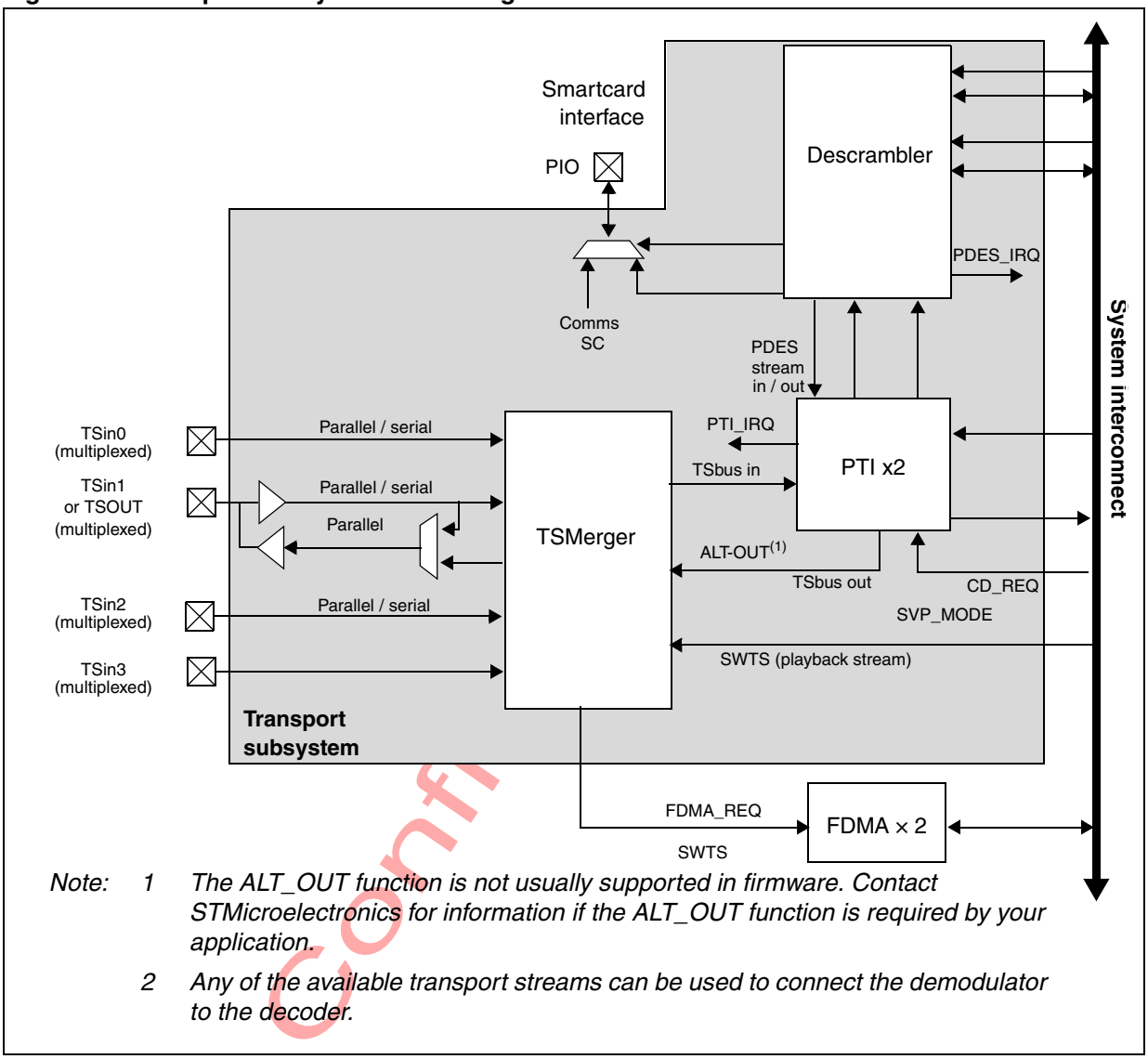
- 2 × 512 Mbits (×16) devices resulting in 128 Mbytes memory space
- 4 × 512 Mbits (×8) devices resulting in 256 Mbytes memory space
- 2 × 1 Gbits (×16) devices resulting in 256 Mbytes memory space
- 2 × 2 Gbits (×16) devices resulting in 512 Mbytes memory space
- 4 × 1 Gbits (×8) devices resulting in 512 Mbytes memory space

3.6 STB transport subsystem

3.6.1 Overview

The transport subsystem (TS) is able to receive ATSC, DVB, DIRECTV, DCII, OpenCable, ARIB BS4 transport streams containing high-definition (HD) and standard-definition (SD) programs. It demultiplexes and descrambles the transport streams to deliver PES packets to the video and audio decoders.

Figure 4. Transport subsystem block diagram



Note: 1 The ALT_OUT function is not usually supported in firmware. Contact STMicroelectronics for information if the ALT_OUT function is required by your application.

2 Any of the available transport streams can be used to connect the demodulator to the decoder.

The STi7197 receives transport streams from broadcast networks through three parallel/serial transport stream inputs and one serial transport stream input. The fourth transport interface can be configured as a fourth input or as an output. Note that one of the transport inputs is dedicated to the output of the internal QAM demodulator/FEC.

Transport streams are processed by two integrated programmable transport stream engines (PTIs). These perform demultiplexing, descrambling, and section filtering on multiple transport streams received from Broadcast, IP, and HDD sources.

3.6.2 Dual programmable transport interface (PTI)

Each PTI is a dedicated transport engine and integrates its own CPU to handle the transport stream PID filtering, demultiplexing, descrambling, and data filtering. It interfaces with the programmable descrambler (PDES) for descrambling. Each PTI receives a transport stream from a dedicated input port, processes it, and outputs it either to the memory through its DMA channels or to a dedicated transport output port.

The PTIs perform PID filtering, demultiplexing, descrambling, and data filtering on up to four transport streams. The PTIs extract PCRs with time stamps and make them available to the CPU for clock recovery and audio/video synchronization.

PES data is transferred by DMA to memory buffers. Section data is transferred by DMA to separate buffers for further processing by the CPU. The PTIs extract indexing information and transfer packets, using DMA, to an intermediate buffer for writing to HDD.

The following transport streams are supported:

- AVS video
- MPEG2 transport stream demultiplexing, and service information extraction, conforming to:
  - MPEG2 systems
  - MPEG4 systems
  - DVB
  - DirecTV DSS format
  - DirecTV AMC stream format
- MPEG2 TS audio/visual formats:
  - MPEG2 A/V over MPEG2 TS
  - H264 video over MPEG2 TS
  - VC-1 over MPEG2 TS
  - WMA9, WMA9 pro over MPEG2 TS
  - AAC and AAC+ audio over MPEG2 TS
- A/V streams encapsulated in RTP packets according to these protocols (parsing):
  - MPEG2 A/V in RTP
  - MPEG 4 pt2 video in RTP
  - MPEG 4 audio including AAC and AAC+ in RTP
  - H264 video in RTP
  - VC-1 video in RTP
  - AVS video in RTP
- Processing of:
  - WMV9/WMA9 streaming content in ASF files using client server interaction
  - Parsing of MP3 or MPEG 4 AAC audio from Audio File format versions 2, 3 and 4
  - A/V streams, such as DivX, delivered in AVI files
  - WAV and AIFF files

Each PTI performs PID filtering to select audio, video, and data packets to be processed. It supports up to 151 PID slots, and routes streams to and from the descrambler. Streams can be descrambled using:

- DES
- TDES
- AES
- Multi-2
- DVB-CSA
- NDS ICAM

Each PTI has a 64 × 16 byte section filter core. Following four filtering modes are available:

- Wide match mode: 64 × 16 byte filters
- Long match mode: 128 × 8 byte filters
- Positive/negative mode: 64 × 8 byte filters with positive/negative filtering at the bit level
- APG filtering mode

Matching sections are transferred to memory buffers for processing by software.

3.7 DVD decryption

CSS (DVD-video), CPRM (DVD-RW), and CPPM (DVD-audio) decryption is provided for the DVD stream.

3.8 Video decoder

The STi7197 video decoding subsystem includes the Delta-Rasta core capable of decoding H264/VC-1/MPEG2 HD/SD streams and AVS SD streams.

The following are Delta-Rasta features:

- Supports H264 in-loop deblocking filter, VC-1 deblocking filter and overlapped transform, AVS deblocking filter, and deblocking and deringing post-processing algorithms for MPEG2
- Supports non-real-time MPEG2 to H264 transcoding

The decoder is partially implemented in software which is executed on a dedicated ST231 CPU core. The decoder gets its data from memory and stores decoded data back into memory.

The decoder uses a mixed hardware and firmware architecture with a hardwired data path and an ST231 core engine. It provides flexibility for firmware upgrades, error concealment, or trick modes. The ST231 core can be used for other coders or decoders at lower resolution, when the VC-1, H264, AVS SD, or MPEG2 decoders are not running.

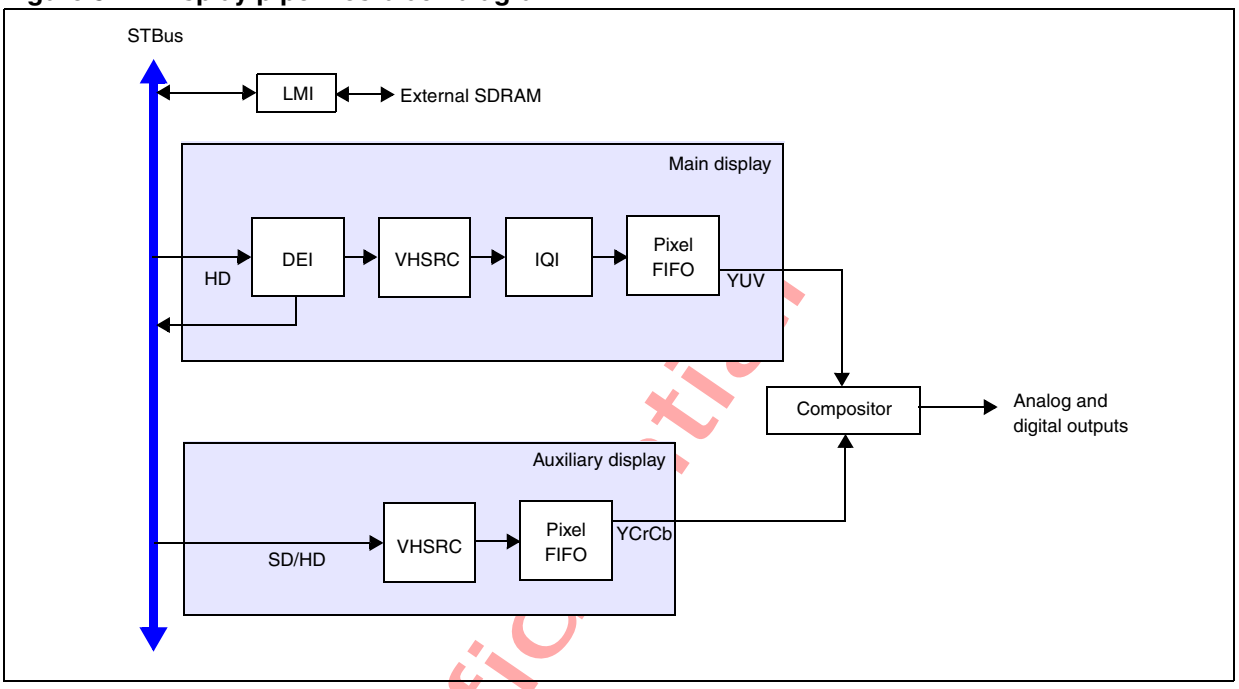
Streams are decoded picture-by-picture from an elementary stream buffer. Decoding, reconstruction, and prediction buffers are set up by the CPU. CPU control of bit-buffer pointers provides flexibility for trick modes and out-of-sequence decoding.

Semantic or syntax errors are detected by the decoder and failing slices are replaced up to the next slice or picture.

3.9 Main and auxiliary display

The main and auxiliary display pipelines form a high-quality scaling engine for video display processing. The two display pipelines are shown in *Figure 5*.

Figure 5. Display pipelines block diagram



The same video is displayed through both pipelines, but each display processor can be set up to format the video differently and to display video with different timing. Separate video timing generators (VTGs) are provided to support this feature. The display processors adapt the decoded video to a format suitable for display, taking into account differences in scanning method, resolution, aspect ratio, and scanning frequency.

The main-display processor receives decoded or acquired video from memory, and performs block-to-line conversion, pan and scan, and vertical and horizontal format conversion. There is also a de-interlacer (DEI) to perform interlace-to-progressive conversion using motion estimation. This is used to display 480i, 576i, or 1080i interlaced sources on a progressive display (480p, 720p, or 1080p). The main display processor has image quality improvement (IQI) that improves the subjective image quality by methods, such as high frequency peaking and edge sharpening.

The auxiliary-display processor receives decoded or acquired (and possibly decimated) video, and performs pan and scan, vertical format conversion, horizontal format conversion, and color tint and saturation control. The output line size is limited to SD on the auxiliary-display processor and is intended to output video for VCR recording.

3.10 Compositor

3.10.1 Overview

The compositor comprises two real-time, multiplane digital mixers.

The main mixer (mixer A), which is intended for main HDTV video output, is composed of:

- one background color
- two video planes (VID1 and VID2)
- three graphics planes (GDP1, GDP2, and GDP3)
- one cursor plane

The auxiliary mixer (mixer B), which is intended for auxiliary SDTV video output, is composed of:

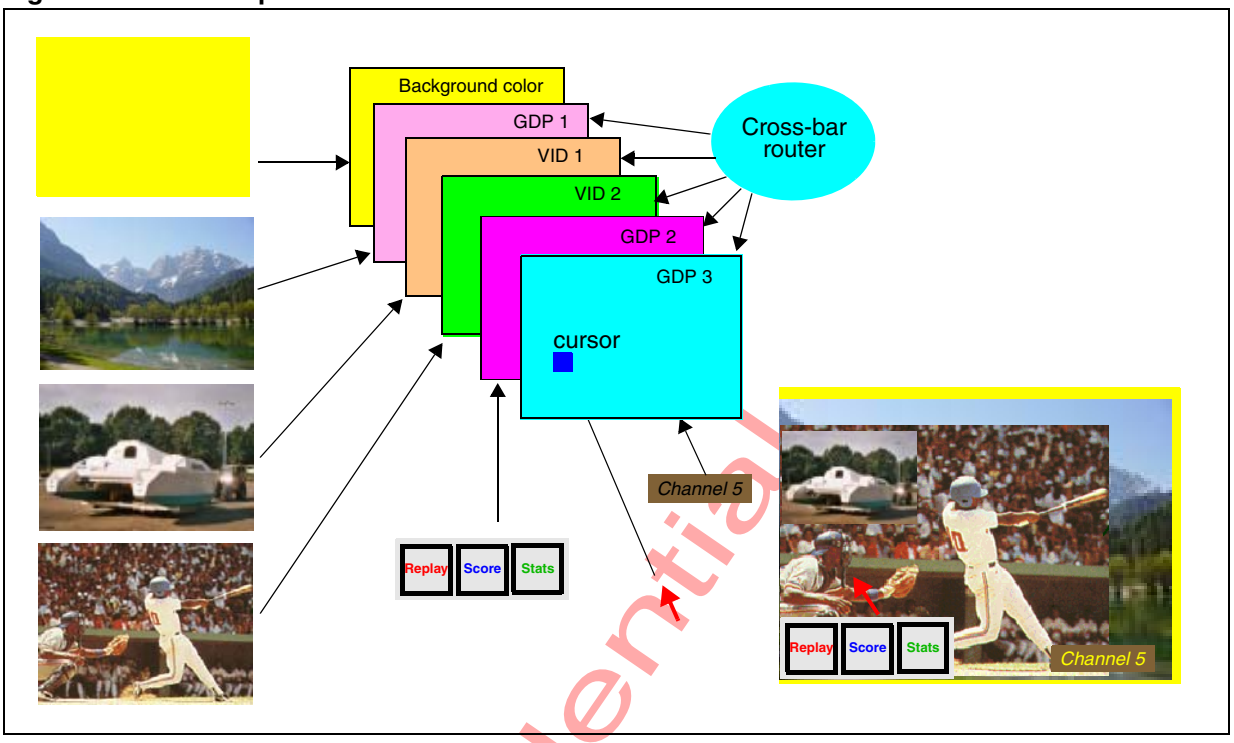
- one background color
- one video plane (VDP2)
- one graphics plane (GDP3)

The compositor receives the video planes from the video display processor, and the 2D graphics planes from the memory through GDP. Each mixer alpha blends graphics and video layers on a pixel basis based on alpha component values provided by each layer.

After real-time processing by the display plane pipelines, pixel data is mixed in mixer A or mixer B. The output of mixer A supports up to full HD resolutions and is intended as the main TV display (*Figure 6*). The output of mixer B (*Figure 7*) supports up to full SD resolutions and is intended as an auxiliary display for applications, including connection to a VCR. The mixer outputs are fed to the STi7197's output stage.

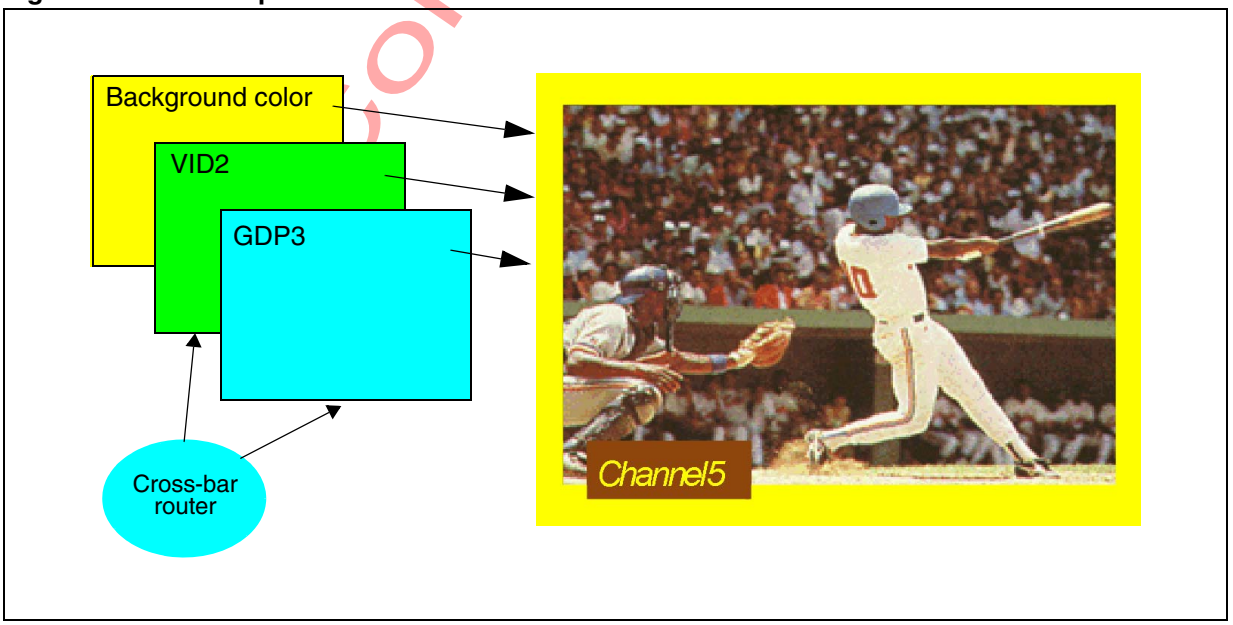
The mixers provide RGB and/or YCbCr digital outputs that are used by the video output subsystem to produce the HDTV video outputs (analog, digital, and composite) and the SDTV video outputs (analog and digital).

Figure 6. Mixer A planes



The compositor also comprises additional components that can be used to enhance the display presentation of video and graphics. These include an alpha plane attachment and a cross-bar router. A capture pipeline is also provided for capturing main video streams or mixer A or B output streams and storing them in memory.

Figure 7. Mixer B planes



3.10.2 Compositor layout

The *Figure 8* shows a block diagram of the compositor. It presents the dataflow and memory access of all compositor modules.

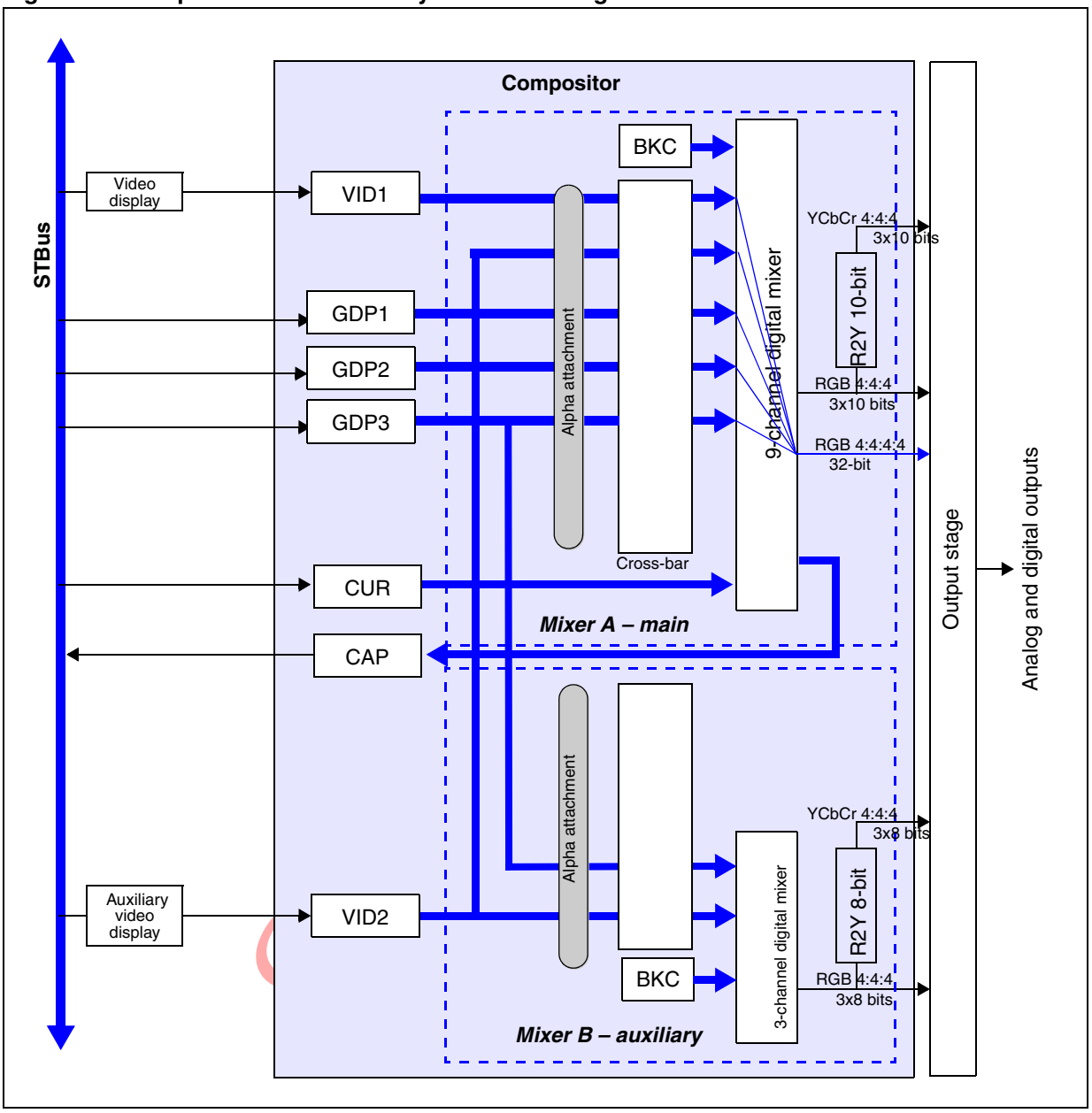
The graphics and cursor pipelines read pixel data and related control information directly from memory. The video input pipelines accept data from the main and auxiliary video display pipelines. Video and graphics data (captured for the compositor data flow by the capture pipeline) is written back to the memory with a resolution up to 32 bits/pixel. The real-time processing performed by each pipeline is controlled by the register programming.

The digital mixer A successively blends video layers (VID1, VID2), graphics layers (GDP1, GDP2, and GDP3), cursor layer (CUR), and a background color. A cross-bar router enables the hierarchy of the GDP1, GDP2, GDP3 and VID1, VID2 layers to be programmed. Each layer can be independently enabled or disabled. The blending operates in the RGB color domain, so each layer supplies an RGB signal (3 × 12 bits), with transparency information that provides the weighting coefficients for the mixing operation at a given depth.

The digital mixer B successively blends one video layer (VID2) with one graphics layer (GDP3) and a background color. A cross-bar router enables the hierarchy of the GDP3 and VID2 layers to be programmed. In the digital mixer B, each layer can be independently enabled or disabled, and blending operates in the RGB color domain.

All sub-blocks are controlled by the hardware registers. All these registers can be read but not necessarily written. The graphics planes are link-list based and have their register set written through the memory (register download is controlled directly by the hardware after initialization). All other registers can be written. Each plane block supports a specific set of bitmap formats. Each plane starts reading data from memory when it is enabled in mixer A or mixer B.

Figure 8. Graphics and video subsystem block diagram

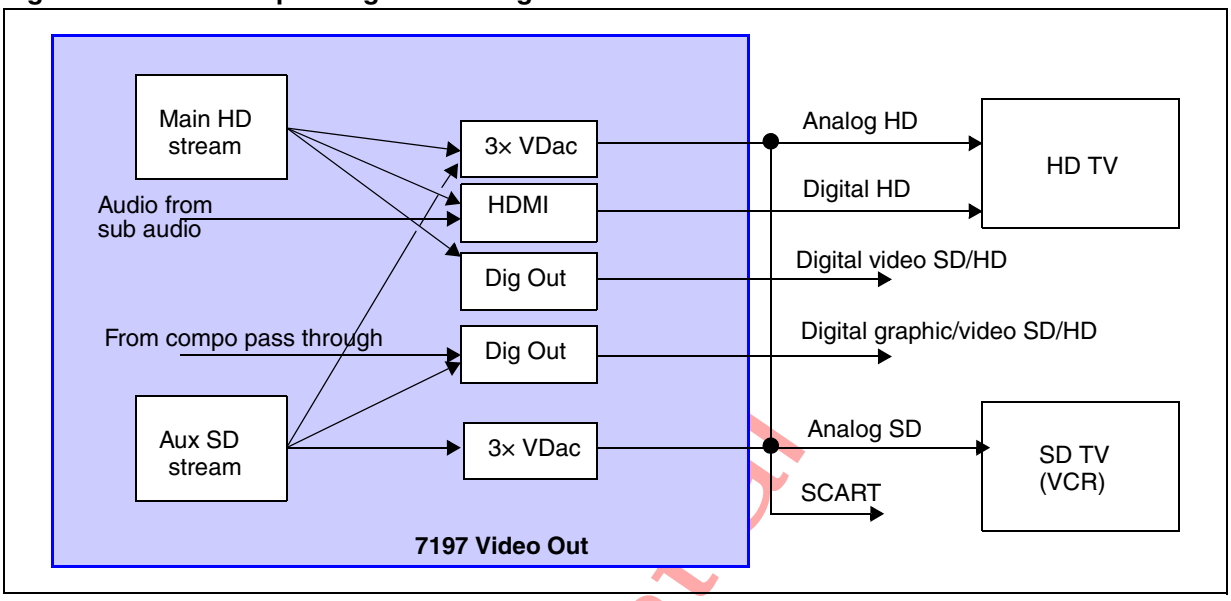


3.11 Video output

The Video Output subsystem is the unit responsible for reading decoded video frames and graphics data from external memory and to reformat, rasterize, and mix them for display.

The STi7197 can output video program on main HD TV Out and on aux SD TV (VCR) Out with separate timebase if required (VTG0, VTG1). It is also able to deliver the same SD video on both main and auxiliary video outputs using the capture feature. The main data paths corresponding to these typical configurations are shown in *Figure 9* as well as the principal units which constitute the Video Output stage.

Figure 9. Video output stage block diagram



3.11.1 Main HDTV video output

The following are the main functional blocks included in the main video flow:

- Main VDP, including High-Definition Display Pipeline with IQI and DEI engines
- VTG0 (free running or master of the aux VTG1)
- Capture output port with vertical and horizontal resizing, shared with auxiliary video flow
- Compositor—Mixer five to four (in: video: RGB or YCbCr, 3x graphic: RGB; out: 2x video: RGB and YCbCr, pass through, capture), shared GDP3 and VDP aux with auxiliary compositor
- TV Out—receives its data from the compositor channel (video: RGB or YCbCr, graphic: RGB); the video data is then formatted and output in digital, analog and audio-video composite to be used by external devices
- DVI-HDCP or HDMI-compliant copy-protected digital output
- Player multichannel (8-ch) and GP FIFO
- S/PDIF player and GP FIFO
- Four S/PDIF players with I²S-to-S/PDIF converters
- Triple HD/SD DAC (analog output)
- Two digital video outputs, that is, DVO0 (video) is 8-bit or 16-bit and DVO1(GFX) is 24-bit
- AWG—arbitrary waveform generator (Dwight Cavendish and Rovi™ copy protection support)

Note: The compositor includes a pipeline, which is able to mix one cursor, one or two video, up to three graphic layers, and one background layer. The data is then delivered to the TV Out. The capture port supports vertical and horizontal resizing output data with filtering for upsizing.

3.11.2 Auxiliary SDTV video flow

The following are the main functional blocks included in the auxiliary video flow:

- VTG1—free running or slave of the main HDTV VTG0
- Video Display Pipe High-definition (VDP aux)
- Capture output port with vertical and horizontal resizing, shared with main HDTV video flow
- Compositor—mixer two to three (YCbCr 8-bit and RGB 8-bit and capture), shared GDP3, and VDP aux with main HDTV compositor
- SD DENC—SDTV/VCR video encoder
- AWG—arbitrary waveform generator (Dwight Cavendish and Rovi™ copy protection support)
- Triple HD/SD DAC (analog output)—The DAC outputs can be components (Y/C) or composite (PAL, SECAM, NTSC CVBS); all six DACs can output the auxiliary display in SD format for SCART output

Note: The compositor includes a pipeline, which is able to mix one video, one graphic layer, and one background layer. The data is then delivered to the TV Out. The capture port supports vertical and horizontal resizing output data with filtering for upsizing.

3.12 2D blitter display engine

The 2D blitter display engine (BDisp 2 engine) is a software controlled output display generator, which can also be used as a CPU accelerator for graphics picture handling. The BDisp 2 engine, is an evolution of BDisp engine. It is a triple-source 2D DMA, with a set of powerful operators.

The 2D blitter display engine retrieves data from the local memory through three input sources, source 1, source 2, and source 3. Sources 1, 2, and 3 are used simultaneously for read/modify/write operations.

2D blitter display engine features are as follows:

- Two composition queues
- Four application queues
- Sub-byte S1 and S2 access
- Five-tap vertical filters
- Eight-tap horizontal filters
- Flicker filter adaptive
- Matrix conversion on input and output for: rgb2ycbcr, ycbcr2rgb,bt601, and bt709
- CLUT 1/2/4/8
- Color reduction
- Logical operation
- Clipmask
- Rotation
- Plane mask
- Color key capability
- BlueRay Disc run-length decoder (BD RLD)
- High definition-DVD 2/8-bit run-length decoder (HD-DVD RLD)

2D blitter display engine functions are as follows:

- Solid color fill of rectangular window
- Solid color shade (fill and alpha blending)
- One-source copy, with one or several operators enabled (color format conversion, 2D scaling)
- Two-source copy with alpha blending
- 4:2:2 / 4:20 capabilities, as source format
- Fully programmable matrix used for color space conversion, PSI, special effects
- Color expansion (CLUT to true color)
- Color correction (gamma, contrast, gain)
- 2D resize engine with high quality filtering
- Adaptive flicker filter from memory-to-memory
- Rectangular clipping
- VC-1 range mapping/range reduction compensation algorithm
- Programmable source/target scanning direction, both horizontally and vertically, to cope correctly with overlapping source and destination area.

3.13 Audio subsystem

Overview

The main function of the STi7197 audio subsystem is to decode and play different standards of multi-channel compressed audio streams. The audio stream (encoded or decoded) is received either from an external source through the PCM input interface or an internal source, such as the transport subsystem through memory.

The audio decoder may have to decode simultaneously two different encoded audio streams when an audio description channel is provided (the main audio stream and a 2-channel audio description channel) or when recording and listening to two different audio streams.

PCM mixing

The decoded audio stream can be mixed with a PCM file stored in memory following an optional sample rate conversion to adapt the sampling rate of the two streams. PCM mixing is also used when a description channel is decoded and then mixed with the main audio stream. The PCM mixing is fully implemented in the software running on the ST231.

PCM output: downmixing

The multi-channel decoded PCM stream can be downmixed to generate a 2-channel PCM stream. This down mixed stream can be then output unmixed through a stereo 24-bit DAC while the PCM-mixed decoded audio stream can be delivered onto a 6-channel digital PCM output and a digital S/PDIF output.

Compressed data: S/PDIF output

Compressed audio data can also be delivered on the S/PDIF output to be decoded by an external decoder/amplifier.

HDMI output

The STi7197 HDMI output can deliver audio data to an HDMI sink device. The audio data is delivered by the audio subsystem to the HDMI subsystem through internal I²S-to-S/PDIF players/converters (see *Figure 10*).

Audio decoder features

The audio decoder features are as follows:

- Decoding of the following audio formats: MPEG1 layer I/II, MP3, MPEG2- Layer II, Dolby Digital, Dolby Digital Plus (up to 7.1), MPEG4 AAC-LC, MPEG4 AACplus (HE-AAC, AAC+SBR) v1 and v2 (up to 5.1), WMA9, WMA9pro (up to 7.1)
- PCM mixing with internal or external source with sample rate conversion (32, 44.1, 48 kHz)
- Encoded (IEC 61937) or decoded (IEC 60958) digital audio on S/PDIF output
- Multi-channel down-mixing for output over HDMI (up to eight channels), PCM output (up to six channels), and analog output (up to two channels)
- PCM audio input (I²S format)
- Audio description channel decoding
- Postprocessing (channel virtualization)—Dolby Prologic downmix, volume control, and bass redirection

Audio transcoding

The STi7197 supports the transcoding of advanced audio formats for output over S/PDIF as formats recognized by external audio decoders. The following two transcode operations are available:

- Dolby Digital Plus-to-Dolby Digital
- MPEG4 AACplus-to-DTS

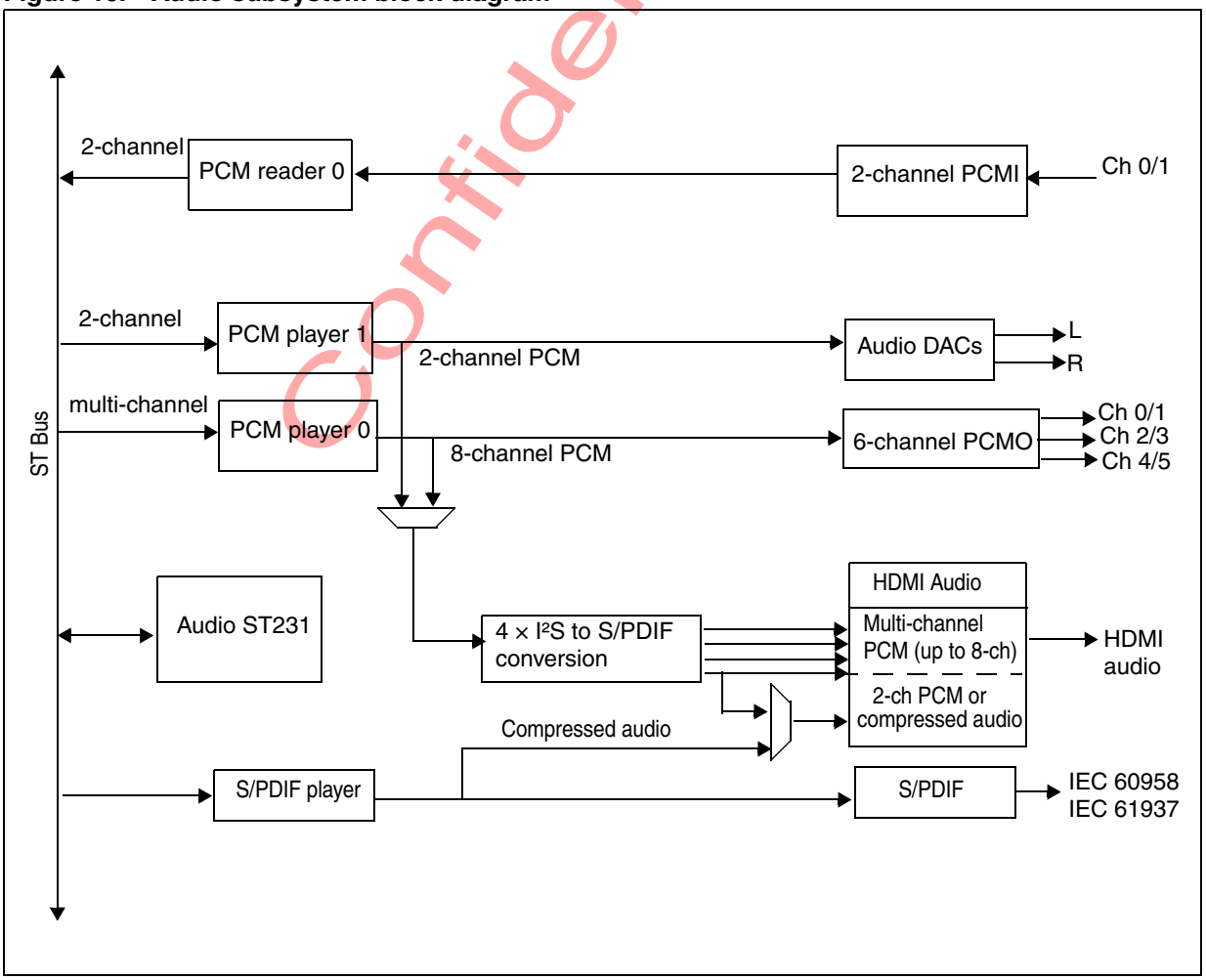
Audio subsystem blocks

The audio subsystem includes the following functional units.

- One audio processor ST231 core, running at 450 MHz, which executes the decoding algorithms, the sample-rate conversion, the postprocessing, and the volume control.
- One PCM reader, which captures the data at the PCM input and stores it in memory through an FDMA channel. (This is mutually exclusive with PCM player 0 since they share the same pads.)
- Two PCM players, which receive decoded PCM data from memory through FDMA channels. One PCM player delivers the down-mixed PCM output to the audio DAC. The other PCM player produces the stereo or multi-channel decoded audio stream on a 7-wire PCM output (I²S protocol).
- Two quad-frequency synthesizers, which generate the PCM clock (oversampling clock 256 × Fs), used by the S/PDIF, PCM players, and audio DAC.
- One stereo 24-bit audio DAC with differential outputs.
- An S/PDIF player, which reads decoded PCM data or encoded data from memory through an FDMA channel, and outputs them on the S/PDIF output.

See *Figure 10* for a detailed block diagram of the audio subsystem.

Figure 10. Audio subsystem block diagram



The host CPU and the FDMA assist in the audio decoding process. Since the audio decoder is a frame decoder, the host CPU (ST40 core) controls the audio processor frame-by-frame. A mailbox is used for communication between the two processors.

The host CPU is also required to do the PES parsing and the frame syncword detection.

The FDMA builds the ES buffer to feed the PCM and S/PDIF players, and stores the data captured by the PCM reader in memory.

The PCM reader, PCM player, and S/PDIF player transfer data to/from memory through FDMA.

3.14 FDMA controllers

The STi7197 has two multichannel, burst-capable, direct memory access controllers:

- FDMA0—real-time paced channels: S/PDIF, PCM Player 0-1, and SWTS
- FDMA1—PES parsing, PCI-Master, SWTS when streaming from Ethernet or USB, UART, SSC, and free-running general-purpose DMAs

External pacing signals are available for DMA transfers with external peripherals.

3.15 Interfaces

3.15.1 Internal peripherals

The STi7197 has many dedicated internal peripherals, including:

- Four ASCs (UARTs), two of which are generally used by the Smartcard controllers, one to support hardware flow control signals
- Two Smartcard interfaces and clock generators
- Four external SSCs for I²C/SPI master/slave interfaces
- One four-channel PWM module with two PWM outputs and programmable frequency
- One Teletext serializer
- 17 GPIO ports (3.3 V tolerant)
- One modem analog front end (MAFE) interface
- One single infrared transmitter/receiver supporting RC5, RC6 and RECS80, RC-MM 1.5, DIRECTV and Echostar codes
- One UHF remote control digital input
- One interrupt level controller with external interrupt inputs
- Two independent USB 2.0 host controllers, each with its own integrated PHY
- One front-panel key scanning support
- One e-SATA interface

3.15.2 Ethernet controller

The STi7197 has an integrated Ethernet controller and MAC processor for delivery of IP-based A/V streams in hybrid IP STBs and for home network connectivity. It also includes an MII/RMII port for connection to an external PHY. Ethernet features are as follows:

- Half/full duplex, full duplex flow control
- VLAN tagging support
- MII and RMII external interface
- Direct interface with STE101P and similar PHYs through MII or RMII
- Able to accept clock from external PHY/Home network device in MII mode
- Dedicated scatter/gather link list DMA
- 100 Mbits/s sustained transfer rates to and from memory
- 32 H/W perfect match MAC address filters

The controller can also be used to interface through overclocked MII interface (up to 300 Mbits/s) to an external non-Ethernet Phy as a MoCA Phy for example.

3.15.3 Dual Smartcard interfaces

Both Smartcard interfaces are ISO7816, EMV2000 and NDS compliant, with the addition of a simple external power switch.

A programmable hardware power control feature allows the power control signal to be switched when card insertion or removal is detected.

3.16 Clock generation

The STi7197 features five clock generation blocks:

- ClockGen A: 2 × PLLs main for CPU and interconnect clocks
- ClockGen B: 2 × FreqSynth for video, display and peripheral clocks
- ClockGen C: 1 × FreqSynth for audio clocks
- ClockGen D: 1 × PLL for memory clocks

3.17 System services

The STi7197 supports a number of on-chip system service functions including:

- integrated VCXOs (DCOs) for clock recovery
- debug through a single JTAG port
- reset and watchdog controller
- two power saving modes: reduced power mode and low power/standby mode

4 Package mechanical data

4.1 27 × 27 package

Package type: FPBGA 700 balls. Body: 27 × 27 mm.

Figure 11. Top view

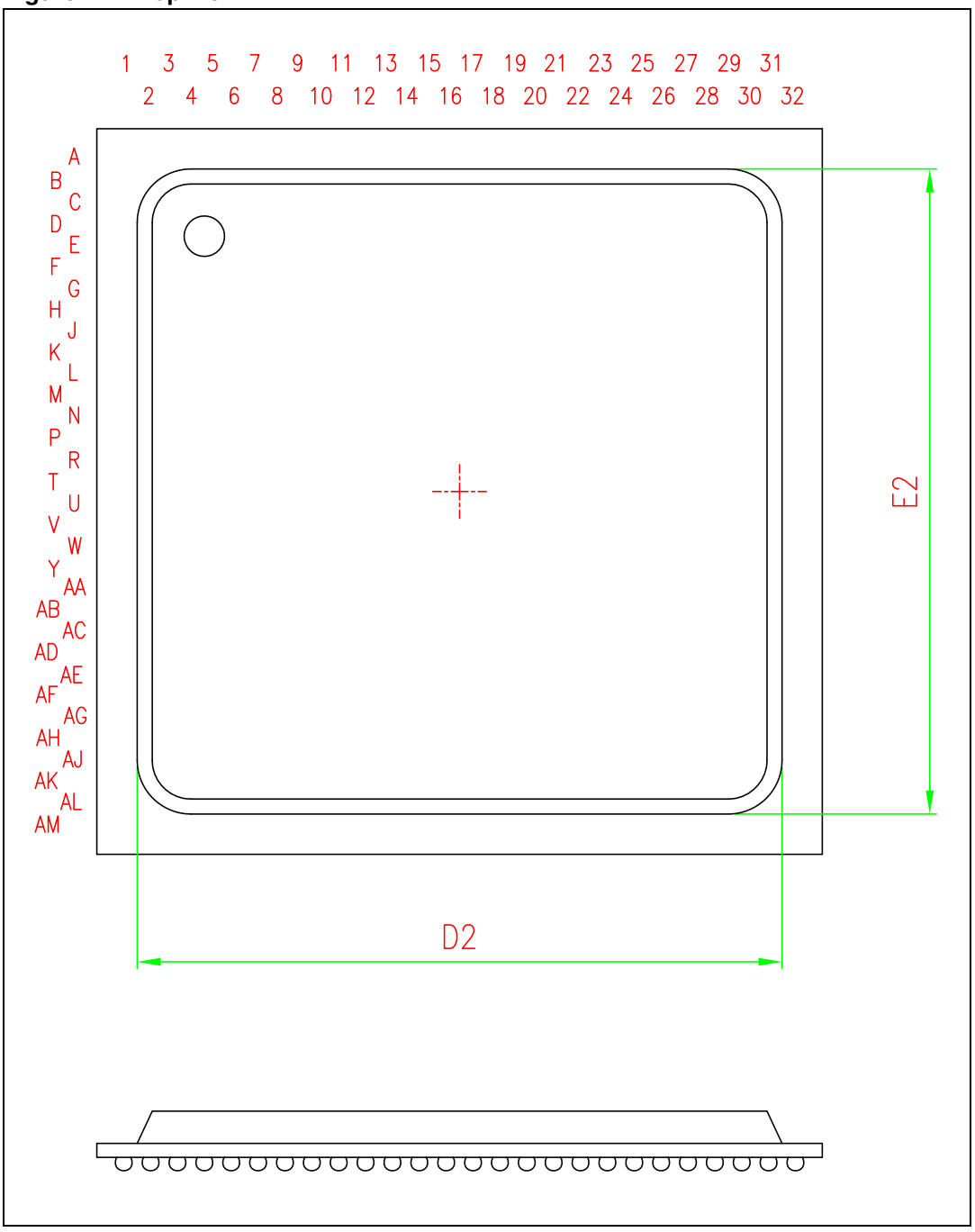


Figure 12. Bottom view

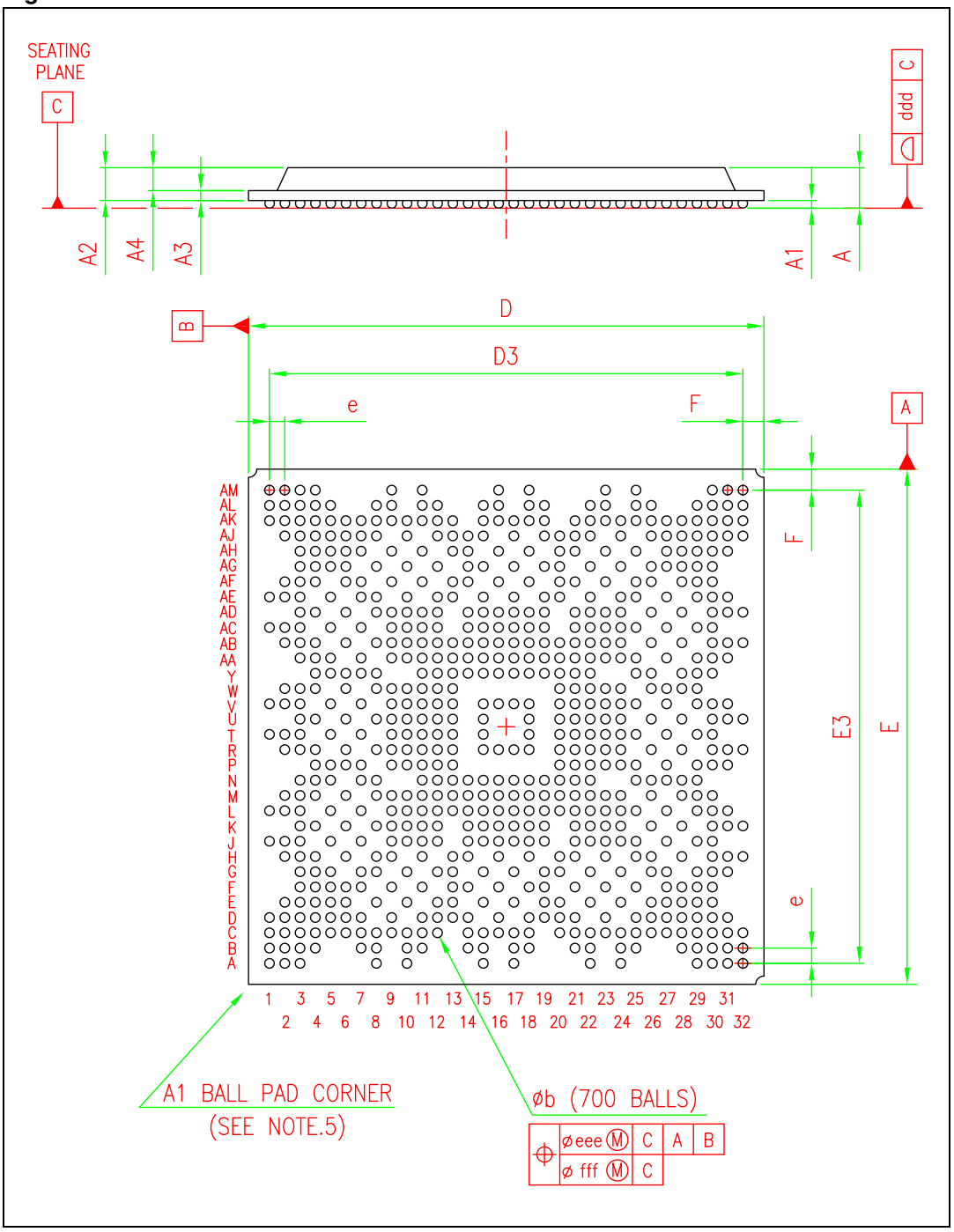


Table 1. JEDEC standard package dimensions

Dimension	Millimeters			Inches			Notes
	Min	Typ	Max	Min	Typ	Max	
A	-	-	2.19		-	0.8622	(1)
A1	0.27	-	-	0.0106	-		-
A2	-	1.72	-	-	0.0677		-
A3	-	0.52	-	-	0.0205		-
A4	-	1.20	-	-	0.0472		-
b	0.45	0.50	0.55	0.0177	0.0197	0.0217	(2)
D	26.80	27.00	27.20	1.055	1.063	1.070	-
D1	-	24.80	-		0.9764	-	-
D2	-	24.00			0.9449	-	-
E	26.80	27.00	27.20	1.055	1.063	1.070	-
E1	-	24.80	-	-	0.9764	-	-
E2	-	24.00	-	-	0.9449	-	-
e	-	0.80	-	-	0.0315	-	-
F	-	1.10	-	-	0.0433	-	-
ddd	-	-	0.20	-	-	0.0079	-
eee	-	-	0.15	-	-	0.0059	(3)
fff	-	-	0.08	-	-	0.0315	(4)

1. FPBGA stands for Fine pitch Plastic Ball Grid Array.
   Fine pitch: e < 1.00 mm
   The total profile height (Dim A) is measured from the seating plane to the top of the component.
   The maximum total package height is calculated by the following methodology:
   A2 Typ+A1 Typ + V ($A1^2+A3^2+A4^2$ tolerance values)
2. The typical ball diameter before mounting is 0.50 mm.
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.
5. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
   A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

4.2 Environmentally friendly packages

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5 Ordering information

Table 2. Ordering information

Order code	Package	Description
STI7197ZUD	FPBGA 27 mm × 27 mm	Development version, all options

6 Front-end registers

Registers are accessed from the processor interface. All writable register bits are reset to 0 unless otherwise stated. Read-only registers have no defined reset value. The processor should not write 1s to undefined register bits. Similarly, when reading a register, the processor should mask undefined bits.

All register addresses are hexadecimal values. Signed registers are 2's complement.

Note: Any addresses not listed in the following table is reserved and must be set to zero.

6.1 Register map

Table 3. Register summary table

Address offset	Register	Description	Reference
Demodulator registers			
0x00	EQU_0	QAM mode	page 45
0x01	EQU_1	Equalizer adaptation step	page 46
0x03	EQU_3	State machine control	page 46
0x04	EQU_4	Corner point control	page 47
0x05	EQU_5	Constellation corner point rate (LSBs)	page 47
0x06	EQU_6	Constellation corner point rate (MSBs)	page 47
0x07	EQU_7	Constellation corner point (MSBs)	page 48
0x08	EQU_8	Noise estimation (LSBs)	page 48
0x09	EQU_9	Noise estimation (MSBs)	page 48
0x0A	EQU_10	Imaginary constellation part	page 49
0x0B	EQU_11	Real constellation part	page 49
0x0C	INITDEM_0	Demodulation frequency (LSBs)	page 49
0x0D	INITDEM_1	Demodulation frequency (MSBs)	page 49
0x0E	INITDEM_2	Scanning latency	page 50
0x10	INITDEM_3	Demodulation scan step (LSBs)	page 50
0x11	INITDEM_4	Demodulation scan step control	page 50
0x12	INITDEM_5	Demodulator control	page 51
0x014	DELAGC_0	Maximum PWM rate for AGC2	page 51
0x015	DELAGC_1	Minimum PWM rate for AGC2	page 51
0x016	DELAGC_2	Maximum PWM rate for AGC1	page 52
0x017	DELAGC_3	Minimum PWM rate for AGC1	page 52
0x18	DELAGC_4	Ratio between AGC1/AGC2 PWM rate slopes	page 52

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0x19	DELAGC_5	AGC2 PWM rate threshold	page 53
0x1A	DELAGC_6	AGC freeze control	page 53
0x1C	DELAGC_7	ADC average magnitude (LSBs)	page 54
0x1D	DELAGC_8	ADC average magnitude (MSBs)	page 54
0x20	DELAGC_10	Analog AGC1	page 55
0x21	DELAGC_11	Analog AGC1	page 55
0x22	DELAGC_12	Analog AGC2	page 55
0x23	DELAGC_13	Analog AGC2	page 55
0x24	WBAGC_0	Analog AGCs	page 56
0x25	WBAGC_1	Analog AGCs	page 56
0x26	WBAGC_2	WBAGC reference	page 56
0x27	WBAGC_3	WBAGC control	page 57
0x28	WBAGC_4	Acquisition counter (LSBs)	page 57
0x29	WBAGC_5	Acquisition counter (MSBs)	page 58
0x2A	WBAGC_6	AGC loop response (LSBs)	page 58
0x2B	WBAGC_7	AGC loop response (MSBs)	page 58
0x2C	STLOOP_1	Symbol timing recovery loop gain (LSBs)	page 58
0x2D	STLOOP_2	Symbol timing recovery loop gain (MSBs)	page 59
0x2E	STLOOP_3	Symbol timing recovery loop integral gain (LSBs)	page 59
0x2F	STLOOP_4	Symbol timing recovery loop gain scale	page 59
0x30	STLOOP_5	Symbol rate (LSBs)	page 60
0x31	STLOOP_6	Symbol rate (lower mid byte)	page 60
0x32	STLOOP_7	Symbol rate (upper mid byte)	page 61
0x33	STLOOP_8	Symbol rate (MSBs)	page 61
0x34	STLOOP_9	Symbol timing recovery loop phase control	page 61
0x35	STLOOP_10	Symbol timing recovery loop algorithm control	page 62
0x38	CRL_1	Carrier recovery loop gain	page 62
0x39	CRL_2	Carrier recovery loop gain reduction factor	page 63
0x3A	CRL_3	Carrier recovery loop control	page 64
0x3B	CRL_4	Carrier recovery loop capture	page 64
0x3C	CRL_5	Carrier recovery loop phase accumulator (LSBs)	page 64
0x3D	CRL_6	Carrier recovery loop phase accumulator (mid byte)	page 65
0x3E	CRL_7	Carrier recovery loop phase accumulator (MSBs)	page 65
0x3F	CRL_8	2nd carrier recovery loop coefficient	page 65

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0x40	CRL_9	Carrier recovery loop frequency offset (LSBs)	page 66
0x41	CRL_10	Carrier recovery loop frequency offset (lower mid byte)	page 66
0x42	CRL_11	Carrier recovery loop frequency offset (upper mid byte)	page 66
0x43	CRL_12	Carrier recovery loop frequency offset (MSBs)	page 67
0x44	CRL_13	Carrier recovery loop sweep value (LSBs)	page 67
0x45	CRL_14	Carrier recovery loop sweep value (MSBs)	page 67
0x48	PMFAGC_0	PMFAGC lock threshold (LSBs)	page 68
0x49	PMFAGC_1	PMFAGC lock threshold (MSBs)	page 68
0x4A	PMFAGC_2	PMFAGC control	page 68
0x4C	PMFAGC_3	Post-filter digital AGC (PMFAGC)	page 69
0x4D	PMFAGC_4	Post-filter digital AGC (PMFAGC)	page 69
0x4E	PMFAGC_5	Post-filter digital AGC (PMFAGC)	page 69
0x50	INTER_0	Interrupt mask 1	page 70
0x51	INTER_1	Interrupt mask 2	page 70
0x52	INTER_2	Interrupt 1	page 71
0x53	INTER_3	Interrupt 2	page 72
0x58	SIG_FAD_0	Signal fading control	page 72
0x59	SIG_FAD_1	Signal fading magnitude	page 73
0x5A	SIG_FAD_2	Signal fading low threshold	page 73
0x5B	SIG_FAD_3	Signal fading high threshold	page 73
0x5C	NEW_CRL_0	CRL direct gain in blind mode	page 73
0x5D	NEW_CRL_1	CRL integral gain in blind mode	page 74
0x5E	NEW_CRL_2	CRL direct gain in LMS_1 mode	page 74
0x5F	NEW_CRL_3	CRL integral gain in LMS_1 mode	page 74
0x60	NEW_CRL_4	CRL direct gain in LMS_2 mode	page 75
0x61	NEW_CRL_5	CRL integral gain in LMS_2	page 75
0x62	NEW_CRL_6	CRL second mode control	page 75
0x64	FREQ_0	Frequency estimator 0	page 76
0x65	FREQ_1	Frequency estimator 1	page 76
0x66	FREQ_2	Frequency estimator blind-mode integration length	page 76
0x67	FREQ_3	Frequency estimator LMS_1-mode integration length	page 77
0x68	FREQ_4	Frequency estimator LMS_2-mode integration length	page 77
0x69	FREQ_5	Frequency estimator corner-point low threshold (LSBs)	page 77
0x6A	FREQ_6	Frequency estimator corner-point thresholds	page 78

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0x6B	FREQ_7	Frequency estimator corner-point high threshold (MSBs)	page 78
0x6C	FREQ_8	Frequency estimation (LSBs)	page 78
0x6D	FREQ_9	Frequency estimation (mid byte)	page 79
0x6E	FREQ_10	Frequency estimation (MSBs)	page 79
0x6F	FREQ_11	Unlocked integration length	page 79
0x70	FREQ_12	Unlocked low threshold (LSBs)	page 79
0x71	FREQ_13	Unlocked low threshold (mid byte)	page 80
0x72	FREQ_14	Unlocked low threshold (MSBs)	page 80
0x73	FREQ_15	CRL control	page 80
0x74	FREQ_16	Unlocked high threshold (LSBs)	page 81
0x75	FREQ_17	Unlocked high threshold (mid byte)	page 81
0x76	FREQ_18	Unlocked high threshold (MSBs)	page 82
0x77	FREQ_19	FFE input in blind mode	page 82
0x78	FREQ_20	CRL unlocked detector current output (LSBs)	page 82
0x79	FREQ_21	CRL unlocked detector current output (mid byte)	page 83
0x7A	FREQ_22	CRL unlocked detector current output (MSBs)	page 83
0x7B	FREQ_23	FFE input in LMS_1 mode	page 83
0x7C	FREQ_24	FFE input in LMS_2 mode	page 83
FEC A/C registers			
0x80	DEINT_SYNC_0	De-interleaver sync detector	page 84
0x81	DEINT_SYNC_1	De-interleaver sync detector	page 84
0x84	BERT_0	Integrated BER tester	page 85
0x85	BERT_1	Integrated BER tester (LSBs)	page 85
0x86	BERT_2	Integrated BER tester	page 86
0x88	DEINT_0	De-interleaver	page 86
0x89	DEINT_1	De-interleaver	page 86
0x8C	OUTFORMAT_0	Output formatter	page 87
0x90	OUTFORMAT_1	Output formatter	page 87
0x91	OUTFORMAT_2	Output formatter	page 88
0x94	RS_DESC_0	MPEG-TS packet counter (LSBs)	page 88
0x95	RS_DESC_1	MPEG-TS packet counter (MSBs)	page 88
0x96	RS_DESC_2	MPEG-TS corrected packet counter (LSBs)	page 89
0x97	RS_DESC_3	MPEG-TS corrected packet counter (MSBs)	page 89

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0x98	RS_DESC_4	MPEG-TS uncorrectable packet counter (LSBs)	page 89
0x99	RS_DESC_5	MPEG-TS uncorrectable packet counter (MSBs)	page 89
0x9A	RS_DESC_6	Reed–Solomon - Descrambler sync detector - Descrambler	page 90
0x9C	RS_DESC_7	Reed–Solomon - Descrambler sync detector - Descrambler	page 90
0x9D	RS_DESC_8	Reed–Solomon - Descrambler sync detector - Descrambler	page 91
Configuration and control registers			
0xA0	CTRL_0	Configuration and control 0	page 91
0xA1	CTRL_1	Configuration and control 1	page 92
0xA2	CTRL_2	Configuration and control 2	page 92
0xA3	CTRL_3	Configuration and control 3	page 93
0xA6	CTRL_4	Configuration and control 4	page 94
0xA8	CTRL_5	Configuration and control 5	page 94
0xA9	CTRL_6	Configuration and control 6	page 95
0xAA	CTRL_7	Configuration and control 7	page 95
0xAB	CTRL_8	Configuration and control 8	page 96
0xAC	CTRL_9	Configuration and control 9	page 96
0xAD	CTRL_10	Configuration and control 10	page 97
0xAE	CTRL_11	Synthesizer fine selector (LSBs)	page 97
0xAF	CTRL_12	Synthesizer fine selector (MSBs)	page 97
FEC-B registers			
0xC0	MPEG_CONTROL	FEC-B control	page 98
0xC1	MPEG_SYNC_ACQ	FEC-B MPEG sync patterns for SYNC state	page 99
0xC2	MPEG_SYNC_LOSS	FEC-B missing MPEG sync patterns to exit SYNC state	page 99
0xC3	DATA_OUT_CONTROL	FEC-B data output control	page 99
0xC4	VITERBI_SYNC_ACQ	FEC-B sync acquired threshold	page 100
0xC5	VITERBI_SYNC_LOSS	FEC-B sync lost threshold	page 100
0xC6	VITERBI_SYNC_GO	FEC-B sync start	page 100
0xC7	VITERBI_SYNC_STOP	FEC-B sync stop	page 101
0xC8	FS_SYNC	FEC-B sync control	page 101
0xC9	IN_DEPTH	FEC-B interleaver depth	page 101
0xCA	RS_CONTROL	FEC-B Reed–Solomon control	page 102
0xCB	DEINT_CONTROL	FEC-B de-interleaver control	page 103

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0xCC	SYNC_STAT	FEC-B sync status	page 103
0xCD	VITERBI_I_RATE	FEC-B	page 104
0xCE	VITERBI_Q_RATE	FEC-B	page 104
0xD0	TX_INTERLEAVER_DEPTH	FEC-B	page 105
0xD1	RS_ERR_CNT	FEC_B Reed–Solomon correctable errors	page 105
0xD4	RS_UNC_COUNT	FEC_B Reed–Solomon uncorrectable errors	page 105
0xD6	RS_RATE	FEC-B	page 106
0xD8	RS_CORR_COUNT	FEC-B	page 106
0xDA	RS_UNERR_COUNT	FEC-B	page 106
TSMF registers			
0xB1	TSMF_SEL	TSMF selection mode	page 107
0xB2	TSMF_CONTROL	TSMF control	page 107
0xB3	AUTOMATIC_SYNC_COUNT	-	page 108
0xB4	TS_ID_L	TS identifier (LSBs)	page 108
0xB5	TS_ID_H	TS identifier (MSBs)	page 108
0xB6	ON_ID_L	Original network identifier (LSBs)	page 108
0xB7	ON_ID_H	Original network identifier (MSBs)	page 109
0xB9	GENERAL_STATUS	TSMF general status	page 109
0xBA	TS_ST_L	One-bit TS ID status (LSBs)	page 109
0xBB	TS_ST_H	One-bit TS ID status (MSBs)	page 110
0xBC	RE_ST_L	Two-bit TS ID status (LSBs)	page 110
0xBD	RE_ST_2	Two-bit TS ID status (lower-mid SBs)	page 110
0xBE	RE_ST_1	Two-bit TS ID status (upper-mid SBs)	page 111
0xBF	RE_ST_H	Two-bit TS ID status (MSBs)	page 111
0xC0	T_ID_L1	TS identifier 1 (LSBs)	page 111
0xC1	T_ID_H1	TS identifier 1 (MSBs)	page 111
0xC2	O_ID_L1	Original network identifier 1 (LSBs)	page 112
0xC3	O_ID_H1	Original network identifier 1 (MSBs)	page 112
0xC4	T_ID_L2	TS identifier 2 (LSBs)	page 112
0xC5	T_ID_H2	TS identifier 2 (MSBs)	page 112
0xC6	O_ID_L2	Original network identifier 2 (LSBs)	page 113
0xC7	O_ID_H2	Original network identifier 2 (MSBs)	page 113
0xC8	T_ID_L3	TS identifier 3 (LSBs)	page 113
0xC9	T_ID_H3	TS identifier 3 (MSBs)	page 113

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0xCA	O_ID_L3	Original network identifier 3 (LSBs)	page 114
0xCB	O_ID_H3	Original network identifier 3 (MSBs)	page 114
0xCC	T_ID_L4	TS identifier 4 (LSBs)	page 114
0xCD	T_ID_H4	TS identifier 4 (MSBs)	page 114
0xCE	O_ID_L4	Original network identifier 4 (LSBs)	page 115
0xCF	O_ID_H4	Original network identifier 4 (MSBs)	page 115
0xD0	T_ID_L5	TS identifier 5 (LSBs)	page 115
0xD1	T_ID_H5	TS identifier 5 (MSBs)	page 115
0xD2	O_ID_L5	Original network identifier 5 (LSBs)	page 116
0xD3	O_ID_H5	Original network identifier 5 (MSBs)	page 116
0xD4	T_ID_L6	TS identifier 6 (LSBs)	page 116
0xD5	T_ID_H6	TS identifier 6 (MSBs)	page 116
0xD6	O_ID_L6	Original network identifier 6 (LSBs)	page 117
0xD7	O_ID_H6	Original network identifier 6 (MSBs)	page 117
0xD8	T_ID_L7	TS identifier 7 (LSBs)	page 117
0xD9	T_ID_H7	TS identifier 7 (MSBs)	page 117
0xDA	O_ID_L7	Original network identifier 7 (LSBs)	page 118
0xDB	O_ID_H7	Original network identifier 7 (MSBs)	page 118
0xDC	T_ID_L8	TS identifier 8 (LSBs)	page 118
0xDD	T_ID_H8	TS identifier 8 (MSBs)	page 118
0xDE	O_ID_L8	Original network identifier 8 (LSBs)	page 119
0xDF	O_ID_H8	Original network identifier 8 (MSBs)	page 119
0xE0	T_ID_L9	TS identifier 9(LSBs)	page 119
0xE1	T_ID_H9	TS identifier 9 (MSBs)	page 119
0xE2	O_ID_L9	Original network identifier 9 (LSBs)	page 120
0xE3	O_ID_H9	Original network identifier 9 (MSBs)	page 120
0xE4	T_ID_L10	TS identifier 10 (LSBs)	page 120
0xE5	T_ID_H10	TS identifier 10 (MSBs)	page 120
0xE6	O_ID_L10	Original network identifier 10 (LSBs)	page 121
0xE7	O_ID_H10	Original network identifier 10 (MSBs)	page 121
0xE8	T_ID_L11	TS identifier 11 (LSBs)	page 121
0xE9	T_ID_H11	TS identifier 11 (MSBs)	page 121
0xEA	O_ID_L11	Original network identifier 11 (LSBs)	page 122
0xEB	O_ID_H11	Original network identifier 11 (MSBs)	page 122

Table 3. Register summary table (continued)

Address offset	Register	Description	Reference
0xEC	T_ID_L12	TS identifier 12 (LSBs)	page 122
0xED	T_ID_H12	TS identifier 12 (MSBs)	page 122
0xEE	O_ID_L12	Original network identifier 12 (LSBs)	page 123
0xEF	O_ID_H12	Original network identifier 12 (MSBs)	page 123
0xF0	T_ID_L13	TS identifier 13 (LSBs)	page 123
0xF1	T_ID_H13	TS identifier 13 (MSBs)	page 123
0xF2	O_ID_L13	Original network identifier 13 (LSBs)	page 124
0xF3	O_ID_H13	Original network identifier 13 (MSBs)	page 124
0xF4	T_ID_L14	TS identifier 14 (LSBs)	page 124
0xF5	T_ID_H14	TS identifier 14 (MSBs)	page 124
0xF6	O_ID_L14	Original network identifier 14 (LSBs)	page 125
0xF7	O_ID_H14	Original network identifier 14 (MSBs)	page 125
0xF8	T_ID_L15	TS identifier 15 (LSBs)	page 125
0xF9	T_ID_H15	TS identifier 15 (MSBs)	page 125
0xFA	O_ID_L15	Original network identifier 15 (LSBs)	page 126
0xFB	O_ID_H15	Original network identifier 15 (MSBs)	page 126

6.2 Register descriptions

6.2.1 Demodulator registers

EQU_0 QAM mode

7	6	5	4	3	2	1	0
MODE_SELECT				U_THRESHOLD			

Address: 0x00

Type: R/W

Reset: 0x09

Description: QAM mode

[7:4] **MODE_SELECT**: QAM mode selection. May be overridden by the automatic constellation state machine (*CTRL_7*). If this state machine is enabled (AUTOCONSTEL_ON = 1 in *CTRL_7*), MODE_SELECT reflects the QAM mode being tried by the state machine.

0000: 16-QAM
0001: 32-QAM
0010: 128-QAM
0011: 256-QAM
0100: 64-QAM
1000: Reserved

[3:0] **U_THRESHOLD**: once in LMS mode, the equalizer gradually decreases the adaptation step size down to $2^{-U\_THRESHOLD}$.

EQU_1 Equalizer adaptation step

7	6	5	4	3	2	1	0
INITIAL_U				BLIND_U			

Address: 0x01

Type: R/W

Reset: 0x69

Description: Equalizer adaptation step

[7:4] **INITIAL_U**: initial adaptation step used when switching to LMS mode is $2^{-INITIAL\_U}$.
Suggested value with STL algorithm #0: 0x6 for 256-QAM, 0x5 for other levels. With STL algorithm #1 to 3: 0x7 for 256-QAM, 0x6 for other levels.

[3:0] **BLIND_U**: adaptation step used as long as equalizer is in blind mode is 2^{-BLIND_U}.
Suggested value with STL algorithm #0: 0x9 for 256-QAM, 0x8 for other levels. With STL algorithm #1 to #3: 0xA for 256-QAM, 0x9 for other levels.

EQU_3 State machine control

7	6	5	4	3	2	1	0
RESERVED		NBLIND	RESERVED	EQ_COEFF_CTL		EQ_FSM_CTL	

Address: 0x03

Type: R/W

Reset: 0x00

Description: State machine control

[7:6] Reserved

[5] **NBLIND**:
0: in blind mode 1: leaving blind mode

[4] Reserved

[3:2] **EQ_COEFF_CTL:**
0X: no forcing
10: disable equalizer coefficient update process
11: force immediate enabling of equalizer coefficient update process

[1:0] **EQ_FSM_CTL:**
0X: no forcing
10: disable state machine controlling blind/LMS equalizer operation, force blind mode
11: force immediate enabling of state machine controlling blind/LMS equalizer operation

EQU_4 Corner point control

7	6	5	4	3	2	1	0
RESERVED			INV_SPEC_MAP	LOCK_DET_ENABLE	TIME_CSTE		

Address: 0x04

Type: R/W

Reset: 0x00

Description: Corner point control

[7:5] Reserved

[4] **INV_SPEC_MAP**: inverse spectrum mapping. Spectrum inversion is performed on the equalizer output.

[3] **LOCK_DET_ENABLE**: when set, enables detection of corner points. Only when the average rate of corner points (time constant used for averaging defined by TIME_CSTE) is above a given threshold (selected through *EQU_5* and *EQU_6*) the equalizer is allowed to lock at 1.1 ms and switch to the decision-directed LMS algorithm.

[2:0] **TIME_CSTE**: time constant to perform rate integration in corner point.

EQU_5 Constellation corner point rate (LSBs)

7	6	5	4	3	2	1	0
TARGET_RATE[7:0]							

Address: 0x05

Type: R/W

Reset: 0xFF

Description: Constellation corner point rate (LSBs)

[7:0] **TARGET_RATE[7:0]**: target rate of occurrence of constellation corner points (LSBs).

EQU_6 Constellation corner point rate (MSBs)

7	6	5	4	3	2	1	0
CORNER_RATE[3:0]				TARGET_RATE[11:8]			

Address: 0x06

Type: R/W

Reset: 0x0F

Description: Constellation corner point rate (MSBs)

[7:4] **CORNER_RATE[3:0]**: corner rate (LSBs of unsigned 12-bit value). See *EQU_7*.

[3:0] **TARGET_RATE[11:8]**: target rate of occurrence of constellation corner points (MSBs).

EQU_7 Constellation corner point (MSBs)

7	6	5	4	3	2	1	0
CORNER_RATE[11:4]							

Address: 0x07

Type: R

Reset: 0x00

Description: Constellation corner point (MSBs)

[7:0] **CORNER_RATE[11:4]**: corner rate (MSBs of unsigned 12-bit value). The actual rate of occurrence of the constellation corner points is: CORNER_RATE/$2^{(5 + TIME\_CSTE)}$. (For TIME_CSTE, see *EQU_4*.)

EQU_8 Noise estimation (LSBs)

7	6	5	4	3	2	1	0
NOISE_EST[7:0]							

Address: 0x08

Type: R

Reset: 0x00

Description: Noise estimation (LSBs)

[7:0] **NOISE_EST[7:0]**: LSBs of the internal noise estimation accumulator. The content of this accumulator is correlated with the spreading of the decoded constellation. It is a measure of the mean distance between calculated points and mapped values. Using a look-up table, an equivalent noise degradation can be calculated (equivalent C/N estimation).
When NOISE_EST[7:0] is read, NOISE_EST[13:8] (*EQU_9*) is frozen until a new read.

EQU_9 Noise estimation (MSBs)

7	6	5	4	3	2	1	0
RESERVED		NOISE_EST[13:8]					

Address: 0x09

Type: R

Reset: 0x00

Description: Noise estimation (MSBs)

[7:6] Reserved

[5:0] **NOISE_EST[13:8]**: MSBs of the internal noise estimation accumulator.

EQU_10 Imaginary constellation part

7	6	5	4	3	2	1	0
Q_CONST[7:0]							

Address: 0x0A

Type: R

Reset: 0x00

Description: Imaginary constellation part

[7:0] **Q_CONST**[7:0]: imaginary part from constellation, truncated to the 8 MSBs. When Q_CONST is read, I_CONST (*EQU_11*) is frozen until a new read.

EQU_11 Real constellation part

7	6	5	4	3	2	1	0
I_CONST[7:0]							

Address: 0x0B

Type: R

Reset: 0x00

Description: Real constellation part

[7:0] **I_CONST**[7:0]: real part from constellation, truncated to the 8 MSBs.

INITDEM_0 Demodulation frequency (LSBs)

7	6	5	4	3	2	1	0
DEM_FQCY[7:0]							

Address: 0x0C

Type: R/W

Reset: 0x00

Description: Demodulation frequency (LSBs)

[7:0] **DEM_FQCY**[7:0]: LSBs of the value that gives the initial demodulation frequency.
demodulation frequency = DEM_FQCY[15:0] x F_{CLK} / 2^{16}.
Therefore resolution = $F_{CLK}/2^{16}$, for example 763 Hz for F_{CLK} = 50 MHz.

INITDEM_1 Demodulation frequency (MSBs)

7	6	5	4	3	2	1	0
DEM_FQCY[15:8]							

Address: 0x0D

Type: R/W

Reset: 0x00

Description: Demodulation frequency (MSBs)

[7:0] **DEM_FQCY**[15:8]: MSBs of the value that gives the initial demodulation frequency. See *INITDEM_0*.

INITDEM_2 Scanning latency

7	6	5	4	3	2	1	0
LATENCY							

Address: 0x0E

Type: R/W

Reset: 0x00

Description: Scanning latency

[7:0] **LATENCY**: defines the duration of each step when using the frequency scanning feature. The effective latency expressed with the system clock period T_{clk} as unit is: 65 536 x latency. (at F_{CLK} = 50 MHz, min = 1.31 ms, max = 334 ms).

INITDEM_3 Demodulation scan step (LSBs)

7	6	5	4	3	2	1	0
SCAN_STEP[7:0]							

Address: 0x10

Type: R/W

Reset: 0x00

Description: Demodulation scan step (LSBs)

[7:0] **SCAN_STEP**[7:0]: LSBs of SCAN_STEP (unsigned 14-bit value) that defines the step between two successive demodulation frequencies: (SCAN_STEP / 2^{16}) x F_{CLK}.

INITDEM_4 Demodulation scan step control

7	6	5	4	3	2	1	0
RESERVED		SCAN_STEP[13:8]					

Address: 0x11

Type: R/W

Reset: 0x40

Description: Demodulation scan step control

[7:6] **Reserved**

[5.0] **SCAN_STEP**[13:8]: six MSBs of SCAN_STEP (unsigned 14-bit value). See *INITDEM_3*.

INITDEM_5 Demodulator control

7	6	5	4	3	2	1	0
IN_DEMOD_EN	SCAN_ON	AUTOSTOP	SCALE_A	SCALE_B		RESERVED	

Address: 0x12

Type: R/W

Reset: 0x08

Description: Demodulator control

[7] **IN_DEMOD_EN**: quadrature demodulation before Nyquist matched filtering.
0: performed using a simpler sequencer that always requires $F_{SAMPLED} = 4 \times F_{CLK}$. In this case, all other bits in registers *INITDEM_0* to *INITDEM_5* are irrelevant.
1: performed by the programmable initial demodulator.

[6] **SCAN_ON**: if 1, enables the frequency scanning feature (IN_DEMOD_EN must be 1 too).

[5] **AUTOSTOP**: if 1, frequency scanning (when enabled) automatically stops as soon as the IC has found a signal to lock onto and enters tracking state.

[4] **SCALE_A**: together with SCALE_B, controls the scaling factor applied in the initial demodulator so that its overall gain is unity. Overall gain is proportional to: $2^{-11} + 2^{-13} \times [2^{(1 + SCALE\_A)} + 2^{SCALE\_B}]$.
Suggested value is 0.

[3:2] **SCALE_B**: together with SCALE_A, controls a scaling factor applied in the initial demodulator so that its overall gain is unity. Suggested value is 10.

[1:0] **Reserved**

DELAGC_0 Maximum PWM rate for AGC2

7	6	5	4	3	2	1	0
AGC2MAX							

Address: 0x14

Type: R/W

Reset: 0x00

Description: Maximum PWM rate for AGC2

[7:0] **AGC2MAX**: defines the maximum PWM rate allowed for AGC2 as:
maximum AGC2 PWM rate = AGC2MAX/0xFF x 100%.
Examples: if AGC2MAX = 0x00, maximum rate = 0% (that is, flat). If 0x40, max. rate = 25%, and so on.

DELAGC_1 Minimum PWM rate for AGC2

7	6	5	4	3	2	1	0
AGC2MIN							

Address: 0x15

Type: R/W

Reset: 0x00

Description: Minimum PWM rate for AGC2

[7:0] **AGC2MIN**: defines the minimum PWM rate allowed for AGC2 as:
minimum AGC2 PWM rate = AGC2MIN/0xFF x 100%.
Examples: if AGC2MIN = 0xFF, minimum rate = 100% (that is, flat). If 0xBF, min. rate = 75%, and so on.

DELAGC_2 Maximum PWM rate for AGC1

7	6	5	4	3	2	1	0
AGC1MAX							

Address: 0x16

Type: R/W

Reset: 0x00

Description: Maximum PWM rate for AGC1

[7:0] **AGC1MAX**: defines the maximum PWM rate allowed for AGC1 as:
maximum AGC1 PWM rate = AGC1MAX/0xFF x 100%.
Examples: if AGC1MAX = 0x00, maximum rate = 0% (that is, flat). If 0x40 max. rate = 25%, and so on.

DELAGC_3 Minimum PWM rate for AGC1

7	6	5	4	3	2	1	0
AGC1MIN							

Address: 0x17

Type: R/W

Reset: 0x00

Description: Minimum PWM rate for AGC1

[7:0] **AGC1MIN**: defines the minimum PWM rate allowed for AGC1 as:
minimum AGC1 PWM rate = AGC1MIN/0xFF x 100%.
Examples: if AGC1MIN = 0xFF, minimum rate = 100% (that is, flat). If 0xBF: min. rate = 75%, and so on.

DELAGC_4 Ratio between AGC1/AGC2 PWM rate slopes

7	6	5	4	3	2	1	0
RATIO_A			RATIO_B		RATIO_C		

Address: 0x18

Type: R/W

Reset: 0x00

Description: Ratio between AGC1/AGC2 PWM rate slopes. For strong RF signals, AGC1 is allowed to decrease from its maximum (nominal) level and the relation between the slopes of AGC1 and AGC2 PWM rates as functions of RF level is user-defined by:

slope[AGC1]/slope[AGC2] = $(2^{RATIO\_A} + 2^{RATIO\_B}) / 2^{RATIO\_C}$.

[7:5] RATIO_A

[4:3] RATIO_B

[2:0] RATIO_C

DELAGC_5 AGC2 PWM rate threshold

7	6	5	4	3	2	1	0
AGC2_THRES							

Address: 0x19

Type: R/W

Reset: 0x00

Description: AGC2 PWM rate threshold

[7:0] **AGC2_THRES**: AGC1 PWM rate is allowed to decrease from its maximum value when the RF input level is above a take-over point defined by the PWM rate of AGC2 falling below the following threshold.

AGC2_THRESH/0d255 x 100%, that is, AGC2_THRESH/0xFF x 100%.

DELAGC_6 AGC freeze control

7	6	5	4	3	2	1	0
DAGC_ON	FRZ2_CTRL		FRZ1_CTRL		RESERVED		

Address: 0x1A

Type: R/W

Reset: 0x00

Description: AGC freeze control

[7] **DAGC_ON**

0: only AGC2 is available for gain control and ACG1 is flat. All other bits in registers 0x14 to 0x1A are irrelevant.

1: delayed AGC feature is active (AGC1 and AGC2 available for optimum tuner and IF stage gain control in application.

[6:5] **FRZ2_CTRL**: (effective only when DAGC_ON = 1).

00: no freeze

01: AGC2 is frozen at its current PWM rate as soon as the AGC loop locks but is released if the AGC loop is forced to unlock (that is, if signal WAGC_ACQ goes back to 0)

10: AGC2 is frozen at its current PWM rate as soon as the AGC loop locks (as flagged by WAGC_ACQ) and is not released until the next general reset (hard or soft)

11: AGC2 is immediately frozen at its current PWM rate

[4:3] **FRZ1_CTRL**: (effective only when DAGC_ON = 1).

00: no freeze

01: AGC1 is frozen at its current PWM rate as soon as the AGC loop locks but is released if the AGC loop is forced to unlock (that is, if signal WAGC_ACQ goes back to 0)

10: AGC1 is frozen at its current PWM rate as soon as the AGC loop locks (as flagged by WAGC_ACQ) and is not released until the next general reset (hard or soft)

11: AGC1 is immediately frozen at its current PWM rate

[2:0] **Reserved**

DELAGC_7 ADC average magnitude (LSBs)

7	6	5	4	3	2	1	0
ADC_AVG_MAG[4:0]				TIME_CST			RESERVED

Address: 0x1C

Type: R/W

Reset: 0x00

Description: ADC average magnitude (LSBs)

[7:4] **ADC_AVG_MAG**[4:0]: four LSBs of ADC average magnitude (unsigned 12-bit value, R). The actual ADC average magnitude rate is: ADC_AVG_MAG/2^4.

For example, if ADC average magnitude = 1024, this means there is an ADC out-of-range event on average every fourth sampling.

[3:1] **TIME_CST**: defines the time constant of the integrator used to measure the ADC average magnitude. The actual time constant (expressed with the clock cycle as time unit) is: $2^{(10 + TIME\_CST)}$, so can range from 2^{10} to 2^{17}.

[0] **Reserved**

DELAGC_8 ADC average magnitude (MSBs)

7	6	5	4	3	2	1	0
ADC_AVG_MAG[11:5]							

Address: 0x1D

Type: R

Reset: 0x00

Description: ADC average magnitude (MSBs)

[7:0] **ADC_AVG_MAG**[11:5]: eight MSBs of ADC average magnitude (unsigned 12-bit value).

DELAGC_10 Analog AGC1

7	6	5	4	3	2	1	0
AGC2SD1[7:0]							

Address: 0x20

Type: R

Reset: Undefined

Description: Analog AGC1

[7:0] **AGC2SD1[7:0]:** 8 LSBs of 2's complement 10-bit value (-512 to +511). AGC2SD1 is sent by delayed AGC.

DELAGC_11 Analog AGC1

7	6	5	4	3	2	1	0
AGC2SD1[9:8]							

Address: 0x21

Type: R

Reset: Undefined

Description: Analog AGC1

[7:2] **Reserved**

[1:0] **AGC2SD1**[9:8]: 2 MSBs of 2's complement 10-bit value (-512 to +511). AGC2SD1 is sent by delayed AGC.

DELAGC_12 Analog AGC2

7	6	5	4	3	2	1	0
AGC2SD2[7:0]							

Address: 0x22

Type: R

Reset: Undefined

Description: Analog AGC2

[7:0] **AGC2SD2**[7:0]: 8 LSBs of 2's complement 10-bit value (-512 to +511). AGC2SD2 is sent by delayed AGC.

DELAGC_13 Analog AGC2

7	6	5	4	3	2	1	0
AGC2SD2[9:8]							

Address: 0x23

Type: R

Reset: Undefined

Description: Analog AGC2

[7:2] **Reserved**

[1:0] **AGC2SD2**[9:8]: 2 MSBs of 2's complement 10-bit value (-512 to +511). AGC2SD2 is sent by delayed AGC.

WBAGC_0 Analog AGCs

7	6	5	4	3	2	1	0
AGC2SD[7:0]]							

Address: 0x24

Type: R/W

Reset: 0x00

Description: Analog AGCs

[7:0] **AGC2SD**[7:0]: 8 LSBs of offset binary 10-bit value AGC2SD sent by the WBAGC block to internal sigma-delta modulator to create AGC1, AGC2 (that is, AGC2SD defines the AGC PWM rates). Its initial value should be programmed to obtain a reasonable initial AGC level given the expected RF input level range to speed up acquisition.

WBAGC_1 Analog AGCs

7	6	5	4	3	2	1	0
RESERVED		ACQ_THRESH				AGC2SD[9:8]	

Address: 0x25

Type: R/W

Reset: 0x02

Description: Analog AGCs

[7:6] **Reserved**

[5:2] **ACQ_THRESH**: WBAGC is considered in lock when the rate of the AGC PWM outputs has not needed any update for $2^{(ACQ\_THRESH)}$ clock cycles. Suggested value: 0xA

[1:0] **AGC2SD**[9:8]: 2 MSBs of offset binary 10-bit value is sent by the WBAGC block to internal sigma-delta modulator to create AGC1, AGC2 and AGC12B. See *WBAGC_0*.

WBAGC_2 WBAGC reference

7	6	5	4	3	2	1	0
RESERVED	I_REF						

Address: 0x26

Type: R/W

Reset: 0x00

Description: WBAGC reference

[7] **Reserved**

[6:0] **I_REF**: WBAGC reference. Defines the value to which the analog AGC loop tries to bring the average magnitude of the signal sampled by the ADC.

WBAGC_3 WBAGC control

7	6	5	4	3	2	1	0
RESERVED	WAGC_CLR	WAGC_INV	WAGC_EN	WAGC_ACQ	SWAP	RESERVED	

Address: 0x27

Type: R/W

Reset: 0x20R

Description: WBAGC control

[7] **Reserved**

[6] **WAGC_CLR**: when 1, resets the WBAGC function (AGC1, AGC2, AGC12B are flat). This bit is self-clearing.

[5] **WAGC_INV**: controls the sense of the WBAGC comparator. Suggested value: 1

[4] **WAGC_EN**: when 1, WBAGC loop is enabled. When 0, it is frozen in its current state (PWM output rates are not allowed to change).

[3] **WAGC_ACQ**: WBAGC lock status (1 when locked).

[2] **SWAP**: defines the ordering of the data bits out of the ADC. (If 0, SAMPLED_IF[0] is LSB; if 1, SAMPLED_IF[0] is MSBs).

[1:0] **Reserved**

WBAGC_4 Acquisition counter (LSBs)

7	6	5	4	3	2	1	0
AGC_COUNT[7:0]							

Address: 0x28

Type: R/W

Reset: 0x00

Description: Acquisition counter (LSBs)

[7:0] **ACQ_COUNT[7:0]:** low byte of the acquisition counter that checks the number of clock cycles without any AGC PWM rate update. Test use only.

WBAGC_5 Acquisition counter (MSBs)

7	6	5	4	3	2	1	0
ACQ_COUNT[15:8]							

Address: 0x29

Type: R/W

Reset: 0x00

Description: Acquisition counter (MSBs)

[7:0] **ACQ_COUNT**[15:8]: high byte of the acquisition counter that checks the number of clock cycles without any PWM_OUT rate update. Test use only.

WBAGC_6 AGC loop response (LSBs)

7	6	5	4	3	2	1	0
ROLL[7:0]							

Address: 0x2A

Type: R/W

Reset: 0x00

Description: AGC loop response (LSBs)

[7:0] **ROLL**[7:0]: low byte of the unsigned value that controls the AGC loop response. The greater this value, the smaller the loop bandwidth.

WBAGC_7 AGC loop response (MSBs)

7	6	5	4	3	2	1	0
ROLL[15:8]							

Address: 0x2B

Type: R/W

Reset: 0x00

Description: AGC loop response (MSBs)

[7:0] **ROLL**[15:8]: high byte of the unsigned value that controls the AGC loop response. The greater this value, the smaller the loop bandwidth.

STLOOP_1 Symbol timing recovery loop gain (LSBs)

7	6	5	4	3	2	1	0
DIRECT_GAIN[7:0]							

Address: 0x2C

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop gain (LSBs)

[7:0] **DIRECT_GAIN**[7:0]: defines the gain of the direct path in the timing recovery loop. The greater this value, the greater the timing loop damping factor. (Damping factor is also defined by INTEGRAL_GAIN below).

Algorithms #1, #2, #3: 7 bits used by these algorithms.

Algorithm #0: 8 LSBs of the 11-bit value for this algorithm.

STLOOP_2 Symbol timing recovery loop gain (MSBs)

7	6	5	4	3	2	1	0
RESERVED					DIRECT_GAIN[10:8]		

Address: 0x2D

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop gain (MSBs)

[7:3] Reserved

[2:0] **DIRECT_GAIN**[10:8]: see *STLOOP_1*.

Not used by algorithms #1, #2, #3. Algorithms #0: MSBs of the 11-bit value for this algorithm.

STLOOP_3 Symbol timing recovery loop integral gain (LSBs)

7	6	5	4	3	2	1	0
INTEGRAL_GAIN[7:0]							

Address: 0x2E

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop integral gain (LSBs)

[7:0] **INTEGRAL_GAIN**[7:0]: defines the gain of the integral path in the timing recovery loop. The greater this value, the wider the timing loop bandwidth and the smaller the damping factor. (Damping factor is also defined by DIRECT_GAIN above). Should not be programmed to 0x1F.

Algorithms #1, #2, #3: LSBs of the 10-bit coding gain value. Algorithm #0: 8 bits of the coding gain.

STLOOP_4 Symbol timing recovery loop gain scale

7	6	5	4	3	2	1	0
GAIN_SCALE_PATH0			GAIN_SCALE_PATH1			INTEGRAL_GAIN[9:8]	

Address: 0x2F

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop gain scale

[7:5] **GAIN_SCALE_PATH0**: not used with STL algorithm #0.
With STL algorithms #1 to 3 (*STLOOP_10*): defines the reduction factor ($2^{GAIN\_SCALE\_PATH0}$) automatically applied to the direct gain once the symbol timing loop has completed and is in tracking mode in order to reduce the jitter on the recovered symbol sampling instants. Causes the damping factor to decrease by $2^{GAIN\_SCALE\_PATH0}$ (damping factor adjustment is also affected by GAIN_SCALE_PATH1).

[4:2] **GAIN_SCALE_PATH1**: not used with STL algorithm #0.
With STL algorithms #1 to 3 (*STLOOP_10*): defines the reduction factor ($2^{GAIN\_SCALE\_PATH1}$) applied to the integral gain once the symbol timing loop has completed and is in tracking mode in order to reduce the jitter on the recovered symbol sampling instants. Causes the STL loop bandwidth to decrease by SQRT ($2^{GAIN\_SCALE\_PATH1}$) and the damping factor to increase by this same factor (damping factor adjustment is also affected by GAIN_SCALE_PATH0).

[1:0] **INTEGRAL_GAIN**[9:8]: not used with STL #0 (INTEGRAL_GAIN_LO only is used with STL #0).
With STL algorithms #1 to 3: MSBs of the 10-bit value coding the gain of the integral path in the timing recovery loop. The greater this value, the wider the STL loop bandwidth.

STLOOP_5 Symbol rate (LSBs)

7	6	5	4	3	2	1	0
SYMB_RATE[7:0]							

Address: 0x30

Type: R/W

Reset: 0x00

Description: Symbol rate (LSBs)

[7:0] **SYMB_RATE**[7:0]: low byte of a 32-bit accumulator that represents the symbol timing frequency. This accumulator must be initialized by the user according to the following formula:
SYMB_RATE[31:0] = 2^{32} x (nominal symbol rate / system clock frequency).
The symbol rate is taken into account only when writing the MSB (*STLOOP_8*).

STLOOP_6 Symbol rate (lower mid byte)

7	6	5	4	3	2	1	0
SYMB_RATE[15:8]							

Address: 0x31

Type: R/W

Reset: 0x00

Description: Symbol rate (lower mid byte)

[7:0] **SYMB_RATE**[15:8]: second byte of a 32-bit accumulator that represents the symbol timing frequency. This accumulator must be initialized by the user according to the formula given for *STLOOP_5*.

STLOOP_7 Symbol rate (upper mid byte)

7	6	5	4	3	2	1	0
SYMB_RATE_2[23:16]							

Address: 0x32

Type: R/W

Reset: 0x00

Description: Symbol rate (upper mid byte)

[7:0] **SYMB_RATE_2**[23:16]: third byte of a 32-bit accumulator that represents the symbol timing frequency. This accumulator must be initialized by the user according to the formula given for *STLOOP_5*.

STLOOP_8 Symbol rate (MSBs)

7	6	5	4	3	2	1	0
SYMB_RATE_3[31:24]							

Address: 0x33

Type: R/W

Reset: 0x00

Description: Symbol rate (MSBs)

[7:0] **SYMB_RATE_3**[31:24]: most significant byte of a 32-bit accumulator that represents the symbol timing frequency. This accumulator must be initialized by the user according to the formula given for *STLOOP_5*.

STLOOP_9 Symbol timing recovery loop phase control

7	6	5	4	3	2	1	0
RESERVED	PHASE_EN	PHASE_CLR	ERR_RANGE				

Address: 0x34

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop phase control

[7] Reserved

[6] **PHASE_EN**: when 1, forces the direct path to be immediately enabled even though previous stages have not locked yet.

[5] **PHASE_CLR**: when 1, clears the STL accumulator, internal symbol enable pulses are no more generated. Also has the effect of freezing all blocks that work at symbol rate, in particular CRL and STL.

[4:0] **ERR_RANGE**: can be used to saturate the timing frequency correction accumulator to $\pm 2^{(ERR\_RANGE + 1)} - 1$. Should not be programmed to 0x1F. Suggested value: 0x1E.

STLOOP_10 Symbol timing recovery loop algorithm control

7	6	5	4	3	2	1	0
ROLLOFF		ALGOSEL		DIR	EN_DIR	ERR_CLR	ERR_EN

Address: 0x35

Type: R/W

Reset: 0x00

Description: Symbol timing recovery loop algorithm control

[7:6] **ROLLOFF**: selection of the Nyquist filter roll-off:
00: 0.15 01: 0.12
10: 0.18

[5:4] **ALGOSEL**: defines the algorithm used for symbol timing recovery in the symbol timing loop.
00: STL algorithm #0. 01: STL algorithm #1.
10: STL algorithm #2. 11: STL algorithm #3.

[3] **DIR**: controls the polarity of the discriminant timing. For test use only - set to 0.

[2] **EN_DIR**: when 1, the timing loop includes a direct path, when 0 only the integral path has an effect. For test use only. Set to 1.

[1] **ERR_CLR**: when 1, clears the STL integral path.

[0] **ERR_EN**: when 1, forces the integral path to be immediately enabled even though the WBAGC has not fully locked yet.

CRL_1 Carrier recovery loop gain

7	6	5	4	3	2	1	0
PN_LOOP_BYPASS	GAIN_DIR			GAIN_INT			

Address: 0x38

Type: R/W

Reset: 0x00

Description: Carrier recovery loop gain

[7] **PN_LOOP_BYPASS**: when set to 1, the phase noise loop is bypassed. When set to 0, the loop is active.

[6:4] **GAIN_DIR**: defines the gain of the direct path in the carrier recovery loop. The greater this value, the greater the damping factor. (Damping factor is also defined by GAIN_INT below).

[3:0] **GAIN_INT**: defines the gain of the integral path in the carrier recovery loop. The greater this value, the wider the carrier loop bandwidth and the smaller the damping factor. (Damping factor is also defined by GAIN_DIR above).

CRL_2 Carrier recovery loop gain reduction factor

7	6	5	4	3	2	1	0
GAIN_DIR_PN				GAIN_DIR_ADJ		GAIN_INT_ADJ	

Address: 0x39

Type: R/W

Reset: 0x06

Description: Carrier recovery loop gain reduction factor

[7:4] **GAIN_DIR_PN**: defines the gain of the phase noise (PN) loop (see *CRL_8*).

[3:2] **GAIN_DIR_ADJ**: defines the reduction factor applied to the direct gain once the chip has acquired and is in tracking mode in order to reduce the jitter on the recovered carrier phase. Causes the damping factor to decrease by a factor $2^{GAIN\_DIR\_ADJ}$. (Damping factor adjustment is also affected by GAIN_INT_ADJ below).

[1:0] **GAIN_INT_ADJ**: defines the reduction factor applied to the integral gain once the chip has acquired and is in tracking mode in order to reduce the jitter on the recovered carrier phase. Causes the carrier loop bandwidth to decrease by factor $SQRT(2^{GAIN\_INT\_ADJ})$ and the damping factor to increase by this same factor. (Damping factor adjustment is also affected by GAIN_DIR_ADJ above).

CRL_3 Carrier recovery loop control

7	6	5	4	3	2	1	0
RESERVED	PN_LOOP_SEL	INT_DIS	DIR_DIS	INT_EN	DIR_EN	PH_EN	SW_EN

Address: 0x3A

Type: R/W

Reset: 0x00

Description: Carrier recovery loop control

[7] **Reserved**

[6] **PN_LOOP_SEL**: carrier recovery loop configuration.
0: CRL uses equalizer output. 1: CRL uses phase-noise loop output.

[5] **INT_DIS**: when 1, disables the integral path of the carrier recovery loop.

[4] **DIR_DIS**: when 1, disables the direct path of the carrier recovery loop.

[3] **INT_EN**: when 1, forces the integral path to be immediately enabled even though previous stages have not locked yet.

[2] **DIR_EN**: when 1, forces the direct path to be immediately enabled even though previous stages have not locked yet.

[1] **PH_EN**: when 1, enables the phase accumulator, when 0, freezes at its current value.

[0] **SW_EN**: when 1, enables the frequency sweep function.

CRL_4 Carrier recovery loop capture

7	6	5	4	3	2	1	0
CRL_SNAPSHOT							

Address: 0x3B

Type: R/W

Reset: 0x00

Description: Carrier recovery loop capture

[7:0] **CRL_SNAPSHOT**: CRL status is captured in APHASE[23:0] and IPHASE[27:0] when a dummy write is performed at this address. Otherwise the contents of these registers are undetermined.

CRL_5 Carrier recovery loop phase accumulator (LSBs)

7	6	5	4	3	2	1	0
APHASE[7:0]							

Address: 0x3C

Type: R/W

Reset: 0x00

Description: Carrier recovery loop phase accumulator (LSBs)

[7:0] **APHASE**[7:0]: low byte of the phase accumulator used for phase and frequency offset compensation. Normally does not need programming. See also *CRL_4*.

CRL_6 Carrier recovery loop phase accumulator (mid byte)

7	6	5	4	3	2	1	0
APHASE[15:8]							

Address: 0x3D

Type: R/W

Reset: 0x00

Description: Carrier recovery loop phase accumulator (mid byte)

[7:0] **APHASE**[15:8]: medium byte of the phase accumulator used for phase and frequency offset compensation. Normally does not need programming. See also *CRL_4*.

CRL_7 Carrier recovery loop phase accumulator (MSBs)

7	6	5	4	3	2	1	0
APHASE[23:16]							

Address: 0x3E

Type: R/W

Reset: 0x00

Description: Carrier recovery loop phase accumulator (MSBs)

[7:0] **APHASE**[23:16]: high byte of the phase accumulator used for phase and frequency offset compensation. Normally does not need programming. See also *CRL_4*.

CRL_8 2nd carrier recovery loop coefficient

7	6	5	4	3	2	1	0
RESERVED		CRL_TH	CRL_COEFF				

Address: 0x3F

Type: R/W

Reset: 0x00

Description: 2nd carrier recovery loop coefficient

[7:6] **Reserved**

[5] **CRL_TH**: carrier recovery loop threshold. When set to 1, the thresholds are -16/+15, when 0, -3/+3.

[4:0] **CRL_COEFF**: carrier recovery loop coefficient. Used to obtain the phase-noise loop gain factor. PN loop gain = (CRL_COEFF/16) x $2^{GAIN\_DIR\_PN + 3}$(see *CRL_2*).
Example: if CRL_COEFF = 0x08, PN loop gain = 8/16 x $2^{GAIN\_DIR\_PN}$ = 0.5 x $2^{GAIN\_DIR\_PN + 3}$.

CRL_9 Carrier recovery loop frequency offset (LSBs)

7	6	5	4	3	2	1	0
IPHASE[7:0]							

Address: 0x40

Type: R/W

Reset: 0x00

Description: Carrier recovery loop frequency offset (LSBs)

[7:0] **IPHASE**[7:0]: low byte of a signed 28-bit accumulator that represents the demodulation frequency offset (after mirroring if spectral inversion is enabled through bit SPEC_INV in *CTRL_5*). This accumulator must be programmed to its nominal value by the user according to the following formula:
F_offset = (IPHASE / 2^{28}) x F_S [F_S = symbol rate]
Important: taken into account only on writing of *CRL_14*. See also *CRL_4*.

CRL_10 Carrier recovery loop frequency offset (lower mid byte)

7	6	5	4	3	2	1	0
IPHASE[15:8]							

Address: 0x41

Type: R/W

Reset: 0x00

Description: Carrier recovery loop frequency offset (lower mid byte)

[7:0] **IPHASE**[15:8]: second byte of a signed 28-bit accumulator. See *CRL_9*.

CRL_11 Carrier recovery loop frequency offset (upper mid byte)

7	6	5	4	3	2	1	0
IPHASE[23:16]							

Address: 0x42

Type: R/W

Reset: 0x00

Description: Carrier recovery loop frequency offset (upper mid byte)

[7:0] **IPHASE**[23:16]: third byte of a signed 28-bit accumulator. See *CRL_9*.

CRL_12 Carrier recovery loop frequency offset (MSBs)

7	6	5	4	3	2	1	0
RESERVED				IPHASE[27:24]			

Address: 0x43

Type: R/W

Reset: 0x00

Description: Carrier recovery loop frequency offset (MSBs)

[7:4] **Reserved**

[3:0] **IPHASE**[27:24]: four MSBs of a signed 28-bit accumulator. See *CRL_9*.

CRL_13 Carrier recovery loop sweep value (LSBs)

7	6	5	4	3	2	1	0
SWEEP[7:0]							

Address: 0x44

Type: R/W

Reset: 0x00

Description: Carrier recovery loop sweep value (LSBs)

[7:0] **SWEEP**[7:0]: low byte of a signed 12-bit frequency sweep value. The sweep operation consists of a frequency shift (with respect to IPHASE) every symbol defined by: Fshift = (sweep_value / 2^{28}) x F_S.
The sweep rate in Hz/s is therefore: Rsweep = (sweep_value / 2^{28}) x F_S^2
Note: Writing of CRL_9 to CRL_12 must be followed by write access to this register.

CRL_14 Carrier recovery loop sweep value (MSBs)

7	6	5	4	3	2	1	0
RESERVED				SWEEP[3:0]			

Address: 0x45

Type: R/W

Reset: 0x00

Description: Carrier recovery loop sweep value (MSBs)

[7:4] **Reserved**

[3:0] **SWEEP**[11:8]: four MSBs of a signed 12-bit frequency sweep value. See *CRL_13*.

PMFAGC_0 PMFAGC lock threshold (LSBs)

7	6	5	4	3	2	1	0
LOCK_THRESH[7:0]							

Address: 0x48

Type: R/W

Reset: 0xFF

Description: PMFAGC lock threshold (LSBs)

[7:0] **LOCK_THRESH**[7:0]: LSBs of the value that codes the number of clock cycles after which it is assumed that the PMFAGC has locked. Suggested value: 0xFF.

PMFAGC_1 PMFAGC lock threshold (MSBs)

7	6	5	4	3	2	1	0
RESERVED				LOCK_THRESH[11:8]			

Address: 0x49

Type: R/W

Reset: 0x04

Description: PMFAGC lock threshold (MSBs)

[7:4] Reserved

[3:0] **LOCK_THRESH**[11:8]: four MSBs of the value that codes the number of clock cycles after which it is assumed that the PMFAGC has locked. Suggested value: 0x4.

PMFAGC_2 PMFAGC control

7	6	5	4	3	2	1	0
RESERVED			PMFA_LOCK_STATE	PMFA_F_UNLOCK	PMFA_F_LOCK	WBAGC_F_LOCK	UP_STOP

Address: 0x4A

Type: R/W

Reset: 0x00

Description: PMFAGC control

[7:5] **Reserved**

[4] **PMFA_LOCK_STATE**: internal flag that indicates if the PMFAGC has locked.

[3] **PMFA_F_UNLOCK**: overrides the internal PMFAGC lock status bit to be unlocked.

[2] **PMFA_F_LOCK**: overrides the internal PMFAGC lock status bit to be locked.

[1] **WBAGC_F_LOCK**: overrides the internal WBAGC lock status bit to be locked.

[0] **UP_STOP**: stops PMFAGC update, post-filter gain is stuck at its current value. Normal value: 0.

PMFAGC_3 Post-filter digital AGC (PMFAGC)

7	6	5	4	3	2	1	0
PMFA_ACC[7:0]							

Address: 0x4C

Type: R/W

Reset: 0x00

Description: Post-filter digital AGC (PMFAGC)

[7:0] **PMFA_ACC**[7:0]: low byte of the unsigned 20-bit accumulator that controls the scaling performed by the PMFAGC block. Normally does not need programming.

PMFAGC_4 Post-filter digital AGC (PMFAGC)

7	6	5	4	3	2	1	0
PMFA_ACC[15:8]							

Address: 0x4D

Type: R/W

Reset: 0x00

Description: Post-filter digital AGC (PMFAGC)

[7:0] **PMFA_ACC**[15:8]: second byte of the unsigned 20-bit accumulator that controls the scaling performed by the PMFAGC block. Normally does not need programming.

PMFAGC_5 Post-filter digital AGC (PMFAGC)

7	6	5	4	3	2	1	0
PMFA_ACC[19:16]							

Address: 0x4E

Type: R/W

Reset: 0x0D

Description: Post-filter digital AGC (PMFAGC)

[7:4] Reserved

[3:0] **PMFA_ACC**[19:16]: four MSBs of an unsigned 20-bit accumulator that controls the scaling performed by the PMFAGC block. Normally does not need programming.

INTER_0 Interrupt mask 1

7	6	5	4	3	2	1	0
MPEGA	UNCORRA	DI_LOCKA	CARRIER_LOCK	LMS2	LMS1	WBAGC_LOCK_ENABLE	MPEGB

Address: 0x50

Type: R/W

Reset: 0xFF

Description: Interrupt mask 1. When a bit is set to 1, it indicates that the corresponding interrupt register is masked.

[7] **MPEGA**: MPEG - FEC A/C mask.

[6] **UNCORRA**: UNCORR - FEC A/C mask.

[5] **DI_LOCKA**: DI_LOCK - FEC A/C mask.

[4] **CARRIER_LOCK**: carrier lock mask.

[3] **LMS2**: EQU_LMS2 mask.

[2] **LMS1**: EQU_LMS1 mask.

[1] **WBAGC_LOCK_ENABLE**: WAGC_IT mask.

[0] **MPEGB**: MPEG - FEC B mask.

INTER_1 Interrupt mask 2

7	6	5	4	3	2	1	0
UNCORRB	SYNCQ	SYNCI	ENFADDET	ENCRL_UL_IT	UPDATE_READY	END_FRAME_HEADER	CONTCNT_EVENT

Address: 0x51

Type: R/W

Reset: 0xFF

Description: Interrupt mask 2. When a bit is set to 1, it indicates that the corresponding interrupt register is masked.

[7] **UNCORRB**: UNCORR - FEC B mask.

[6] **SYNCQ**: Viterbi sync Q mask.

[5] **SYNCI**: Viterbi sync I mask.

[4] **ENFADDET**: fading detection mask.

[3] **ENCRL_UL_IT**: lock-to-unlock detection mask.

[2] **UPDATE_READY**: new TSMF from header receive mask.

[1] **END_FRAME_HEADER**: TSMF frame header receive mask.

[0] **CONTCNT_EVENT**: TSMF from header receive with an invalid continuity counter field mask.

INTER_2 Interrupt 1

7	6	5	4	3	2	1	0
MPEGA	UNCORRA	DI_LOCKA	CARRIER_LOCK	LMS2	LMS1	WBAGC_LOCK_ENABLE	MPEGB

Address: 0x52

Type: R

Reset: 0x00

Description: Software interrupt register. When a bit is set to 1, it indicates that the corresponding source has caused an exception. These bits can only be set to 1 by an exception.

[7] **MPEGA**: MPEG - FEC A/C. FEC A/C has fully locked on MPEG data.

[6] **UNCORRA**: UNCORR - FEC A/C. Reed–Solomon uncorrectable error for FEC A/C.

[5] **DI_LOCKA**: DI_LOCK - FEC A/C. De-interleaver sync detector is in lock in FEC A/C.

[4] **CARRIER_LOCK**: carrier lock (corner lock). CRL (CARRIER_LOOP) is in lock state.

[3] **LMS2**: EQU_LMS2. Equalizer has sufficiently converged and has entered step 2 of LMS algorithm.

[2] **LMS1**: EQU_LMS1. Equalizer has sufficiently converged and has entered step 1 of LMS algorithm.

[1] **WBAGC_LOCK_ENABLE**: WAGC_IT. WBAGC has locked; asserted on rise of WAGC_ACQ in *WBAGC_3*.

[0] **MPEGB**: MPEG - FEC B. FEC B has fully locked on MPEG data.

INTER_3 Interrupt 2

7	6	5	4	3	2	1	0
UNCORRB	SYNCQ	SYNCI	ENFADDET_IT	ENCRL_UL_IT	UPDATE_READY	END_FRAME_HEADER	CONTCNT_EVENT

Address: 0x53

Type: R

Reset: 0x00

Description: Software interrupt register. When a bit is set to 1, it indicates that the corresponding source has caused an exception. These bits can only be set to 1 by an exception.

[7] **UNCORRB**: UNCORR - FEC B. Reed–Solomon uncorrectable error for FEC B.

[6] **SYNCQ**: Viterbi sync Q acquired for FEC B.

[5] **SYNCI**: Viterbi sync I acquired for FEC B.

[4] **ENFADDET_IT**: signal fading detected.

[3] **ENCRL_UL_IT**: CRL switch from locked to unlocked.

[2] **UPDATE_READY**: TSMF receives a new frame header.

[1] **END_FRAME_HEADER**: TSMF receives frame header.

[0] **CONTCNT_EVENT**: an invalid continuity counter field received with the frame header.

SIG_FAD_0 Signal fading control

7	6	5	4	3	2	1	0
RESERVED			MAGMEANLENGTH				ENFADDET

Address: 0x58

Type: R/W

Reset: 0x14

Description: Signal fading control

[7:5] **Reserved**

[4:1] **MAGMEANLENGTH**: $2^{MAGMEANLENGTH}$ is the integration length used for signal fading detection.

[0] **ENFADDET**: When 1, the signal fading detection/correction is active.

SIG_FAD_1 Signal fading magnitude

7	6	5	4	3	2	1	0
MAGMEAN							

Address: 0x59

Type: R

Reset: 0x00

Description: Signal fading magnitude

[7:0] **MAGMEAN**: measured mean magnitude.

SIG_FAD_2 Signal fading low threshold

7	6	5	4	3	2	1	0
MAGMEAN_TH1							

Address: 0x5A

Type: R/W

Reset: 0x06

Description: Signal fading low threshold

[7:0] **MAGMEAN_TH1**: low threshold for fading detection.

SIG_FAD_3 Signal fading high threshold

7	6	5	4	3	2	1	0
MAGMEAN_TH2							

Address: 0x5B

Type: R/W

Reset: 0x12

Description: Signal fading high threshold

[7:0] **MAGMEAN_TH2**: high threshold for fading detection.

NEW_CRL_0 CRL direct gain in blind mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_DIR_BLIND				

Address: 0x5C

Type: R/W

Reset: 0x00

Description: CRL direct gain in blind mode

[7:5] **Reserved**

[4:0] **GAIN_DIR_BLIND**: CRL filter direct gain when in blind mode.

NEW_CRL_1 CRL integral gain in blind mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_INT_BLIND				

Address: 0x5D

Type: R/W

Reset: 0x00

Description: CRL integral gain in blind mode

[7:5] **Reserved**

[4:0] **GAIN_INT_BLIND**: CRL filter integral gain when in blind mode.

NEW_CRL_2 CRL direct gain in LMS_1 mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_DIR_LMS1				

Address: 0x5E

Type: R/W

Reset: 0x00

Description: CRL direct gain in LMS_1 mode

[7:5] **Reserved**

[4:0] **GAIN_DIR_LMS1**: CRL filter direct gain when in LMS_1 mode.

NEW_CRL_3 CRL integral gain in LMS_1 mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_INT_LMS1				

Address: 0x5F

Type: R/W

Reset: 0x00

Description: CRL integral gain in LMS_1 mode

[7:5] **Reserved**

[4:0] **GAIN_INT_LMS1**: CRL filter integral gain when in LMS_1 mode.

NEW_CRL_4 CRL direct gain in LMS_2 mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_DIR_LMS2				

Address: 0x60

Type: R/W

Reset: 0x00

Description: CRL direct gain in LMS_2 mode

[7:5] **Reserved**

[4:0] **GAIN_DIR_LMS2**: CRL filter direct gain when in LMS_2 mode.

NEW_CRL_5 CRL integral gain in LMS_2 mode

7	6	5	4	3	2	1	0
RESERVED			GAIN_INT_LMS2				

Address: 0x61

Type: R/W

Reset: 0x00

Description: CRL integral gain in LMS_2 mode

[7:5] **Reserved**

[4:0] **GAIN_INT_LMS2**: CRL filter integral gain when in LMS_2 mode.

NEW_CRL_6 CRL second mode control

7	6	5	4	3	2	1	0
RESERVED				HIGHLOOPGAIN_EN	CORRECTIONFLAG_F		CRLLOCKEDFLAG

Address: 0x62

Type: R/W

Reset: 0x00

Description: CRL second mode control

[7:4] **Reserved**

[3] **HIGHLOOPGAIN_EN**: When 0, use of 297 like gains.

[2:1] **CORRECTIONFLAG_F**
0X: default mode.
11: PHASECORRECTIONFLAG is forced to 1.
10: PHASECORRECTIONFLAG is forced to 0.

[0] **CRLLOCKEDFLAG**: copy of the internal value of CRLLOCKEDFLAG.

FREQ_0 Frequency estimator 0

7	6	5	4	3	2	1	0
PHASEOFF_TH[1:0]		MAXDIST_TH					

Address: 0x64

Type: R/W

Reset: 0x00

Description: Frequency estimator 0

[7:6] **PHASEOFF_TH[1:0]:** Phase difference maximum value (LSBs).

[5:0] **MAXDIST_TH**: Maximum inter-corner points distance.

FREQ_1 Frequency estimator 1

7	6	5	4	3	2	1	0
PHASEOFF_TH[9:2]							

Address: 0x65

Type: R/W

Reset: 0x00

Description: Frequency estimator 1

[7:0] **PHASEOFF_TH[9:2]**: Phase difference maximum value (MSBs).

FREQ_2 Frequency estimator blind-mode integration length

7	6	5	4	3	2	1	0
RESERVED		MEANLENGTHDOPPLER_BLIND					

Address: 0x66

Type: R/W

Reset: 0x00

Description: Frequency estimator blind-mode integration length

[7:6] **Reserved**

[5:0] **MEANLENGTHDOPPLER_BLIND**: Integration length of the frequency estimator in blind mode.

FREQ_3 Frequency estimator LMS_1-mode integration length

7	6	5	4	3	2	1	0
RESERVED		MEANLENGTHDOPPLER_LMS1					

Address: 0x67

Type: R/W

Reset: 0x00

Description: Frequency estimator LMS_1-mode integration length

[7:6] **Reserved**

[5:0] **MEANLENGTHDOPPLER_LMS1**: integration length of the frequency estimator in LMS_1 mode.

FREQ_4 Frequency estimator LMS_2-mode integration length

7	6	5	4	3	2	1	0
RESERVED		MEANLENGTHDOPPLER_LMS2					

Address: 0x68

Type: R/W

Reset: 0x00

Description: Frequency estimator LMS_2-mode integration length

[7:6] **Reserved**

[5:0] **MEANLENGTHDOPPLER_LMS2**: integration length of the frequency estimator in LMS_2 mode.

FREQ_5 Frequency estimator corner-point low threshold (LSBs)

7	6	5	4	3	2	1	0
CORNETPTS_LOW_TH[7:0]							

Address: 0x69

Type: R/W

Reset: 0xF4

Description: Frequency estimator corner-point low threshold (LSBs)

[7:0] **CORNETPTS_LOW_TH[7:0]:** low threshold value (LSBs).

FREQ_6 Frequency estimator corner-point thresholds

7	6	5	4	3	2	1	0
CORNETPTS_HIGH_TH[1:0]		STD_EST_CRL_SHIFT				CORNETPTS_LOW_TH[9:8]	

Address: 0x6A

Type: R/W

Reset: 0x80

Description: Frequency estimator corner-point thresholds

[7:6] **CORNETPTS_HIGH_TH**[1:0]: high threshold value (LSBs).

[5:2] **STD_EST_CRL_SHIFT**: provides gain applied to the CRL unlocked detector when the input is the integral path of the CRL filter output. Gain is: $2^{(STD\_EST\_CRL\_SHIFT + 4)}$. See also *FREQ_15*.

[1:0] **CORNETPTS_LOW_TH**[9:8]: low threshold value (MSBs).

FREQ_7 Frequency estimator corner-point high threshold (MSBs)

7	6	5	4	3	2	1	0
CORNETPTS_HIGH_TH[9:2]							

Address: 0x6B

Type: R/W

Reset: 0x45

Description: Frequency estimator corner-point high threshold (MSBs)

[7:0] **CORNETPTS_HIGH_TH**[9:2]: high threshold value (MSBs).

FREQ_8 Frequency estimation (LSBs)

7	6	5	4	3	2	1	0
FREQESTCURRENT[7:0]							

Address: 0x6C

Type: R

Reset: 0x00

Description: Frequency estimation (LSBs)

[7:0] **FREQESTCURRENT**[7:0]: Current estimation produced by the frequency estimator is given by: Frequency = (FREQESTCURRENT[23:0]/2^{24}) x SYMB_RATE.

FREQ_9 Frequency estimation (mid byte)

7	6	5	4	3	2	1	0
FREQESTCURRENT[15:8]							

Address: 0x6D

Type: R

Reset: 0x00

Description: Frequency estimation (mid byte)

[7:0] **FREQESTCURRENT**[15:8]: Current estimation realized by the frequency estimator.

FREQ_10 Frequency estimation (MSBs)

7	6	5	4	3	2	1	0
FREQESTCURRENT[23:16]							

Address: 0x6E

Type: R

Reset: 0x00

Description: Frequency estimation (MSBs)

[7:0] **FREQESTCURRENT**[23:16]: Current estimation realized by the frequency estimator.

FREQ_11 Unlocked integration length

7	6	5	4	3	2	1	0
NSTDEST_FREQEST				NSTDEST_INTPATH			

Address: 0x6F

Type: R/W

Reset: 0x00

Description: Unlocked integration length

[7:4] **NSTDEST_FREQEST**: $2^{NSTDEST\_FREQEST}$ is the integration length used in the CRL unlocked detector when its input is the frequency estimator.

[3:0] **NSTDEST_INTPATH**: $2^{NSTDEST\_INTPATHT}$ is the integration length used in the CRL unlocked detector when its input is the integral path of the CRL filter output.

FREQ_12 Unlocked low threshold (LSBs)

7	6	5	4	3	2	1	0
STDEST_TH1[7:0]							

Address: 0x70

Type: R/W

Reset: 0x00

Description: Unlocked low threshold (LSBs)

[7:0] **STDEST_TH1**[7:0]: low threshold for the CRL unlocked detector.

FREQ_13 Unlocked low threshold (mid byte)

7	6	5	4	3	2	1	0
STDEST_TH1[15:8]							

Address: 0x71

Type: R/W

Reset: 0x00

Description: Unlocked low threshold (mid byte)

[7:0] **STDEST_TH1**[15:8]: low threshold for the CRL unlocked detector.

FREQ_14 Unlocked low threshold (MSBs)

7	6	5	4	3	2	1	0
STDEST_TH1[23:16]							

Address: 0x72

Type: R/W

Reset: 0x00

Description: Unlocked low threshold (MSBs)

[7:0] **STDEST_TH1**[23:16]: Low threshold for the CRL unlocked detector.

FREQ_15 CRL control

7	6	5	4	3	2	1	0
CRL_UL_F		FREQESTCORR_BLIND_EN	FREQESTCORR_LMS1_EN	FREQESTCORR_LMS2_EN	RESERVED	FREQ_OFFSET	RESET_CRL

Address: 0x73

Type: R/W

Reset: 0x02

Description: CRL control

[7:6] **CRL_UL_F**
0x: state machine take decision
10: forces the unlocked detector input with the frequency estimator
11: forces the unlocked detector input with the CRL filter integral path
Suggested value: 10

[5] **FREQESTCORR_BLIND_EN**: when 1, the frequency estimation is used to initialize the NCO in blind mode.

[4] **FREQESTCORR_LMS1_EN**: when 1, the frequency estimation is used to initialize the NCO in LMS_1 mode.

[3] **FREQESTCORR_LMS2_EN**: when 1, the frequency estimation is used to initialize the NCO in LMS_2 mode.

[2] **Reserved**

[1] **FREQ_OFFSET**: *FREQ_8*, *FREQ_9*, *FREQ_10* indication.
0: registers show current estimation 1: registers show frequency offset

[0] **RESET_CRL**: when 1, the frequency estimator is reset until a 0 is written.

FREQ_16 Unlocked high threshold (LSBs)

7	6	5	4	3	2	1	0
STDEST_TH2[7:0]							

Address: 0x74

Type: R/W

Reset: 0x00

Description: Unlocked high threshold (LSBs)

[7:0] **STDEST_TH2**[7:0]: high threshold for the CRL unlocked detector.

FREQ_17 Unlocked high threshold (mid byte)

7	6	5	4	3	2	1	0
STDEST_TH2[15:8]							

Address: 0x75

Type: R/W

Reset: 0x00

Description: Unlocked high threshold (mid byte)

[7:0] **STDEST_TH2**[15:8]: high threshold for the CRL unlocked detector.

FREQ_18 Unlocked high threshold (MSBs)

7	6	5	4	3	2	1	0
STDEST_TH2[23:16]							

Address: 0x76

Type: R/W

Reset: 0x00

Description: Unlocked high threshold (MSBs)

[7:0] **STDEST_TH2**[23:16]: high threshold for the CRL unlocked detector.

FREQ_19 FFE input in blind mode

7	6	5	4	3	2	1	0
RESERVED	FFE_IN_UNLOCKED				FFE_IN_LOCKED		EQ_UP_CRL_UL

Address: 0x77

Type: R/W

Reset: 0x00

Description: FFE input in blind mode

[7] **Reserved**

[6:4] **FFE_IN_UNLOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is unlocked in blind mode.

[3:1] **FFE_IN_LOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is locked in blind mode.

[0] **EQ_UP_CRL_UL**: when 1, the equalizer coefficients update process is stopped when the CRL is unlocked.

FREQ_20 CRL unlocked detector current output (LSBs)

7	6	5	4	3	2	1	0
STDEST_CURRENT[7:0]							

Address: 0x78

Type: R

Reset: 0x00

Description: CRL unlocked detector current output (LSBs)

[7:0] **STDEST_CURRENT**[7:0]: current output of the CRL unlocked detector.

FREQ_21 CRL unlocked detector current output (mid byte)

7	6	5	4	3	2	1	0
STDEST_CURRENT[15:8]							

Address: 0x79

Type: R

Reset: 0x00

Description: CRL unlocked detector current output (mid byte)

[7:0] **STDEST_CURRENT**[15:8]: current output of the CRL unlocked detector.

FREQ_22 CRL unlocked detector current output (MSBs)

7	6	5	4	3	2	1	0
STDEST_CURRENT[23:16]							

Address: 0x7A

Type: R

Reset: 0x00

Description: CRL unlocked detector current output (MSBs)

[7:0] **STDEST_CURRENT**[23:16]: current output of the CRL unlocked detector.

FREQ_23 FFE input in LMS_1 mode

7	6	5	4	3	2	1	0
FFE_IN_UNLOCKED			FFE_IN_LOCKED			RESERVED	

Address: 0x7B

Type: R/W

Reset: 0x00

Description: FFE input in LMS_1 mode

[7:5] **FFE_IN_UNLOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is unlocked in LMS_1 mode.

[4:2] **FFE_IN_LOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is locked in LMS_1 mode.

[1:0] **Reserved**

FREQ_24 FFE input in LMS_2 mode

7	6	5	4	3	2	1	0
FFE_IN_UNLOCKED			FFE_IN_LOCKED			RESERVED	

Address: 0x7C

Type: R/W

Reset: 0x00

Description: FFE input in LMS_2 mode

[7:5] **FFE_IN_UNLOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is unlocked in LMS_2 mode.

[4:2] **FFE_IN_LOCKED**: specifies the input place of the FFE (from 1 to 7) when CRL is locked in LMS_2 mode.

[1:0] **Reserved**

6.2.2 FEC A/C registers

DEINT_SYNC_0 De-interleaver sync detector

7	6	5	4	3	2	1	0
DI_UNLOCK	DI_FREEZE	MISMATCH		ACQ_MODE		TRKMODE	

Address: 0x80

Type: R/W

Reset: 0x01

Description: De-interleaver sync detector

[7] **DI_UNLOCK**: when 1, forces the de-interleaver sync detector to unlock. Normal value is 0.

[6] **DI_FREEZE**: when 1, freezes the de-interleaver sync detector in locked mode. Normal value is 0.

[5:4] **MISMATCH**: indicates the number of bit mismatches in a sync byte allowed during track state (more erroneous bits and the byte is regarded as mismatching).

[3:2] **ACQ_MODE**: defines the number of states required to declare acquisition. The de-interleaver sync detector declares an acquisition and enters tracking when it has detected at least (ACQ_MODE + 3) successive correct sync bytes out of which one must be the inverted sync byte.

[1:0] **TRKMODE**: defines the number of states (number of successive mismatching sync bytes) required to unlock. TRK_MODE + 1 correct sync bytes are required.

DEINT_SYNC_1 De-interleaver sync detector

7	6	5	4	3	2	1	0
RESERVED		SYNLOST	SMCNTR			SYNCSTATE	

Address: 0x81

Type: R

Reset: 0x00

Description: De-interleaver sync detector

[7:6] **Reserved**

[5] **SYNLOST**: goes to 1 when the de-interleaver looses sync (even if it is forced to stay in locked state by bit DI_FREEZE in *DEINT_SYNC_0*). (Cleared in case of relocking).

[4:2] **SMCNTR**: increases each time the detected sync byte matches, decreases each time it mismatches. Saturates at 0 and ACQ_MODE + 2. For test only.

[1:0] **SYNCSTATE**: current state of the sync state machine. For test only.

BERT_0 Integrated BER tester

7	6	5	4	3	2	1	0
BERT_ON	RESERVED		ERR_SOURCE	ERR_MODE	NBYTE		

Address: 0x84

Type: R/W

Reset: 0x00

Description: Integrated BER tester

[7] **BERT_ON**: set to 1 to start counting bit/byte errors (before R/S correction). If ERR_MODE = 0 (see below), BERT_ON is automatically reset to 0 when the number of data bytes programmed through NBYTE (see below) has elapsed. If ERR_MODE = 1, it is not automatically reset.

[6:5] **Reserved**

[4] **ERR_SOURCE**:
0: count bit errors 1: count byte errors

[3] **ERR_MODE**:
0: the internal error counter stops automatically when the number of bytes defined by NBYTE (see below) has elapsed
1: it does not stop automatically, NBYTE is ignored and BERT_ON must be explicitly cleared by the user to stop the error counter

[2:0] **NBYTE**: the number of data bytes during which bit/byte errors are to be detected: $2^{(2 \times NBYTE + 12)}$. The count period can range from 4096 to 2^{26} bytes. (Used only if ERR_MODE = 0).

BERT_1 Integrated BER tester (LSBs)

7	6	5	4	3	2	1	0
ERRCOUNT[7:0]							

Address: 0x85

Type: R/W

Reset: 0x00

Description: Integrated BER tester (LSBs)

[7:0] **ERRCOUNT**[7:0]: internal byte/bit error counter, low byte. Note that this result is the raw bit/byte error count and includes any error falling within the R/S redundancy bytes.

BERT_2 Integrated BER tester

7	6	5	4	3	2	1	0
ERRCOUNT[15:8]							

Address: 0x86

Type: R/W

Reset: 0x00

Description: Integrated BER tester

[7:0] **ERRCOUNT**[15:8]: internal byte/bit error counter, high byte. Note that this result is the raw bit/byte error count and includes any error falling within the R/S redundancy bytes.

DEINT_0 De-interleaver

7	6	5	4	3	2	1	0
RESERVED	DAVIC	RESERVED	M				

Address: 0x88

Type: R/W

Reset: 0x91

Description: De-interleaver

[7] **Reserved**: Must be set to zero.

[6] **DAVIC**: selects DAVIC mapping. Reset value: 0

[5] **Reserved**

[4:0] **M**: interleaving depth parameter. Default: 0x11. Write to 1 and set DEPTH (*DEINT_1*) to 0 to bypass de-interleaver.

DEINT_1 De-interleaver

7	6	5	4	3	2	1	0
DEPTH							

Address: 0x89

Type: R/W

Reset: 0x0B

Description: De-interleaver

[7:0] **DEPTH**: de-interleaver depth - 1. Default: 0x0B. Write to 0 and set M (*DEINT_0*) to 0 to bypass de-interleaver.

OUTFORMAT_0 Output formatter

7	6	5	4	3	2	1	0
TSMF_EN	REFRESH47	BE_BYPASS	CKOUTPAR	CT_NBST	S_NP	TEI_ENA	DS_ENA

Address: 0x8C

Type: R/W

Reset: 0x53

Description: Output formatter

[7] **TSMF_EN**
0: TSMF bypassed 1: MPEG/TS send to TSMF

[6] **REFRESH47**: if 1, inverted MPEG sync bytes are re-inverted from 0xB8 back to 0x47. Reset value is 1. Do not set to 0.

[5] **BE_BYPASS**: when 1, all back-end stages, that is, those following symbol-to-byte (de-interleaving, R/S, descrambler) are bypassed. Reset value is 0.

[4] **CKOUTPAR**: selects polarity of M_CKOUT when common interface format is disabled. Reset value is 1.

[3] **CT_NBST**: when high, all MPEG/TS bits are output, else R/S parity is discarded. In TSMF mode, this bit must be setup high, the TSMF function discarding the R/S parity bytes. Reset value is 0.

[2] **S_NP**: selects serial (if 1) or parallel (if 0) interface. Reset value: 0.

[1] **TEI_ENA**: when high, enables setting of MPEG-2 TEI bit in case of uncorrectable packet error. Reset value is 1.

[0] **DS_ENA**: when high, descrambling is enabled. Reset/normal value is 1.

OUTFORMAT_1 Output formatter

7	6	5	4	3	2	1	0
SYNC_STRIP	CI_EN	CICLK_POL	TS_SWAP	RESERVED			

Address: 0x90

Type: R/W

Reset: 0x00

Description: Output formatter

[7] **SYNC_STRIP**: when 1, the sync word at the head of MPEG/TS packets is stripped off (the corresponding M_VAL pulse is suppressed).

[6] **CI_EN**: DVB CA common interface enable. When 1, the MPEG/TS output interface conforms to the DVB common interface specification. When 0, it is ST's parallel or serial format as indicated by *OUTFORMAT_0*.

[5] **CICLK_POL**: selects the polarity of the common interface clock supplied on M_CKOUT pin. Common interface control signals toggle on M_CKOUT rising edge if 0, on falling edge if 1.

[4] **TS_SWAP**: swap MSBs and LSBs from TS data.

[3:0] **Reserved**

OUTFORMAT_2 Output formatter

7	6	5	4	3	2	1	0
CI_DIVRANGE							

Address: 0x91

Type: R/W

Reset: 0x44

Description: Output formatter

[7:0] **CI_DIVRANGE**: defines the division ratio N between the base clock (defined in *OUTFORMAT_1*) and the common interface clock M_CKOUT:

N = N1 + N2 with N1 = CI_DIVRANGE[7:4] and N2 = CI_DIVRANGE[3:0].

N1 represents the number of base clock cycles during which M_CKOUT is high, N2 is the number of base clock cycles during which M_CKOUT is low. (Polarity given for CICLK_POL = 0 (*OUTFORMAT_1*), opposite result if this bit is 1).

Resulting M_CKOUT frequency = base clock frequency / N. Duty cycle ratio depends on N1/N2 ratio (50% if N1 = N2).

RS_DESC_0 MPEG-TS packet counter (LSBs)

7	6	5	4	3	2	1	0
BK_CT[7:0]							

Address: 0x94

Type: R

Reset: 0x00

Description: MPEG-TS packet counter (LSBs)

[7:0] **BK_CT**[7:0]: low byte of the block counter. Counts the number of MPEG-TS packets elapsed since the block counters were enabled. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_1 MPEG-TS packet counter (MSBs)

7	6	5	4	3	2	1	0
BK_CT[15:8]							

Address: 0x95

Type: R

Reset: 0x00

Description: MPEG-TS packet counter (MSBs)

[7:0] **BK_CT**[15:8]: high byte of the block counter. Counts the number of MPEG-TS packets elapsed since the block counters were enabled. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_2 MPEG-TS corrected packet counter (LSBs)

7	6	5	4	3	2	1	0
CORR_CT[7:0]							

Address: 0x96

Type: R

Reset: 0x00

Description: MPEG-TS corrected packet counter (LSBs)

[7:0] **CORR_CT**[7:0]: low byte of the corrected block counter. Counts the number of MPEG-TS packets that were R/S corrected since the block counters were enabled. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_3 MPEG-TS corrected packet counter (MSBs)

7	6	5	4	3	2	1	0
CORR_CT[15:8]							

Address: 0x97

Type: R

Reset: 0x00

Description: MPEG-TS corrected packet counter (MSBs)

[7:0] **CORR_CT**[15:8]: high byte of the corrected block counter. Counts the number of MPEG-TS packets that were R/S corrected since the block counters were enabled. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_4 MPEG-TS uncorrectable packet counter (LSBs)

7	6	5	4	3	2	1	0
UNCORR_CT[7:0]							

Address: 0x98

Type: R

Reset: 0x00

Description: MPEG-TS uncorrectable packet counter (LSBs)

[7:0] **UNCORR_CT**[7:0]: low byte of the uncorrected block counter. Counts packets that were detected as erroneous by the R/S but not correctable. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_5 MPEG-TS uncorrectable packet counter (MSBs)

7	6	5	4	3	2	1	0
UNCORR_CT[15:8]							

Address: 0x99

Type: R

Reset: 0x00

Description: MPEG-TS uncorrectable packet counter (MSBs)

[7:0] **UNCORR_CT**[15:8]: high byte of the uncorrected block counter. Counts packets that were detected as erroneous by the R/S but not correctable. Refer to CT_CLEAR (*RS_DESC_8*).

RS_DESC_6 Reed–Solomon - Descrambler sync detector - Descrambler

7	6	5	4	3	2	1	0
SYNCSTATE	RESERVED						

Address: 0x9A

Type: R/W

Reset: 0x00

Description: Reed–Solomon - Descrambler sync detector - Descrambler

[7] SYNCSTATE

[6:0] **Reserved**

RS_DESC_7 Reed–Solomon - Descrambler sync detector - Descrambler

7	6	5	4	3	2	1	0
RESERVED					DIS_UNLOCK	MODE	

Address: 0x9C

Type: R/W

Reset: 0x00

Description: Reed-Solomon - Descrambler sync detector - Descrambler

[7:3] **Reserved**

[2] **DIS_UNLOCK**: disables the capability of the de-interleaver sync detector to switch the descrambler sync detector to unlocked mode. Normal value is 0.

[1:0] **MODE**: defines the descrambler sync state machine tracking operation. This machine has two states—acquisition and tracking. The current state conditions the operation of MPEG-TS output pins and is reflected in SYNCSTATE bit (*RS_DESC_6*).

00: Descrambler sync detector cares only for inverted sync byte. If it is found at the expected time, it goes to tracking and if not it goes to acquisition.

10: Complete tracking mode. Descrambler sync detector cares only for inverted sync bytes to lock, but checks all sync bytes (inverted or not) once in tracking state; if one of them is wrong, it goes back to acquisition.

X1: Freeze mode. Once locked, the de-interleaver sync detector stays in tracking state (MPEG output pins stay active) even if there is a missing sync byte.

RS_DESC_8 Reed–Solomon - Descrambler sync detector - Descrambler

7	6	5	4	3	2	1	0
RESERVED					RS_NOCORR	CT_HOLD	CT_CLEAR

Address: 0x9D

Type: R/W

Reset: 0x00

Description: Reed-Solomon - Descrambler sync detector - Descrambler

[7:3] **Reserved**

[2] **RS_NOCORR**
0: the Reed-Solomon block operates normally (default)
1: the Reed-Solomon block does not correct any errors, but all of its other functions operate normally

[1] **CT_HOLD**: when 1, the block counters described in *RS_DESC_0* through *RS_DESC_5* are prevented from being updated, when 0 they can be updated.

[0] **CT_CLEAR**
0: the block counters described in *RS_DESC_0* through *RS_DESC_5* are cleared
1: the block counters described in *RS_DESC_0* through *RS_DESC_5* are enabled

6.3 Configuration and control registers

CTRL_0 Configuration and control 0

7	6	5	4	3	2	1	0
FEC_MODE	PAGE_MODE	RESERVED				IRQ_CLEAR	SOFT_RESET

Address: 0xA0

Type: R/W

Reset: 0x00

Description: Configuration and control 0

[7] **FEC_MODE**: FEC A/C or FEC B.
0: FEC B is used 1: FEC A/C is used

[6] **PAGE_MODE**: when register address greater than 0xB0, then if
0: FEC B registers area 1: TSMF registers area

[5:2] **Reserved**

[1] **IRQ_CLEAR**

[0] **SOFT_RESET**: when 1, forces most of the chip to reset (same as grounding pin NRESET). However, blocks that can be individually reset under software control are not affected (equalizer, refer to *CTRL_1* bit[0]), FEC (refer to *CTRL_1* bit[4]), framing and data syncing (*CTRL_1* bit[0]).
This bit is not self-clearing and can be used to put the chip in low consumption mode.

CTRL_1 Configuration and control 1

7	6	5	4	3	2	1	0
RESERVED		RESET_EQL	RESET_RS	RESET_PMFAGC	RESET_STL	RESET_CRL	RESET_DEINTERLEAVER

Address: 0xA1

Type: R/W

Reset: 0x00

Description: Configuration and control 1

[7:6] **Reserved**

[5] **RESET_EQL**: when 1, clears the equalizer coefficients. This bit is not self clearing. Reset value: 0

[4] **RESET_RS**: when 1, resets the Reed–Solomon block. This bit is not self-clearing.

[3] **RESET_PMFAGC**: if set to 1, resets the PMFAGC.

[2] **RESET_STL**: if set to 1, resets the STL.

[1] **RESET_CRL**: if set to 1, resets the CRL.

[0] **RESET_DEINTERLEAVER**: if set to 1, resets the de-interleaver, de-interleaver sync detector and descrambler sync detector for FEC A. This bit is not self-clearing.

CTRL_2 Configuration and control 2

7	6	5	4	3	2	1	0
IT_OD	LOCK_OD	AGC_OD	M_OEN	IT_STATUS	M_ERROR_STATUS	OSCIBYPASS	RESERVED

Address: 0xA2

Type: R/W

Reset: 0xE0

Description: Configuration and control 2

[7] **IT_OD**:
1: IT pin behaves as an open-drain (and pull-up can be connected to voltage up to 5.5 V)
0: IT pin behaves as normal CMOS outputs
Reset value is 1.

[6] **LOCK_OD**:
1: LOCK pin behaves as an open-drain (and pull-up can be connected to voltage up to 5.5 V)
0: LOCK pin behaves as normal CMOS outputs
Reset value is 1.

[5] **AGC_OD**:
1: AGC1, AGC2 pins behave as open-drain (and pull-up can be connected to voltage up to 5.5 V)
0: AGC1, AGC2 pins behave as normal CMOS outputs
Reset value is 1.

[4] **M_OEN**:
1: all MPEG outputs are disabled (pins are in high impedance mode)

[3] **IT_STATUS**: mapping of IT pin.
0: mapped to interrupt 1: mapped to LSB of TSMF RECEIVE_STATUS

[2] **M_ERROR_STATUS**: mapping of M_ERR pin.
0: mapped to TS error bit 1: mapped to MSB of TSMF RECEIVE_STATUS

[1] **OSCIBYPASS**: when 1, the pad oscillator is disabled and an external clock can be used on XTAL1.

[1:0] **Reserved**

CTRL_3 Configuration and control 3

7	6	5	4	3	2	1	0
LOCKPOL	DI_SY_MASK	DI_SY_EV	DI_SY_DIR	RESERVED	SYNC_MSK	SYNC_EV	SYNC_DIR

Address: 0xA3

Type: R/W

Reset: 0x00

Description: Configuration and control 3

[7] **LOCKPOL**: selects the polarity of the lock indicator signal LOCK that may be output on the LOCK pin.
0: active high 1: active low

[6] **DI_SY_MASK**: when 0, masks interrupts from de-interleaver sync detector.

[5] **DI_SY_EV**: goes to 1 when de-interleaver detects a sync acquisition/loss event.

[4] **DI_SY_DIR**: specifies what the event was (0: loss of sync, 1: got sync). R bit.

[3] **Reserved**

[2] **SYNC_MSK**: when 0, masks interrupts from descrambler sync detector.

[1] **SYNC_EV**: goes to 1 when descrambler detects a sync acquisition/loss event.

[0] **SYNC_DIR**: specifies what the event was (0: loss of sync, 1: got sync). R bit.

CTRL_4 Configuration and control 4

7	6	5	4	3	2	1	0
I2CT_EN	LOCKSCE	DI_SY_EV	PRGCLKDIV				AUXCLKSEL

Address: 0xA6

Type: R/W

Reset: 0x00

Description: Configuration and control 4

[7] **I2CT_EN**: when set to 1, enables the I²C repeater for one I²C access, that is, from the end of the message that sets this bit until detection of the next stop condition on the I²C bus.

[6:5] **LOCKSCE**: selects the source of hardware lock indicator signal LOCK.

00: lock indicator LOCK = bit SYNCSTATE for FEC A/MPEG_LOCK_FECB for FEC B. This signal is the ultimate lock flag and indicates if the full chip (including FEC and data framing) has locked. (This is also available by software as *RS_DESC_6*, bit[7] for FEC A).

01: lock indicator LOCK = bit EQU_LMS2. This signal indicates if the demodulator has firmly converged. (This information is also made available by software through *CTRL_8*, bit[2]).

10: lock indicator LOCK = bit EQU_LMS1. This signal indicates if the demodulator is converging (equalizer leaves the blind mode at that point). (This information is also made available by software through *CTRL_8*, bit[1]).

11: lock indicator LOCK = bit WAGC_ACQ indicating if analog AGC has converged. (This is also made available by software through *WBAGC_3*).

[4:1] **PRGCLKDIV**: defines the division ratio used to obtain the programmable clock PRGCLK that may be output on AUXCLK pin and which is also used by some I²C repeater internal logic.

[0] **AUXCLKSEL**:

0 and TSMF_EN = 1 (*OUTFORMAT_0*): AUXCLK pin displays the emergency signal from TSMF. When TSMF is disabled, AUXCLK pin is tied to 0.

1: AUXCLK pin carries programmable clock PRGCLK derived from 50 MHz by integer division.

CTRL_5 Configuration and control 5

7	6	5	4	3	2	1	0
RESERVED				SPEC_INV	GMAP_SEL	DFS	RESERVED

Address: 0xA8

Type: R/W

Reset: 0x00

Description: Configuration and control 5

[7:4] **Reserved**

[3] **SPEC_INV**: allows the demodulator to cope with any spectrum inversion possibly introduced in the transmission chain.

[2] **GMAP_SEL**:

1: bit mapper module works in test mode 0: it works in normal mode

For test only. Set to 0 for normal operation.

[1] **DFS**: input data format selection.
1: IF data from ADC is interpreted as 2's complement
0: IF data from ADC is interpreted as offset binary
For test only. Normal value for STi7197 ADC: 0.

[0] **Reserved**

CTRL_6 Configuration and control 6

7	6	5	4	3	2	1	0
RESERVED		SIGMA_INV_1	SIGMA_INV_2	RESERVED			

Address: 0xA9

Type: R/W

Reset: 0x00

Description: Configuration and control 6

[7:6] **Reserved**

[5] **SIGMA_INV_1**: if 1, inverts the polarity of signal AGC1.

[4] **SIGMA_INV_2**: if 0, inverts the polarity of signal AGC2.

[3:0] **Reserved**: write to 0x0.

CTRL_7 Configuration and control 7

7	6	5	4	3	2	1	0
AUTO_QAMMODE_SEL	AUTOCONSTEL_TIMER				AUTOSTOP_CONSTEL	AUTOCONSTEL_ON	RESERVED

Address: 0xAA

Type: R/W

Reset: 0x00

Description: Configuration and control 7

[7] **AUTO_QAMMODE_SEL**:
0: QAM mode (that is, constellation) is manually selected through *EQU_0* (0x00).
1: a state machine controlled by the bits below tries iteratively all QAM modes (16-QAM, 64-QAM, 256-QAM, 128-QAM and finally 32-QAM).

[6:3] **AUTOCONSTEL_TIMER**: defines the time spent in each QAM mode as:
AUTOCONSTEL_TIMER x 2^{13} x Ts (where Ts is the symbol duration).

[2] **AUTOSTOP_CONSTEL**: If 1, the state machine stops automatically and stays in its current QAM mode upon detection of full equalizer lock.

[1] **AUTOCONSTEL_ON**: setting this bit to 1 starts the QAM mode state machine, setting it to 0 stops the state machine, and the chip stays in its current QAM mode.

[0] **Reserved**

CTRL_8 Configuration and control 8

7	6	5	4	3	2	1	0
TSMF_HEADER	TSMF_ERROR	TSMF_LOCK	MPEG_LOCK_FECA	MPEG_LOCK_FECB	LMS_STEP2	LMS_STEP1	WAGC_LOCK

Address: 0xAB

Type: R

Reset: 0x00

Description: Configuration and control 8

[7] **TSMF_HEADER**: for description, see *AUTOMATIC_SYNC_COUNT* from TSMF section.
0: no TSMF header detected 1: a TSMF header detected

[6] **TSMF_ERROR**: for detail, see bit[7] of *GENERAL_STATUS* register.

[5] **TSMF_LOCK**: for detail, bit[0] of *GENERAL_STATUS* register.

[4] **MPEG_LOCK_FECA**: for detail, bit[7] of *INTER_2* register.

[3] **MPEG_LOCK_FECB**: for detail, bit[0] of *INTER_2* register.

[2] **LMS_STEP2**: for detail, bit[3] of *INTER_2* register.

[1] **LMS_STEP1**: for detail, bit[2] of *INTER_2* register.

[0] **WAGC_LOCK**: for detail, bit[1] of *INTER_2* register.

CTRL_9 Configuration and control 9

7	6	5	4	3	2	1	0
TEST_SEL							

Address: 0xAC

Type: R/W

Reset: 0x00

Description: Configuration and control 9

[7:0] **TEST_SEL**: test mode register. For test only. Set to 0x00 for normal operation.

CTRL_10 Configuration and control 10

7	6	5	4	3	2	1	0
SOURCESEL	RESERVED	SYNTH_DIS	COARE_FS_SEL				

Address: 0xAD

Type: R/W

Reset: 0x9C

Description: Configuration and control 10

[7] **SOURCESEL**: SAMPLED_IF source selection.
0: data comes from internal ADC 1: data comes from external source
Normal value: 0. Reset value is 1 (for production test reasons).

[6] **Reserved**: must be set to 0.

[5] **SYNTH_DIS**:
1: The frequency synthesizer is disabled

[4:0] **COARE_FS_SEL**: coarse selector bus for synthesizer. -floor{1 + 32(1 - f_{SYS}/f_{OUT})};
f_{OUT}[50:100] MHz.
(floor is the nearest integer towards minus infinity. floor(-1.4) = -2; floor(1.4) = 1).

CTRL_11 Synthesizer fine selector (LSBs)

7	6	5	4	3	2	1	0
FINE_FS_SEL[7:0]							

Address: 0xAE

Type: R/W

Reset: 0x04

Description: Synthesizer fine selector (LSBs)

[7:0] **FINE_FS_SEL**[7:0]: LSBs fine selector bus for synthesizer.
Reset value is for a 57 MHz serial clock output frequency. Put 0xDB for a 56 MHz clock.
FINE_FS_SEL = round{2^{15}(32 - 32 f_{IN}/f_{OUT} + coarse + 1)}; f_{OUT}[50:100] MHz;
$f_{IN} = f_{SYS} = 2 \times f_{XTAL}$.
(round is the nearest integer. round(4.8) = 5; round(4.3) = 4).

CTRL_12 Synthesizer fine selector (MSBs)

7	6	5	4	3	2	1	0
FINE_FS_SEL[15:8]							

Address: 0xAF

Type: R/W

Reset: 0x77

Description: Synthesizer fine selector (MSBs)

[7:0] **FINE_FS_SEL**[15:8]: MSBs fine selector bus for synthesizer.
Reset value is for a 57 MHz serial clock output frequency. Put 0x36 for a 56 MHz clock.

6.4 FEC-B registers

MPEG_CONTROL — FEC-B control

7	6	5	4	3	2	1	0
64/256	PARAM_DIS	MPEG_DIS	RS_EN	VITERBI_RESET	MPEG_HDR_DIS	RS_FLAG	MPEG_FLAG

Address: 0xC0

Type: R/W

Reset: 0x00

Description: FEC-B control

[7] **64/256**: determines the FEC operating mode.
0: 256-QAM 1: 64-QAM

[6] **PARAM_DIS**: controls the test parameters. Always set to 0.

[5] **MPEG_DIS**: controls the MPEG sync byte output.
0: enables clock cycles of the sync byte
1: disables clock cycles of the sync byte (Note that in this case the sync signal is unavailable on the external pin).

[4] **RS_EN**: controls the Reed–Solomon correction.
0: disables RS correction 1: enables RS correction

[3] **VITERBI_RESET**: resetting this bit to 0 resets the FEC. When it changes from 0 to 1, the Viterbi decoder enters hunt mode and the FEC begins normal operation.

[2] **MPEG_HDR_DIS**: controls the replacement of the MPEG syndrome/checksum header byte with 0x47.
0: replaces with 0x47 1: does not replace

[1] **RS_FLAG**: controls the setting of the error bit in the beginning of the MPEG frame if the MPEG frame has an uncorrectable RS codeword.
0: disables set error bit 1: enables set error bit

[0] **MPEG_FLAG**: controls the setting of the error bit in the beginning of the MPEG frame if the MPEG checksum/syndrome byte for that frame was incorrect.
0: disables set error bit 1: enables set error bit

MPEG_SYNC_ACQ FEC-B MPEG sync patterns for SYNC state

7	6	5	4	3	2	1	0
RESERVED				MPEG_GET			

Address: 0xC1

Type: R/W

Reset: 0x00

Description: FEC-B MPEG sync patterns for SYNC state

[7:4] **Reserved**

[3:0] **MPEG_GET**: used to program the number of sequential matching MPEG sync patterns that must be found to enter the SYNC state.

MPEG_SYNC_LOSS FEC-B missing MPEG sync patterns to exit SYNC state

7	6	5	4	3	2	1	0
RESERVED		MPEG_DROP					

Address: 0xC2

Type: R/W

Reset: 0x00

Description: FEC-B missing MPEG sync patterns to exit SYNC state

[7:6] **Reserved**

[5:0] **MPEG_DROP**: used to program the number of sequential missing MPEG sync patterns that must be found to leave the SYNC state.

DATA_OUT_CONTROL FEC-B data output control

7	6	5	4	3	2	1	0
RESERVED					STI5518	OUTPUT_CLK_POL	OUTPUT_DATA_MODE

Address: 0xC3

Type: R/W

Reset: 0x00

Description: FEC-B data output control

[7:3] **Reserved**

[2] **STI5518**: when set, TS output is compatible with the STi5518.

[1] **OUTPUT_CLK_POL**: if set to 0, the output serial clock for MPEG stream is in phase with the system clock.

[0] **OUTPUT_DATA_MODE**:
0: the MPEG data stream parallel mode is byte formatted according to the output byte clock (output serial clock divided by 8)
1: serial mode

VITERBI_SYNC_ACQ FEC-B sync acquired threshold

7	6	5	4	3	2	1	0
VITERBI_SYNC_GET							

Address: 0xC4

Type: R/W

Reset: 0x00

Description: FEC-B sync acquired threshold

[7:0] **VITERBI_SYNC_GET**: determines the threshold at which the rollover rate needs to be lower than where the sync counter begins to increment. The recommended value is decimal 13.

VITERBI_SYNC_LOSS FEC-B sync lost threshold

7	6	5	4	3	2	1	0
VITERBI_SYNC_DROP							

Address: 0xC5

Type: R/W

Reset: 0x00

Description: FEC-B sync lost threshold

[7:0] **VITERBI_SYNC_DROP**: determines the lowest threshold for the rollover rate, after which the sync counter will begin decrementing. The recommended value is decimal 220.

VITERBI_SYNC_GO FEC-B sync start

7	6	5	4	3	2	1	0
RESERVED		VITERBI_SYNC_GO					

Address: 0xC6

Type: R/W

Reset: 0x00

Description: FEC-B sync start

[7:6] **Reserved**

[5:0] **VITERBI_SYNC_GO**: corresponds to the number that the sync counter has to reach before Viterbi sync is declared. Recommended value is decimal 8.

VITERBI_SYNC_STOP FEC-B sync stop

7	6	5	4	3	2	1	0
RESERVED				VITERBI_SYNC_STOP			

Address: 0xC7

Type: R/W

Reset: 0x00

Description: FEC-B sync stop

[7:6] **Reserved**

[5:0] **VITERBI_SYNC_STOP**: corresponds to the number of sequential readings of the rollover rate needed to drop Viterbi sync and return to HUNT state. Recommended value is decimal 8.

FS_SYNC FEC-B sync control

7	6	5	4	3	2	1	0
FRAME_SYNC_DROP				FRAME_SYNC_GET			

Address: 0xC8

Type: R/W

Reset: 0x00

Description: FEC-B sync control

[7:4] **FRAME_SYNC_DROP**: setting this register to a value between 1 and 15 sets that as the number of missing or incorrect frame sync symbols which must be received for the frame sync state machine to leave SYNC state and return to HUNT state. Recommended values are in the 6 - 10 range.

[3:0] **FRAME_SYNC_GET**: setting this register to a value between 1 and 15 sets that as the number of correctly positioned frame symbols that must be received sequentially for the frame sync state machine to enter the SYNC state. Recommended values are in the 4 - 8 range.

IN_DEPTH FEC-B interleaver depth

7	6	5	4	3	2	1	0
FEC_RESET	RESERVED			INTERLEAVER_DEPTH			

Address: 0xC9

Type: R/W

Reset: 0x00

Description: FEC-B interleaver depth

[7] **FEC_RESET**: performs a soft reset on the FEC core.
0: resets the FEC 1: normal FEC operation

[6:4] **Reserved**

[3:0] **INTERLEAVER_DEPTH**: controls the interleaver depth (control word)

Control word	Number of taps (I)	Increment (J)
0001	128	1
0010	128	2
0100	128	3
0110	128	4
0011	64	2
0101	32	4
0111	16	8
1001	8	16

RS_CONTROL FEC-B Reed-Solomon control

7	6	5	4	3	2	1	0
RS_CORRECTED_CNT_CLEAR	RS_UNERRORED_CNT_CLEAR	RS_4_ERROR	RS_CLR_ERR	RS_CLR_UNC	RS_RATE_ADJ		

Address: 0xCA

Type: R/W

Reset: 0x00

Description: FEC-B Reed-Solomon control

[7] **RS_CORRECTED_CNT_CLEAR**: (active 1) if set to 1, the block counters described in the *RS_CORR_COUNT* register are cleared.

[6] **RS_UNERRORED_CNT_CLEAR**: (active 1) if set to 1, the block counters described in the *RS_UNERR_COUNT* register are cleared.

[5] **RS_4_ERROR**: directs how the RS monitoring circuit is to treat uncorrectable codeword errors.
0: counts uncorrected codeword errors as 0 error
1: counts uncorrected codeword errors as 4 errors

[4] **RS_CLR_ERR**: a transition from 0 to 1 on this register clears the correctable error counter.

[3] **RS_CLR_UNC**: a transition from 0 to 1 on this register clears the uncorrectable error counter.

[2:0] **RS_RATE_ADJ**: indicates the number of FEC frames over which the RS rate register accumulates data.

000: 4 frames
001: 16 frames
010: 64 frames
011: 256 frames
100: 1024 frames
101: 4096 frames
110: 16384 frames
111: 65536 frames

DEINT_CONTROL FEC-B de-interleaver control

7	6	5	4	3	2	1	0
RESERVED	DEINTERLEAVER_DEPTH_AUTO_MODE	FRAME_SYNC_COUNT					

Address: 0xCB

Type: R/W

Reset: 0x80

Description: FEC-B de-interleaver control

[7] **Reserved**

[6] **DEINTERLEAVER_DEPTH_AUTO_MODE**

0: manual mode. Writing bit [3:0] of the *IN_DEPTH* register is necessary.

1: no need to write bit [3:0] of the *IN_DEPTH* register.

[5:0] **FRAME_SYNC_COUNT**: minimum number of consecutive good frame sync as required to capture the interleaver depth (control word). Only used with DEINTERLEAVER_DEPTH_AUTO_MODE.

Minimum value: 0 Maximum value: 64

Suggested value: 4

SYNC_STAT FEC-B sync status

7	6	5	4	3	2	1	0
RESERVED			MPEG_SYNC	VITERBI_I_SYNC	VITERBI_Q_SYNC	COMB_STATE	

Address: 0xCC

Type: R

Reset:

Description: FEC-B sync status

[7:5] **Reserved**

[4] **MPEG_SYNC**: this signal is asserted when the state machine in the MPEG module is in the SYNC state.

[3] **VITERBI_I_SYNC**: indicates the state of the Viterbi sync. For the Viterbi to be in SYNC, this bit and VITERBI_Q_SYNC must be set.

[2] **VITERBI_Q_SYNC**: indicates the state of the Viterbi sync. For the Viterbi to be in SYNC, this bit and VITERBI_I_SYNC must be set.

[1:0] **COMB_STATE**: frame sync status indicator.

00: the circuit is searching for a pattern to match the J83 frame sync pattern

01: the circuit has found a pattern that matches and is looking for FS_GET_SYNC sequential frame sync patterns in the correct position

10: the state machine is in SYNC state and has not received FS_DROP_SYNC missing frame sync patterns

VITERBI_I_RATE FEC-B

7	6	5	4	3	2	1	0
VITERBI_RATE_I							

Address: 0xCD

Type: R

Reset:

Description: FEC-B

[7:0] **VITERBI_RATE_I**: contains filtered values of the Viterbi decoder's rollover rate.

VITERBI_Q_RATE FEC-B

7	6	5	4	3	2	1	0
VITERBI_RATE_Q							

Address: 0xCE

Type: R

Reset:

Description: FEC-B

[7:0] **VITERBI_RATE_Q**: contains filtered values of the Viterbi decoder's rollover rate.

TX_INTERLEAVER_DEPTH FEC-B

7	6	5	4	3	2	1	0
RESERVED				TX_INTERLEAVER_DEPTH			

Address: 0xD0

Type: R

Reset:

Description: FEC-B

[7:4] **Reserved**

[3:0] **TX_INTERLEAVER_DEPTH**: this register holds the interleaver depth (control word) captured from the received data stream.

RS_ERR_CNT FEC_B Reed-Solomon correctable errors

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RS_ERROR_COUNT											

Address: 0xD1, 0xD2

Type: R

Reset:

Description: FEC_B Reed–Solomon correctable errors

[15:12] **Reserved**

[11:0] **RS_ERROR_COUNT**: this register contains a running count of the number of correctable errors (in 7-bit symbol units) in each RS codeword. This counter can be cleared by writing a 1 into the configuration bit (*RS_CONTROL*, bit [4]). This register saturates at 0xFFF if it is not cleared before reaching this value.

RS_UNC_COUNT FEC_B Reed–Solomon uncorrectable errors

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RS_UNC_COUNT											

Address: 0xD4, 0xD5

Type: R

Reset:

Description: FEC_B Reed–Solomon uncorrectable errors

[15:12] **Reserved**

[11:0] **RS_UNC_COUNT**: this register is a counter that contains the number of RS codewords which were determined to have an uncorrectable number of errors. This counter can be cleared by writing a 1 to the configuration bit, that is bit [3] of *RS_CONTROL* register. MSBs in register 0xD5 [3:0], LSBs in register 0xD4.

RS_RATE FEC_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						RS_RATE									

Address: 0xD6, 0xD7

Type: R

Reset:

Description: FEC_B

[15:10] **Reserved**

[9:0] **RS_RATE**: this register contains the count of the number of correctable errors (in 7-bit symbol units) in each RS codeword over a number of FEC frames defined by RS_RATE_ADJ (*RS_CONTROL*, bit [2:0]).
MSBs in register 0xD7 [1:0], LSBs in register 0xD6.

RS_CORR_COUNT FEC_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RS_CORRECTED_COUNT															

Address: 0xD8, 0xD9

Type: R

Reset:

Description: FEC_B

[15:0] **RS_CORRECTED_COUNT**: this register is a counter that contains the number of RS codewords which were determined to have a correctable number of errors. This register can be cleared by writing a 1 to the configuration bit, that is bit[7] of the *RS_CONTROL* register. MSBs in register 0xD9, LSBs in register 0xD8.

RS_UNERR_COUNT FEC_B

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RS_UNERRORED_COUNT															

Address: 0xDA, 0xDB

Type: R

Reset:

Description: FEC_B

[15:0] **RS_UNERRORED_COUNT**: this register contains a running count of the number of RS codewords presenting no error. This register can be cleared by writing a 1 to the configuration bit, that is bit[6] of the *RS_CONTROL* register. MSBs in register 0xDB, LSBs in register 0xDA.

6.5 TSMF registers

TSMF_SEL TSMF selection mode

7	6	5	4	3	2	1	0
RESERVED			TS_NUMBER	SEL_MODE			

Address: 0xB1

Type: R/W

Reset: 0x00

Description: TSMF selection mode

[7:5] **Reserved**

[4:1] **TS_NUMBER**

[0] **SEL_MODE**: selection mode.
0: selection by TS ID 1: selection by TS number

TSMF_CONTROL TSMF control

7	6	5	4	3	2	1	0
CHECK_ERROR_BIT	CHECK_F_SYNC	RESERVED		H_MODE	D_V_MODE	MODE	

Address: 0xB2

Type: R/W

Reset: 0x00

Description: TSMF control

[7] **CHECK_ERROR_BIT**: when 1, frame header TS error indicator bit checked.

[6] **CHECK_F_SYNC**: when 1, FRAME_SYNC bytes of the frame header are checked.

[5:4] **Reserved**

[3] **H_MODE**:
0: PID of multiple frame header is overwritten by null PID 0x1FFF
1: PID of multiple frame header is output

[2] **D_V_MODE**
0: DATAVALID signal is asserted for all output frames
1: DATAVALID signal is asserted only for desired output frames

[1:0] **MODE**
00: force single TS mode 01: force multiple TS mode
10: automatic detect mode 11: reserved

AUTOMATIC_SYNC_COUNT — Automatic sync count

7	6	5	4	3	2	1	0
SYNC_IN_COUNT				SYNC_OUT_COUNT			

Address: 0xB3

Type: R/W

Reset: 0x43

Description: Automatic sync count

[7:4] **SYNC_IN_COUNT**: number of consecutive good frame headers required to go to TSMF_SYNC state when in automatic detect mode. It is also the number of consecutive good frame headers required to raise TSMF_HEADER (bit[7], *CTRL_8*).

[3:0] **SYNC_OUT_COUNT**: number of consecutive bad frame headers required to leave TSMF_SYNC state when in automatic mode detect. It is also the number of consecutive bad frame headers required to lower TSMF_HEADER (bit[7], *CTRL_8*).

TS_ID_L — TS identifier (LSBs)

7	6	5	4	3	2	1	0
TS_ID[7:0]							

Address: 0xB4

Type: R/W

Reset: 0x00

Description: TS identifier (LSBs)

[7:0] **TS_ID**[7:0]: LSBs from the selected TS identifier to be provided by the controlling device.

TS_ID_H — TS identifier (MSBs)

7	6	5	4	3	2	1	0
TS_ID[15:8]							

Address: 0xB5

Type: R/W

Reset: 0x00

Description: TS identifier (MSBs)

[7:0] **TS_ID**[15:8]: MSBs from the selected TS identifier to be provided by the controlling device.

ON_ID_L — Original network identifier (LSBs)

7	6	5	4	3	2	1	0
ON_ID[7:0]							

Address: 0xB6

Type: R/W

Reset: 0x00

Description: Original network identifier (LSBs)

[7:0] **ON_ID**[7:0]: LSBs from the original network identifier to be provided by the controlling device.

ON_ID_H Original network identifier (MSBs)

7	6	5	4	3	2	1	0
ON_ID[15:8]							

Address: 0xB7

Type: R/W

Reset: 0x00

Description: Original network identifier (MSBs)

[7:0] **ON_ID**[15:8]: MSBs from the original network identifier to be provided by the controlling device.

GENERAL_STATUS TSMF general status

7	6	5	4	3	2	1	0
ERROR	EMERGENCY	CRE_TS[1:0]		VER[2:0]			M_LOCK

Address: 0xB9

Type: R

Description: TSMF general status

[7] **ERROR:**
0: the provided TS_ID and ON_ID are valid and their corresponding TS_STATUS is active
1: the above condition is not met

[6] **EMERGENCY**: emergency indicator.

[5:4] **CRE_TS**[1:0]: the receive status of the currently selected TS.

[3:1] **VER**[2:0]: TSMF version number.

[0] **M_LOCK**
0: multiple TS unlocked 1: multiple TS locked

TS_ST_L One-bit TS ID status (LSBs)

7	6	5	4	3	2	1	0
TS_STATUS[7:0]							

Address: 0xBA

Type: R

Description: One-bit TS ID status (LSBs)

[7:0] **TS_STATUS**[7:0]: one bit status per RELATIVE_TS_ID.
TS_STATUS[0] for RELATIVE_TS_ID_#1 to TS_STATUS[7] for RELATIVE_TS_ID_#8

TS_ST_H One-bit TS ID status (MSBs)

7	6	5	4	3	2	1	0
TS_STATUS[14:8]							

Address: 0xBB

Type: R

Description: One-bit TS ID status (MSBs)

[7] Reserved

[6:0] **TS_STATUS**[14:8]: one bit status per RELATIVE_TS_ID
TS_STATUS[8] for RELATIVE_TS_ID_#9 to TS_STATUS[14] for RELATIVE_TS_ID_#15

RE_ST_L Two-bit TS ID status (LSBs)

7	6	5	4	3	2	1	0
RECEIVE_STATUS[7:0]							

Address: 0xBC

Type: R

Description: Two-bit TS ID status (LSBs)

[7:0] **RECEIVE_STATUS**[7:0]: two bits status per RELATIVE_TS_ID.
RECEIVE_STATUS[1:0] for RELATIVE_TS_ID#1RECEIVE_STATUS[3:2] for RELATIVE_TS_ID#2
RECEIVE_STATUS[5:4] for RELATIVE_TS_ID#3RECEIVE_STATUS [7:6] for RELATIVE_TS_ID#4

RE_ST_2 Two-bit TS ID status (lower-mid SBs)

7	6	5	4	3	2	1	0
RECEIVE_STATUS[15:8]							

Address: 0xBD

Type: R

Description: Two-bit TS ID status (lower-mid SBs)

[7:0] **RECEIVE_STATUS**[15:8]: two bits status per RELATIVE_TS_ID.
RECEIVE_STATUS[9:8] for RELATIVE_TS_ID#5RECEIVE_STATUS[11:10] for RELATIVE_TS_ID#6
RECEIVE_STATUS[13:12] for RELATIVE_TS_ID#7RECEIVE_STATUS [15:14] for RELATIVE_TS_ID#8

RE_ST_1 Two-bit TS ID status (upper-mid SBs)

7	6	5	4	3	2	1	0
RECEIVE_STATUS[23:16]							

Address: 0xBE

Type: R

Description: Two-bit TS ID status (upper-mid SBs)

[7:0] **RECEIVE_STATUS**[23:16]: two bits status per RELATIVE_TS_ID.
RECEIVE_STATUS[17:16] for RELATIVE_TS_ID#9
RECEIVE_STATUS[19:18] for RELATIVE_TS_ID#10
RECEIVE_STATUS[21:20] for RELATIVE_TS_ID#11
RECEIVE_STATUS [23:22] for RELATIVE_TS_ID#12

RE_ST_H Two-bit TS ID status (MSBs)

7	6	5	4	3	2	1	0
RESERVED		RECEIVE_STATUS[29:24]					

Address: 0xBF

Type: R

Description: Two-bit TS ID status (MSBs)

[7:6] **Reserved**

[5:0] **RECEIVE_STATUS**[29:24]: two bits status per RELATIVE_TS_ID.
RECEIVE_STATUS[25:24] for RELATIVE_TS_ID#13
RECEIVE_STATUS[27:26] for RELATIVE_TS_ID#14
RECEIVE_STATUS[29:28] for RELATIVE_TS_ID#15

T_ID_L1 TS identifier 1 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_1[7:0]							

Address: 0xC0

Type: R

Description: TS identifier 1 (LSBs)

[7:0] **TS_ID_1**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#1.

T_ID_H1 TS identifier 1 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_1[15:8]							

Address: 0xC1

Type: R

Description: TS identifier 1 (MSBs)

[7:0] **TS_ID_1**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#1.

O_ID_L1 Original network identifier 1 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_1[7:0]							

Address: 0xC2

Type: R

Description: Original network identifier 1 (LSBs)

[7:0] **ON_ID_1**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#1.

O_ID_H1 Original network identifier 1 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_1[15:8]							

Address: 0xC3

Type: R

Description: Original network identifier 1 (MSBs)

[7:0] **ON_ID_1**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#1.

T_ID_L2 TS identifier 2 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_2[7:0]							

Address: 0xC4

Type: R

Description: TS identifier 2 (LSBs)

[7:0] **TS_ID_2**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#2.

T_ID_H2 TS identifier 2 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_2[15:8]							

Address: 0xC5

Type: R

Description: TS identifier 2 (MSBs)

[7:0] **TS_ID_2**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#2.

O_ID_L2 Original network identifier 2 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_2[7:0]							

Address: 0xC6

Type: R

Description: Original network identifier 2 (LSBs)

[7:0] **ON_ID_2**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#2.

O_ID_H2 Original network identifier 2 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_2[15:8]							

Address: 0xC7

Type: R

Description: Original network identifier 2 (MSBs)

[7:0] **ON_ID_2**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#2.

T_ID_L3 TS identifier 3 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_3[7:0]							

Address: 0xC8

Type: R

Description: TS identifier 3 (LSBs)

[7:0] **TS_ID_3**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#3.

T_ID_H3 TS identifier 3 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_3[15:8]							

Address: 0xC9

Type: R

Description: TS identifier 3 (MSBs)

[7:0] **TS_ID_3**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#3.

O_ID_L3 Original network identifier 3 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_3[7:0]							

Address: 0xCA

Type: R

Description: Original network identifier 3 (LSBs)

[7:0] **ON_ID_3**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#3.

O_ID_H3 Original network identifier 3 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_3[15:8]							

Address: 0xCB

Type: R

Description: Original network identifier 3 (MSBs)

[7:0] **ON_ID_3**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#3.

T_ID_L4 TS identifier 4 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_4[7:0]							

Address: 0xCC

Type: R

Description: TS identifier 4 (LSBs)

[7:0] **TS_ID_4**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#4.

T_ID_H4 TS identifier 4 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_4[15:8]							

Address: 0xCD

Type: R

Description: TS identifier 4 (MSBs)

[7:0] **TS_ID_4**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#4.

O_ID_L4 Original network identifier 4 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_4[7:0]							

Address: 0xCE

Type: R

Description: Original network identifier 4 (LSBs)

[7:0] **ON_ID_4**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#4.

O_ID_H4 Original network identifier 4 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_4[15:8]							

Address: 0xCF

Type: R

Description: Original network identifier 4 (MSBs)

[7:0] **ON_ID_4**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#4.

T_ID_L5 TS identifier 5 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_5[7:0]							

Address: 0xD0

Type: R

Description: TS identifier 5 (LSBs)

[7:0] **TS_ID_5**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#5.

T_ID_H5 TS identifier 5 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_5[15:8]							

Address: 0xD1

Type: R

Description: TS identifier 5 (MSBs)

[7:0] **TS_ID_5**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#5.

O_ID_L5 Original network identifier 5 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_5[7:0]							

Address: 0xD2

Type: R

Description: Original network identifier 5 (LSBs)

[7:0] **ON_ID_5**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#5.

O_ID_H5 Original network identifier 5 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_5[15:8]							

Address: 0xD3

Type: R

Description: Original network identifier 5 (MSBs)

[7:0] **ON_ID_5**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#5.

T_ID_L6 TS identifier 6 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_6[7:0]							

Address: 0xD4

Type: R

Description: TS identifier 6 (LSBs)

[7:0] **TS_ID_6**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#6.

T_ID_H6 TS identifier 6 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_6[15:8]							

Address: 0xD5

Type: R

Description: TS identifier 6 (MSBs)

[7:0] **TS_ID_6**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#6.

O_ID_L6 Original network identifier 6 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_6[7:0]							

Address: 0xD6

Type: R

Description: Original network identifier 6 (LSBs)

[7:0] **ON_ID_6**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#6.

O_ID_H6 Original network identifier 6 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_6[15:8]							

Address: 0xD7

Type: R

Description: Original network identifier 6 (MSBs)

[7:0] **ON_ID_6**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#6.

T_ID_L7 TS identifier 7 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_7[7:0]							

Address: 0xD8

Type: R

Description: TS identifier 7 (LSBs)

[7:0] **TS_ID_7**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#7.

T_ID_H7 TS identifier 7 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_7[15:8]							

Address: 0xD9

Type: R

Description: TS identifier 7 (MSBs)

[7:0] **TS_ID_7**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#7.

O_ID_L7 Original network identifier 7 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_7[7:0]							

Address: 0xDA

Type: R

Description: Original network identifier 7 (LSBs)

[7:0] **ON_ID_7**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#7.

O_ID_H7 Original network identifier 7 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_7[15:8]							

Address: 0xDB

Type: R

Description: Original network identifier 7 (MSBs)

[7:0] **ON_ID_7**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#7.

T_ID_L8 TS identifier 8 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_8[7:0]							

Address: 0xDC

Type: R

Description: TS identifier 8 (LSBs)

[7:0] **TS_ID_8**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#8.

T_ID_H8 TS identifier 8 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_8[15:8]							

Address: 0xDD

Type: R

Description: TS identifier 8 (MSBs)

[7:0] **TS_ID_8**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#8.

O_ID_L8 Original network identifier 8 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_8[7:0]							

Address: 0xDE

Type: R

Description: Original network identifier 8 (LSBs)

[7:0] **ON_ID_8**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#8.

O_ID_H8 Original network identifier 8 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_8[15:8]							

Address: 0xDF

Type: R

Description: Original network identifier 8 (MSBs)

[7:0] **ON_ID_8**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#8.

T_ID_L9 TS identifier 9 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_9[7:0]							

Address: 0xE0

Type: R

Description: TS identifier 9 (LSBs)

[7:0] **TS_ID_9**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#9.

T_ID_H9 TS identifier 9 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_9[15:8]							

Address: 0xE1

Type: R

Description: TS identifier 9 (MSBs)

[7:0] **TS_ID_9**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#9.

O_ID_L9 Original network identifier 9 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_9[7:0]							

Address: 0xE2

Type: R

Description: Original network identifier 9 (LSBs)

[7:0] **ON_ID_9**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#9.

O_ID_H9 Original network identifier 9 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_9[15:8]							

Address: 0xE3

Type: R

Description: Original network identifier 9 (MSBs)

[7:0] **ON_ID_9**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#9.

T_ID_L10 TS identifier 10 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_10[7:0]							

Address: 0xE4

Type: R

Description: TS identifier 10 (LSBs)

[7:0] **TS_ID_10**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#10.

T_ID_H10 TS identifier 10 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_10[15:8]							

Address: 0xE5

Type: R

Description: TS identifier 10 (MSBs)

[7:0] **TS_ID_10**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#10.

O_ID_L10 Original network identifier 10 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_10[7:0]							

Address: 0xE6

Type: R

Description: Original network identifier 10 (LSBs)

[7:0] **ON_ID_10**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#10.

O_ID_H10 Original network identifier 10 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_10[15:8]							

Address: 0xE7

Type: R

Description: Original network identifier 10 (MSBs)

[7:0] **ON_ID_10**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#10.

T_ID_L11 TS identifier 11 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_11[7:0]							

Address: 0xE8

Type: R

Description: TS identifier 11 (LSBs)

[7:0] **TS_ID_11**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#11.

T_ID_H11 TS identifier 11 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_11[15:8]							

Address: 0xE9

Type: R

Description: TS identifier 11 (MSBs)

[7:0] **TS_ID_11**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#11.

O_ID_L11 Original network identifier 11 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_11[7:0]							

Address: 0xEA

Type: R

Description: Original network identifier 11 (LSBs)

[7:0] **ON_ID_11**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#11.

O_ID_H11 Original network identifier 11 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_11[15:8]							

Address: 0xEB

Type: R

Description: Original network identifier 11 (MSBs)

[7:0] **ON_ID_11**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#11.

T_ID_L12 TS identifier 12 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_12[7:0]							

Address: 0xEC

Type: R

Description: TS identifier 12 (LSBs)

[7:0] **TS_ID_12**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#12.

T_ID_H12 TS identifier 12 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_12[15:8]							

Address: 0xED

Type: R

Description: TS identifier 12 (MSBs)

[7:0] **TS_ID_12**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#12.

O_ID_L12 Original network identifier 12 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_12[7:0]							

Address: 0xEE

Type: R

Description: Original network identifier 12 (LSBs)

[7:0] **ON_ID_12**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#12.

O_ID_H12 Original network identifier 12 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_12[15:8]							

Address: 0xEF

Type: R

Description: Original network identifier 12 (MSBs)

[7:0] **ON_ID_12**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#12.

T_ID_L13 TS identifier 13 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_13[7:0]							

Address: 0xF0

Type: R

Description: TS identifier 13 (LSBs)

[7:0] **TS_ID_13**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#13.

T_ID_H13 TS identifier 13 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_13[15:8]							

Address: 0xF1

Type: R

Description: TS identifier 13 (MSBs)

[7:0] **TS_ID_13**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#13.

O_ID_L13 Original network identifier 13 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_13[7:0]							

Address: 0xF2

Type: R

Description: Original network identifier 13 (LSBs)

[7:0] **ON_ID_13**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#13.

O_ID_H13 Original network identifier 13 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_13[15:8]							

Address: 0xF3

Type: R

Description: Original network identifier 13 (MSBs)

[7:0] **ON_ID_13**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#13.

T_ID_L14 TS identifier 14 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_14[7:0]							

Address: 0xF4

Type: R

Description: TS identifier 14 (LSBs)

[7:0] **TS_ID_14**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#14.

T_ID_H14 TS identifier 14 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_14[15:8]							

Address: 0xF5

Type: R

Description: TS identifier 14 (MSBs)

[7:0] **TS_ID_14**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#14.

O_ID_L14 Original network identifier 14 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_14[7:0]							

Address: 0xF6

Type: R

Description: Original network identifier 14 (LSBs)

[7:0] **ON_ID_14**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#14.

O_ID_H14 Original network identifier 14 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_14[15:8]							

Address: 0xF7

Type: R

Description: Original network identifier 14 (MSBs)

[7:0] **ON_ID_14**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#14.

T_ID_L15 TS identifier 15 (LSBs)

7	6	5	4	3	2	1	0
TS_ID_15[7:0]							

Address: 0xF8

Type: R

Description: TS identifier 15 (LSBs)

[7:0] **TS_ID_15**[7:0]: LSBs TS identifier extracted from the header for RELATIVE_TS_ID#15.

T_ID_H15 TS identifier 15 (MSBs)

7	6	5	4	3	2	1	0
TS_ID_15[15:8]							

Address: 0xF9

Type: R

Description: TS identifier 15 (MSBs)

[7:0] **TS_ID_15**[15:8]: MSBs TS identifier extracted from the header for RELATIVE_TS_ID#15.

O_ID_L15 Original network identifier 15 (LSBs)

7	6	5	4	3	2	1	0
ON_ID_15[7:0]							

Address: 0xFA

Type: R

Description: Original network identifier 15 (LSBs)

[7:0] **ON_ID_15**[7:0]: LSBs original network identifier extracted from the header for RELATIVE_TS_ID#15.

O_ID_H15 Original network identifier 15 (MSBs)

7	6	5	4	3	2	1	0
ON_ID_15[15:8]							

Address: 0xFB

Type: R

Description: Original network identifier 15 (MSBs)

[7:0] **ON_ID_15**[15:8]: MSBs original network identifier extracted from the header for RELATIVE_TS_ID#15.

7 BGA footprint

7.1 Ball grid array

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

Signal names are identified by including ‘NOT’ if they are active low; otherwise they are active high.

For a complete list of pins arranged alphabetically with their signal names, see *Table 5 on page 132*.

Table 4. Key to BGA diagrams

Function	Type	Key
Transport	SIG	
PIO/peripheral	SIG	
Video	SIG	
Audio	SIG	
System (JTAG, interrupts)	SIG	
Memory (EMI, LMI)	SIG	
Power	VCC/VDD	
Ground	VSS/GND	
No connect	NC	
No ball		

Figure 13. Ballout - Top-left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	VDD1V2	VDD1V2	PIO14[7]					PIO7[1]		TCK					LMIDATA[26]	
B	DGND	DGND	PIO12[1]	PIO12[2]			PIO13[1]	PIO7[2]		TMS	VDD1V8_2V5			LMIDQSN[2]	LMIDATA[29]	
C	PIO14[5]	PIO14[4]	PIO14[6]	PIO12[0]	PIO12[5]	PIO12[7]	PIO7[3]	PIO6[2]	PIO6[3]	TDO	NOTLMICLK[1]	LMIDATA[21]		LMIDATA[31]	LMIDATA[24]	LMIDQSN[3]
D	PIO14[1]	PIO14[3]	PIO14[2]	PIO12[3]	PIO12[6]	PIO13[2]	PIO6[5]		PIO7[0]		LMIPLL_AVDD2V5	LMIDATA[16]	LMIDATA[18]	LMIDQS[2]		LMIDQS[3]
E		PIO13[6]	PIO13[4]	PIO14[0]	PIO13[7]	PIO12[4]		PIO6[4]		NOTTRST		LMICLK[1]	LMIDATA[23]		LMIADDR[0]	
F			PIO13[5]	NOTEMICSB	DGND	DGND	PIO13[3]		PIO6[0]		PIO6[1]		NOTLMICS[1]	NOTLMICS[0]		LMIADDR[4]
G			NOTEMICSC	EMIFLASHCLK	DGND		DGND	PIO13[0]		PIO6[6]		LMIVREF[1]	LMICLKEN[1]		LMIADDR[2]	
H		EMIADDR[1]	NOTEMICSA	EMIADDR[2]		NOTEMICSD		NOTEMIBAA	PIO6[7]		TDI		NOTLMIRAS	NOTLMICAS		LMIADDR[6]
J	EMIADDR[3]	EMIADDR[6]	EMIADDR[5]		EMIADDR[12]		EMITREADYORWAIT			VDD1V2	VDD1V8_2V5	VDD1V8_2V5		LMIDUMMY[0]	VDD1V8_2V5	VDD1V8_2V5
K			EMIADDR[7]	EMIADDR[4]		EMIADDR[11]		NOTEMICSE	VDD1V2	VDD1V2	VDD1V8_2V5	VDD1V8_2V5		LMIDUMMY[1]	VDD1V8_2V5	VDD1V8_2V5
L	NOTEMIOE	EMIRDNOTWR	EMIADDR[8]		EMIADDR[18]		NOTEMIBE[0]		DGND	DGND	LMIPLL_AGND2V5	LMIPLL_AGND1V2	DGND	DGND	DGND	VDD1V2
M		EMIADDR[9]	EMIADDR[14]	EMIADDR[10]		EMIBUSREQ		EMIADDR[21]	VDD1V2	VDD1V2	VDD1V2	VDD1V2	DGND	DGND	DGND	VDD1V2
N			EMIADDR[13]	EMIADDR[15]	EMIADDR[22]		CKGA_AVDD2V5	CKGA_AVDD2V5			VDD1V2	VDD1V2	DGND	DGND	DGND	DGND
P				EMIADDR[24]	EMIADDR[23]	EMIADDR[20]	EMIADDR[16]		DGND	VDD3V3	VDD3V3	VDD3V3	DGND			
R		EMIADDR[25]	EMIDATA[15]	EMIADDR[17]		NOTEMIBE[1]		EMIBUSGNT	DGND	VDD3V3	VDD3V3	VDD3V3	DGND		DGND	DGND
T	EMIDATA[13]	EMIDATA[14]	EMIDATA[6]		NOTEMILBA		EMIADDR[19]		DGND	VDD3V3	VDD3V3	VDD3V3	DGND		DGND	

Figure 14. Ballout - Top-right

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A	LMIDATAMASK[3]					LMIDATA[5]		LMIBA[2]					LMIDATA[6]	LMIDATA[4]	LMI_COMP_GND	VDD1V8_2V5
B	LMIDATA[25]	LMIDATA[28]			LMICLK[0]	LMIDATA[0]		LMIDATA[13]	LMIDATA[10]			LMIDATA[12]	LMIDATA[1]	LMI_COMP_REF	DGND	DGND
C	LMIDATAMASK[2]	LMIDATA[27]		LMIDATA[20]	NOTLMICLK[0]	LMIDATA[7]	LMIDATA[2]	LMIDQSN[0]	LMIDATA[8]	LMIDQSN[1]	LMIDATAMASK[1]	LMIDATA[11]	LMIDATA[3]	LMIVREF[0]	ODT[1]	VDD1V2
D		LMIDATA[30]	LMIDATA[17]	LMIDATA[19]	LMIBA[1]		LMIDQS[0]		LMIDATA[15]	LMIDQS[1]	LMIDATAMASK[0]	LMIDATA[14]		SYSCLKOUT	SYSITRQ[3]	
E	LMIADDR[8]		LMIDATA[22]	LMIBA[0]		LMIADDR[3]		DGND		DGND	LMIDATA[9]	DGND	SYSITRQ[1]	SYSITRQ[0]		
F		LMIADDR[13]	DGND		LMIADDR[7]		LMIADDR[1]		VDD1V8_2V5		DGND	SYSCLKINALT	TRIGGERIN	NMI		
G	LMIADDR[11]		DGND	LMIADDR[12]		LMIADDR[5]		VDD1V8_2V5		LMICLKEN[0]	WDOGRSTOUT		PIO16[2]	PIO16[4]	PIO16[3]	
H		ODT[0]		DGND	LMIADDR[9]		LMIADDR[10]		NOTLMIWE	NOTASEBRK		SYSITRQ[2]		PIO11[7]	PIO16[1]	PIO16[0]
J	VDD1V8_2V5	VDD1V8_2V5	VDD1V8_2V5		VDD1V8_2V5	VDD1V8_2V5	VDD3V3	VDD3V3	TRIGGEROUT		NOTRESETIN		PIO16[7]	PIO11[3]		
K	VDD1V8_2V5	VDD1V8_2V5	VDD1V8_2V5		VDD1V8_2V5	VDD1V8_2V5	VDD3V3	VDD3V3		FDMAREQ[2]		DAA_C1A		PIO11[4]	PIO11[6]	PIO11[5]
L	VDD1V2	VDD1V2	VDD1V2	VDD1V2	DGND	DGND	VDD3V3	VDD3V3	FDMAREQ[3]		DAA_C2A		PIO16[5]	PIO9[7]	PIO11[2]	
M	VDD1V2	VDD1V2	VDD1V2	DGND	DGND	DGND	VDD3V3	VDD3V3		FDMAREQ[0]		PIO16[6]	PIO15[6]	PIO15[7]		
N	DGND	DGND	DGND	DGND	DGND	DGND			VDD3V3	PIO5[3]	FDMAREQ[1]	GND_SENSE	VDD_SENSE			
P				DGND	DGND	DGND	VDD1V2	VDD3V3	VDD3V3		PIO5[2]		PIO5[1]	PIO5[5]	PIO5[0]	
R	DGND	DGND		DGND	DGND	DGND	VDD1V2	VDD3V3		PIO4[4]		PIO3[4]		PIO4[6]	PIO4[5]	PIO4[0]
T		DGND		DGND	DGND	DGND	VDD1V2	VDD3V3	VDD3V3		PIO4[7]		PIO5[7]	PIO5[6]		

Figure 15. Ballout - Bottom-left

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
U			EMIDATA[4]	EMIDATA[11]		EMIDATA[2]		NANDWAIT	DGND	VDD3V3	VDD3V3	VDD3V3	DGND		DGND	
V	EMIDATA[12]	EMIDATA[1]	EMIDATA[3]		EMIDATA[7]		EMIDATA[8]		DGND	VDD3V3	VDD3V3	VDD3V3	DGND		DGND	DGND
W		EMIDATA[10]	EMIDATA[9]	PIO15[3]		EMIDATA[0]		EMIDATA[5]	DGND	VDD3V3	VDD1V2	VDD1V2	DGND			
Y				VDD3V3	VDD3V3	VDD3V3	VDD3V3	VDD3V3			VDD1V2	VDD1V2	DGND	DGND	DGND	DGND
AA			PIO15[0]	PIO15[1]	PIO15[2]		PIO15[5]		DGND	DGND	VDD3V3	VDD3V3	DGND	DGND	DGND	DGND
AB		VDD3V3_297J	VDD3V3_297J	VDD3V3_297J		DATA0		PIO15[4]	DGND	DGND	VDD3V3	VDD3V3	VDD1V2	VDD1V2	ANA1_GND2V5	ANA1_GND2V5
AC	STR_OUT	CLK_OUT	DATA7		DATA2		DATA1		VDD3V3_297J	DGND	VDD1V2	VDD1V2		CKGC_AVDD2V5	ANA1_VDD2V5	GNDSATA
AD			D_NOT_P	ERROR		DATA4		DATA3	VDD3V3_297J	DGND	VDD1V2	VDD1V2		ANA1_VDD2V5	PIO10[0]	SATAVSS
AE	VDD1V8_297J	TEST[1]			DATA5		DATA6	NOT_RESET		SCL		PIO8[3]	PIO10[7]		PIO10[3]	
AF		TEST[0]	TEST[5]	TEST[3]		DGND	DGND		CK_TEST		PIO9[3]		PIO8[4]	PIO10[4]		PIO10[2]
AG			LOCK	TEST[4]	DGND	DGND		DGND		SDA		PIO9[6]		PIO11[1]	PIO10[6]	
AH			TEST[2]	IT	DGND	DGND	DGND		AUX_CLK		PIO9[4]		PIO7[5]	PIO8[6]		PIO10[1]
AJ						DGND	DGND			VDD3V3_297J		PIO7[6]	PIO7[4]	PIO8[7]	PIO9[0]	
AK	VDD1V8_297J	VDD1V8_297J	VDD1V8_297J	TEST_MODE	REFM	SCLT	SDAT	XTAL_I		VDD3V3_297J	PIO8[1]	PIO9[2]	PIO8[5]		PIO9[5]	AUDA_LEFTOUTN
AL				IREF	INP			XTAL_O	AGC2		PIO7[7]	PIO8[2]			PIO9[1]	AUDA_RIGHTOUTN
AM	DGND		REFP	INM					AGC1		PIO8[0]					AUDA_RIGHTOUTP

Figure 16. Ballout- Bottom-right

	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
U		DGND		DGND	DGND	DGND	VDD1V2	VDD1V2		VDD2V5		PIO4[1]		PIO3[5]	PIO3[6]	PIO3[7]
V	DGND	DGND		DGND	DGND	DGND	VDD1V2	VDD1V2	MEM_AVDD2V5		PIO0[3]		PIO4[3]	PIO4[2]	PIO5[4]	
W				DGND	DGND	DGND	ANA2_VDDE2V5	ANA2_VDDE2V5		CKGB0_AVDD2V5	CKGB1_AVDD2V5	PIO1[6]	PIO1[4]			
Y	DGND	DGND	DGND	DGND	DGND	DGND			HDMIPLL_AVDD2V5			PIO2[3]	PIO2[4]	PIO2[6]		
AA	VDD1V2	VDD1V2	VDD1V2	DGND	DGND	DGND	VDD1V2	VDD1V2	ANA2_GNDE2V5		PIO0[0]		PIO2[0]	PIO2[1]	PIO2[2]	
AB	VDD1V2	VDD1V2	VDD1V2	TMDS_GND	TMDS_GND	TMDS_GND	VDD1V2	VDD1V2		PIO0[5]		PIO0[1]		PIO1[1]	PIO2[7]	PIO2[5]
AC	SATAVSS_PLL	USB_VDD1V2	USB_VDD1V2		TMDS_VDD1V2	TMDS_VDD1V2	HDMI_VDD1V2	HDMIPLL_AVDD1V2	PIO0[6]		PIO0[2]		PIO1[5]	PIO1[7]		
AD	SATAVSS	USB_VDD1V2	USB_GND1V2		TMDS_VDD1V2	TMDS_VDD1V2	HDMI_GND3V3	HDMIPLL_AGND2V5		PIO1[2]		PIO0[7]		PIO1[0]	PIO1[3]	PIO3[2]
AE	PIO10[5]		USB_GND1V2	USB_GND1V2		HDMI_VDD3V3		DGND	HDMIPLL_AGND1V2		PIO0[4]		PIO3[1]	PIO3[3]	PIO3[0]	
AF		SATAVDDR		USB2VDDB3V3	USB_GND2V5		DGND		DGND	VIDA1_GNDA1		VIDA1_COUT	VIDA1_YOUT	VIDA1_CVOUT		
AG	PIO11[0]		USB1VDDB3V3	USB_VDD2V5		USB2DP		DGND		DGND	VIDA1_GNDAS	VIDA1_MASSQUIET	VIDA1_REXT	VIDA1_IDUMP		
AH		DGND		USB_VDD2V5	SATAVDD2_PLL		USB2DM		DGND		DGND	DGND	VIDA1_GNDA2	VIDA1_VCCA2	VIDA1_VCCA1	
AJ	DGND		DGND	SATAVDDT	SATATXP0	DGND		DGND		DGND	TMDSTXCN	TMDSTX0N	VIDA0_GNDA2	VIDA0_GNDA1	VIDA0_ROUT	VIDA0_GOUT
AK	AUDA_LEFTOUTP	AUDA_IREF	SATARXN0		SATATXN0	SATAVDD_PLL	DGND	(1) REXT	DGND	HDMI_CEC	TMDSTXCP	TMDSTX0P	TMDSTX1N	VIDA0_GNDAS	VIDA0_MASSQUIET	VIDA0_BOUT
AL		AUDA_GNDAS	SATARXP0			SATAREF	SYSCLKIN		USB1DP	TMDSREF			TMDSTX1P	TMDSTX2N	VIDA0_REXT	VIDA0_IDUMP
AM		AUDA_VBGOUT					SYSCLKOSC		USB1DM					TMDSTX2P	VIDA0_VCCA1	VIDA0_VCCA2

(1)REXT (on AK24) is the USB reference USBREF.

8 Connections

This chapter contains detail of pins, pad reset conditions, alternative functions and connection diagrams, listed in the following functional groups:

8.1 Ball list sorted by ball number

Table 5. Ball list

Ball number	Ball name
A1	VDD1V2
A2	VDD1V2
A3	PIO14[7]
A8	PIO7[1]
A10	TCK

Table 5. Ball list (continued)

Ball number	Ball name
A15	LMIDATA[26]
A17	LMIDATAMASK[3]
A22	LMIDATA[5]
A24	LMIBA[2]
A29	LMIDATA[6]
A30	LMIDATA[4]
A31	LMI_COMP_GND
A32	VDD1V8_2V5
B1	DGND
B2	DGND
B3	PIO12[1]
B4	PIO12[2]
B7	PIO13[1]
B8	PIO7[2]
B10	TMS
B11	VDD1V8_2V5
B14	LMIDQSN[2]
B15	LMIDATA[29]
B17	LMIDATA[25]
B18	LMIDATA[28]
B21	LMICLK[0]
B22	LMIDATA[0]
B24	LMIDATA[13]
B25	LMIDATA[10]
B28	LMIDATA[12]
B29	LMIDATA[1]
B30	LMI_COMP_REF
B31	DGND
B32	DGND
C1	PIO14[5]
C2	PIO14[4]
C3	PIO14[6]
C4	PIO12[0]
C5	PIO12[5]
C6	PIO12[7]

Table 5. Ball list (continued)

Ball number	Ball name
C7	PIO7[3]
C8	PIO6[2]
C9	PIO6[3]
C10	TDO
C11	NOTLMICLK[1]
C12	LMIDATA[21]
C14	LMIDATA[31]
C15	LMIDATA[24]
C16	LMIDQSN[3]
C17	LMIDATAMASK[2]
C18	LMIDATA[27]
C20	LMIDATA[20]
C21	NOTLMICLK[0]
C22	LMIDATA[7]
C23	LMIDATA[2]
C24	LMIDQSN[0]
C25	LMIDATA[8]
C26	LMIDQSN[1]
C27	LMIDATAMASK[1]
C28	LMIDATA[11]
C29	LMIDATA[3]
C30	LMIVREF[0]
C31	ODT[1]
C32	VDD1V2
D1	PIO14[1]
D2	PIO14[3]
D3	PIO14[2]
D4	PIO12[3]
D5	PIO12[6]
D6	PIO13[2]
D7	PIO6[5]
D9	PIO7[0]
D11	LMIPLL_AVDD2V5
D12	LMIDATA[16]
D13	LMIDATA[18]

Table 5. Ball list (continued)

Ball number	Ball name
D14	LMIDQS[2]
D16	LMIDQS[3]
D18	LMIDATA[30]
D19	LMIDATA[17]
D20	LMIDATA[19]
D21	LMIBA[1]
D23	LMIDQS[0]
D25	LMIDATA[15]
D26	LMIDQS[1]
D27	LMIDATAMASK[0]
D28	LMIDATA[14]
D29	NC
D30	SYSCLKOUT
D31	SYSITRQ[3]
E2	PIO13[6]
E3	PIO13[4]
E4	PIO14[0]
E5	PIO13[7]
E6	PIO12[4]
E8	PIO6[4]
E10	NOTTRST
E12	LMICLK[1]
E13	LMIDATA[23]
E15	LMIADDR[0]
E17	LMIADDR[8]
E19	LMIDATA[22]
E20	LMIBA[0]
E22	LMIADDR[3]
E24	DGND
E26	DGND
E27	LMIDATA[9]
E28	DGND
E29	SYSITRQ[1]
E30	SYSITRQ[0]
F3	PIO13[5]

Table 5. Ball list (continued)

Ball number	Ball name
F4	NOTEMICSB
F5	DGND
F6	DGND
F7	PIO13[3]
F9	PIO6[0]
F11	PIO6[1]
F13	NOTLMICS[1]
F14	NOTLMICS[0]
F16	LMIADDR[4]
F18	LMIADDR[13]
F19	DGND
F21	LMIADDR[7]
F23	LMIADDR[1]
F25	VDD1V8_2V5
F27	DGND
F28	SYSCLKINALT
F29	TRIGGERIN
F30	NMI
G3	NOTEMICSC
G4	EMIFLASHCLK
G5	DGND
G7	DGND
G8	PIO13[0]
G10	PIO6[6]
G12	LMIVREF[1]
G13	LMICLKEN[1]
G15	LMIADDR[2]
G17	LMIADDR[11]
G19	DGND
G20	LMIADDR[12]
G22	LMIADDR[5]
G24	VDD1V8_2V5
G26	LMICLKEN[0]
G27	WDOGRSTOUT
G29	PIO16[2]

Table 5. Ball list (continued)

Ball number	Ball name
G30	PIO16[4]
G31	PIO16[3]
H2	EMIADDR[1]
H3	NOTEMICSA
H4	EMIADDR[2]
H6	NOTEMICSD
H8	NOTEMIBAA
H9	PIO6[7]
H11	TDI
H13	NOTLMIRAS
H14	NOTLMICAS
H16	LMIADDR[6]
H18	ODT[0]
H20	DGND
H21	LMIADDR[9]
H23	LMIADDR[10]
H25	NOTLMIWE
H26	NOTASEBRK
H28	SYSITRQ[2]
H30	PIO11[7]
H31	PIO16[1]
H32	PIO16[0]
J1	EMIADDR[3]
J2	EMIADDR[6]
J3	EMIADDR[5]
J5	EMIADDR[12]
J7	EMITREADYORWAIT
J9	NC
J10	VDD1V2
J11	VDD1V8_2V5
J12	VDD1V8_2V5
J14	LMIDUMMY[0]
J15	VDD1V8_2V5
J16	VDD1V8_2V5
J17	VDD1V8_2V5

Table 5. Ball list (continued)

Ball number	Ball name
J18	VDD1V8_2V5
J19	VDD1V8_2V5
J21	VDD1V8_2V5
J22	VDD1V8_2V5
J23	VDD3V3
J24	VDD3V3
J25	TRIGGEROUT
J27	NOTRESETIN
J29	PIO16[7]
J30	PIO11[3]
K3	EMIADDR[7]
K4	EMIADDR[4]
K6	EMIADDR[11]
K8	NOTEMICSE
K9	VDD1V2
K10	VDD1V2
K11	VDD1V8_2V5
K12	VDD1V8_2V5
K14	LMIDUMMY[1]
K15	VDD1V8_2V5
K16	VDD1V8_2V5
K17	VDD1V8_2V5
K18	VDD1V8_2V5
K19	VDD1V8_2V5
K21	VDD1V8_2V5
K22	VDD1V8_2V5
K23	VDD3V3
K24	VDD3V3
K26	FDMAREQ[2]
K28	DAA_C1A
K30	PIO11[4]
K31	PIO11[6]
K32	PIO11[5]
L1	NOTEMIOE
L2	EMIRDNOTWR

Table 5. Ball list (continued)

Ball number	Ball name
L3	EMIADDR[8]
L5	EMIADDR[18]
L7	NOTEMIBE[0]
L9	DGND
L10	DGND
L11	LMIPLL_AGND2V5
L12	LMIPLL_AGND1V2
L13	DGND
L14	DGND
L15	DGND
L16	VDD1V2
L17	VDD1V2
L18	VDD1V2
L19	VDD1V2
L20	VDD1V2
L21	DGND
L22	DGND
L23	VDD3V3
L24	VDD3V3
L25	FDMAREQ[3]
L27	DAA_C2A
L29	PIO16[5]
L30	PIO9[7]
L31	PIO11[2]
M2	EMIADDR[9]
M3	EMIADDR[14]
M4	EMIADDR[10]
M6	EMIBUSREQ
M8	EMIADDR[21]
M9	VDD1V2
M10	VDD1V2
M11	VDD1V2
M12	VDD1V2
M13	DGND
M14	DGND

Table 5. Ball list (continued)

Ball number	Ball name
M15	DGND
M16	VDD1V2
M17	VDD1V2
M18	VDD1V2
M19	VDD1V2
M20	DGND
M21	DGND
M22	DGND
M23	VDD3V3
M24	VDD3V3
M26	FDMAREQ[0]
M28	PIO16[6]
M29	PIO15[6]
M30	PIO15[7]
N3	EMIADDR[13]
N4	EMIADDR[15]
N5	EMIADDR[22]
N7	CKGA_AVDD2V5
N8	CKGA_AVDD2V5
N11	VDD1V2
N12	VDD1V2
N13	DGND
N14	DGND
N15	DGND
N16	DGND
N17	DGND
N18	DGND
N19	DGND
N20	DGND
N21	DGND
N22	DGND
N25	VDD3V3
N26	PIO5[3]
N27	FDMAREQ[1]
N28	GND_SENSE

Table 5. Ball list (continued)

Ball number	Ball name
N29	VDD_SENSE
P4	EMIADDR[24]
P5	EMIADDR[23]
P6	EMIADDR[20]
P7	EMIADDR[16]
P9	DGND
P10	VDD3V3
P11	VDD3V3
P12	VDD3V3
P13	DGND
P20	DGND
P21	DGND
P22	DGND
P23	VDD1V2
P24	VDD3V3
P25	VDD3V3
P27	PIO5[2]
P29	PIO5[1]
P30	PIO5[5]
P31	PIO5[0]
R2	EMIADDR[25]
R3	EMIDATA[15]
R4	EMIADDR[17]
R6	NOTEMIBE[1]
R8	EMIBUSGNT
R9	DGND
R10	VDD3V3
R11	VDD3V3
R12	VDD3V3
R13	DGND
R15	DGND
R16	DGND
R17	DGND
R18	DGND
R20	DGND

Table 5. Ball list (continued)

Ball number	Ball name
R21	DGND
R22	DGND
R23	VDD1V2
R24	VDD3V3
R26	PIO4[4]
R28	PIO3[4]
R30	PIO4[6]
R31	PIO4[5]
R32	PIO4[0]
T1	EMIDATA[13]
T2	EMIDATA[14]
T3	EMIDATA[6]
T5	NOTEMILBA
T7	EMIADDR[19]
T9	DGND
T10	VDD3V3
T11	VDD3V3
T12	VDD3V3
T13	DGND
T15	DGND
T18	DGND
T20	DGND
T21	DGND
T22	DGND
T23	VDD1V2
T24	VDD3V3
T25	VDD3V3
T27	PIO4[7]
T29	PIO5[7]
T30	PIO5[6]
U3	EMIDATA[4]
U4	EMIDATA[11]
U6	EMIDATA[2]
U8	NANDWAIT
U9	DGND

Table 5. Ball list (continued)

Ball number	Ball name
U10	VDD3V3
U11	VDD3V3
U12	VDD3V3
U13	DGND
U15	DGND
U18	DGND
U20	DGND
U21	DGND
U22	DGND
U23	VDD1V2
U24	VDD1V2
U26	VDD2V5
U28	PIO4[1]
U30	PIO3[5]
U31	PIO3[6]
U32	PIO3[7]
V1	EMIDATA[12]
V2	EMIDATA[1]
V3	EMIDATA[3]
V5	EMIDATA[7]
V7	EMIDATA[8]
V9	DGND
V10	VDD3V3
V11	VDD3V3
V12	VDD3V3
V13	DGND
V15	DGND
V16	DGND
V17	DGND
V18	DGND
V20	DGND
V21	DGND
V22	DGND
V23	VDD1V2
V24	VDD1V2

Table 5. Ball list (continued)

Ball number	Ball name
V25	MEM_AVDD2V5
V27	PIO0[3]
V29	PIO4[3]
V30	PIO4[2]
V31	PIO5[4]
W2	EMIDATA[10]
W3	EMIDATA[9]
W4	PIO15[3]
W6	EMIDATA[0]
W8	EMIDATA[5]
W9	DGND
W10	VDD3V3
W11	VDD1V2
W12	VDD1V2
W13	DGND
W20	DGND
W21	DGND
W22	DGND
W23	ANA2_VDDE2V5
W24	ANA2_VDDE2V5
W26	CKGB0_AVDD2V5
W27	CKGB1_AVDD2V5
W28	PIO1[6]
W29	PIO1[4]
Y4	VDD3V3
Y5	VDD3V3
Y6	VDD3V3
Y7	VDD3V3
Y8	VDD3V3
Y11	VDD1V2
Y12	VDD1V2
Y13	DGND
Y14	DGND
Y15	DGND
Y16	DGND

Table 5. Ball list (continued)

Ball number	Ball name
Y17	DGND
Y18	DGND
Y19	DGND
Y20	DGND
Y21	DGND
Y22	DGND
Y25	HDMIPLL_AVDD2V5
Y26	NC
Y28	PIO2[3]
Y29	PIO2[4]
Y30	PIO2[6]
AA3	PIO15[0]
AA4	PIO15[1]
AA5	PIO15[2]
AA7	PIO15[5]
AA9	DGND
AA10	DGND
AA11	VDD3V3
AA12	VDD3V3
AA13	DGND
AA14	DGND
AA15	DGND
AA16	DGND
AA17	VDD1V2
AA18	VDD1V2
AA19	VDD1V2
AA20	DGND
AA21	DGND
AA22	DGND
AA23	VDD1V2
AA24	VDD1V2
AA25	ANA2_GNDE2V5
AA27	PIO0[0]
AA29	PIO2[0]
AA30	PIO2[1]

Table 5. Ball list (continued)

Ball number	Ball name
AA31	PIO2[2]
AB2	VDD3V3_297J
AB3	VDD3V3_297J
AB4	VDD3V3_297J
AB6	DATA0
AB8	PIO15[4]
AB9	DGND
AB10	DGND
AB11	VDD3V3
AB12	VDD3V3
AB13	VDD1V2
AB14	VDD1V2
AB15	ANA1_GND2V5
AB16	ANA1_GND2V5
AB17	VDD1V2
AB18	VDD1V2
AB19	VDD1V2
AB20	TMDS_GND
AB21	TMDS_GND
AB22	TMDS_GND
AB23	VDD1V2
AB24	VDD1V2
AB26	PIO0[5]
AB28	PIO0[1]
AB30	PIO1[1]
AB31	PIO2[7]
AB32	PIO2[5]
AC1	STR_OUT
AC2	CLK_OUT
AC3	DATA7
AC5	DATA2
AC7	DATA1
AC9	VDD3V3_297J
AC10	DGND
AC11	VDD1V2

Table 5. Ball list (continued)

Ball number	Ball name
AC12	VDD1V2
AC14	CKGC_AVDD2V5
AC15	ANA1_VDD2V5
AC16	GNDSATA
AC17	SATAVSS_PLL
AC18	USB_VDD1V2
AC19	USB_VDD1V2
AC21	TMDS_VDD1V2
AC22	TMDS_VDD1V2
AC23	HDMI_VDD1V2
AC24	HDMIPLL_AVDD1V2
AC25	PIO0[6]
AC27	PIO0[2]
AC29	PIO1[5]
AC30	PIO1[7]
AD3	D_NOT_P
AD4	ERROR
AD6	DATA4
AD8	DATA3
AD9	VDD3V3_297J
AD10	DGND
AD11	VDD1V2
AD12	VDD1V2
AD14	ANA1_VDD2V5
AD15	PIO10[0]
AD16	SATAVSS
AD17	SATAVSS
AD18	USB_VDD1V2
AD19	USB_GND1V2
AD21	TMDS_VDD1V2
AD22	TMDS_VDD1V2
AD23	HDMI_GND3V3
AD24	HDMIPLL_AGND2V5
AD26	PIO1[2]
AD28	PIO0[7]

Table 5. Ball list (continued)

Ball number	Ball name
AD30	PIO1[0]
AD31	PIO1[3]
AD32	PIO3[2]
AE1	VDD1V8_297J
AE2	TEST[1]
AE3	NC
AE5	DATA5
AE7	DATA6
AE8	NOT_RESET
AE10	SCL
AE12	PIO8[3]
AE13	PIO10[7]
AE15	PIO10[3]
AE17	PIO10[5]
AE19	USB_GND1V2
AE20	USB_GND1V2
AE22	HDMI_VDD3V3
AE24	DGND
AE25	HDMIPLL_AGND1V2
AE27	PIO0[4]
AE29	PIO3[1]
AE30	PIO3[3]
AE31	PIO3[0]
AF2	TEST[0]
AF3	TEST[5]
AF4	TEST[3]
AF6	DGND
AF7	DGND
AF9	CK_TEST
AF11	PIO9[3]
AF13	PIO8[4]
AF14	PIO10[4]
AF16	PIO10[2]
AF18	SATAVDDR
AF20	USB2VDDB3V3

Table 5. Ball list (continued)

Ball number	Ball name
AF21	USB_GND2V5
AF23	DGND
AF25	DGND
AF26	VIDA1_GNDA1
AF28	VIDA1_COUT
AF29	VIDA1_YOUT
AF30	VIDA1_CVOUT
AG3	LOCK
AG4	TEST[4]
AG5	DGND
AG6	DGND
AG8	DGND
AG10	SDA
AG12	PIO9[6]
AG14	PIO11[1]
AG15	PIO10[6]
AG17	PIO11[0]
AG19	USB1VDDB3V3
AG20	USB_VDD2V5
AG22	USB2DP
AG24	DGND
AG26	DGND
AG27	VIDA1_GNDAS
AG28	VIDA1_MASSQUIET
AG29	VIDA1_REXT
AG30	VIDA1_IDUMP
AH3	TEST[2]
AH4	IT
AH5	DGND
AH6	DGND
AH7	DGND
AH9	AUX_CLK
AH11	PIO9[4]
AH13	PIO7[5]
AH14	PIO8[6]

Table 5. Ball list (continued)

Ball number	Ball name
AH16	PIO10[1]
AH18	DGND
AH20	USB_VDD2V5
AH21	SATAVDD2_PLL
AH23	USB2DM
AH25	DGND
AH27	DGND
AH28	DGND
AH29	VIDA1_GNDA2
AH30	VIDA1_VCCA2
AH31	VIDA1_VCCA1
AJ2	NC
AJ3	NC
AJ4	NC
AJ5	NC
AJ6	DGND
AJ7	DGND
AJ8	NC
AJ10	VDD3V3_297J
AJ12	PIO7[6]
AJ13	PIO7[4]
AJ14	PIO8[7]
AJ15	PIO9[0]
AJ17	DGND
AJ19	DGND
AJ20	SATAVDDT
AJ21	SATATXP0
AJ22	DGND
AJ24	DGND
AJ26	DGND
AJ27	TMDSTXCN
AJ28	TMDSTX0N
AJ29	VIDA0_GNDA2
AJ30	VIDA0_GNDA1
AJ31	VIDA0_ROUT

Table 5. Ball list (continued)

Ball number	Ball name
AJ32	VIDA0_GOUT
AK1	VDD1V8_297J
AK2	VDD1V8_297J
AK3	VDD1V8_297J
AK4	TEST_MODE
AK5	REFM
AK6	SCLT
AK7	SDAT
AK8	XTAL_I
AK9	NC
AK10	VDD3V3_297J
AK11	PIO8[1]
AK12	PIO9[2]
AK13	PIO8[5]
AK15	PIO9[5]
AK16	AUDA_LEFTOUTN
AK17	AUDA_LEFTOUTP
AK18	AUDA_IREF
AK19	SATARXN0
AK21	SATATXN0
AK22	SATAVDD_PLL
AK23	DGND
AK24	REXT (Note: REXT is the USB reference USBREF)
AK25	DGND
AK26	HDMI_CEC
AK27	TMDSTXCP
AK28	TMDSTX0P
AK29	TMDSTX1N
AK30	VIDA0_GNDAS
AK31	VIDA0_MASSQUIET
AK32	VIDA0_BOUT
AL1	NC
AL2	NC
AL3	NC
AL4	IREF

Table 5. Ball list (continued)

Ball number	Ball name
AL5	INP
AL8	XTAL_O
AL9	AGC2
AL11	PIO7[7]
AL12	PIO8[2]
AL15	PIO9[1]
AL16	AUDA_RIGHTOUTN
AL18	AUDA_GNDAS
AL19	SATARXP0
AL22	SATAREF
AL23	SYSCLKIN
AL25	USB1DP
AL26	TMDSREF
AL29	TMDSTX1P
AL30	TMDSTX2N
AL31	VIDA0_REXT
AL32	VIDA0_IDUMP
AM1	DGND
AM2	NC
AM3	REFP
AM4	INM
AM9	AGC1
AM11	PIO8[0]
AM16	AUDA_RIGHTOUTP
AM18	AUDA_VBGOUT
AM23	SYSCLKOSC
AM25	USB1DM
AM30	TMDSTX2P
AM31	VIDA0_VCCA1
AM32	VIDA0_VCCA2

8.2 Power supplies

Table 6. Power/ground pins

Ball	Assignment	Voltage	Type	Description
USB 2.0				
AC18	USB_VDD1V2	1.2	Analog	USB 1.2 V power
AC19				
AD18				
AD19	USB_GND1V2	0	Analog	USB ground
AE19				
AE20				
AF21	USB_GND2V5	0	Analog	USB ground
AG19	USB1VDDB3V3	3.3	Analog	USB1 3.3 V power
AF20	USB2VDDB3V3	3.3	Analog	USB2 3.3 V power
AG20	USB_VDD2V5	2.5	Analog	USB 2.5 V power
AH20				
SATA				
AD16	SATAVSS	0	-	SATA ground
AD17	SATAVSS	0	-	SATA ground
AF18	SATAVDDR	1.2	Analog	SATA power
AJ20	SATAVDDT	1.2	Analog	SATA power
AK22	SATAVDD_PLL	1.2	Analog	SATA PLL power
AC17	SATAVSS_PLL	0	-	SATA PLL ground
AH21	SATAVDD2_PLL	2.5	Analog	SATA PLL power
AC16	GNDSATA	0	-	SATA ground
HDMI				
AC21	TMDS_VDD1V2	1.2	Analog	TMDS 1.2 V power
AC22	TMDS_VDD1V2	1.2	Analog	TMDS 1.2 V power
AD21	TMDS_VDD1V2	1.2	Analog	TMDS 1.2 V power
AD22	TMDS_VDD1V2	1.2	Analog	TMDS 1.2 V power
AB20	TMDS_GND	0	-	TMDS ground
AB21	TMDS_GND	0	-	TMDS ground
AB22	TMDS_GND	0	-	TMDS ground
Y25	HDMIPLL_AVDD2V5	2.5	Analog	HDMI PLL 2.5 V power
AD24	HDMIPLL_AGND2V5	0	-	HDMI PLL ground
AC24	HDMIPLL_AVDD1V2	1.2	Analog	HDMI PLL power
AE25	HDMIPLL_AGND1V2	0	-	HDMI PLL ground
AD23	HDMI_GND3V3	0	-	HDMI ground

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
AE22	HDMI_VDD3V3	3.3	Digital	HDMI 3.3 V power
AC23	HDMI_VDD1V2	1.2	Digital	HDMI 1.2 V power
LMIPLL				
D11	LMIPLL_AVDD2V5	2.5	Analog	LMI PLL 2.5 V power
L11	LMIPLL_AGND2V5	0	-	LMI PLL ground
L12	LMIPLL_AGND1V2	0	-	LMI PLL ground
Video DACs				
AK30	VIDA0_GNDAS	0	-	Ground
AJ29	VIDA0_GNDA2	0	-	Ground
AM31	VIDA0_VCCA1	2.5	Analog	2.5 V power
AM32	VIDA0_VCCA2	2.5	Analog	2.5 V power
AJ30	VIDA0_GNDA1	0	-	Ground
AG27	VIDA1_GNDAS	0	-	Ground
AH29	VIDA1_GNDA2	0	-	Ground
AH30	VIDA1_VCCA2	2.5	Analog	2.5 V power
AH31	VIDA1_VCCA1	2.5	Analog	2.5 V power
AF26	VIDA1_GNDA1	0	-	Ground
W23	ANA2_VDDE2V5	2.5	Analog	2.5 V power
AA25	ANA2_GNDE2V5	0	-	Ground
W24	ANA2_VDDE2V5	2.5	Analog	2.5 V power
Audio DAC				
AB15	ANA1_GND2V5	0	-	Ground
AB16	ANA1_GND2V5	0	-	Ground
AC15	ANA1_VDD2V5	2.5	Analog	2.5 V power
AD14	ANA1_VDD2V5	2.5	Analog	2.5 V power
ClockGenA				
N7	CKGA_AVDD2V5	2.5	Analog	2.5 V power
N8				2.5 V power
ClockGenB				
W26	CKGB0_AVDD2V5	2.5	Analog	CKGB FS0 2.5 V power
W27	CKGB1_AVDD2V5			CKGB FS1 2.5 V power
ClockGenC				
AC14	CKGC_AVDD2V5	2.5	Analog	CKGC FS 2.5 V power

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
LMI				
A32	VDD1V8_2V5	1.8	Digital	LMI DDR2 1.8/2.5 V power
B11				
F25				
G24				
J11				
J12				
J15				
J16				
J17				
J18				
J19				
J21				
J22				
K11				
K12				
K15				
K16				
K17				
K18				
K19				
K21				
K22				
Analog 2.5V				
V25	MEM_AVDD2V5	2.5	Analog	
Digital 2.5V				
U26	VDD2V5	2.5	Digital	Digital 2.5 V power

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
Digital 3.3 V				
AA11	VDD3V3	3.3	Digital	Digital 3.3 V power
AA12				
AB11				
AB12				
J23				
J24				
K23				
K24				
L23				
L24				
M23				
M24				
N25				
P10				
P11				
P12				
P24				
P25				
R10				
R11				
R12				
R24				
T10				
T11				
T12				
T24				
T25				
U10				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
U11	VDD3V3	3.3	Digital	Digital 3.3 V power
U12				
V10				
V11				
V12				
W10				
Y4				
Y5				
Y6				
Y7				
Y8				
AB2	VDD3V3_297J	3.3	Digital	Digital I/O supply
AB3				
AB4				
AC9				
AD9				
AJ10				
AK10				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
DGND				
AA10	DGND	0		Digital 3.3/2.5/1.2 V ground
AA13				
AA14				
AA15				
AA16				
AA20				
AA21				
AA22				
AA9				
AB10				
AB9				
AC10				
AD10				
AE24				
AF23				
AF25				
AF6				
AF7				
AG24				
AG26				
AG5				
AG6				
AG8				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
AH18	DGND	0		Digital 3.3/2.5/1.2 V ground
AH25				
AH27				
AH28				
AH5				
AH6				
AH7				
AJ17				
AJ19				
AJ22				
AJ24				
AJ26				
AJ6				
AJ7				
AK23				
AK25				
AM1				
B1				
B2				
B31				
B32				
E24				
E26				
E28				
F19				
F27				
F5				
F6				
G19				
G5				
G7				
H20				
L10				
L13				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
L14				
L15				
L21				
L22				
L9				
M13				
M14				
M15				
M20				
M21				
M22				
N13				
N14				
N15				
N16				
N17				
N18				
N19	DGND	0		Digital 3.3/2.5/1.2 V ground
N20				
N21				
N22				
P13				
P20				
P21				
P22				
P9				
R13				
R15				
R16				
R17				
R18				
R20				
R21				
R22				
R9				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
T13	DGND	0		Digital 3.3/2.5/1.2 V ground
T15				
T18				
T20				
T21				
T22				
T9				
U13				
U15				
U18				
U20				
U21				
U22				
U9				
V13				
V15				
V16				
V17				
V18				
V20				
V21				
V22				
V9				
W13				
W20				
W21				
W22				
W9				
Y13				
Y14				
Y15				
Y16				
Y17				
Y18				
Y19				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
Y20	DGND	0		Digital 3.3/2.5/1.2 V ground
Y21				
Y22				
Digital 1.2 V				
A1	VDD1V2	1.2	Digital	Digital power 1.2 V core power
A2				
AA17				
AA18				
AA19				
AA23				
AA24				
AB13				
AB14				
AB17				
AB18				
AB19				
AB23				
AB24				
AC11				
AC12				
AD11				
AD12				
C32				
J10				
K10				
K9				
L16				
L17				
L18				
L19				
L20				
M10				
M11				
M12				
M16				

Table 6. Power/ground pins (continued)

Ball	Assignment	Voltage	Type	Description
M17	VDD1V2	1.2	Digital	Digital power 1.2 V core power
M18				
M19				
M9				
N11				
N12				
P23				
R23				
T23				
U23				
U24				
V23				
V24				
W11				
W12				
Y11				
Y12				
Digital 1.8 V				
AE1	VDD1V8_297J	1.8	Digital	Digital core supply 1.8 V
AK1				
AK2				
Ak3				

8.3 System

Table 7. System pins

Pin	Assignment	I/O	Voltage	Description	Comments
J27	NOTRESETIN	I	3.3	System input power-on reset	System reset
G27	WDOGRSTOUT	O	3.3	System reset-out (from System reset-in or Internal Watchdog timer reset)	
H26	NOTASEBRK	I/O	3.3	ST40 debugger breakpoint	CPUs debug
F29	TRIGGERIN	I	3.3	ST231 debugger controller in	
J25	TRIGGEROUT	O	3.3	ST231 debugger controller out	
E30	SYSITRQ[0]	I/O	3.3	Interrupt line	Interrupts
E29	SYSITRQ[1]				
H28	SYSITRQ[2]				
D31	SYSITRQ[3]				
F30	NMI	I	3.3	Nonmaskable interrupt	
F28	SYSCLKINALT	I	3.3	2nd system alternate clock (30 MHz) with external VCXO	
D30	SYSCLKOUT	O	3.3	Programmable output clock for debug	
AL23	SYSCLKIN	I	2.5	30 MHz oscillator (USB/SATA) with internal VCXO	
AM23	SYSCLKOSC	O	2.5		
N28	GND_SENSE	A	-	Ground voltage sense	
N29	VDD_SENSE	A	-	Voltage sense	

8.4 JTAG

Table 8. JTAG pins

Pin	Assignment	I/O	Voltage	Description	Comments
H11	TDI	I	3.3	CPUs debug port and TAP data input	TCK and TDO have internal pull-up/pull-down disabled, rest have pull-up.
B10	TMS	I	3.3	CPUs debug port and TAP mode select	
A10	TCK	I	3.3	CPUs debug port and TAP clock	
E10	NOTTRST	I	3.3	CPUs debug port and TAP logic reset	
C10	TDO	O	3.3	CPUs debug port and TAP data output	

8.5 Transport interface

This transport interface is an alternative to the PIO bits. By default, the PIO is bypassed. To enable the transport interface, the PIO setting must be done at boot.

Note: The parallel/serial mode selection is done by selecting the TSmerger channel.

Table 9. Parallel mode transport pins

Signal	I/O	Voltage	PIO	Description	Comments
TSIN0BYTECLK	I/O	3.3	PIO13[5]	TSIN0 control signals	
TSIN0BYTECLKVALID	I/O	3.3	PIO13[6]		
TSIN0ERROR	I/O	3.3	PIO13[7]		
TSIN0PACKETCLK	I/O	3.3	PIO14[0]		
TSIN0DATA[0]	I/O	3.3	PIO14[7]	TSIN0 parallel data	
TSIN0DATA[1]			PIO14[6]		
TSIN0DATA[2]			PIO14[5]		
TSIN0DATA[3]			PIO14[4]		
TSIN0DATA[4]			PIO14[3]		
TSIN0DATA[5]			PIO14[2]		
TSIN0DATA[6]			PIO14[1]		
TSIN0DATA[7]			PIO13[4]		
TSIN1BYTECLK	I	3.3	PIO12[1]/PIO15[1]	TSIN1 control signals	
TSIN1BYTECLKVALID	I	3.3	PIO12[2]/PIO15[2]		
TSIN1ERROR	I	3.3	PIO12[3]/PIO15[3]		
TSIN1PACKETCLK	I	3.3	PIO12[4]/PIO15[0]		
TSIN1DATA[0]	I	3.3	PIO13[3]	TSIN1 parallel data	
TSIN1DATA[1]			PIO13[2]		
TSIN1DATA[2]			PIO13[1]		
TSIN1DATA[3]			PIO13[0]		
TSIN1DATA[4]			PIO12[7]		
TSIN1DATA[5]			PIO12[6]		
TSIN1DATA[6]			PIO12[5]		
TSIN1DATA[7]			PIO12[0]/PIO15[4]		

Table 9. Parallel mode transport pins (continued)

Signal	I/O	Voltage	PIO	Description	Comments
TSIN2BYTECLK	I	3.3	PIO6[1], PIO14[2]	TSIN2 control signals	
TSIN2BYTECLKVALID	I	3.3	PIO6[2], PIO14[3]		
TSIN2ERROR	I	3.3	PIO6[3], PIO14[4]		
TSIN2PACKETCLK	I	3.3	PIO6[4], PIO14[5]		
TSIN2DATA[0]	I	3.3	PIO7[3]	TSIN2 parallel data	
TSIN2DATA[1]			PIO7[2]		
TSIN2DATA[2]			PIO7[1]		
TSIN2DATA[3]			PIO7[0]		
TSIN2DATA[4]			PIO6[7]		
TSIN2DATA[5]			PIO6[6]		
TSIN2DATA[6]			PIO6[5]		
TSIN2DATA[7]			PIO6[0], PIO14[1]		
TSIN3BYTECLK	I	3.3	PIO12[6]	TSIN3 control signals	
TSIN3BYTECLKVALID	I	3.3	PIO12[7]		
TSIN3ERROR	I	3.3	PIO13[0]		
TSIN3PACKETCLK	I	3.3	PIO13[1]		

Table 10. Serial mode transport pins

Signal	I/O	Voltage	PIO	Description	Comments
TSIN0SER/DATA[7]	I	3.3	PIO13[4]	TSIN0 serial data	
TSIN1SER/DATA[7]	I	3.3	PIO12[0]/PIO15[4]	TSIN1 serial data	
TSIN2SER/DATA[7]	I	3.3	PIO6[0]/ PIO14[1]	TSIN2 serial data	
TSIN3SER/DATA[7	I	3.3	PIO12[5]	TSIN3 serial data	
TSOUTSER/DATA[7]	O	3.3	PIO12[0]	TSOUT serial data	

Table 11. 1394OUT mode transport pins

Signal	I/O	Voltage	PIO	Description	Comments
TSOUTBYTECLK	O	3.3	PIO12[1]	TSOUT control signals	
TSOUTBYTECLKVALID	O	3.3	PIO12[2]		
TSOUTERROR	O	3.3	PIO12[3]		
TSOUTPACKETCLK	O	3.3	PIO12[4]		
TSOUTDATA[0]	O	3.3	PIO13[3]	TSOUT parallel data	
TSOUTDATA[1]			PIO13[2]		
TSOUTDATA[2]			PIO13[1]		
TSOUTDATA[3]			PIO13[0]		
TSOUTDATA[4]			PIO12[7]		
TSOUTDATA[5]			PIO12[6]		
TSOUTDATA[6]			PIO12[5]		

8.6 Display analog output interface

Table 12. Display analog output pins

Pin	Assignment	I/O	Voltage (1)	Description	Comments
AJ31	VIDA0_ROUT	O	-	Analog main display - red output	Connect an external 140 Ω 1% resistor between these pins and analog ground.
AJ32	VIDA0_GOUT	O	-	Analog main display -green output	
AK32	VIDA0_BOUT	O	-	Analog main display - blue output	
AL31	VIDA0_REXT	-	-	VDAC0 external resistor interface	Connect an external 7.81 kΩ 1% resistor between each of these pins
AF28	VIDA1_COUT	O	-	Analog auxiliary display - chrominance output	Connect an external 140 Ω 1% resistor between these pins and analog ground.
AF30	VIDA1_CVOUT	O	-	Analog auxiliary display - CVBS output	
AF29	VIDA1_YOUT	O	-	Analog auxiliary display - luminance output	
AG29	VIDA1_REXT	-	-	VDAC1 external resistor interface	Connect an external 7.81 kΩ 1% resistor between each of these pins
AK31	VIDA0_MASSQUIET	-	-	Analog ground connection	It must be connected to noiseless board analog ground because it is sensitive pin for DAC output signal performance.
AL32	VIDA0_IDUMP	O	-	Current return path for the DAC output	It is tied to PCB ground plane.

Table 12. Display analog output pins (continued)

Pin	Assignment	I/O	Voltage (1)	Description	Comments
AG28	VIDA1_MASSQUIET	-	-	Analog ground connection	It must be connected to noiseless board analog ground because it is sensitive pin for DAC output signal performance
AG30	VIDA1_IDUMP	O	-	Current return path for the DAC output	It is tied to PCB ground plane

1. For voltage values, please refer *Section 19.4: Triple HD video DACs on page 344*.

8.7 HDMI interface

Table 13. HDMI pins

Pin	Assignment	I/O	Voltage(1)	Description	Comments
AK27	TMDSTXCP	O	-	TMDS Control plus	
AJ27	TMDSTXCN	O	-	TMDS Control minus	
AK28	TMDSTX0P	O	-	TMDS Data0 plus	
AJ28	TMDSTX0N	O	-	TMDS Data0 minus	
AL29	TMDSTX1P	O	-	TMDS Data1 plus	
AK29	TMDSTX1N	O	-	TMDS Data1 minus	
AM30	TMDSTX2P	O	-	TMDS Data2 plus	
AL30	TMDSTX2N	O	-	TMDS Data2 minus	
AL26	TMDSREF	-	-	TMDS voltage reference	Used by compensation cell to determine the current drive of output buffers. Pulled up externally to 3.3 V using a 50 Ω resistor.
AK26	HDMI_CEC	I/O	-	HDMI CEC line	

1. For voltage values, please contact your local ST representative to provide you specific internal document.

HDMI pins as PIO alternates

Signal	I/O	Voltage(1)	Description	Comments
HDMI_PLUGIN	I	-	HDMI HOT PLUG detection input	PIO9[7]

8.8 Audio digital interface

For audio digital pins, refer to PIO10 and PIO11 alternate functions in *Alternate functions on PIO*.

8.9 Audio analog interface

Table 14. Audio analog pins

Pin	Assignment	I/O	Voltage (1)	Description	Comments
AK16	AUDA_LEFTOUTN	O	-	DAC left-channel negative differential current output	
AK17	AUDA_LEFTOUTP	O	-	DAC left-channel positive differential current output	
AL16	AUDA_RIGHTOUTN	O	-	DAC right-channel negative differential current output	
AM16	AUDA_RIGHTOUTP	O	-	DAC right-channel positive differential current output	
AM18	AUDA_VBGOUT	O		DAC output bandgap voltage	
AK18	AUDA_IREF	-	-	DAC output reference current	Connect an external 575 Ω 1% resistor to AUDA_AGND2V5
AL18	AUDA_GNDAS			Analog ground	

1. For voltage values, please refer *Section 19.3: Audio DAC on page 343*.

8.10 Serial ATA interface

Table 15. SATA pins

Pin	Assignment	I/O	Voltage (1)	Description	Comments
AJ21	SATATXP0	O	-	SATA transmit plus	
AK21	SATATXN0	O	-	SATA transmit minus	
AL19	SATARXP0	I	-	SATA receive plus	
AK19	SATARXN0	I	-	SATA receive minus	
AL22	SATAREF	I/O	-	SATA external reference	It is an external 475 Ω resistor with the other end connected to AF18 pin (SATAVDD_PLL).

1. For voltage values, please refer *Section 19.7: SATA PHY electrical characteristics on page 348*.

8.11 FDMA interface

Table 16. FDMA pins

Pin	Assignment	I/O	Voltage	Description	Comments
M26	FDMAREQ[0]	I/O	3.3	FDMA request	
N27	FDMAREQ[1]	I/O	3.3	FDMA request	
K26	FDMAREQ[2]	I/O	3.3	FDMA request	
L25	FDMAREQ[3]	I/O	3.3	FDMA request	

8.12 Programmable inputs/outputs (PIOs)

Note: All PIO pins are rated at 4 mA sink/source.

Table 17. PIO pins

Pin	Assignment	I/O	Voltage	Description
AA27	PIO0[0]	I/O	3.3	Programmable input/output bank0
AB28	PIO0[1]			
AC27	PIO0[2]			
V27	PIO0[3]			
AE27	PIO0[4]			
AB26	PIO0[5]			
AC25	PIO0[6]			
AD28	PIO0[7]			
AD30	PIO1[0]	I/O	3.3	Programmable input/output bank1
AB30	PIO1[1]			
AD26	PIO1[2]			
AD31	PIO1[3]			
W29	PIO1[4]			
AC29	PIO1[5]			
W28	PIO1[6]			
AC30	PIO1[7]			

Table 17. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
AA29	PIO2[0]	I/O	3.3	Programmable input/output bank2
AA30	PIO2[1]			
AA31	PIO2[2]			
Y28	PIO2[3]			
Y29	PIO2[4]			
AB32	PIO2[5]			
Y30	PIO2[6]			
AB31	PIO2[7]			
AE31	PIO3[0]	I/O	3.3	Programmable input/output bank3
AE29	PIO3[1]			
AD32	PIO3[2]			
AE30	PIO3[3]			
R28	PIO3[4]			
U30	PIO3[5]			
U31	PIO3[6]			
U32	PIO3[7]			
R32	PIO4[0]	I/O	3.3	Programmable input/output bank4
U28	PIO4[1]			
V30	PIO4[2]			
V29	PIO4[3]			
R26	PIO4[4]			
R31	PIO4[5]			
R30	PIO4[6]			
T27	PIO4[7]			
P31	PIO5[0]	I/O	3.3	Programmable input/output bank5
P29	PIO5[1]			
P27	PIO5[2]			
N26	PIO5[3]			
V31	PIO5[4]			
P30	PIO5[5]			
T30	PIO5[6]			
T29	PIO5[7]			

Table 17. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
F9	PIO6[0]	I/O	3.3	Programmable input/output bank6
F11	PIO6[1]			
C8	PIO6[2]			
C9	PIO6[3]			
E8	PIO6[4]			
D7	PIO6[5]			
G10	PIO6[6]			
H9	PIO6[7]			
D9	PIO7[0]	I/O	3.3	Programmable input/output bank7
A8	PIO7[1]			
B8	PIO7[2]			
C7	PIO7[3]			
AJ13	PIO7[4]			
AH13	PIO7[5]			
AJ12	PIO7[6]			
AL11	PIO7[7]			
AM11	PIO8[0]	I/O	3.3	Programmable input/output bank8
AK11	PIO8[1]			
AL12	PIO8[2]			
AE12	PIO8[3]			
AF13	PIO8[4]			
AK13	PIO8[5]			
AH14	PIO8[6]			
AJ14	PIO8[7]			
AJ15	PIO9[0]	I/O	3.3	Programmable input/output bank9
AL15	PIO9[1]			
AK12	PIO9[2]			
AF11	PIO9[3]			
AH11	PIO9[4]			
AK15	PIO9[5]			
AG12	PIO9[6]			
L30	PIO9[7]			

Table 17. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
AD15	PIO10[0]	I/O	3.3	Programmable input/output bank10
AH16	PIO10[1]			
AF16	PIO10[2]			
AE15	PIO10[3]			
AF14	PIO10[4]			
AE17	PIO10[5]			
AG15	PIO10[6]			
AE13	PIO10[7]			
AG17	PIO11[0]	I/O	3.3	Programmable input/output bank11
AG14	PIO11[1]			
L31	PIO11[2]			
J30	PIO11[3]			
K30	PIO11[4]			
K32	PIO11[5]			
K31	PIO11[6]			
H30	PIO11[7]			
C4	PIO12[0]	I/O	3.3	Programmable input/output bank12
B3	PIO12[1]			
B4	PIO12[2]			
D4	PIO12[3]			
E6	PIO12[4]			
C5	PIO12[5]			
D5	PIO12[6]			
C6	PIO12[7]			
G8	PIO13[0]	I/O	3.3	Programmable input/output bank13
B7	PIO13[1]			
D6	PIO13[2]			
F7	PIO13[3]			
E3	PIO13[4]			
F3	PIO13[5]			
E2	PIO13[6]			
E5	PIO13[7]			

Table 17. PIO pins (continued)

Pin	Assignment	I/O	Voltage	Description
E4	PIO14[0]	I/O	3.3	Programmable input/output bank14
D1	PIO14[1]			
D3	PIO14[2]			
D2	PIO14[3]			
C2	PIO14[4]			
C1	PIO14[5]			
C3	PIO14[6]			
A3	PIO14[7]			
AA3	PIO15[0]	I/O	3.3	Programmable input/output bank15
AA4	PIO15[1]			
AA5	PIO15[2]			
W4	PIO15[3]			
AB8	PIO15[4]			
AA7	PIO15[5]			
M29	PIO15[6]			
M30	PIO15[7]			
H32	PIO16[0]	I/O	3.3	Programmable input/output bank16
H31	PIO16[1]			
G29	PIO16[2]			
G31	PIO16[3]			
G30	PIO16[4]			
L29	PIO16[5]			
M28	PIO16[6]			
J29	PIO16[7]			

8.13 External memory interface (EMI)

Note: The various configurations of the EMI (SRAM, Flash, PCI) are shown in Section 9.4.

Table 18. EMI pins

Pin	Assignment	I/O	Voltage	Description	Comments
H3	NOTEMICSA	I/O	3.3	Peripheral chip select A	
F4	NOTEMICSB	I/O	3.3	Peripheral chip select B	
G3	NOTEMICSC	I/O	3.3	Peripheral chip select C	
H6	NOTEMICSD	I/O	3.3	Peripheral chip select D	
K8	NOTEMICSE	I/O	3.3	Peripheral chip select E	
L7	NOTEMIBE[0]	I/O	3.3	External device databus byte enable	
R6	NOTEMIBE[1]				
L1	NOTEMIOE	O2	3.3	External device output enable	
T5	NOTEMILBA	I/O	3.3	Flash device load burst address	
H8	NOTEMIBAA	I/O	3.3	Flash burst address advanced	
J7	EMITREADYORWAIT	I/O	3.3	External memory device target ready indicator	
L2	EMIRDNOTWR	I/O	3.3	External read/write access indicator. Common to all devices.	
W6	EMIDATA[0]	I/O	3.3	External common data bus	
V2	EMIDATA[1]				
U6	EMIDATA[2]				
V3	EMIDATA[3]				
U3	EMIDATA[4]				
W8	EMIDATA[5]				
T3	EMIDATA[6]				
V5	EMIDATA[7]				
V7	EMIDATA[8]				
W3	EMIDATA[9]				
W2	EMIDATA[10]				
U4	EMIDATA[11]				
V1	EMIDATA[12]				
T1	EMIDATA[13]				
T2	EMIDATA[14]				
R3	EMIDATA[15]				

Table 18. EMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
H2	EMIADDR[1]				
H4	EMIADDR[2]				
J1	EMIADDR[3]				
K4	EMIADDR[4]				
J3	EMIADDR[5]				
J2	EMIADDR[6]				
K3	EMIADDR[7]				
L3	EMIADDR[8]				
M2	EMIADDR[9]				
M4	EMIADDR[10]				
K6	EMIADDR[11]				
J5	EMIADDR[12]				
N3	EMIADDR[13]	O	3.3	External common address bus	23-bit address(1)
M3	EMIADDR[14]				
N4	EMIADDR[15]				
P7	EMIADDR[16]				
R4	EMIADDR[17]				
L5	EMIADDR[18]				
T7	EMIADDR[19]				
P6	EMIADDR[20]				
M8	EMIADDR[21]				
N5	EMIADDR[22]				
P5	EMIADDR[23]				
P4	EMIADDR[24]				
R2	EMIADDR[25]				
G4	EMIFLASHCLK	I/O	3.3	Flash clock	
M6	EMIBUSREQ	I/O	3.3	Bus access request	For master/slave configuration
R8	EMIBUSGNT	I/O	3.3	Bus access grant	
U8	NANDWAIT		3.3		

1. No pull-up. External resistors to define mode at boot.

Table 19. EMI pins as PIO alternates

Signal	I/O	Voltage	Description	Comments
EMI_SS_BUS_FREE_ACCESSPEND/ EMI_SS_BUS_FREE_OUT	I	3.3	Access Pending Flag	PIO15[2]
SPIBOOT_DATA_IN	I	3.3	SPI boot data in	PIO15[3]
SPIBOOT_DATA_OUT	O	3.3	SPI boot data out	PIO15[1]
SPIBOOT_CLOCK	O	3.3	SPI boot clock	PIO15[0]
SPIBOOT_CS	O	3.3	SPI boot chip select	PIO15[2]

Table 20. PCI pins as PIO alternates

Signal	I/O	Voltage	Description	Comments
PCI_LOCK_IN	I	3.3	PCI lock function	PIO7[0], PIO15[5]
PCI_INT_FROM_DEVICE[0]	I	3.3	PCI interrupt input (when host)	PIO6[0], PIO15[3]
PCI_INT_FROM_DEVICE[1]	I	3.3	PCI interrupt input (when host)	PIO6[1]
PCI_INT_FROM_DEVICE[2]	I	3.3	PCI interrupt input (when host)	PIO6[2]
PCI_INT_TO_HOST	O	3.3	PCI interrupt output (when device)	PIO6[0], PIO15[3]
PCI_RESETN_FROM_HOST_TO_DEVICE	I	3.3	PCI reset input (when host)	PIO15[7]
PCI_SYSTEM_ERROR	O	3.3	PCI error flag	PIO15[4]
PCI_PME_IN	I	3.3	PCI PME function	PIO15[6]
PCI_BUS_GNT[1]	O	3.3	Bus access grant	PIO7[1]
PCI_BUS_GNT[2]	O	3.3	Bus access grant	PIO7[2]
PCI_BUS_REQ[1]	I	3.3	Bus access req	PIO6[5]
PCI_BUS_REQ[2]	I	3.3	Bus access req	PIO6[6]

8.14 Local memory interface

Table 21. LMI pins

Pin	Assignment	I/O	Voltage	Description	Comments
B21	LMICLK[0]	O	1.8	Clock to DDR0	
C21	NOTLMICLK[0]	O	1.8	Inverted clock to DDR0	
E12	LMICLK[1]	O	1.8	Clock to DDR1	
C11	NOTLMICLK[1]	O	1.8	Inverted clock to DDR1	
F14	NOTLMICS[0]	O	1.8	Chip select0	
F13	NOTLMICS[1]	O	1.8	Chip select1	

Table 21. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
H13	NOTLMIRAS	O	1.8	Row address strobe	
H14	NOTLMICAS	O	1.8	Column address strobe	
H25	NOTLMIWE	O	1.8	Write enable	
E15	LMIADDR[0]	O	1.8	Address	
F23	LMIADDR[1]				
G15	LMIADDR[2]				
E22	LMIADDR[3]				
F16	LMIADDR[4]				
G22	LMIADDR[5]				
H16	LMIADDR[6]				
F21	LMIADDR[7]				
E17	LMIADDR[8]				
H21	LMIADDR[9]				
H23	LMIADDR[10]				
G17	LMIADDR[11]				
G20	LMIADDR[12]				
F18	LMIADDR[13]				

Table 21. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
B22	LMIDATA[0]	I/O	1.8	Bidirectional data bus	
B29	LMIDATA[1]				
C23	LMIDATA[2]				
C29	LMIDATA[3]				
A30	LMIDATA[4]				
A22	LMIDATA[5]				
A29	LMIDATA[6]				
C22	LMIDATA[7]				
C25	LMIDATA[8]				
E27	LMIDATA[9]				
B25	LMIDATA[10]				
C28	LMIDATA[11]				
B28	LMIDATA[12]				
B24	LMIDATA[13]				
D28	LMIDATA[14]				
D25	LMIDATA[15]				
D12	LMIDATA[16]				
D19	LMIDATA[17]				
D13	LMIDATA[18]				
D20	LMIDATA[19]				
C20	LMIDATA[20]				
C12	LMIDATA[21]				
E19	LMIDATA[22]				
E13	LMIDATA[23]				
C15	LMIDATA[24]				
B17	LMIDATA[25]				
A15	LMIDATA[26]				
C18	LMIDATA[27]				
B18	LMIDATA[28]				
B15	LMIDATA[29]				
D18	LMIDATA[30]				
C14	LMIDATA[31]				

Table 21. LMI pins (continued)

Pin	Assignment	I/O	Voltage	Description	Comments
D27	LMIDATAMASK[0]	O	1.8	Data write mask	
C27	LMIDATAMASK[1]				
C17	LMIDATAMASK[2]				
A17	LMIDATAMASK[3]				
C30	LMIVREF[0]	I	1.8	SSTL reference voltage0	
G12	LMIVREF[1]	I	1.8	SSTL reference voltage1	
G26	LMICLKEN[0]	O	1.8	Memory clock enable	
G13	LMICLKEN[1]	O	1.8	Memory clock enable	
H18	ODT[0]	O	1.8	Memory on-die termination	
C31	ODT[1]	O	1.8	Memory on-die termination	
B30	LMI_COMP_REF	A	-	LMI compensation external resistor	
A31	LMI_COMP_GND	A	-	LMI compensation ground	
J14	LMIDUMMY[0]	A	-	LMI PCB track delay estimator	
K14	LMIDUMMY[1]	A	-	LMI PCB track delay estimator	
D23	LMIDQS[0]	I/O	1.8	Write/read data strobe	
D26	LMIDQS[1]				
D14	LMIDQS[2]				
D16	LMIDQS[3]				
C24	LMIDQSN[0]	I/O	1.8	Write/read data strobe	
C26	LMIDQSN[1]				
B14	LMIDQSN[2]				
C16	LMIDQSN[3]				
E20	LMIBA[0]	O	1.8	Bank select	
D21	LMIBA[1]				
A24	LMIBA[2]				

8.15 Front end

Table 22. Front-end interface pins

Pin	Assignment	Type	Voltage	Description
AGC interface				
AM9	AGC1	O(1)		First sigma-delta output for AGC in dual AGC application (Open drain programmable)
AL9	AGC2	O(1)		Second sigma-delta output for AGC in dual AGC application (Open drain programmable)

Table 22. Front-end interface pins (continued)

Pin	Assignment	Type	Voltage	Description
Analog interface				
AM4	INM	Analog	1.5	Analog differential input
AL5	INP	Analog	1.5	Analog differential input
AL4	IREF	Analog		ADC reference current
AK5	REFM	Analog		
AM3	REFP	Analog		
Clocks and resets				
AE8	NOT_RESET	I		Hardware reset – active low
AK8	XTAL_I	I		Crystal oscillator input/external clock
AL8	XTAL_O	O		Crystal oscillator output
AH9	AUX_CLK	I/O		Auxiliary clock derived from CKEXT by division (integer ratio)
I²C interface				
AE10	SCL	I		Serial clock
AK6	SCLT	O		SCL tuner (open drain)
AG10	SDA	I/O		Serial data (open drain)
AK7	SDAT	I/O		SDA tuner (open drain)
Interrupt and status pins				
AH4	IT	I/O(1)		Maskable interrupt triggered by a lock or unlock event in the de-interleaver sync detector or in the descrambler sync detector or by channel scanning (open-drain programmable)
AG3	LOCK	I/O(1)		Lock indicator (open-drain programmable)
Test interface				
AF2	TEST[0]	I		Reserved for test. Tie to ground for normal use.
AE2	TEST[1]	I		Reserved for test. Tie to ground for normal use.
AH3	TEST[2]	I		Reserved for test. Tie to ground for normal use.
AF4	TEST[3]	I		Reserved for test. Tie to ground for normal use.
AG4	TEST[4]	I		Reserved for test. Tie to ground for normal use.
AF3	TEST[5]	I		Reserved for test. Tie to ground for normal use.
AK4	TEST_MODE	I		Reserved for test. Tie to ground for normal use.
AF9	CK_TEST	I		Test clock. Tie to ground for normal use.

1. Open-drain programmable. Open-drain programmable outputs can be configured by software to behave either as normal CMOS push-pull outputs, or as open-drain outputs.

8.16 Front-end transport stream output

Table 23. Front-end transport stream output pins

Pin	Assignment	I/O	Voltage	Description
AC2	CLK_OUT	O		MPEG byte or bit clock
AD3	D_NOT_P	O		MPEG data valid/parity
AB6	DATA0	O		Parallel MPEG data bits [0:6]
AC7	DATA1	O		
AC5	DATA2	O		
AD8	DATA3	O		
AD6	DATA4	O		
AE5	DATA5	O		
AE7	DATA6	O		
AC3	DATA7	O		Serial MPEG data or parallel MPEG data (bit 7)
AD4	ERROR	O		MPEG packet error
AC1	STR_OUT	O		MPEG first byte sync

Note: All pins in the above table are tri-state capable outputs. The tri-state capable outputs can be disabled (high impedance) by software.

8.17 Ethernet

Note: This Ethernet interface is an alternative of PIO bits. By default, the PIO is selected. To enable the Ethernet interface, the PIO setting must be done at boot (refer to Chapter 21: Alternate functions on PIO on page 364 for programming details).

Table 24. MII interface pin mapping

Signal	I/O	Voltage	PIO mapping	Description	Comments
MII_TXCLK	I	3.3	PIO9[2]	Timing reference for ETH_MII_TXEN and ETH_MII_TXD	
MII_TXEN	O	3.3	PIO8[2]	Indicates that the MAC is presenting nibbles on the MII for transmission	
MII_TXD[3]	O	3.3	PIO8[1]	Data signals driven by the MAC	
MII_TXD[2]	O	3.3	PIO8[0]		
MII_TXD[1]	O	3.3	PIO7[7]		
MII_TXD[0]	O	3.3	PIO7[6]		
MII_RXCLK	I	3.3	PIO8[5]	Timing reference for ETH_MII_RXDV, ETH_MII_RXER, and ETH_MII_RXD	

Table 24. MII interface pin mapping (continued)

Signal	I/O	Voltage	PIO mapping	Description	Comments
MII_RXDV	I	3.3	PIO7[4]	Receive data valid	
MII_RXER	I	3.3	PIO7[5]	Receive error	
MII_RXD[3]	I	3.3	PIO9[1]	Data signals that transition synchronously with respect to ETH_MII_RXCLK	
MII_RXD[2]	I	3.3	PIO9[0]		
MII_RXD[1]	I	3.3	PIO8[7]		
MII_RXD[0]	I	3.3	PIO8[6]		
MII_CRS	I	3.3	PIO9[4]	Asserted when either the transmit or receive medium is not idle	
MII_COL	I	3.3	PIO9[3]	Asserted on detection of a collision on the medium	
MII_MDC	O	3.3	PIO8[4]	Timing reference for transfer of information on the ETH_MII_MDIO signals	
MII_MDIO	I/O	3.3	PIO8[3]	Management Data input/output signal	
MII_MDINT	I	3.3	PIO9[6]	Management data interrupt from PHY	
MII_PHYCLK	O	3.3	PIO9[5]	PHY clock	

Table 25. RMII interface pin mapping

Signal	I/O	Voltage	PIO mapping	Description	Comments
RMII_TXEN	O	3.3	PIO8[2]	Indicates that the MAC is presenting nibbles on the MII for transmission	
RMII_TXD[1]	O	3.3	PIO7[7]	Data signals driven by the MAC	
RMII_TXD[0]	O	3.3	PIO7[6]		
RMII_RXD[1]	I	3.3	PIO8[7]	Data signals received by the MAC	
RMII_RXD[0]	I	3.3	PIO8[6]		
RMII_CRSDV	I	3.3	PIO7[4]	Asserted when either the transmit or receive medium is not idle	
RMII_RXER	I	3.3	PIO7[5]		
RMII_MDC	O	3.3	PIO8[4]	Timing reference for transfer of information on the ETH_MII_MDIO signals	
RMII_MDIO	I/O	3.3	PIO8[3]	Management Data input/output signal	
RMII_MDINT	I	3.3	PIO9[6]	Management data interrupt from PHY	
RMII_REFCLK	I/O	3.3	PIO9[5]	Reference clock	

8.18 USB 2.0 interface

Table 26. USB pins

Pin	Assignment	I/O	Voltage	Description	Comments
AM25	USB1DM	I/O	2.5	USB receive minus	
AL25	USB1DP	I/O	2.5	USB receive plus	
AH23	USB2DM	I/O	2.5	USB receive minus	
AG22	USB2DP	I/O	2.5	USB receive plus	
AK24	REXT(1)			External resistor	1.5 kΩ resistor

1. REXT is the USB reference USBREF.

Table 27. USB pin mapping

Signal	I/O	Voltage	Description	Assignment
USB1_PRT_OVCUR	I	3.3	USB 2.0 interface 1	PIO4[4], PIO12[5]
USB1_PRT_PWR	O	3.3		PIO4[5], PIO12[6]
USB2_PRT_OVCUR	I	3.3	USB 2.0 interface 2	PIO4[6]/PIO14[6]
USB2_PRT_PWR	O	3.3		PIO4[7]/PIO14[7]

8.19 Peripherals

8.19.1 DAA

Table 28. DAA pins

Pin	Assignment	I/O	Voltage	Description	Comments
K28	DAA_C1A	I/O	3.3	DAA differential data(1)	
L27	DAA_C2A	I/O	3.3	DAA differential data(2)	

1. ISO-Link capacitors C1 and C2, (33 pF) should be as close to the line-side device as possible.

2. After satisfying the above, C1 and C2 should be as close to the embedded system-side DAA module as possible and no further than 6 inches away.

8.19.2 Asynchronous serial controller (ASC)

Table 29. ASC / SCIF pins

Signal	I/O	Voltage	Description	Comments
ASC0				
UART0_RXD	I	3.3	ASC 0 receive signal	PIO0[1]

Table 29. ASC / SCIF pins (continued)

Signal	I/O	Voltage	Description	Comments
UART0_TXD	O	3.3	ASC 0 transmit signal	PIO0[0]
UART0_CTS	I	3.3	ASC 0 clear to send signal	PIO0[4]
UART0_RTS	O	3.3	ASC 0 request to send signal	PIO0[3]
UART0_NOT_OE	O	3.3		PIO0[2]
ASC1				
UART1_RXD	I	3.3	ASC 1 receive signal	PIO1[1]
UART1_TXD	O	3.3	ASC 1 transmit signal	PIO1[0]
UART1_CTS	I	3.3	ASC 1 clear to send signal	PIO1[4]
UART1_RTS	O	3.3	ASC 1 request to send signal	PIO1[3]
ASC2				
UART2_RXD	I	3.3	ASC 2 receive signal	PIO12[1], PIO4[1]
UART2_TXD	O	3.3	ASC 2 transmit signal	PIO12[0], PIO4[0]
UART2_CTS	I	3.3	ASC 2 clear to send signal	PIO12[2], PIO4[2]
UART2_RTS	O	3.3	ASC 2 request to send signal	PIO12[3], PIO4[3]
ASC3				
UART3_RXD	I	3.3	ASC 3 receive signal	PIO5[1]
UART3_TXD	O	3.3	ASC 3 transmit signal	PIO5[0]
UART3_CTS	I	3.3	ASC 3 clear to send signal	PIO5[3]
UART3_RTS	O	3.3	ASC 3 request to send signal	PIO5[2]

8.19.3 Infrared transmitter/receiver

Table 30. Infrared transmitter/receiver pins

Signal	I/O	Voltage	Description	Comments
IRB_IR_IN	I	3.3	IR data input	PIO3[0]
IRB_UHF_IN	I	3.3	UHF data input	PIO3[1]
IRB_IR_DATAOUT	O	3.3	IR data output	PIO3[2]
IRB_IR_DATAOUT_OD	O	3.3	IR data output. It is open drain.	PIO3[3]

8.19.4 Modem analog front-end interface (MAFE)

Table 31. MAFE pins

Signal	I/O	Voltage	Description	Comments
MAFE_HC1	O	3.3	Indicates a control/status exchange	PIO1[2]
MAFE_DOUT	O	3.3	Line for serially transmitting samples	PIO1[3]

Table 31. MAFE pins

Signal	I/O	Voltage	Description	Comments
MAFE_DIN	I	3.3	Line for serially receiving samples	PIO1[0]
MAFE_SCLK	I	3.3	Modem system clock	PIO1[1]
MAFE_FS	I	3.3	Start of a sampling period latched on falling edges of SCLK	PIO1[5]

8.19.5 Pulse width modulator (PWM)

Table 32. PWM pins

Signal	I/O	Voltage	Description	Comments
PWM 0				
PWM_OUT0	O	3.3	PWM 0	PIO13[0], PIO4[4]
PWM_CAPTURE_IN0	I			PIO4[3]
PWM 1				
PWM_OUT1	O	3.3	PWM 1	PIO13[1], PIO4[5]
PWM_CAPTURE_IN1	I	3.3		PIO4[7]
PWM_COMPARE_OUT1	O	3.3		PIO4[6]

8.19.6 Smartcard

Table 33. Smartcard pins

Signal	I/O	Voltage	Description	Comments
Smartcard 0				
SC0_EXTCLKIN	I	3.3	External clock	PIO0[2]
SC0_CLKOUT	O	3.3	Clock for Smartcard from 100 MHz system clock	PIO0[3]
SC0_DATAOUT	O	3.3	Serial data output	PIO0[0]
SC0_DATAIN	I	3.3	Serial data input	PIO0[1]
SC0_RESET	O	3.3	Serial data reset	PIO0[4]
SC0_COND_VCC	O	3.3	VCC control flag	PIO0[5]
SC0_COND_VPP	O	3.3	VPP control flag	PIO0[6]
SCO_DETECT	I	3.3	Detection flag	PIO0[7]
Smartcard 1				
SC1_EXTCLKIN	I	3.3	External clock	PIO1[2]
SC1_CLKOUT	O	3.3	Clock for Smartcard from 100MHz system clock	PIO1[3]
SC1_DATAOUT	O	3.3	Serial data output	PIO1[0]

Table 33. Smartcard pins

Signal	I/O	Voltage	Description	Comments
SC1_DATAIN	I	3.3	Serial data input	PIO1[1]
SC1_RESET	O	3.3	Serial data reset	PIO1[4]
SC1_COND_VCC	O	3.3	VCC control flag	PIO1[5]
SC1_COND_VPP	O	3.3	VPP control flag	PIO1[6]
SC1_DETECT	I	3.3	Detection flag	PIO1[7]

8.19.7 Synchronous serial controller (SSC)

Table 34. SSC pins

Signal	I/O	Voltage	Description	Comments
SSC 0				
SSC0_SCL	I/O	3.3	SSC 0 serial clock	PIO2[2]
SSC0_MTSR/SSC0_MRST	I/O	3.3	SSC 0 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[3]
SSC0_MRST	I/O	3.3	SSC 0 data: master receive, slave transmit (full duplex mode)	PIO2[4]
SSC 1				
SSC1_SCL	I/O	3.3	SSC 1 serial clock	PIO2[5]
SSC1_MTSR/SSC1_MRST	I/O	3.3	SSC 1 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[6]
SSC1_MRST	I/O	3.3	SSC 1 data: master receive, slave transmit (full duplex mode)	PIO2[7]
SSC 2				
SSC2_SCL	I/O	3.3	SSC 2 serial clock	PIO3[4], PIO12[0], PIO13[4]
SSC2_MTSR/SSC2_MRST	I/O	3.3	SSC 2 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[0], PIO3[5], PIO12[1], PIO13[5]
SSC 3				
SSC3_SCL	I/O	3.3	SSC 3 serial clock	PIO3[6], PIO13[2], PIO13[6]
SSC3_MTSR/SSC3_MRST	I/O	3.3	SSC3 data: master transmit, slave receive/master receive, slave transmit (half duplex mode for example I^2C)	PIO2[1], PIO3[7], PIO13[3], PIO13[7]

8.19.8 Key Scanner (KS)

Table 35. KS pins

Signal	I/O	Voltage	Description	Comments
KEY_SCAN_OUT[0]	O	3.3	Key Scanner outputs	PIO7[0], PIO5[0]
KEY_SCAN_OUT[1]				PIO7[1], PIO5[1]
KEY_SCAN_OUT[2]				PIO7[2], PIO5[2]
KEY_SCAN_OUT[3]				PIO7[3], PIO5[3]
KEY_SCAN_IN[0]	I	3.3	Key Scanner inputs	PIO5[4]
KEY_SCAN_IN[1]				PIO5[5]
KEY_SCAN_IN[2]				PIO5[6]
KEY_SCAN_IN[3]				PIO5[7]

8.20 Pad reset conditions

Table 36 describes the pad reset conditions.

Table 36. Pad reset conditions

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
System				
SYSCLKIN	I	–	1	–
SYSCLKOSC	I/O	–	0	–
NOTASEBRK	I/O	I	1	Pull-up
TRIGGERIN	I	I	0	Pull-down
TRIGGEROUT	O	O	0	Pull-down
SYSITRQ[3:0]	I/O	I	0	Pull-down
NMI	I	I	0	Pull-down
WDOGRSTOUT	O	O	1	Pull-down
SYSCLKOUT	O	I	1	Pull-down
SYSCLKINALT	I	I	0	Pull-down
FDMAREQ[3:0]	I/O	I	0	–
NOTRESETIN	I	I	1	–
JTAG				
TDI	I	I	0	Pull-up
TMS	I	I	0	Pull-up
TCK	I	I	0	–
NOTTRST	I	I	1	Pull-up
TDO	O	O	1	–
EMI				
NOTEMICSA	I/O	I	1	Pull-up
NOTEMICSB	I/O	I	1	Pull-up
NOTEMICSC	I/O	I	1	Pull-up
NOTEMICSD	I/O	I	1	Pull-up
NOTEMICSE	I/O	I	1	Pull-up
NOTEMIBE[1:0]	I/O	I	1	Pull-up
NOTEMIOE	O	O	1	Pull-up
NOTEMILBA	I/O	I	1	Pull-up
NOTEMIBAA	I/O	I	1	Pull-up

Table 36. Pad reset conditions (continued)

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
EMIREADYORWAIT	I/O	I	0	Pull-down
NANDWAIT	I	I	1	Pull-up
EMIRDNOTWR	I/O	I	1	Pull-up
EMIDATA[15:0]	I/O	I	0	Pull-down
EMIADDR[16:1]	I/O	I	1	Pull-up
EMIADDR[25:17]	I/O	I	1	Pull-up
EMIFLASHCLK	I/O	I	0	Pull-down
EMIBUSREQ	I/O	I	0	Pull-down
EMIBUSGNT	I/O	O	0	Pull-down
PIO				
PIO0[7:0]	I/O	I	1	Weak pull-up
PIO1[7:0]	I/O	I	1	Weak pull-up
PIO2[7:0]	I/O	I	1	Weak pull-up
PIO3[7:0]	I/O	I	1	Weak pull-up
PIO4[7:0]	I/O	I	1	Weak pull-up
PIO5[7:0]	I/O	I	1	Weak pull-up
PIO6[7:0]	I/O	I	1	Weak pull-up
PIO7[7:4]	I/O	I	x	Weak pull-up
PIO7[3:0]	I/O	I	1	Weak pull-up
PIO8[7:6]	I/O	I	x	Weak pull-up
PIO8[5]	I/O	I	1	Weak pull-up
PIO8[4:0]	I/O	I	x	Weak pull-up
PIO9[7]	I/O	I	0	Weak pull-up
PIO9[6]	I/O	I	x	Weak pull-up
PIO9[5:2]	I/O	I	1	Weak pull-up
PIO9[1:0]	I/O	I	x	Weak pull-up
PIO10[7:0]	I/O	I	1	Weak pull-up
PIO11[7:0]	I/O	I	1	Weak pull-up
PIO12[7:0]	I/O	I	1	Weak pull-up
PIO13[7:0]	I/O	I	1	Weak pull-up
PIO14[7:0]	I/O	I	1	Weak pull-up
PIO15[3:0]	I/O	O	0	–

Table 36. Pad reset conditions (continued)

Ball/Signal name	Functional direction	Pad reset conditions		
		I/O	Reset value	Pull up/pull down
PIO15[7:6]	I/O	I	0	Weak pull-up
PIO15[5:4]	I/O	I	1	Weak pull-up
PIO16[7:5]	I/O	I	1	–
PIO16[4:0]	I/O	I	x	Weak pull-up

9 Basic chip operating modes and multiplexing scenarios

The STi7197 has one basic chip operating mode. However, other chip operating modes are supported through pad multiplexing.

Following interfaces include ball multiplexing:

- Ethernet interface, which can support MII and ReducedMII(RMII)
- External memory interface (EMI), valid in several operating modes, attached to various types of devices

9.1 Transport interfaces multiplexing

The PIO multiplexing used for transport interfaces can be configured in the following ways:

- serial transport stream inputs: up to four serial IN (mapping details in *Table 37*)
- parallel transport stream inputs/output: one parallel IN/OUT and two parallel IN (mapping details in *Table 38*)

Table 37. STi7197 Serial Transport Stream inputs mapping

Pin	Parameter	Interface	Details
PIO13[4]	Name	Serial transport stream input 0	TSIN0SER/DATA[7]
	Description		Transport stream0 serial data input
	Direction		I
	Configuration		No configuration is required
PIO13[5]	Name		TSIN0BYTECLK
	Description		Transport stream0 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000 For INPUT selection: No configuration is required
PIO13[6]	Name		TSIN0BYTECLKVALID
	Description		Transport stream0 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[7]	Name		TSIN0ERROR
	Description		Transport stream0 data error input
	Direction		I
	Configuration		No configuration is required
PIO14[0]	Name		TSIN0PACKETCLK
	Description		Transport stream0 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 37. STi7197 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO12[0]/ PIO15[4]	Name	Serial transport stream input 1	TSIN1SER/DATA[7]
	Description		Transport stream1 serial data input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO12[0], *SYSTEM_CONFIG4*[9] = 0 when PIO15[4], *SYSTEM_CONFIG4*[9] = 1
PIO12[1]/ PIO15[1]	Name		TSIN1BYTECLK
	Description		Transport stream1 data clock input/output
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO12[1], *SYSTEM_CONFIG4*[9] = 0 when PIO15[1], *SYSTEM_CONFIG4*[9] = 1
PIO12[2]/ PIO15[2]	Name		TSIN1BYTECLKVALID
	Description		Transport stream1 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO12[2], *SYSTEM_CONFIG4*[9] = 0 when PIO15[2], *SYSTEM_CONFIG4*[9] = 1
PIO12[3]/ PIO15[3]	Name		TSIN1ERROR
	Description		Transport stream1 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO12[3], *SYSTEM_CONFIG4*[9] = 0 when PIO15[3], *SYSTEM_CONFIG4*[9] = 1
PIO12[4]/ PIO15[0]	Name		TSIN1PACKETCLK
	Description		Transport stream1 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO12[4], *SYSTEM_CONFIG4*[9] = 0 when PIO15[0], *SYSTEM_CONFIG4*[9] = 1

Table 37. STi7197 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]/ PIO6[0]	Name	Serial transport stream input 2	TSIN2SER/DATA[7]
	Description		Transport stream2 serial data input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[0], *SYSTEM_CONFIG4*[10] = 0 when PIO14[1], *SYSTEM_CONFIG4*[10] = 1
PIO14[2]/ PIO6[1]	Name		TSIN2BYTECLK
	Description		Transport stream2 data clock input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[1], *SYSTEM_CONFIG4*[10] = 0 when PIO14[2], *SYSTEM_CONFIG4*[10] = 1
PIO14[3]/ PIO6[2]	Name		TSIN2BYTECLKVALID
	Description		Transport stream2 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[2], *SYSTEM_CONFIG4*[10] = 0 when PIO14[3], *SYSTEM_CONFIG4*[10] = 1
PIO14[4]/ PIO6[3]	Name		TSIN2ERROR
	Description		Transport stream2 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[3], *SYSTEM_CONFIG4*[10] = 0 when PIO14[4], *SYSTEM_CONFIG4*[10] = 1
PIO14[5]/ PIO6[4]	Name		TSIN2PACKETCLK
	Description		Transport stream2 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[4], *SYSTEM_CONFIG4*[10] = 0 when PIO14[5], *SYSTEM_CONFIG4*[10] = 1

Table 37. STi7197 Serial Transport Stream inputs mapping (continued)

Pin	Parameter	Interface	Details
PIO12[5]	Name	Serial transport stream Input 3	TSIN3SER/DATA[7]
	Description		Transport stream3 serial data input
	Direction		I
	Configuration		No configuration is required
PIO12[6]	Name		TSIN3BYTECLK
	Description		Transport stream3 data clock input/output
	Direction		I
	Configuration		No configuration is required
PIO12[7]	Name		TSIN3BYTECLKVALID
	Description		Transport STREAM3 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[0]	Name		TSIN3ERROR
	Description		Transport stream3 data error input
	Direction		I
	Configuration		No configuration is required
PIO13[1]	Name		TSIN3PACKETCLK
	Description		Transport stream3 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 38. STi7197 Parallel Transport Stream inputs/output mapping

Pin	Parameter	Interface	Details
PIO13[4]	Name	Parallel transport stream input 0	TSIN0DATA[7]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO13[5]	Name		TSIN0BYTECLK
	Description		Transport stream0 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000
PIO13[6]	Name		TSIN0BYTECLKVALID
	Description		Transport stream0 data valid input
	Direction		I
	Configuration		No configuration is required
PIO13[7]	Name		TSIN0ERROR
	Description		Transport stream0 data error input
	Direction		I
	Configuration		No configuration is required
PIO14[0]	Name		TSIN0PACKETCLK
	Description		Transport stream0 packet clock input
	Direction		I
	Configuration		No configuration is required

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]	Name	Parallel transport stream input 0	TSIN0DATA[6]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[2]	Name		TSIN0DATA[5]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[3]	Name		TSIN0DATA[4]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[4]	Name		TSIN0DATA[3]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[5]	Name		TSIN0DATA[2]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[6]	Name		TSIN0DATA[1]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO14[7]	Name		TSIN0DATA[0]
	Description		Transport stream0 parallel data input
	Direction		I
	Configuration		No configuration is required

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO12[0]	Name	Parallel transport stream input 1/ output 0	TSIN1DATA[7]/TSOUTDATA[7]
	Description		Transport STREAM1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x001
PIO12[1]	Name		TSIN1BYTECLK/TSOUTBYTECLK
	Description		Transport stream1 data clock input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x001
PIO12[2]	Name		TSIN1BYTECLKVALID/TSOUTBYTECLKVALID
	Description		Transport stream1 data valid input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x001
PIO12[3]	Name		TSIN1ERROR/TSOUTERROR
	Description		Transport stream1 data error input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x001
PIO12[4]	Name		TSIN1PACKETCLK
	Description		Transport stream1 packet clock input/output
	Direction		I
	Configuration		No configuration is required

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO12[5]	Name	Parallel transport stream input 1/ output 0	TSIN1DATA[6]/TSOUTDATA[6]
	Description		Transport stream1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[5]=0x001
PIO12[6]	Name		TSIN1DATA[5]/TSOUTDATA[5]
	Description		Transport stream1 serial data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[6]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[6]=0x001
PIO12[7]	Name		TSIN1DATA[4]/TSOUTDATA[4]
	Description		Transport stream1 parallel data input/output
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG48*[23:0] Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7]=0x000 PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7]=0x001
PIO13[0]	Name		TSIN1DATA[3]/TSOUTDATA[3]
	Description		Transport STREAM1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[0]=0x001
PIO13[1]	Name		TSIN1DATA[2]/TSOUTDATA[2]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[1]=0x001

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO13[2]	Name		TSIN1DATA[1]/TSOUTDATA[1]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[2]=0x001
PIO13[3]	Name		TSIN1DATA[0]/TSOUTDATA[0]
	Description		Transport stream1 parallel data input
	Direction		B
	Configuration		For OUTPUT selection: Config register: *SYSTEM_CONFIG49*[23:0] Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x000 PIO13_ALTFOP[2:0]_MUX_SEL_BUS[3]=0x001

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO14[1]/ PIO6[0]	Name	Parallel transport stream input 2	TSIN2SER/DATA[7]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[0], *SYSTEM_CONFIG4*[10] = 0 when PIO14[1], *SYSTEM_CONFIG4*[10] = 1
PIO14[2]/ PIO6[1]	Name		TSIN2BYTECLK
	Description		Transport stream2 data clock input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[1], *SYSTEM_CONFIG4*[10] = 0 when PIO14[2], *SYSTEM_CONFIG4*[10] = 1
PIO14[3]/ PIO6[2]	Name		TSIN2BYTECLKVALID
	Description		Transport stream2 data valid input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[2], *SYSTEM_CONFIG4*[10] = 0 when PIO14[3], *SYSTEM_CONFIG4*[10] = 1
PIO14[4]/ PIO6[3]	Name		TSIN2ERROR
	Description		Transport stream2 data error input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[3], *SYSTEM_CONFIG4*[10] = 0 when PIO14[4], *SYSTEM_CONFIG4*[10] = 1
PIO14[5]/ PIO6[4]	Name		TSIN2PACKETCLK
	Description		Transport stream2 packet clock input
	Direction		I
	Configuration		For INPUT selection: Config register: *SYSTEM_CONFIG4*[31:0] Config bus: when PIO6[4], *SYSTEM_CONFIG4*[10] = 0 when PIO14[5], *SYSTEM_CONFIG4*[10] = 1

Table 38. STi7197 Parallel Transport Stream inputs/output mapping (continued)

Pin	Parameter	Interface	Details
PIO6[5]	Name	Parallel transport stream input 2	TSIN2DATA[6]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO6[6]	Name		TSIN2DATA[5]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO6[7]	Name		TSIN2DATA[4]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[0]	Name		TSIN2DATA[3]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[1]	Name		TSIN2DATA[2]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[2]	Name		TSIN2DATA[1]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required
PIO7[3]	Name		TSIN2DATA[0]
	Description		Transport stream2 parallel data input
	Direction		I
	Configuration		No configuration is required

9.2 Ethernet interface multiplexing in standard mode

The Ethernet interface can be configured in the following ways:

- MII mode
- RMII mode

The mapping is shown in *Table 39*.

Table 39. STi7197 Ethernet muxing details (in standard mode)

Pin	Parameter	Configuration0	Configuration1
		Ethernet MII mode	Ethernet RMII mode
	Configuration	*SYSTEM_CONFIG7*[16] =1 *SYSTEM_CONFIG7*[18] =1 *SYSTEM_CONFIG7*[26:25] =00	*SYSTEM_CONFIG7*[16] =1 *SYSTEM_CONFIG7*[18] =0 *SYSTEM_CONFIG7*[26:25] =01
ETH_MII_TXCLK	Name	ETH_MII_TXCLK	-
	Description	Transmit clock	-
	Direction	I	-
ETH_MII_TXEN	Name	ETH_MII_TXEN	ETH_RMII_TXEN
	Description	Transmit enable flag	Transmit enable flag
	Direction	O	O
ETH_MII_TXD[3]	Name	ETH_MII_TXD[3]	-
	Description	Transmit data BIT3	-
	Direction	O	-
ETH_MII_TXD[2]	Name	ETH_MII_TXD[2]	-
	Description	Transmit data BIT2	-
	Direction	O	-
ETH_MII_TXD[1]	Name	ETH_MII_TXD[1]	ETH_RMII_TXD[1]
	Description	Transmit data BIT1	Transmit data BIT1
	Direction	O	O
ETH_MII_TXD[0]	Name	ETH_MII_TXD[0]	ETH_RMII_TXD[0]
	Description	Transmit data BIT0	Transmit data BIT0
	Direction	O	O
ETH_MII_RXCLK	Name	ETH_MII_RXCLK	-
	Description	Receive clock	-
	Direction	I	-
ETH_MII_RXDV	Name	ETH_MII_RXDV	ETH_RMII_CRSDV
	Description	Receive data valid flag	Receive data valid flag
	Direction	I	I
ETH_MII_RXER	Name	ETH_MII_RXER	ETH_RMII_RXER
	Description	Receive data error flag	Receive data error flag

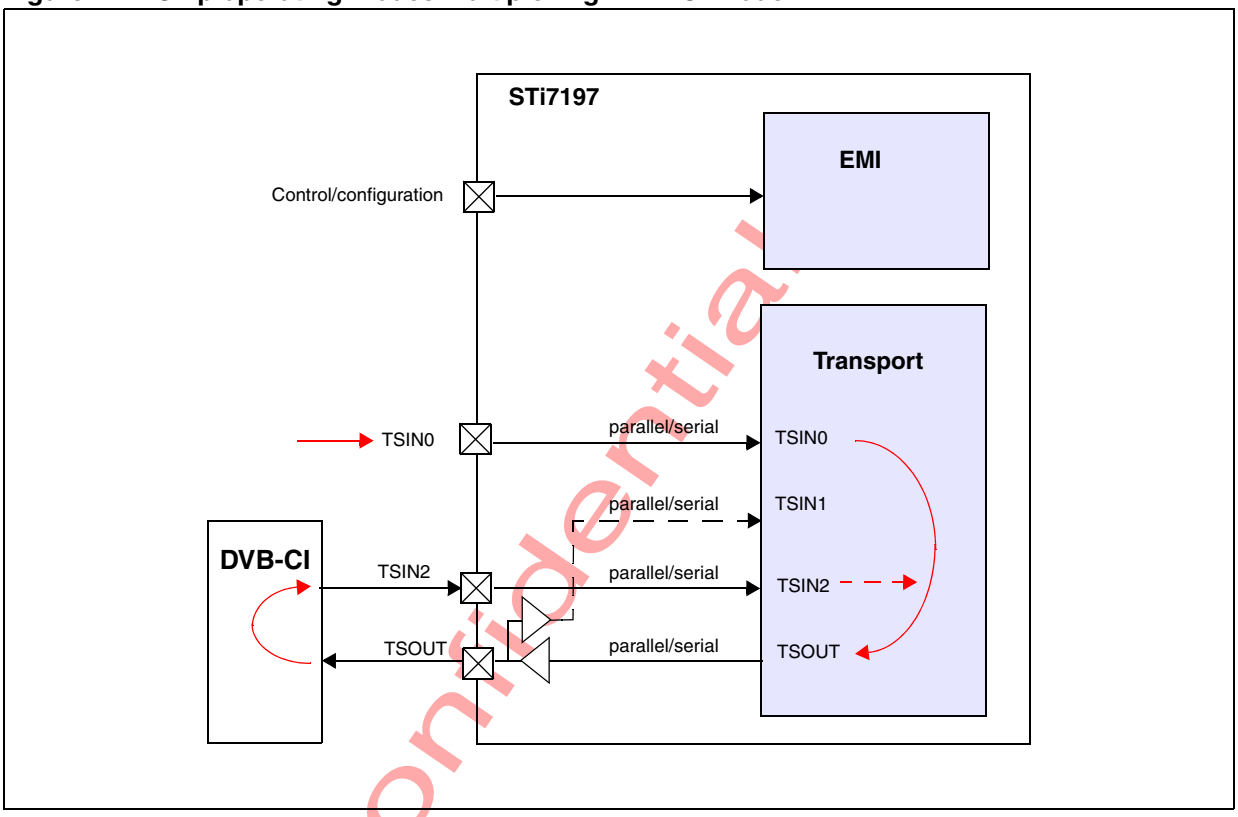
Table 39. STi7197 Ethernet muxing details (in standard mode) (continued)

Pin	Parameter	Configuration0	Configuration1
	Direction	I	I
ETH_MII_RXD[3]	Name	ETH_MII_RXD[3]	-
	Description	Receive data BIT3	-
	Direction	I	-
ETH_MII_RXD[2]	Name	ETH_MII_RXD[2]	-
	Description	Receive data BIT2	-
	Direction	I	-
ETH_MII_RXD[1]	Name	ETH_MII_RXD[1]	ETH_RMII_RXD[1]
	Description	Receive data BIT1	Receive data BIT1
	Direction	I	I
ETH_MII_RXD[0]	Name	ETH_MII_RXD[0]	ETH_RMII_RXD[0]
	Description	Receive data BIT0	Receive data BIT0
	Direction	I	I
ETH_MII_CRS	Name	ETH_MII_CRS	-
	Description	Carrier sense flag	-
	Direction	I	-
ETH_MII_COL	Name	ETH_MII_COL	-
	Description	Carrier collision detect flag	-
	Direction	I	-
ETH_MII_MDC	Name	ETH_MII_MDC	ETH_RMII_MDC
	Description	Management data clock	Management data clock
	Direction	O	O
ETH_MII_MDIO	Name	ETH_MII_MDIO	ETH_RMII_MDIO
	Description	Management data	Management data
	Direction	B	B
ETH_MII_MDINT	Name	ETH_MII_MDINT	ETH_RMII_MDINT
	Description	Management data interrupt	Management data interrupt
	Direction	I	I
ETH_MII_PHYCLK	Name	ETH_MII_PHYCLK	ETH_RMII_PHYCLK
	Description	PHY clock	PHY clock
	Direction	O	O

9.3 DVB common interface (DVB-CI) transport mode

In the DVB common interface mode, the transport stream is demodulated by the front-end subsystem, sent to the external DVB-CI decryption module through the transport interface (in parallel mode) and sent back again (in parallel mode) to the STi7197.

Figure 17. Chip operating modes multiplexing: DVB-CI mode



Details of transport interface mapping on PIOs are provided in *Section 9.1: Transport interfaces multiplexing* and *Table 38*.

Refer to *Section 9.4.6: DVB-CI modes* for DVB-CI mapping on EMI pads.

9.4 External memory interface (EMI) operating modes

The EMI can support the following device types, each one associated with different pin mappings:

1. Peripheral/SRAM on *page 207*
2. Asynchronous NOR-FLASH on *page 207*
3. Synchronous NOR-FLASH on *page 208*
4. NAND-FLASH on *page 209*
5. Serial FLASH on *page 210*
6. DVB-CI on *page 210*
7. ATAPI-PIO on *page 211*
8. PCI on *page 211*
9. Multi-Chip; independent from all other modes (except PCI) on *page 212*

9.4.1 Peripheral/SRAM mode

Table 40. EMI peripheral/SRAM mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Peripheral chip select E,D,C,B,A
NOTEMIBE[1:0]	NOTEMIBE[1:0]	O	3.3	External device databus byte enable
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. Common to all devices.
EMIDATA[15:0]	EMIDATA[0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[25:1]	O	3.3	External common address bus

Note: NOTEMILBA, NOTEMIBAA, EMINANDREADYNOTBUSY, and EMIFLASHCLK are not used.

9.4.2 Asynchronous NOR-Flash mode

Table 41. EMI asynchronous NOR-Flash mode: pin mapping

EMI assignment	Asynchronous NOR-Flash mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Chip select E,D,C,B,A
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator

Table 41. EMI asynchronous NOR-Flash mode: pin mapping (continued)

EMI assignment	Asynchronous NOR-Flash mode assignment	I/O	Voltage	Description
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. Common to all devices.
EMIDATA[15:0]	EMIDATA[15:0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[24:0]	O	3.3	External common address bus

Note: NOTEMILBA, NOTEMIBAA, EMINANDREADYNOTBUSY, and EMIFLASHCLK are not used.

9.4.3 Synchronous NOR-Flash mode

Table 42. EMI synchronous NOR-Flash mode: pin mapping

EMI assignment	Synchronous NOR-Flash mode assignment	I/O	Voltage	Description
NOTEMICSE,D,C,B,A	NOTEMICSE,D,C,B,A	O	3.3	Chip select E,D,C,B,A
NOTEMIOE	NOTEMIOE	O	3.3	External device output enable
NOTEMILBA	NOTEMILBA	O	3.3	Flash device load burst address
NOTEMIBAA	NOTEMIBAA	O	3.3	Flash burst address advanced
EMITREADYORWAIT	EMITREADYORWAIT	I	3.3	External memory device target ready indicator
EMIRDNOTWR	EMIRDNOTWR	O	3.3	External read/write access indicator. common to all devices.
EMIDATA[15:0]	EMIDATA[15:0]	I/O	3.3	External common databus
EMIADDR[25:1]	EMIADDR[24:0]	O	3.3	External common address bus
EMIFLASHCLK	EMIFLASHCLK	I/O	3.3	Flash clock

9.4.4 NAND-Flash mode

Features

- Embeds a 1-bit error correcting code (ECC) hardware controller.
- Can support single level cell (SLC) NAND Flash devices from the main Flash providers.
- Multiple Flash devices can be addressed; each EMI_CS being configured statically by software, such as EMI Flash CS. An external NOR is issued on READY_NOT_BUSY signals in that case.

Table 43. EMI NAND-Flash mode: pin mapping

EMI assignment	NAND-Flash mode assignment	I/O	Voltage	Description
NOTEMICSA	NAND_CS0	O	3.3	Chip select E,D,C,B,A
NOTEMICSB	NAND_CS1	O	3.3	
NOTEMICSC	NAND_CS2	O	3.3	
NOTEMICSD	NAND_CS3	O	3.3	
NOTEMICSE	NAND_CS4	O	3.3	
NOTEMIOE	NAND_REN	O	3.3	External device output enable
EMIRDNOTWR	NAND_WEN	O	3.3	External read/write access indicator
EMIDATA[15:0]	NAND_AD[15:0]	I/O	3.3	External common address/databus
EMIADDR[18]	NAND_ALE	O	3.3	-
EMIADDR[17]	NAND_CLE	O	3.3	-

Note: NOTEMIBE[1:0], NOTEMILBA, NOTEMIBAA, EMITREADYORWAIT, EMIADDR[25:19], EMIADDR[16:1], and EMIFLASHCLK are not used.

9.4.5 Serial-Flash mode

Table 44. EMI Serial-Flash pins as PIO alternates

Assignment	I/O	Voltage	Description	Comments
SPIBOOT_CLOCK	O	3.3	-	PIO15[0]
SPIBOOT_DATA_OUT	O	3.3	-	PIO15[1]
SPIBOOT_DATA_IN	I	3.3	-	PIO15[3]
SPIBOOT_CS	O	3.3	-	PIO15[2]

9.4.6 DVB-CI modes

The DVB-CI modes are only available on banks 2 and 3.

Table 45. EMI DVB-CI mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSD,C	DVBCI_NOTCEx	O	3.3	Peripheral chip select D,C
NOTEMIBE[0]	DVBCI_NOTIOWR	O	3.3	Write command
NOTEMIOE	DVBCI_NOTOE	O	3.3	Output enable
NOTEMILBA	DVBCI_NOTWE	O	3.3	Write enable DVBCI
NOTEMIBAA	DVBCI_NOTIORD	O	3.3	Read command
EMITREADYORWAIT	DVBCI_NOTWAIT	I	3.3	Wait signal
EMIDATA[7:0]	DVBCI_DATA[7:0]	I/O	3.3	External common databus
EMIADDR[14:1]	DVBCI_A[14:1]	O	3.3	Address bus
NOTEMIBE[1]	DVBCI_A[0]	O	3.3	Address bit 0

Note: NOTEMICSE/B/A, EMINANDREADYNOTBUSY, EMIDATA[15:8], EMIADDR[25:16], EMIFLASHCLK are not used.

9.4.7 ATAPI-PIO modes

The ATAPI-PIO modes are only available on banks 2 and 3.

Table 46. EMI ATAPI-PIO mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSD,C	ATAPI_NOTCEx	O	3.3	Peripheral chip select D,C
NOTEMIBE[0]	ATAPI_NOTDIOWR	O	3.3	Write command
NOTEMIBAA	ATAPI_NOTDIORD	O	3.3	Read command
EMITREADYORWAIT	ATAPI_IORDY	I	3.3	Wait signal
EMIDATA[15:0]	ATAPI_DATA[15:0]	I/O	3.3	External common databus
EMIADDR[20:19]	ATAPI_CS[1:0]	O	3.3	Chip select
EMIADDR[2:1]	ATAPI_A[2:1]	O	3.3	Address bus

Note: NOTEMICSE/B/A, NOTEMIBE[1], NOTEMIOE, NOTEMILBA, EMIADDR[25:21], EMIADDR[18:3], EMIFLASHCLK are not used.

9.4.8 PCI mode

Table 47. EMI PCI mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
NOTEMICSE	PCI_NOTFRAME	I/O	3.3	PCI frame
NOTEMIBE[1:0]	PCI_CBE[1:0]	I/O	3.3	PCI command/byte enable
EMIRDNOTWR	PCI_NOTPERR	I/O	3.3	PCI parity error flag
EMIDATA[15:0]	PCI_AD[15:0]	I/O	3.3	Common PCI address/data bus
EMIADDR[24:23]	PCI_CBE[3:2]	I/O	3.3	PCI command/byte enable
EMIADDR[22]	PCI_NOTDEVSEL	I/O	3.3	PCI device select
EMIADDR[20]	PCI_NOTSTOP	I/O	3.3	PCI target stop request
EMIADDR[19]	PCI_NOTIRDY	I/O	3.3	PCI initiator ready flag
EMIADDR[18]	PCI_NOTTRDY	I/O	3.3	PCI target ready flag
EMIADDR[17]	PCI_PAR	I/O	3.3	PCI parity flag
EMIADDR[16:1]	PCI_AD[31:16]	I/O	3.3	Common PCI address/data bus
EMIFLASHCLK	PCI_CLK	I/O	3.3	PCI clock
EMIBUSREQ	PCI_REQ[0]	I/O	3.3	PCI bus access request
EMIBUSGNT	PCI_GNT[0]	I/O	3.3	PCI bus access grant

Note: NOTEMICSD/C/B/A, NOTEMIOE, EMIADDR[25], EMIADDR[21], NOTEMILBA, and EMITREADYORWAIT are not used.

Caution: Memory read transfers from non-prefetchable memory are always signalled as 32 bits transfers (all byte enables active) by the STi7197. This should be taken into account when considering PCI devices to be used with STi7197.

Table 48. EMI PCI pins as PIO alternates

Assignment	I/O	Voltage	Description	Comments
PCI_BUS_REQ[1]	I	3.3	PCI bus access request	PIO6[5]
PCI_BUS_REQ[2]	I	3.3	PCI bus access request	PIO6[6]
PCI_BUS_GNT[1]	O	3.3	PCI bus access grant	PIO7[1]
PCI_BUS_GNT[2]	O	3.3	PCI bus access grant	PIO7[2]
PCI_LOCK_IN	I	3.3	PCI lock function	PIO7[0], PIO15[5]
PCI_PME_IN	I	3.3	PCI PME function	PIO15[6]
PCI_INT_FROM_DEVICE[0]	I	3.3	PCI interrupt input (when host)	PIO6[0]/PIO15[3]
PCI_INT_FROM_DEVICE[1]	I	3.3	PCI interrupt input (when host)	PIO6[1]
PCI_INT_FROM_DEVICE[2]	I	3.3	PCI interrupt input (when host)	PIO6[2]
PCI_INT_TO_HOST	O	3.3	PCI interrupt output (when device)	PIO15[3], PIO6[0]
PCI_RESETN_FROM_HOST_TO_DEVICE	I	3.3	PCI reset input (when host)	PIO15[7]
PCI_SYSTEM_ERROR	O	3.3	PCI error flag	PIO15[4]

9.4.9 Multi-chip mode

With the exception of PCI, this mode is independent from all other modes and uses dedicated balls.

Table 49. EMI multi-chip mode: pin mapping

EMI assignment	Peripheral/SRAM mode assignment	I/O	Voltage	Description
EMIBUSREQ	EMIBUSREQ	I/O	3.3	Bus access request
EMIBUSGNT	EMIBUSGNT	I/O	3.3	Bus access grant

EMI multi-chip mode: pins as PIO alternates

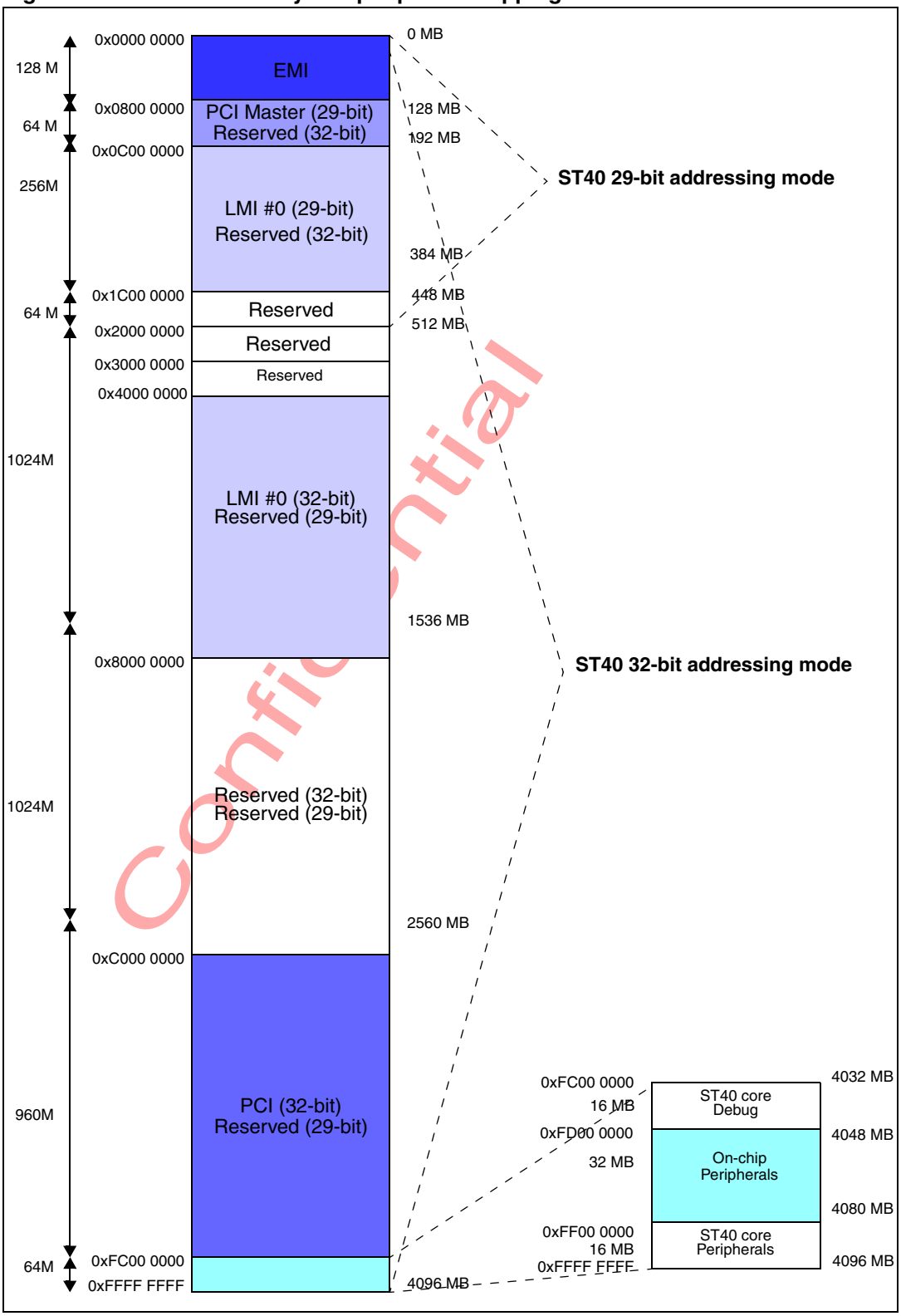
Assignment	I/O	Voltage	Description	Comments
EMI_SS_BUS_FREE_ACCESSPEND/ EMI_SS_BUS_FREE_OUT	I	3.3	Access pending flag	PIO15[2]

10 Memory map

The STi7197's memory space is populated with non-volatile memories, with external peripherals (EMI) at base address 0x0000 0000 (ST40 boots at address 0), and with DDR2-SDRAM devices (LMI) at base address 0x0C00 0000 (128 Mbytes) in 29-bit mode or at base address 0x4000 0000 (1024 Mbytes) in 32-bit mode.

The STi7197 on-chip peripherals are mapped in area 6 of the ST40 in 29-bit mode. The *Figure 18* shows the STi7197 memory and peripheral mapping.

Figure 18. STi7197 memory and peripheral mapping



Note: In SE mode, the ST40 Core Peripherals (P4) appear twice in the STBUS address map. The LMI base address is programmable.

10.1 Global Mapping

The internal peripherals addresses are located in ST40-300 P4 region. Grouping is done so that peripherals which belong to the same physical block have contiguous addresses, requiring only one address decoder in each physical block.

The *Table 50* gives the base address of the external interfaces and internal peripherals.

Table 50. Internal peripheral base addresses

Target Name	Start Offset	End Offset	Size (bytes)	Description
EMI	0x0000 0000	0x07FF FFFF	128 M	EMI
PCI_MASTER_29B	0x0800 0000	0x0BFF FFFF	64 M	PCI Master, 29-bit mode
LMI0_HP_29B	0x0C00 0000	0x1BFF FFFF	256 M	LMI #0 - HP, 29-bit mode
LMI0_LP_29B	0x0C00 0000	0x1BFF FFFF	256 M	LMI #0 - LP, 29-bit mode
RESERVED	0x1C00 0000	0x3FFF FFFF	576 M	Reserved
LMI0_HP_32B	0x4000 0000	0x7FFF FFFF	1024 M	LMI #0 - HP, 32-bit mode
LMI0_LP_32B	0x4000 0000	0x7FFF FFFF	1024 M	LMI #0 - LP, 32-bit mode
RESERVED	0x8000 0000	0xBFFF FFFF	1024 M	Reserved
PCI_MASTER_32B	0xC000 0000	0xFBFF FFFF	960 M	PCI Master, 32-bit mode
SH4 CORE DEBUG	0xFC00 0000	0xFCFF FFFF	16 M	ST40 Core Debug
COMMs	0xFD00 0000	0xFD0F FFFF	1 M	Comms config registers (details in *Table 51*)
SPARE0_PLUG	0xFD10 0000	0xFD10 0FFF	4 K	Spare 0 plug
RESERVED	0xFD10 1000	0xFD10 17FF	2 K	Reserved
PCMP1	0xFD10 1800	0xFD10 1FFF	4 K	PCM player 1 port & config registers
PCMR0	0xFD10 2000	0xFD10 2FFF	4 K	PCM reader port & config registers
CPXM	0xFD10 3000	0xFD10 3FFF	4 K	CPXM registers
TVOUT_FDMA	0xFD10 4000	0xFD10 5FFF	8 K	TVOUT FDMA (HDMI, PCM_p1,SPDIF_p, TTxT) (details in *Table 52*)
RESERVED	0xFD10 6000	0xFD10 FFFF	44 K	Reserved
GMAC0	0xFD11 0000	0xFD11 7FFF	32 K	Ethernet 0 config registers
RESERVED	0xFD11 8000	0xFD11 FFFF	32 K	Reserved
SPARE1_PLUG	0xFD12 0000	0xFD12 7FFF	32 K	Spare 1 plug
RESERVED	0xFD12 8000	0xFDFF FFFF	15200 K	Reserved
CLKGENB	0xFE00 0000	0xFE00 0FFF	4 K	Clock Generator B config registers
SYSC_A	0xFE00 1000	0xFE00 1FFF	4 K	System config registers (GP Registers)
HD_DISPLAY	0xFE00 2000	0xFE00 2FFF	4 K	HD display config registers

Table 50. Internal peripheral base addresses (continued)

Target Name	Start Offset	End Offset	Size (bytes)	Description
SD_DISPLAY	0xFE00 3000	0xFE00 3FFF	4K	SD display config registers
RESERVED	0xFE00 4000	0xFE00 BFFF	32K	Reserved
RESERVED	0xFE00 C000	0xFE00 FFFF	16K	Reserved
T1_PIO	0xFE01 0000	0xFE01 FFFF	64K	T1 PIO - 10 Banks PIOs config registers
KEY_SCAN	0xFE02 0000	0xFE02 07FF	2 K	Key scanning
RESERVED	0xFE02 0800	0xFE02 FFFF	62 K	Reserved
TVOUT_CPU	0xFE03 0000	0xFE03 7FFF	32 K	TVOUT Config Regs (Denc, VTGs, TVO_glue, FlexDVO, HD formatter, CEC) (details in *Table 53*)
RESERVED	0xFE03 8000	0xFE0F FFFF	800 K	Reserved
USB2_1	0xFE10 0000	0xFE1F FFFF	1 M	USB 2.0 #1 config registers
RESERVED	0xFE20 0000	0xFE20 7FFF	32 K	Reserved
RESERVED	0xFE20 8000	0xFE20 8FFF	4 K	Reserved
SATA	0xFE20 9000	0xFE20 9FFF	4 K	SATA config registers
COMPO	0xFE20 A000	0xFE20 AFFF	4 K	Compositor config registers
BLITTER	0xFE20 B000	0xFE20 BFFF	4 K	Blitter display config registers
RESERVED	0xFE20 C000	0xFE20 D3FF	5 K	Reserved
RESERVED	0xFE20 D400	0xFE20 FFFF	11 K	Reserved
AUDIO_CONF	0xFE21 0000	0xFE21 0FFF	4 K	Audio config registers
MBX0	0xFE21 1000	0xFE21 17FF	2 K	Mailbox #0 (LX Delta_Mu) config registers
RESERVED	0xFE21 1800	0xFE21 1FFF	2 K	Reserved
MBX1	0xFE21 2000	0xFE21 27FF	2 K	Mailbox #1 (LX Delta_Mu) config registers
RESERVED	0xFE21 2800	0xFE21 2FFF	2 K	Reserved
CLKGENA	0xFE21 3000	0xFE21 3FFF	4 K	Clock Generator A config registers
RESERVED	0xFE21 4000	0xFE21 FFFF	48 K	Reserved
FDMA_0	0xFE22 0000	0xFE22 FFFF	64 K	FDMA_0 memory and config registers
PTI_0	0xFE23 0000	0xFE23 FFFF	64 K	PTI_0 config registers
RESERVED	0xFE24 0000	0xFE24 0FFF	4 K	Reserved
DVP	0xFE24 1000	0xFE24 1FFF	4 K	DVP config registers
TSMERGER	0xFE24 2000	0xFE24 2FFF	4 K	TSMerger config registers
RESERVED	0xFE24 3000	0xFE24 FFFF	52 K	Reserved
RESERVED	0xFE25 0000	0xFE25 0FFF	4 K	Reserved

Table 50. Internal peripheral base addresses (continued)

Target Name	Start Offset	End Offset	Size (bytes)	Description
RESERVED	0xFE25 1000	0xFE25 FFFF	60 K	Reserved
PTI_1	0xFE26 0000	0xFE26 FFFF	64 K	PTI_1 config registers
RESERVED	0xFE27 0000	0xFE3F FFFF	1600 K	Reserved
EMISS	0xFE40 0000	0xFE40 7FFF	32 K	EMISS config registers (EMISS) (details in *Table 54*)
RESERVED	0xFE40 8000	0xFE40 FFFF	32 K	Reserved
FDMA_1	0xFE41 0000	0xFE41 FFFF	64 K	FDMA_1 config registers
FDMA_MUX	0xFE42 0000	0xFE42 0FFF	4 K	FDMA Mux config registers
RESERVED	0xFE42 1000	0xFE53 FFFF	1148 K	Reserved
DMU	0xFE54 0000	0xFE55 FFFF	128 K	Delta Mu configuration registers
PCI_MASTER_REGS	0xFE56 0000	0xFE56 0FFF	4 K	AHB-PCI config registers (on T3 I)
RESERVED	0xFE56 1000	0xFE5F FFFF	636 K	Reserved
LX_DMU	0xFE60 0000	0xFE6F FFFF	1 M	ST231 Delta Mu peripherals
EMIREG	0xFE70 0000	0xFE7F FFFF	1 M	EMI configuration registers (details in *Table 54*)
LX_AUD	0xFE80 0000	0xFE8F FFFF	1 M	ST231 audio peripherals
TSMERGER_T2	0xFE90 0000	0xFE90 0FFF	4 K	TSMerger-Type2 space
LMI0_REG	0xFE90 1000	0xFE90 1FFF	4 K	GPLMI0 control registers
RESERVED	0xFE90 2000	0xFE9F FFFF	1016 K	Reserved
USB2_2	0xFEA0 0000	0xFEAF FFFF	1 M	USB 2.0 #2 config registers
RESERVED	0xFEB0 0000	0xFEFF FFFF	4 M	Reserved
SH4 CORE PERIPH	0xFF00 0000	0xFFFF FFFF	16 M	ST40 core peripherals

Table 51. STi7197 Comms sub-blocks memory map (base address: 0xFD00 0000)

Region Name	Start Offset	End Offset	Size (bytes)	Description
ILC3	0x00000	0x0FFF	4K	ILC
RESERVED	0x01000	0x07FFF	28K	Reserved
LPC	0x08000	0x08FFF	4K	LPC
RESERVED	0x09000	0x0FFFF	28K	Reserved
PWM0	0x10000	0x10FFF	4K	PWM0
RESERVED	0x11000	0x17FFF	28K	Reserved
IRB	0x18000	0x18FFF	4K	IRB group
RESERVED	0x19000	0x1FFFF	28K	Reserved

Table 51. STi7197 Comms sub-blocks memory map (base address: 0xFD00 0000) (continued)

Region Name	Start Offset	End Offset	Size (bytes)	Description
PIO0	0x20000	0x20FFF	4K	PIO
PIO1	0x21000	0x21FFF	4K	
PIO2	0x22000	0x22FFF	4K	
PIO3	0x23000	0x23FFF	4K	
PIO4	0x24000	0x24FFF	4K	
PIO5	0x25000	0x25FFF	4K	
PIO6	0x26000	0x26FFF	4K	
PIO7	0x0101 0000	0x0101 0FFF	4K	
PIO8	0x0101 1000	0x0101 1FFF	4K	PIO
PIO9	0x0101 2000	0x0101 2FFF	4K	
PIO10	0x0101 3000	0x0101 3FFF	4K	
PIO11	0x0101 4000	0x0101 4FFF	4K	
PIO12	0x0101 5000	0x0101 5FFF	4K	
PIO13	0x0101 6000	0x0101 6FFF	4K	
PIO14	0x0101 7000	0x0101 7FFF	4K	
PIO15	0x0101 8000	0x0101 8FFF	4K	
PIO16	0x0101 9000	0x0101 9FFF	4K	
RESERVED	0x27000	0x2FFFF	36K	Reserved
UART0	0x30000	0x30FFF	4K	UART
UART1	0x31000	0x31FFF	4K	
UART2	0x32000	0x32FFF	4K	
UART3	0x33000	0x33FFF	4K	
RESERVED	0x34000	0x3FFFF	48K	Reserved
SSC0	0x40000	0x40FFF	4K	Synchronous Serial Controller
SSC1	0x41000	0x41FFF	4K	
SSC2	0x42000	0x42FFF	4K	
SSC3	0x43000	0x43FFF	4K	
RESERVED	0x44000	0x47FFF	16K	Reserved
RESERVED	0x48000	0x48FFF	4K	Reserved
RESERVED	0x49000	0x49FFF	4K	
RESERVED	0x4A000	0x57FFF	56K	Reserved
MAFE	0x58000	0x58FFF	4K	MAFE
RESERVED	0x59000	0xFFFFF	668K	Reserved

Table 52. STi7197 TVOUT_FDMA sub-blocks memory map (base address: 0xFD10 4000)

Region Name	Start offset	End offset	Size (bytes)	Description
HDMI_REG	0x0000	0x07FC	2K	HDMI registers
HDCP	0x0800	0x09FC	512	HDCP registers
RESERVED	0x0A00	0x0BFC	512	Reserved
SPDIFPLAYER_REG	0x0C00	0x0CFC	256	S/PDIF player
PCMPLAYER	0x0D00	0xDFC	256	PCM player registers
TVO_GLUE_AUX	0x0E00	0x0EFC	256	TVO glue AUX registers
RESERVED	0x0F00	0x0FFC	256	Reserved
I2S2SPDIF_1	0x1000	0x13FC	1K	I2S to S/PDIF 1 registers
I2S2SPDIF_2	0x1400	0x17FC	1K	I2S to S/PDIF 2 registers
I2S2SPDIF_3	0x1800	0x1BFC	1K	I2S to S/PDIF 3 registers
I2S2SPDIF_4	0x1C00	0x1FFC	1K	I2S to S/PDIF 4 registers

Table 53. STi7197 TVOUT_CPU sub-blocks memory map (base address: 0xFE03 0000)

Region Name	Start offset	End offset	Size (bytes)	Description
DENC	0x0000	0x01FC	512	DENC registers
AUX_VTG	0x0200	0x02FC	256	AUX VTG registers
MAIN_VTG	0x0300	0x03FC	256	Main VTG registers
TVO_GLUE_MAIN	0x0400	0x04FC	256	TVO glue main registers
RESERVED	0x0500	0x05FC	256	Reserved
Flex-DVO0	0x0600	0x07FC	512	Flex DVO0 register
HD FORMATTER	0x0800	0x0BFC	1K	HD formatter
CEC	0x0C00	0x0C7C	128	CEC register
RESERVED	0x0C80	0x45FC	14.37K	Reserved
Flex-DVO1	0x4600	0x47FC	512	Flex DVO 1 register
RESERVED	0x4800	0xFFFC	46K	Reserved

Table 54. STi7197 EMISS and EMI sub-blocks memory map

Region name	Start offset	End Offset	Size (bytes)	Description
EMISS_ARBITER_REG	0xFE40 0000 + 0x1000	0xFE40 0000 + 0x13FF	1K	EMI/PCI arbiter registers
EMISS_PCI_BRIDGE_REG	0xFE40 0000 + 0x1400	0xFE40 0000 + 0x17FF	1K	PCI STbus bridge registers
EMI_CONF_REG	0xFE70 0000 + 0x0000	0xFE70 0000 + 0x0FFF	4K	EMI registers
EMI_NAND_REG	0xFE70 0000 + 0x1000	0xFE70 0000 + 0x1FFF	4K	EMI NAND controller registers

Table 54. STi7197 EMISS and EMI sub-blocks memory map (continued)

Region name	Start offset	End Offset	Size (bytes)	Description
EMI_SPI_REG	0xFE70 0000 + 0x2000	0xFE70 0000 + 0x2FFF	4K	EMI SPI controller registers
RESERVED	0xFE70 0000 + 0x3000	0xFE70 0000 + 0xFFFF	52K	Reserved

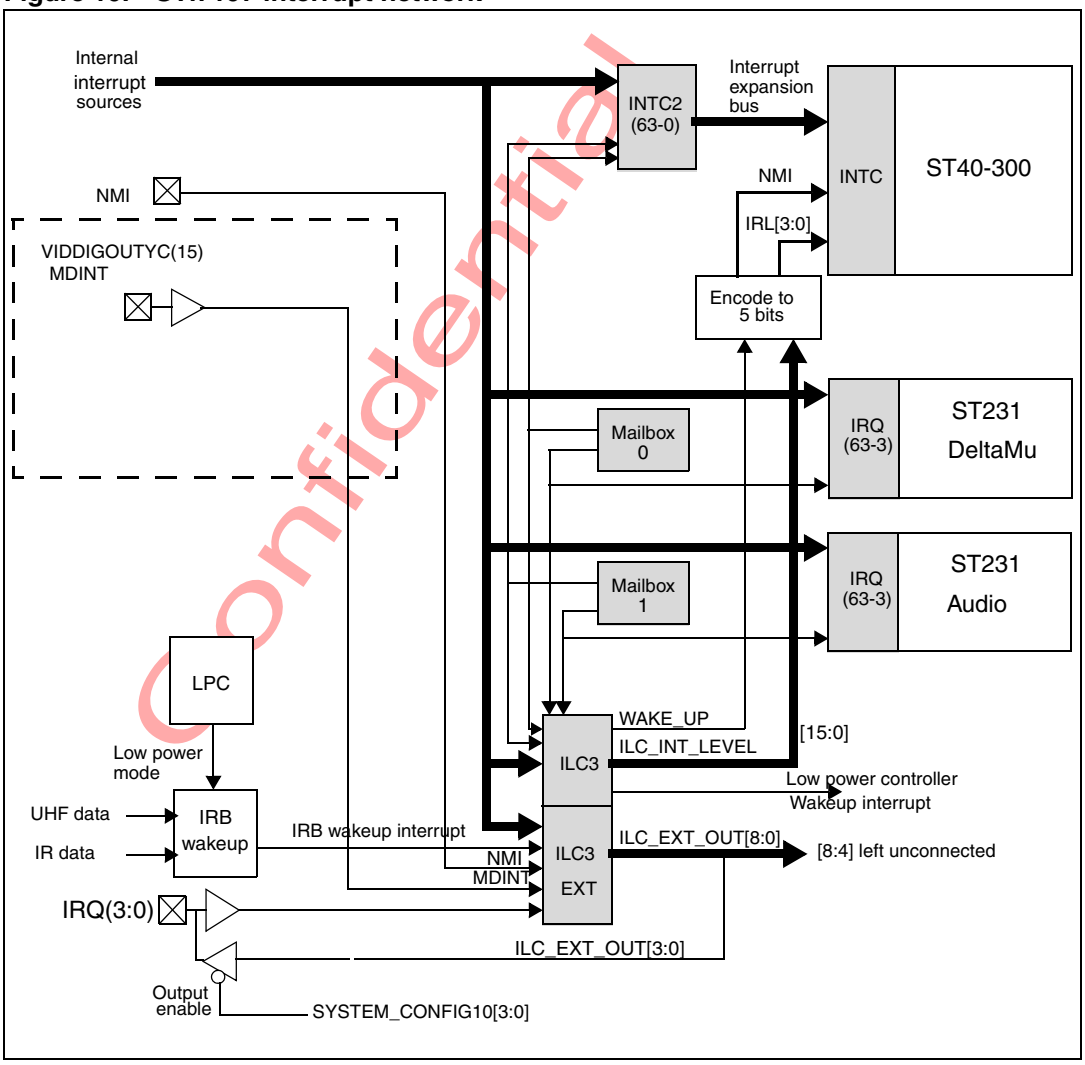
11 Interrupt networks

11.1 Interrupt network organization

The STi7197 has multiple interrupt networks. One network is associated with the ST40 CPU through INTC2 or/and ILC3 interrupt controller, a second network is associated with the DeltaMu-ST231 CPU, and the third network is associated with the Audio-ST231 CPU.

The interrupt lines are routed to ST40 and partially to DeltaMu-ST231 and Audio-ST231. It is up to the software to handle the interrupts with ST40 or DeltaMu-ST231 or Audio-ST231.

Figure 19. STi7197 interrupt network



11.1.1 STi7197 interrupt network

ILC3 interrupt level controller

The STi7197 interrupt network includes an ILC3 interrupt level controller. The ILC3 accepts 96 synchronous interrupt inputs and eight asynchronous interrupt inputs. The external interrupts can have up to five programmable triggering conditions (active high, active low, falling edge, rising edge, or any edge).

The ILC3 maps any of these interrupts onto a group of 16 interrupt level outputs that are used in the STi7197 for internal and external interrupts and onto a group of four interrupt levels that are not used.

The ILC3 mapping is described in *Table 55* and *Table 56*.

Wake up by interrupt

The ILC3 also has an interrupt output dedicated to the wake-up process. A pulse stretcher receives a transition from the UHF and IR input pins and generates an interrupt connected to one of the external interrupt inputs.

Internal peripheral interrupts

Both the ST40 and the DeltaMu ST231 receive all the internal interrupt requests. It is up to the software to define the CPU that will serve each interrupt request.

All the internal interrupts are routed to the INTC2, ST231 Interrupt controller and ILC3. All the internal interrupts are level sensitive and active HIGH.

External interrupts inputs

The four external asynchronous interrupts and the MDINT interrupts (the Ethernet phy interrupt or fifth IRQ if the Ethernet/DVO pins are configured for Ethernet but the Ethernet phy is either not connected or does not use the MDINT) are routed to the ILC3 interrupt controller before reaching the ST40 and ST231 in order to synchronize and change the polarity if needed. The ST40 expects the interrupts to be active high. These interrupts are then output from the ILC3 to be routed toward the ST40 and DeltaMu ST231.

External interrupts outputs

The ILC3 has the capability to output a subset of the interrupts that are connected to it. Four of these interrupts are software selectable to be output externally for remote devices.

Control of the external interrupts direction

The direction of the external interrupts is controlled by the configuration register *SYSTEM_CONFIG10*.

Table 55. ILC3 internal interrupt mapping

Interrupt source		ILC3 mapping
Comms/PIO	PIO0_INTERRUPT	0
	PIO1_INTERRUPT	1
	PIO2_INTERRUPT	2
	PIO3_INTERRUPT	3
	PIO4_INTERRUPT	4
	PIO5_INTERRUPT	5
	PIO6_INTERRUPT	6
SSC	SSC0_INTERRUPT	7
	SSC1_INTERRUPT	8
	SSC2_INTERRUPT	9
	SSC3_INTERRUPT	10
Comms/UART	UART0_INTERRUPT	11
	UART1_INTERRUPT	12
	UART2_INTERRUPT	13
	UART3_INTERRUPT	14
Comms/MAFE	MAFE_INTERRUPT	15
Comms/PWM	PWM_INTERRUPT	16
Comms/IRB	IRB_INTERRUPT	17
Comms/TTXT	TTXT_INTERRUPT	18
Comms/DAA	DAA_INTERRUPT	19
DVP	DVP_INTERRUPT	20
Reserved	RESERVED	21
ClockGen	DCXO_INTERRUPT	22
PTI1	PTI1_INTERRUPT	23
MAILBOX	ST40_LX_DELTAMU_INTERRUPT	24
	LX_DELTAMU_ST40_INTERRUPT	25
	ST40_AUDIO_INTERRUPT	26
	LX_AUDIO_ST40_INTERRUPT	27
FDMA0/1	FDMA_1_MBOX_INTERRUPT	28
	FDMA_0_MBOX_INTERRUPT	29
Audio	I2S2SPDIF_INTERRUPT0	30
	SPDIFPLYR_INTERRUPT	31
	PCMRDR_INTERRUPT	32
	PCMPLYR1_INTERRUPT	33
	PCMPLYR0_INTERRUPT	34

Table 55. ILC3 internal interrupt mapping (continued)

Interrupt source		ILC3 mapping
Reserved	RESERVED	35
TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	36
	MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	37
Main Video Display Pipe	MAIN_VDP_END_PROCESSING_IRQ	38
	MAIN_VDP_FIFO_EMPTY_IRQ	39
HDMI/HDCP	HDCP_INTERRUPT	40
	HDMI_INTERRUPT	41
	HDMI_CEC_IRQ	42
	HDMI_CEC_WAKEUP_INT	43
Blitter display	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	44
RESERVED	RESERVED	45
	RESERVED	46
	RESERVED	47
PTI0	PTI0_INTERRUPT	48
RESERVED	RESERVED	52
USBH	EHCI_INTERRUPT	53
	OHCI_INTERRUPT	54
RESERVED	RESERVED	55
	RESERVED	56
RESERVED	RESERVED	57
TS Merger	TS_MERGER_INTERRUPT	58
Ethernet GMAC	PMT_INT	59
PCI	INT_PCI_DMA	60
BLITTER DISPLAY	BDISP_CQ1_IRQP OR BDISP_CQ2_IRQP	62
RESERVED	RESERVED	63

Table 56. ILC3 external interrupt mapping table

Interrupt source		ILC3 mapping
External Interrupts from external devices	EXT_INTERRUPT[0]	0
	EXT_INTERRUPT[1]	1
	EXT_INTERRUPT[2]	2
	EXT_INTERRUPT[3]	3

Table 56. ILC3 external interrupt mapping table (continued)

Interrupt source		ILC3 mapping
From pins through pulse stretcher	IRB_WAKEUP_INTERRUPT	4
NMI Pin	NMI_INTERRUPT	5
Ethernet PHY interrupt /SYSITRQ[4]	MDINT	6
From LPC timer	LOWPOWEROUT_FROM_LPC	7
From Pads through PIO alt (PCI wake-up interrupts)	PCI_PME_IN	8
FDMA0 requests line	selected FDMA_REQ among 32 FDMA DREQ lines	9
eSATA	SATA_IINTRQ_DMAC_0	10
	SATA_IINTRQ_HOSTC_0	11
Key Scanner	KEY_SCANNER_INTERRUPT	12
Ethernet Gmac	GMAC_MAC_INTR	13
Standalone 10 banks PIOs	STANDALONE_10_BANKS_PIO (10 ORED INTERRUPTS)	14
VDP AUX	AUX_VDP_END_PROCESSING_IRQ	15
	AUX_VDP_FIFO_EMPTY_IRQ	16
Compo Capture	COMPO_CAP_BF	17
Compo Capture	COMPO_CAP_TF	18
FDMA1 requests lines	SELECTED FDMA_REQ AMONG 32 FDMA DREQ LINES	19
Reserved	RESERVED	20
ClockGen A	IRQ_CLKOBS	21
DeltaMu	DELPHI_MBE_INTERRUPT	22
	DELPHI_PRE0_INTERRUPT	23
NAND Controller	INT_NAND	24
PCI	IRQ_PCI_ERROR	25
	IRQ_PCI_FROM_DEVICE[0]	26
	IRQ_PCI_FROM_DEVICE[1]	27
	IRQ_PCI_FROM_DEVICE[2]	28
	RESERVED	29
Audio	I2S2SPDIF_INTERRUPT1	30
	I2S2SPDIF_INTERRUPT2	31
	I2S2SPDIF_INTERRUPT3	32
Reserved	RESERVED	33-95

11.1.2 ST40 interrupt network

Internal and external interrupts

The ST40-300 CPU has two types of interrupts.

External interrupts

- Non-Maskable Interrupts (NMI)—external interrupt source.
- Interrupt Request Level INTerrupts (IRLINT)—four external interrupt sources IRL0 to IRL3 which can be configured as four independent interrupts, or encoded to provide 15 external interrupt levels.

These interrupts are managed by the INTC interrupt controller integrated into the ST40-300 CPU core.

The four external asynchronous interrupts and the MDINT interrupts (that is, the Ethernet phy interrupt or fifth IRQ if the Ethernet phy is either not connected or does not use the MDINT) are routed to the ILC3 interrupt controller before reaching the ST40 and ST231 in order to synchronize and change the polarity if needed.

Internal peripheral interrupts

- On-chip peripherals interrupt sources.

  These interrupts are managed by INTC and INTC2, which is an expansion to INTC.

All interrupts (except NMI) are assigned a priority level between 0 and 15: level 15 is the highest and level 1 the lowest; level 0 means that the interrupt is masked. The NMI is defined to have a fixed priority level of 16.

INTC controls the following interrupt sources:

- NMI, IRL[3…0] from external inputs
- ST40-P130 peripherals interrupts:
  - user debug interface (UDI)
  - timer unit (TMU0, 1)
  - real-time clock (RTC)
  - serial controller interface (SCI)
  - watchdog timer (WDT)

The INTC2 controls all the on-chip peripherals interrupts and is connected to the INTC through an interrupt expansion bus.

The INTC2 accepts 16 groups of four interrupts (64 total), each group can be assigned a priority by software (INTPRIxx registers). Within each group (of four interrupts), there is a fixed priority, with interrupt four having the highest priority. All interrupts are synchronized in INTC2.

Interrupt service routine address

Whenever an interrupt occurs, the ST40 CPU branches to the interrupt handling vector address determined by adding the fixed offset 0x600 to the vector base address (VBR) register. Each interrupt type is assigned a code which is stored in the INTEVT (Interrupt Event)register when the interrupt occurs. This enables the interrupt service routine to identify the interrupt source type.

The interrupt controller is responsible for mapping each interrupt to its code (INTEVT).

Figure 20 displays the ST40-300 interrupt network, and *Table 57* describes the internal interrupts with their INTEVT code.

Figure 20. ST40 interrupt network

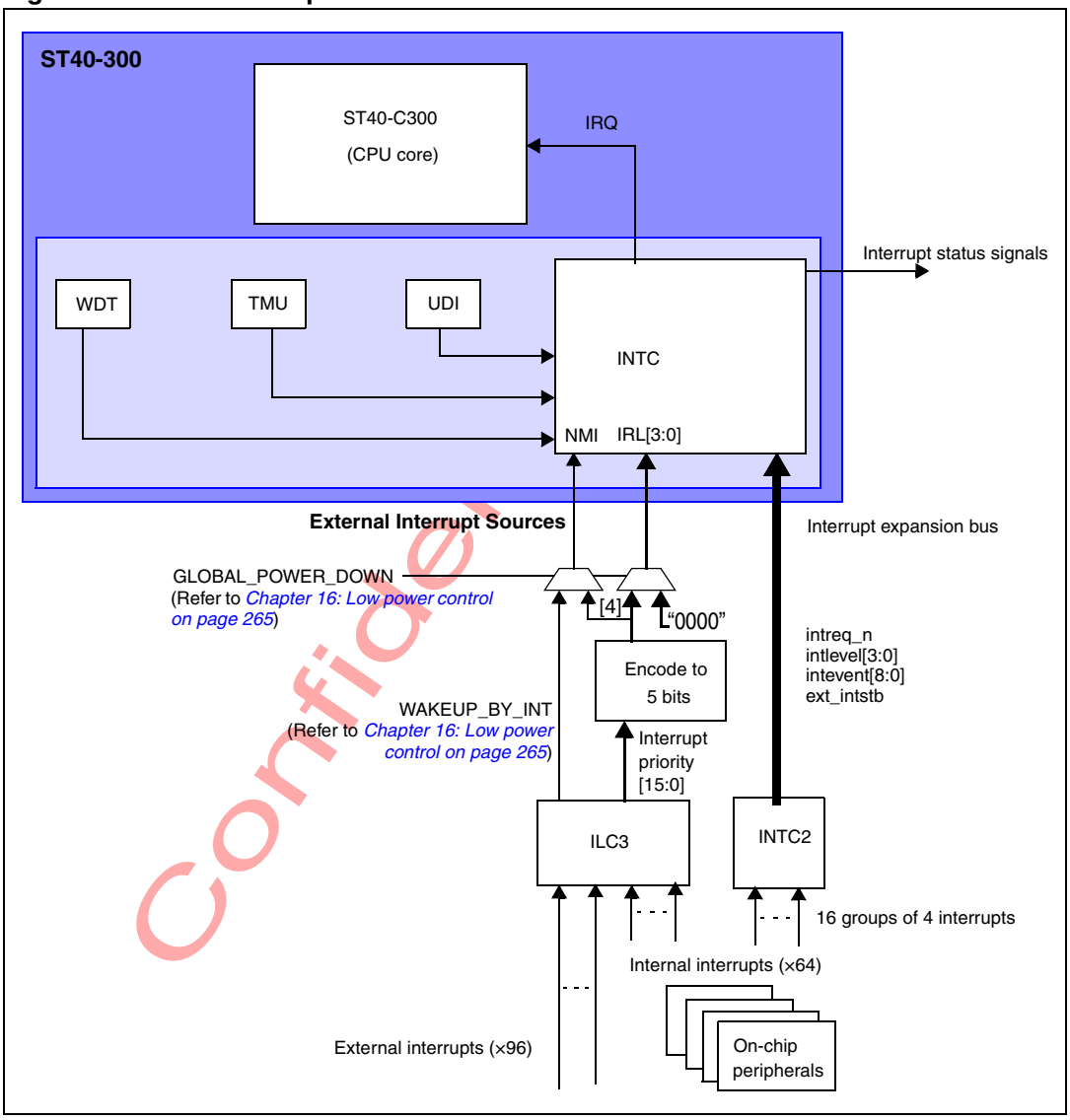


Table 57. ST40-300 P130 interrupts

Interrupt source		INTEVT code	IPR (bit numbers)	Interrupt priority (initial value)
NMI		0x1C0	-	16
IRL independent encoding	IRL0	0x240	IPRD[15:12]	15-0 (13)
	IRL1	0x2A0	IPRD[11:8]	15-0 (10)
	IRL2	0x300	IPRD[7:4]	15-0 (7)
	IRL3	0x360	IPRD[3:0]	15-0 (4)

Table 57. ST40-300 P130 interrupts (continued)

Interrupt source		INTEVT code	IPR (bit numbers)	Interrupt priority (initial value)
IRL	level encoding	0x200~0x3C0	-	1-15
TMU0	TUNI0	0x400	IPRA[15:12]	15-0 (0)
TMU1	TUNI1	0x420	IPRA[11:8]	15-0 (0)
TMU2	TUNI2	0x440	IPRA[7:4]	15-0 (0)
	TICPI2	0x460		
WDT	ITI	0x560	IPRB[15:12]	15-0 (0)
UDI	H-UDI	0x600	IPRC[3:0]	15-0 (0)

Table 58. ST40-300 on-chip peripheral interrupts

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group 0	AUDIO	I2S2SPDIF_INTERRUPT0	0xA00	INTPRI00[3:0]	INTREQ00[0]
		I2S2SPDIF_INTERRUPT1	0xA20		INTREQ00[1]
		I2S2SPDIF_INTERRUPT2	0xA40		INTREQ00[2]
		I2S2SPDIF_INTERRUPT3	0xA60		INTREQ00[3]
	eSATA	INTRQ_DMAC	0xA80	INTPRI00[7:4]	INTREQ00[4]
		INTRQ_HOSTC	0xB00		INTREQ00[5]
	DVP	DVP_INTERRUPT	0xB20		INTREQ00[6]
	Standalone 10 banks PIOs	STANDALONE_10_BANKS_PIO (10 ORED INTERRUPTS)	0xB40		INTREQ00[7]
	VDP AUX	AUX_VDP_END_PROCESSING_IRQ	0xB60	INTPRI00[11:8]	INTREQ00[8]
		AUX_VDP_FIFO_EMPTY_IRQ	0xB80		INTREQ00[9]
	Compo Capture	COMPO_CAP_BF	0xBA0		INTREQ00[10]
		COMPO_CAP_FF	0xBC0		INTREQ00[11]
	COMMs/PIO	PIO0_INTERRUPT	0xC00	INTPRI00[15:12]	INTREQ00[12]
		PIO1_INTERRUPT	0xC80	INTPRI00[19:16]	INTREQ00[13]
		PIO2_INTERRUPT	0xD00	INTPRI00[23:20]	INTREQ00[14]
group1	COMMs/PIO	PIO6_INTERRUPT	0x1000	INTPRI04[3:0]	INTREQ04[0]
		PIO5_INTERRUPT	0x1020		INTREQ04[1]
		PIO4_INTERRUPT	0x1040		INTREQ04[2]
		PIO3_INTERRUPT	0x1060		INTREQ04[3]
group2	SSC	SSC0_INTERRUPT	0x10E0	INTPRI04[7:4]	INTREQ04[7]
		SSC1_INTERRUPT	0x10C0		INTREQ04[6]
		SSC2_INTERRUPT	0x10A0		INTREQ04[5]
		SSC3_INTERRUPT	0x1080		INTREQ04[4]

Table 58. ST40-300 on-chip peripheral interrupts (continued)

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group3	COMMs/UART	UART0_INTERRUPT	0x1160	INTPRI04[11:8]	INTREQ04[11]
		UART1_INTERRUPT	0x1140		INTREQ04[10]
		UART2_INTERRUPT	0x1120		INTREQ04[9]
		UART3_INTERRUPT	0x1100		INTREQ04[8]
group4	COMMs/MAFE	MAFE_INTERRUPT	0x11E0	INTPRI04[15:12]	INTREQ04[15]
	COMMs/PWM	PWM_INTERRUPT	0x11C0		INTREQ04[14]
	COMMs/IRB	IRB_INTERRUPTS	0x11A0		INTREQ04[13]
		IRB_WAKEUP_INTERRUPT	0x1180		INTREQ04[12]
group5	COMMs/TTXT-DAA	TTXT_INTERRUPT	0x1260	INTPRI04[19:16]	INTREQ04[19]
		DAA_INTERRUPT	0x1240		INTREQ04[18]
	BLITTER DISPLAY	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	0x1220		INTREQ04[17]
	RESERVED	RESERVED	0x1200		INTREQ04[16
group 6	TS merger	TS_MERGER_INTERRUPT	0x12E0	INTPRI04[23:20]	INTREQ04[23]
	Ethernet GMAC	PMT_INT	0x12A0		INTREQ04[21]
		GMAC_MAC_INTR	0x12C0		INTREQ04[22]
	PCI	INT_PCI_DMA	0x1280		INTREQ04[20]
group7	PTI1	PTI1_INTERRUPT	0x1360	INTPRI04[27:24]	INTREQ04[27]
	ClockGen	DCXO INTERRUPT	0x1340		INTREQ04[26]
	MAILBOXes	LX_AUDIO_ST40_INTERRUPT	0x1320		INTREQ04[25]
		LX_DELTAMU_ST40_INTERRUPT	0x1300		INTREQ04[24]
group8	USB2	EHCI1_INTERRUPT	0x13E0	INTPRI04[31:28]	INTREQ04[31]
		OHCI1_INTERRUPT	0x13C0		INTREQ04[30]
	FDMA0/1	FDMA_1_MBOX_INTERRUPT	0x13A0		INTREQ04[29]
		FDMA_0_MBOX_INTERRUPT	0x1380		INTREQ04[28]
group9	Audio	SPDIFPLYR_INTERRUPT	0x1460	INTPRI08[3:0]	INTREQ08[3]
		PCMRDR_INTERRUPT	0x1440		INTREQ08[2]
		PCMPLYR1_INTERRUPT (AUDIO SS)	0x1420		INTREQ08[1]
		PCMPLYR0_INTERRUPT (TVOUT SS)	0x1400		INTREQ08[0]

Table 58. ST40-300 on-chip peripheral interrupts (continued)

Group	Interrupt source		INTEVT code	IPR (bit numbers)	INTREQ/INTMSK (bit number)
group10	VIDEO DELTAMU	DELTAMU_MBE_INTERRUPT	0x14E0	INTPRI08[7:4]	INTREQ08[7]
		DELTAMU_PP_INTERRUPT	0x14C0		INTREQ08[6]
	NAND Controller	INT_NAND	0x14A0		INTREQ08[5]
	RESERVED	RESERVED	0x1480		INTREQ08[4]
group11	TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	0x1560	INTPRI08[11:8]	INTREQ08[11]
		MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	0x1540		INTREQ08[10]
	VDP MAIN DISPLAY PIPE	MAIN_VDP_END_PROCESSING_IRQ	0x1520		INTREQ08[9]
		MAIN_VDP_FIFO_EMPTY_IRQ	0x1500		INTREQ08[8]
group12	HDMI/HDCP	HDCP_INTERRUPT	0x15E0	INTPRI08[15:12]	INTREQ08[15]
		HDMI_INTERRUPT	0x15C0		INTREQ08[14]
		HDMI_CEC_INT	0x15A0		INTREQ08[13]
		HDMI_CEC_WAKEUP_INT	0x1580		INTREQ08[12]
group13	RESERVED	RESERVED	0x1660	INTPRI08[19:16]	INTREQ08[19]
		RESERVED	0x1640		INTREQ08[18]
		RESERVED	0x1620		INTREQ08[17]
	PTI0	PTI0_INTERRUPT	0x1600		INTREQ08[16]
group14	RESERVED	RESERVED	0x16E0	INTPRI08[23:20]	INTREQ08[23]
	RESERVED	RESERVED	0x16C0		INTREQ08[22]
	RESERVED	RESERVED	0x16A0		INTREQ08[21]
	RESERVED	RESERVED	0x1680		INTREQ08[20]
group15	BLITTER DISPLAY	BDISP_CQ1_IRQP OR BDISP_CQ2_IRQP	0x1760	INTPRI08[27:24]	INTREQ08[27]
	RESERVED	RESERVED	0x1740		INTREQ08[26]
	USB1	EHCI_INTERRUPT	0x1720		INTREQ08[25]
		OHCI_INTERRUPT	0x1700		INTREQ08[24]
group16	RESERVED	RESERVED	0x17E0	INTPRI08[31:28]	INTREQ08[31]
	Key Scanner	KEY_SCANNER_INTERRUPT	0x17C0		INTREQ08[30]
	RESERVED	RESERVED	0x17A0		INTREQ08[29]
		RESERVED	0x1780		INTREQ08[28]

11.1.3 DeltaMU and LX_AUDIO ST231 interrupt network

The ST231 accepts 60 external interrupts (from 63 to 3). Interrupts 0 to 2 are Reserved to the ST231 internal timers. All the interrupts are maskable but with a single level of priority. Multiple level priority must be implemented in the software.

When used as an application processor, the DeltaMU ST231 processor receives a subset of the internal interrupts from the ST40 processor.

The interrupts are active high and are re-synchronized in the ST231 clk_bus clock domain.

When used as an application processor, the DeltaMU ST231 processor receives the same internal interrupts as the ST40 processor except the interrupts generated by the DeltaMU coprocessors, the MES, ICAM3 interrupts, and Blitter Display interrupts.

The DeltaMu ST231 also receives the external interrupts through the ILC3 interrupt controller.

The AUDIO_LX receives audio peripherals and FDMA interrupts in order to manage audio applications without relying on the ST40 Host. Also, it executes soft modem (MAFE, DAA interrupts)

Table 59 describes the mapping of the interrupts on the DeltaMU ST231 interrupt controller.

Table 59. DeltaMU ST231 interrupts

Interrupt source		INT number
ST231 Timers	TIMER0_INTERRUPT	0
	TIMER1_INTERRUPT	1
	TIMER2_INTERRUPT	2
	RESERVED	3
Comms/PIO	PIO0_INTERRUPT	4
	PIO1_INTERRUPT	5
	PIO2_INTERRUPT	6
	PIO3_INTERRUPT	7
	PIO4_INTERRUPT	8
	PIO5_INTERRUPT	9
SSC	SSC0_INTERRUPT	10
	SSC1_INTERRUPT	11
	SSC2_INTERRUPT	12
	SSC3_INTERRUPT	13
Comms/UART	UART0_INTERRUPT	14
	UART1_INTERRUPT	15
	UART2_INTERRUPT	16
	UART3_INTERRUPT	17
Comms/MAFE	MAFE_INTERRUPT	18
Comms/PWM	PWM_INTERRUPT	19

Table 59. DeltaMU ST231 interrupts (continued)

Interrupt source		INT number
Comms/IRB	IRB_INTERRUPT	20
	IRB_WAKEUP_INTERRUPT	21
Comms/TTXT	TTXT_INTERRUPT	22
Comms/DAA	DAA_INTERRUPT	23
DVP	DVP_INTERRUPT	24
TS Merger	TS_MERGER_INTERRUPT	25
Ethernet GMAC	GMAC_MAC_INTR	26
	PMT_INT	27
ClockGen	DCXO_INTERRUPT	28
MAILBOX	ST40_TX_DELTAMU_INTERRUPT	29
PTI1	PTI1_INTERRUPT	30
FDMAs	FDMA_1_MBOX_INTERRUPT	31
	FDMA_0_MBOX_INTERRUPT	32
Audio	I2S2SPDIF_INTERRUPT0 OR I2S2SPDIF_INTERRUPT1 OR I2S2SPDIF_INTERRUPT2 OR I2S2SPDIF_INTERRUPT3	33
	SPDIFPLYR_INTERRUPT	34
	PCMRDR_INTERRUPT	35
	PCMPLYR1_INTERRUPT	36
	PCMPLYR0_INTERRUPT	37
RESERVED	RESERVED	38
TVOUT/VTGs	AUX_VTG_INTERRUPT (1) OR AUX_VTG_INTERRUPT (0)	39
	MAIN_VTG_INTERRUPT (1) OR MAIN_VTG_INTERRUPT (0)	40
Main Video Display Pipe	VDP_END_PROCESSING_IRQ	41
	VDP_FIFO_EMPTY_IRQ	42
HDMI/HDCP	HDCP_INTERRUPT	43
	HDMI_INTERRUPT	44
	HDMI_CEC_IRQ	45
	HDMI_CEC_WAKEUP_IRQ	46
BLITTER DISPLAY	BDISP_AQ1_IRQP OR BDISP_AQ2_IRQP OR BDISP_AQ3_IRQP OR BDISP_AQ4_IRQP	47
RESERVED	RESERVED	48
	RESERVED	49
	RESERVED	50

Table 59. DeltaMU ST231 interrupts (continued)

Interrupt source		INT number
PTI0	PTI0_INTERRUPT	51
RESERVED	RESERVED	54
RESERVED	RESERVED	55
USB1	EHCI0_INTERRUPT	56
	OHCI0_INTERRUPT	57
PADS	NMI_INTERRUPT	58
	RESERVED	59
External interrupts	EXT_INTERRUPT[0]	60
	EXT_INTERRUPT[1]	61
	EXT_INTERRUPT[2]	62
	EXT_INTERRUPT[3]	63

The *Table 60* describes the mapping of the interrupts on the LX_AUDIO ST231 interrupt controller.

Table 60. LX_AUDIO ST231 interrupts

Interrupt source		INT number
ST231 timers	TIMER0_INTERRUPT	0
	TIMER1_INTERRUPT	1
	TIMER2_INTERRUPT	2
MAILBOX1	ST40_LX_AUDIO_INTERRUPT	3
RESERVED	RESERVED	17-4
Comms/MAFE	MAFE_INTERRUPT	18
RESERVED	RESERVED	22-19
Comms/DAA	DAA_INTERRUPT	23
RESERVED	RESERVED	30-24
Audio	RESERVED(CPXM_INTERRUPT)	31
	I2S2SPDIF_INTERRUPT	32
FDMA	FDMA_1_MBOX_INTERRUPT	33
	FDMA_0_MBOX_INTERRUPT	34

Table 60. LX_AUDIO ST231 interrupts (continued)

Interrupt source		INT number
Audio	SPDIFPLYR_INTERRUPT0	35
	SPDIFPLYR_INTERRUPT1	36
	SPDIFPLYR_INTERRUPT2	37
	SPDIFPLYR_INTERRUPT3	38
	PCMRDR_INTERRUPT	39
	PCMPLYR1_INTERRUPT	40
	PCMPLYR0_INTERRUPT	41
RESERVED	RESERVED	42-51
RESERVED	RESERVED	54
	RESERVED	55
RESERVED	RESERVED	56-62
Reserved	RESERVED	63

12 FDMA

12.1 Overview

The STi7197 integrates two multiple-channel general-purpose (Flexible) DMA engines, FDMA0 and FDMA1. Each FDMA engine is a general-purpose direct memory access controller capable of supporting 16 independent DMA channels. Their purpose is to move data efficiently from memory to memory, memory to peripheral, and peripheral to peripheral.

The FDMA supports free-running and paced transfers. The CPU sets up each DMA transfer by writing linked-lists of data structures into main memory, then the CPU initializes the transfer by writing the pointer to the first node in the control word interface (CWI) of the FDMA. The FDMA then executes the necessary operations to complete the transfer and informs the CPU (through interrupts) after completion of the transfer.

The FDMA1 includes video stream parsing functionalities:

- video PES parsing and start-code detection (PES/SCD) for H264, VC1, AVS, and MPEG2
- dual PES parsing channel on same FDMA

12.1.1 FDMA0 and FDMA1 partitioning

In the STi7197, one FDMA is dedicated to serve real-time processes while the other FDMA handles the other processes, such as PES parsing, free-running, and non-critical paced channels.

The partitioning between FDMA0 and FDMA1 is as follows:

- FDMA0—real time paced channels: PCM players 0, 1, S/PDIF players, and SWTS (or playback)
- FDMA1—free-running channels, PES parsing, and non-real-time paced channels (that is, COMMS and PCI)

This partitioning is defined by software and is flexible. The Dreq crossbar-router, in front of the FDMAs, can route any paced peripheral Dreq signal to any FDMA Dreq input.

12.1.2 Peripheral and memory access

Each FDMA has two STBus Type-2 initiator ports. The Port0 (high priority port) has a direct connection to the paced peripherals. This direct connection minimizes the latency between the FDMA and peripherals. While defining the FDMA node, the Port0 is used to access the peripherals and Port1 (low priority port) is used to access the memory.

LMI can be accessed by FDMA0 and FDMA1.

12.1.3 FDMA processing power

The FDMA slim core frequency is configurable up to 450 MHz.

12.1.4 FDMA firmware

FDMA0 uses real-time firmware, and FDMA1 uses non-real-time firmware.

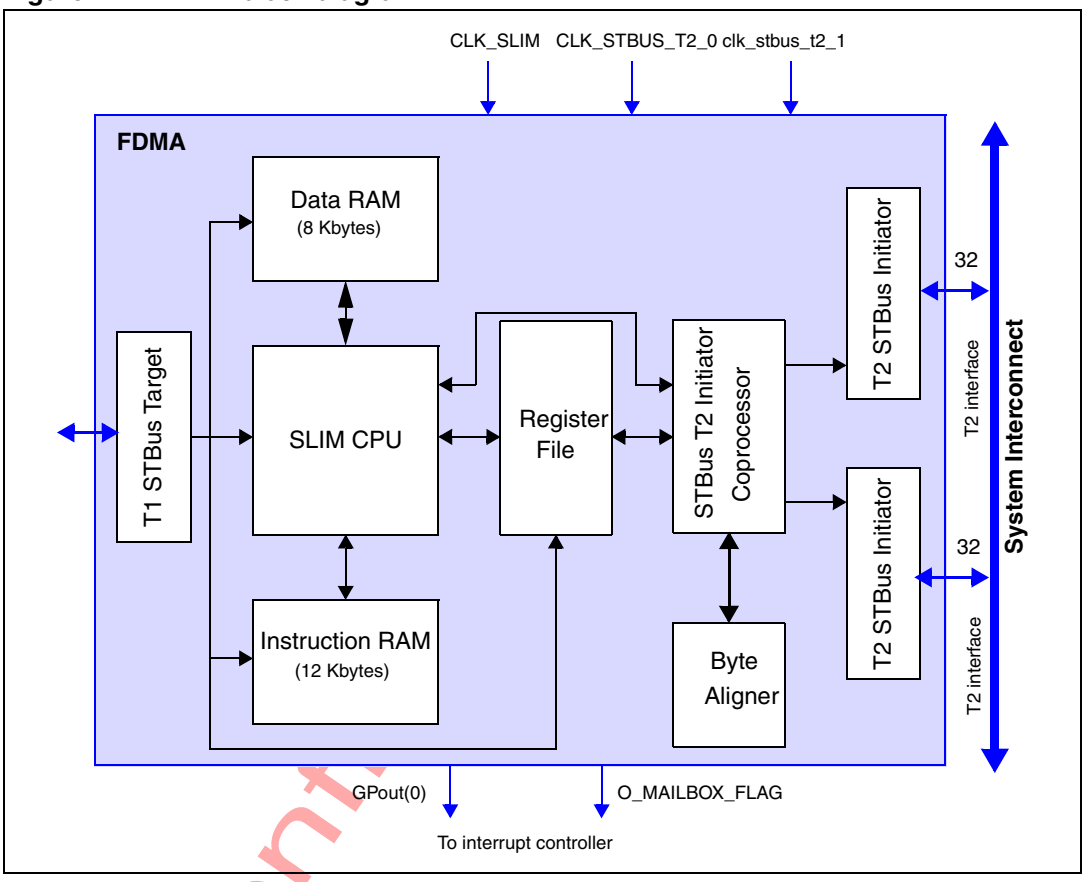
12.1.5 FDMA features

Following are the FDMA features:

- Support for 16 concurrent DMA channels
- Free-running transfer of aligned or unaligned data structure
  - Single location (0D)
  - Incrementing linear arrays (1D)
  - Incrementing rectangular arrays (2D)
- Transfer units of 1 to 32 bytes
- Up to 128 bytes message support
- Programmable opcode for paced transfer, support for up to 30 request generating peripherals (Dreq)
- Linked-list control allowing complex transfer sequence
- Video PES parsing (VC1, H264, MPEG2, AVS) on channel 0 and 1
- Audio compressed or PCM data output through S/PDIF player
- Hold-off support per channel
- Secure/insecure transfer support
- NAND controller channel for AFM mode transfer to/from NAND devices

12.2 Block diagram

Figure 21. FDMA block diagram



Each FDMA comprises a SLIM CPU, an instruction memory, a data memory, peripherals, an STBus T1 target interface, and a SLIM STBus initiator coprocessor.

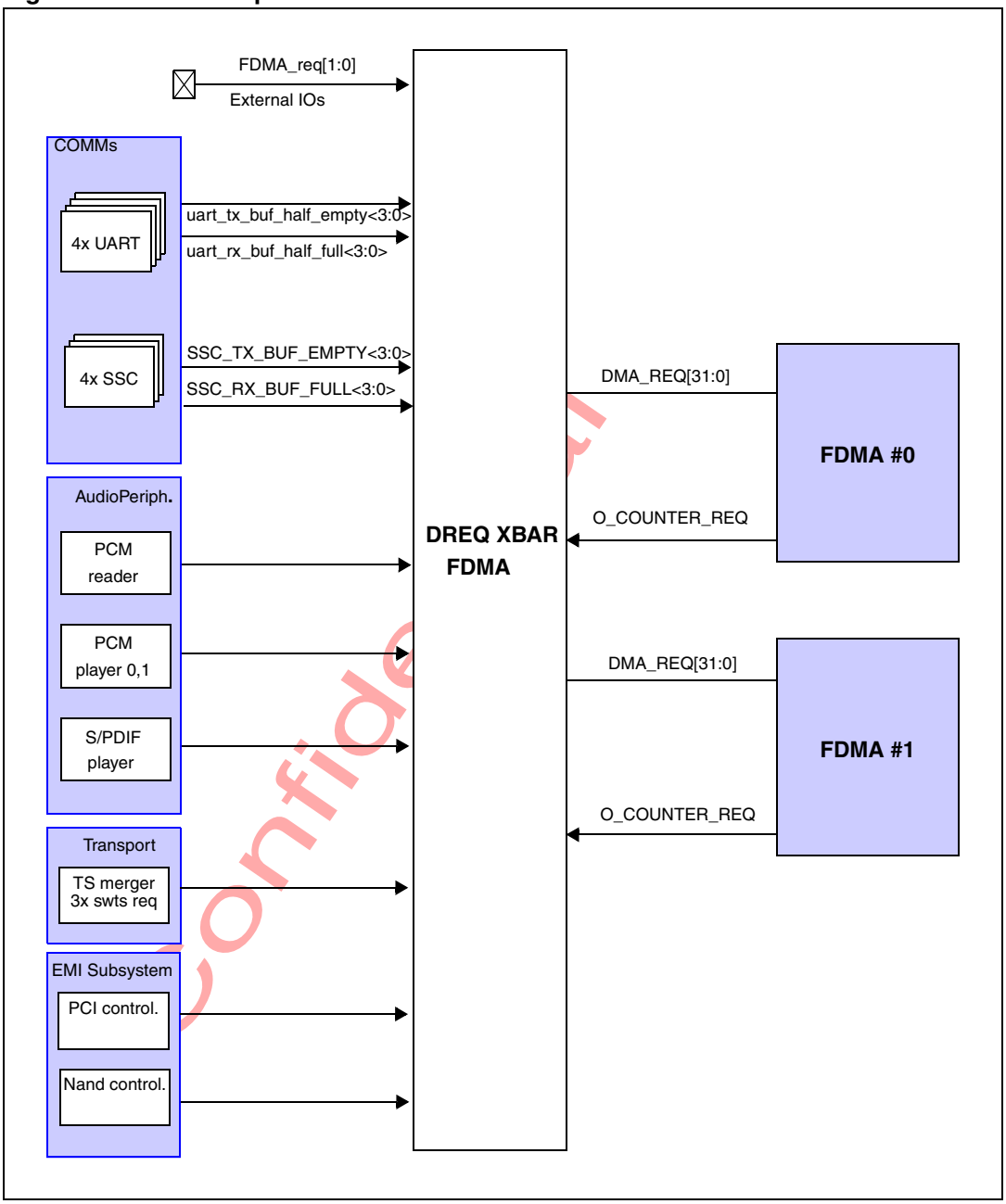
Each FDMA interfaces with the STBus interconnect through two STBus T2 initiator ports to execute the data transfers and through one STBus T1 target port to access the FDMA2 registers and memories.

Each STBus port has its own separate asynchronous clock input.

12.3 DMA requests

The FDMA receives a number of requests where pacing is required for flow control in the system. This signal is a simple high-level sensitive signal used in conjunction with a hold-off counter. The blocks generating a request signal are the audio peripherals (PCM players, PCM reader, and S/PDIF player), transport TSMerger (software stream), UARTs, SSCs, PCI controller, NAND controller and external DMA requests.

Figure 22. FDMA requests



The FDMA accepts up to 30 DMA requests or events that are used to drive the paced channels of the FDMA. Requests 0 and 31 are reserved for the counter request and are internally connected to the FDMA counter to provide timed DMA channels. Request #0 has the lowest priority and request #31 has the highest priority.

Table 61. FDMA request configuration

Unit	PACING SIGNAL	Xbar Input Index	FDMA #0	FDMA #1	FDMA DREQ line index	Opcode	Transfer Size	Comments
PCI controller	PCI_HALF_FULL	52	x		10	ST32	ST32 x4	
NAND controller	NAND_AFM_DATA_REQ	50		x	28	ST32	ST32 x1	Data request in Advanced Flex mode
	NAND_AFM_SEQ_REQ	49		x	27	LD32	LD32 xn	Sequence request in Advanced Flex mode
IRB/UHF	IRB_UHF_RX_BUFFER_FULL	46		x	19	LD4	LD4 x1	IRB requests
	IRB_UHF_RX_BUFFER_HALF8FULL	45		x	18	LD4	LD4 x1	
TeleText DENC #0	TELETEXT_DREQ	42		x	30	ST4	ST4 x11	Ttxt FIFO is 2x48 bytes = 2 lines
HDMI S/PDIF Player	HDMI_SPDIF_DREQ	40	x		30	ST4	ST4 x4	Includes a 24 bytes FIFO
HDMI PCM Player #0	HDMI_PCM_DREQ	39	x		29	ST4	ST4 x20	Includes a 160 bytes FIFO
PCM reader	PCMIN_DREQ	37	x		27	LD4	LD4 x2	Includes a 8 bytes FIFO
PCM Player #1	PCMOUT1_DREQ	34	x		23	ST4	ST4 x20	Includes a 160 bytes FIFO
CSS/CPxM encryption	CPXM_ENCRYPT_OUT_DREQ	32	x		21	LD4	LD4 x32	128 bytes fifo
	CPXM_ENCRYPT_IN_DREQ	31	x		20	ST4	ST4 x32	
CSS/CPxM decryption	CPXM_DECRYPT_OUT_DREQ	30	x		19	LD4	LD4 x32	128 bytes fifo
	CPXM_DECRYPT_IN_DREQ	29	x		18	ST4	ST4 x32	
External DMA req	EXTDMAREQ1_DREQ	28	x		16	ST/LD32	ST/LD32 x4	
	EXTDMAREQ0_DREQ	27		x	21	ST/LD32	ST/LD32 x4	
	EXTDMAREQ2_DREQ	3	x		17	ST/LD32	ST/LD32 x4	
	EXTDMAREQ3_DREQ	4		x	20	ST/LD32	ST/LD32 x4	
UART#3 Tx	UART3_TX_HALF_EMPTY	26		x	16	ST4	ST4 x1	
UART#2 Tx	UART2_TX_HALF_EMPTY	25		x	15	ST4	ST4 x1	
UART#1 Tx	UART1_TX_HALF_EMPTY	24		x	14	ST4	ST4 x1	
UART#0 Tx	UART0_TX_HALF_EMPTY	23		x	13	ST4	ST4 x1	
UART#3 Rx	UART3_RX_HALF_FULL	22		x	12	LD4	LD4 x1	
UART#2 Rx	UART2_RX_HALF_FULL	21		x	11	LD4	LD4 x1	
UART#1 Rx	UART1_RX_HALF_FULL	20		x	10	LD4	LD4 x1	
UART#0 Rx	UART0_RX_HALF_FULL	19		x	9	LD4	LD4 x1	

Table 61. FDMA request configuration (continued)

Unit	PACING SIGNAL	Xbar Input Index	FDMA #0	FDMA #1	FDMA DREQ line index	Opcode	Transfer Size	Comments
SSC#3 Tx	SSC3_TX_BUF_EMPTY	17		x	7	ST4	ST4 x1	
SSC#2 Tx	SSC2_TX_BUF_EMPTY	16		x	6	ST4	ST4 x1	
SSC#1 Tx	SSC1_TX_BUF_EMPTY	15		x	5	ST4	ST4 x1	
SSC#0 Tx	SSC0_TX_BUF_EMPTY	14	x		15	ST4	ST4 x1	
SSC#3 Rx	SSC3_RX_BUF_FULL	12		x	3	LD4	LD4 x1	
SSC#2 Rx	SSC2_RX_BUF_FULL	11		x	2	LD4	LD4 x1	
SSC#1 Rx	SSC1_RX_BUF_FULL	10		x	1	LD4	LD4 x1	
SSC#0 Rx	SSC0_RX_BUF_FULL	9	x		14	LD4	LD4 x1	
TS Merger	SWTS0_REQ	7		x	24	ST32	ST32 x1	Software Transport Stream play through PTI4L.
	SWTS1_REQ	6		x	23	ST32	ST32 x1	
	SWTS2_REQ	5		x	22	ST32	ST32 x1	
HDMI AVI buffer	AVI_BUFF_EMPTY	2		x	26	ST4	ST4 x1	Should be handled by Host CPU not FDMA
FDMA #1 counter	FDMA1_COUNTER_REQ	1		x	0			Connects counter output to dreq #0
FDMA #0 counter	FDMA0_COUNTER_REQ	0	x		0			Connects counter output to dreq #0

Table 62. FDMA requests table

Request source	REQUEST SIGNAL	Request index	Description
FDMA# counter	O_COUNTER_REQ	31:0	FDMA internal counter output, used for timed DMA-channel.
FDMA# cross-bar	REQ_OUT[31:0]		
FDMA# counter	O_COUNTER_REQ		FDMA internal counter output, used for timed DMA-channel.

Note: # in Table 62 is 0 or 1.

12.4 Examples of DMA Data flow

The following figures describe various DMA data flows.

Figure 23. DMA data flows (I)

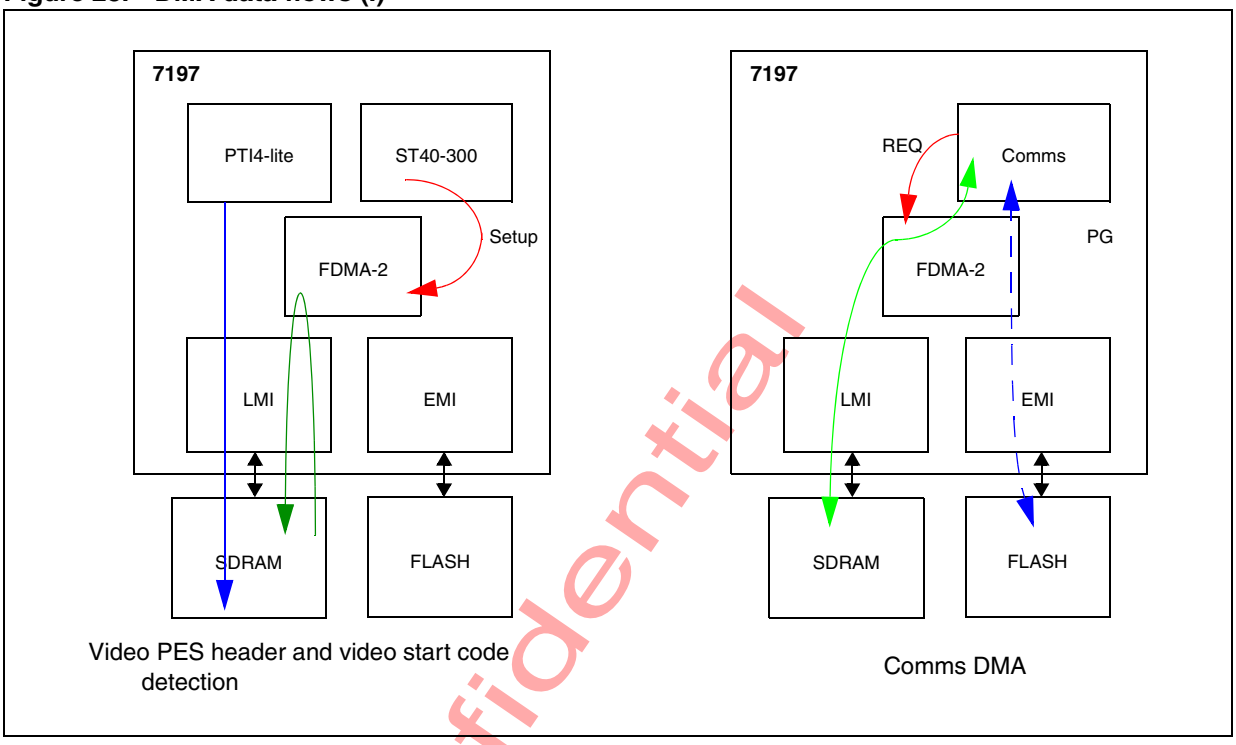
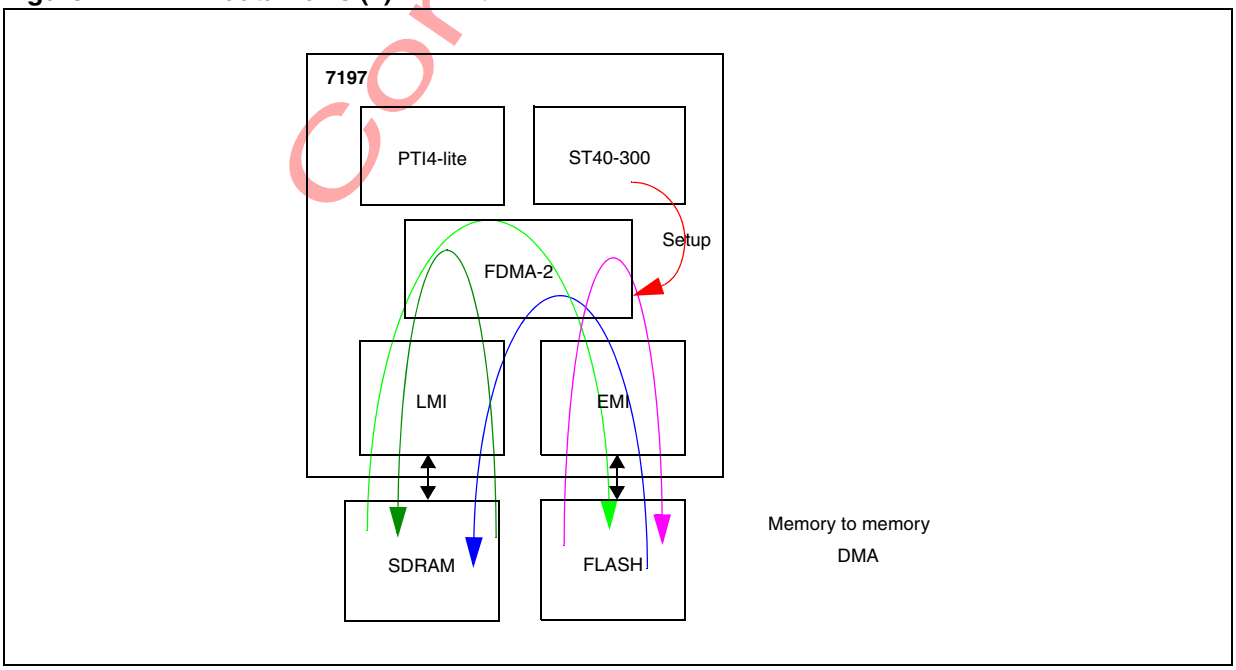


Figure 24. DMA data flows (II)



13 Clocking

The STi7197 includes four clock generator subsystems:

- ClockGen A: 2× PLLs main CPU, transport, and interconnect clocks
- ClockGen B: 2× FreqSynth: video, display, and peripheral clocks
- ClockGen C: 1× FreqSynth and audio clocks
- ClockGen D: 1× PLL memory clocks

13.1 Clock input/output pins

The SYSCLKIN/SYSCLKOSC pair is a crystal interface, a part of the SATA analog interface, integrating an oscillator requiring a 30 MHz crystal. In addition to driving the SATA and two USB interfaces, the clock can also be used as a reference clock to generate the Group A, B, C, and D clocks.

The SYSCLKINALT input provides an alternate reference clock for the Group A, B, C, and D clocks instead of using an oscillator clock inside the SATA Phy. The default state is to use the 30 MHz SATA clock. However, an alternate reference clock can be selected through a configuration register. The SYSCLKINALT pin is driven by either a 27 MHz fixed or voltage controllable oscillator or a fixed 30 MHz oscillator. A PWM output is provided as a part of an external VCXO configuration.

The internal clocks can be observed:

- ClockGen A through the TRIGGEROUT pad
- ClockGenB through the SYSCLKOUT pad
- ClockGen C frequency synthesizer #2 through the PIO10[3] pad
- ClockGen D through the LMICLKOUT pad

Encoder clock recovery

The STi7197 integrates a clock recovery module to recover the encoder clock. This module (DCXO) uses the digitally controllable frequency synthesizers and an integrated digital clock recovery module. This feature replaces the external VCXO functionality and allows the usage of a fixed oscillator. Nevertheless, the external VCXO functionality is still available.

When the external VCXO functionality is used, the VCXO oscillator must be connected to the SYSCLKINALT, and the SYSCLKIN is connected either to a fixed oscillator or to the VCXO oscillator.

When the DCXO is used the SYSCLKIN pin is connected to a fixed oscillator, and the SYSCLKINALT is connected either to the SYSCLKIN or left unconnected (in which case the SATA/USB 30 MHz clock is used).

The system counter inside the programmable transport interface (PTI), which is used to compare the arriving PCRs, is clocked by the recovered 27 MHz clock generated by the Clock Generator B.

Figure 25. STi7197 clocking scheme sources with optional external VCXO

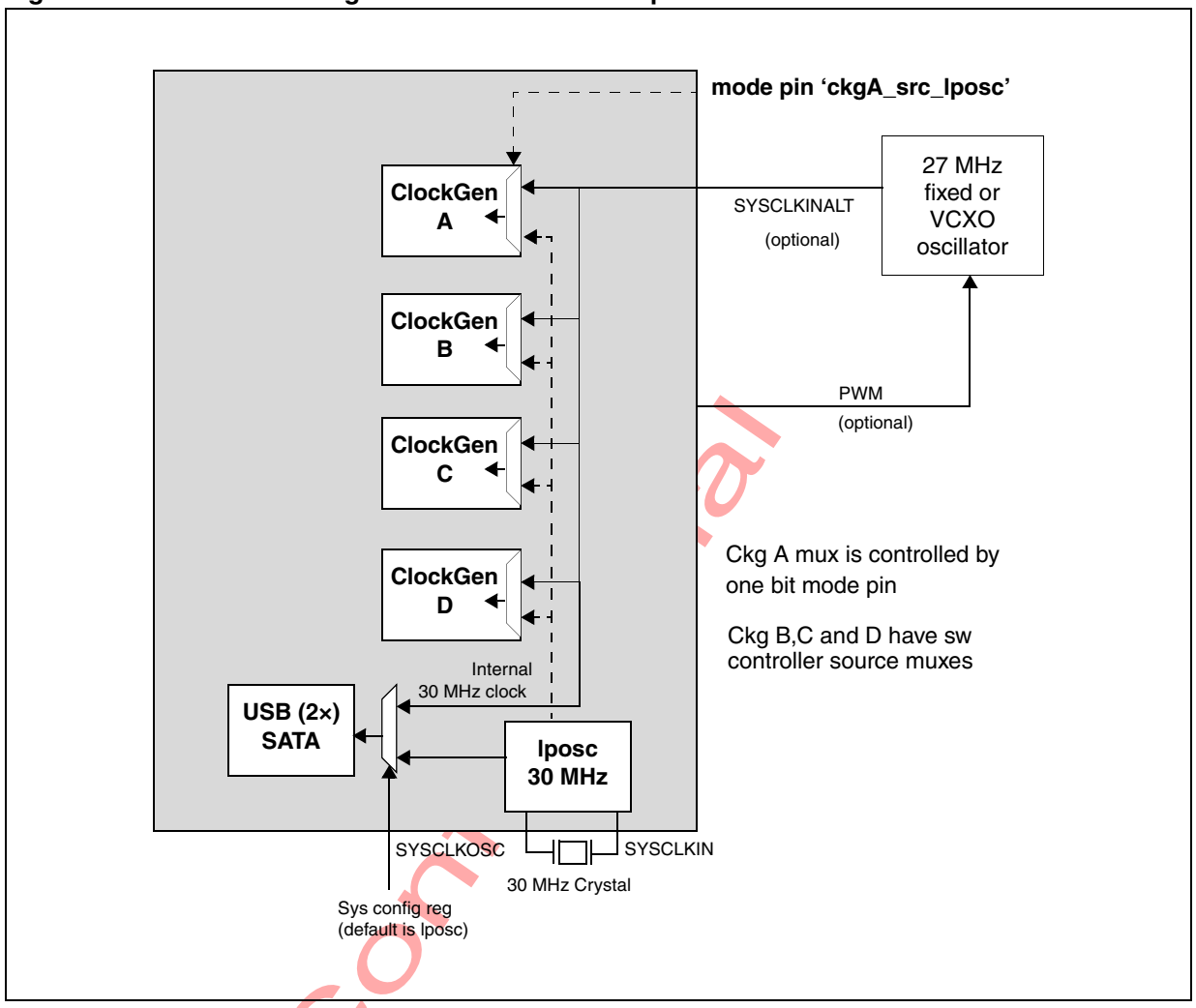


Table 63. STi7197 clocking scheme sources

ClockGen module	Reset default STi7197	Clock selection
A	Selection by modepin	STi7197 has mode pin to select default clock reference for ClockGen A
B	SATA/USB LP-Osc 30 MHz	ClockGen B config register
C	SATA/USB LP-Osc 30 MHz	Audio SS config register
D	SATA/USB LP-Osc 30 MHz	System config register
USB/SATA	SATA/USB LP-Osc 30 MHz	System config register

13.2 Clock domains

The *Table 64* describes the clocking of the functional units integrated in STi7197. Column S is the clock source, indicating A, B, C, D for ClockGen, or T for Tap.

Table 64. Functional blocks clocking

Block	Clock pin	Clock signal	S	Max frequency	Comment
TMC					
TMC	TCK	TCK	T	50 MHz	JTAG clock from pad
MAIN Interconnect and NOC					
STNoC		CLK_IC_STNOC	A	400 MHz	CPU processing clock
N_CPU		CLK_IC_IF_200	A	200 MHz	-
N_PERIPH		CLK_IC_IF_100	A	100 MHz	-
RESERVED		RESERVED		-	-
N_DVP		CLK_IC_DISP_200	A	-	-
N_DISPLAY		CLK_IC_DISP_200	A	-	-
N_COMPO		CLK_IC_COMPO_200	A	-	-
N_DMU		CLK_BLIT_PROC	A	266 MHz	-
N_PCI		CLK_EMI_MASTER	A	-	-
N_PCI_TS		CLK_IC_TS_200	A	-	-
N_TS		CLK_IC_TS_200	A	-	-
N_IF		CLK_IC_IF_100	A	-	-
N_BDISP		CLK_IC_BDISP_200	A	-	-
N_CPU_REG		CLK_IC_IF_100	A	-	-
SYSTEM					
SYSCLKINALT	pad	SYSCLKINALT	IN	30 MHz	These are the clock sources, from the two possible inputs Clock from pad Clock from SATA/USB osc
LPOSC	ZI	CLK_LPOSC_30		30 MHz	
ClockGenA	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	-
	CLK_OSC_A	NOT USED		-	-
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED		-	-
ClockGenB	CLK_IC	CLK_IC_IF_100	A	-	STBus clock
	CLK_OSC_A	NOT USED		-	-
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED		-	-
ClockGen C	CLK_OSC_A	NOT USED		-	-
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED		-	-

Table 64. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
ClockGenD	CLK_OSC_A	NOT USED		-	-
	CLK_OSC_B	CLK_LPOSC_30		30 MHz	from SATA/USB oscillator
	CLK_OSC_C	SYSCLKINALT		27/30 MHz	direct from pad crystal
	CLK_OSC_D	NOT USED		-	-
MAIN CPU					
SH4-300	CLK_ST40_ICK	CLK_SH4_ICK	A	450 MHz	CPU processing clock
	CLK_ST40_PCK	CLK_IC_IF_100	A	100 MHz	Interface clock
Mailbox	CLK	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
DMA					
BlitterDisplay	IC_CK	CLK_IC_BDISP_200	A	200 MHz	Type 3 interconnect clock
	CPU_CK	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	BDISP_CK	CLK_BLIT_PROC	A	266 MHz	Bdisp processing clock
FDMA0	CLK_SLIM	CLK_FDMA0	A	450 MHz	SLIM Processing clock
	CLK_STBUS_T2_0	CLK_IC_IF_100	A	100 MHz	High priority FDMA port
	CLK_STBUS_T2_1	CLK_IC_TS_200	A	200 MHz	Low priority FDMA port
	CLK_STBUS_T1	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
FDMA1	CLK_SLIM	CLK_FDMA1	A	450 MHz	SLIM Processing clock
	CLK_STBUS_T2_0	CLK_IC_IF_100	A	100 MHz	High priority FDMA port
	CLK_STBUS_T2_1	CLK_IC_TS_200	A	200 MHz	Low priority FDMA port
	CLK_STBUS_T1	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
DISPLAYS COMPOSITION					
HD Display	CLK_PROC	CLK_DISP_PIPE_200	A	200 MHz	Display pipeline processing clock
	CLK_SYS	CLK_IC_DISP_200	A	200 MHz	Type 3 interconnect clock
	CLK_PIX	CLK_DISP_HD	B	148.5 MHz	Display-to-Compositor pixel clock
	CLK_REG	CLK_IC_DISP_200	A	200 MHz	Type 1 interconnect clock
SD Display	CLK_DISP	CLK_DISP_PIPE_200	A	200 MHz	Display pipeline processing clock
	CLK_IC	CLK_IC_DISP_200	A	200 MHz	Type 3 interconnect clock
	CLK_PIXEL	CLK_DISP_ID or CLK_DISP_HD	B	13.5 MHz in SD and 148.5 MHz in HD (PIP)	Display-to-Compositor pixel clock
	CLK_REG	CLK_IC_DISP_200	A	200 MHz	Type 1 interconnect clock

Table 64. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
Compositor	ST_CK	CLK_IC_COMPO_200	A	200 MHz	Type 3 Interconnect clock
	MAIN_CK	CLK_DISP_HD	B	148.5 MHz Max	Main mixer (HD) pixel clock
	AUX_CK	CLK_DISP_ID	B	108 MHz Max	Aux mixer (SD) pixel clock
	VP2_CK	CLK_DISP_ID	B	108 MHz Max	Video2 pixel clock (SD or HD)
	GDP3_CK	CLK_DISP_HD or CLK_DISP_ID (CLK_GDP3)	B	148.5 MHz	GDP3 pixel clock (HD or SD)
VIDEO OUTPUT STAGE					
DENC	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	PIX_CLK	CLK_PIX_SD	B	27MHz Max	DENC processing clock
	PIX_CLK_FROM _PAD	VIDINCLK FROM PAD	B	27 MHz	This clock is used by DVP in functional mode. Used for testing also.
RGB-to-YCbCr 601/709/240M	CLK_DISP_HD	CLK_DISP_HD	B	148.5 MHz	HD Display Clock
DWCS AWG	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 interconnect clock
	CLK_PIX	CLK_PIX_SD	B	27MHz	SD pixel input clock
UpSampler	CLK_DISP_HD	CLK_DISP_HD	B	148.5 MHz	HD pixel input clock
	CLK_PIXEL_SD	CLK_PIX_SD	B	27 MHz	SD pixel input clock
	CLK_PIXEL_HD	CLK_PIX_HD	B	148.5 MHz	Pixel output clock
VTG0	CLK_DISP	CLK_DISP_HD	B	148.5 MHz	HD display clock
VTG1	CLK_DISP	CLK_DISP_SD	B	13.5 MHz	ID display clock
HD Video DAC	CLK	CLK_PIX_HD	B	148.5 MHz	HD Video DAC sampling clock
SD Video DAC	CLK	CLK_PIX_SD	B	108 MHz	SD Video DAC sampling clock
AUDIO DECODING					
LX- Audio	CLK_CPU	CLK_LX_AUD_CPU	A	450 MHz Max	LX processing clock
	CLK_BUS	CLK_IC_100	A	100 MHz	Peripheral Interconnect clock
Audio Glue	CLK_IC	CLK_IC_IF_100	A	100 MHz	Peripheral Interconnect clock in audio peripherals
PCM player 1 see audio clocking scheme	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Interconnect clock
	CLK_PCM	CLK_PCM1	C	50 MHz Max	PCM oversampling clock (256xFs) = 256x 192kHz

Table 64. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
PCM reader see audio clocking scheme	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Interconnect clock
	CLK_I2S	I2S_SCLK	C	5 MHz	PCM input serial clock
Audio DAC see audio clocking scheme	MCLK	CLK_PCM1	C	256 x Fs, 15 MHz Max	Oversampling clock (Fs = 48 kHz Max)
VIDEO DECODING					
DeltaMu ST231	CLK_CPU	CLK_LX_DMU_CPU	A	450 MHz	LX Processing clock
	CLK_BUS	CLK_IC_IF_100	A	100 MHz	Peripheral Interconnect clock
DeltaMu Hdw	CLK_VID	CLK_VID	A	225 MHz (clk_lx_dh_cpu/2)	DeltaMu Hdw processing clock
	CLK_BUS (CLK_IC_DELTA_200 ON SS)	CLK_BLIT_PROC	A	266 MHz	DeltaMu STBus initiator and target port clock
	CLK_PP	CLK_PP	B	150 MHz	DeltaMu Hdw Pre-processor clock
TRANSPORT					
TSMerger	CLK_SYSTEM	CLK_IC_TS_200	A	200 MHz	Interconnect clock
	CLK_27MHZ	CLK_PIX_SD	B	27 MHz	For free running and programmable counters (timestamp)
PTI	CLK_SYSTEM	CLK_IC_TS_200	A	200 MHz	200 MHzType 1 & 2 Interconnect clock
	CLK_TIMER	CLK_PIX_SD	B	27 MHz Max	PCR Timer clock for AV services
RESERVED	RESERVED	RESERVED		-	-
CONNECTIVITY					
GMAC	CLK100	CLK_IC_IF_100	A	100 MHz	Type 1 and 2 interconnect clock
	PAD	CLK_ETHERNET	A	75 MHz	potential clock for Ethernet interface
	PHY_TX_CLK PHY_TX_CLK_PS	PAD		75 MHz	Timing reference for MII RX interface (_ps is inverted clock)
	PHY_RX_CLK PHY_RX_CLK_PS	PAD		75 MHz	Timing reference for MII TX interface (_ps is inverted clock)
	PHY_RMII_CLK	CLK_ETHERNET (VIA PAD)	A	50 MHz	Clock to PHY in MII mode (output through PIOX(Y) pad) REF clock in RMII mode (input or output through PIOX(Y) pad)

Table 64. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
USB2.0 Host	STBUS_CLOCK	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 Interconnect clock
	CLOCK48	CLK_USB48	B	48 MHz	From USB FSyn pending confirmation that PHY will supply
	PHY_CLK_I	CLK_USB60		60 MHz	From USB PLL
	UTMI_PHY_CLK_I	CLK_PHY_USB60		60 MHz	From USB2.0 Phy
USB2.0 Phy	REFCLK_CUST	CLK_USB60		60 MHz	From USB PLL
	REFCLKBYPASS_CUST	TST_CLK_USB60		60 MHz	From pad for test
HDMI Frame formatter	STBUS_CLOCK	CLK_IC_IF_100	A	100 MHz	Type-1 interconnect clock
	PIX_CLOCK	CLK_DISP_HD	B	148.5 MHz Max	Pixel clock
	TMDS_CLOCK	CLK_TMDS_HDMI	B	148.5 MHz Max	TMDS clock is 1x or 2x pixel clock
	BCH_CLOCK	CLK_BCH_HDMI	B	148.5 MHz Max	BCH clock is 2x or 4x TMDS clock
PCM player 0	CLK_PCM	CLK_PCM0	C	50 MHz Max	PCM oversampling clock (256xFs, Fs = 192 kHz Max)
S/PDIF player	SPDIF_CLOCK	CLK_PCM2	C	15 MHz Max	S/PDIF clock 256xFs = 256 x 48 kHz
HDMI Analog	CKPXDLL	CLK_PLL_HDMI_PHY	B	148.5 MHz	From rejection PLL
	CKPX	CLK_TMDS_HDMI	B	74.25 MHz	From ClockGen B
DVP	ST_CK	CLK_IC_IF_200	A	200 MHz	Type 1 & 2 interconnect clock
	DVP_PIX2_CK	CLK_DVP	B	148.5 MHz in HD mode	D1 video stream clock provided by ClockGen B when in compositor capture mode
		VidInClk from pad	B	148.5 MHz in HD mode	D1 video stream clock
SATA HOST	CLK_STBUS	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 interconnect clock
	CLK_RBC0	CLK_RBC0		75 MHz	Recovery clock, synchronous with received data (75 MHz) (provided by SATA PHY)
	CLK_ASIC	CLK_ASIC		75 MHz	Used into transport and link layer blocks (75 MHz) (provided by SATA PHY)
	CLK_RXOOB	CLK_SATA		30 MHz	Used to OOB detection and also used as possible reference clock for ClockGen B and C (provided by SATA PHY)

Table 64. Functional blocks clocking (continued)

Block	Clock pin	Clock signal	S	Max frequency	Comment
MEMORY INTERFACES					
EMI-PCI Subsystem	SYSTEM_CLOCK	CLK_EMI_MASTER	A	100 MHz	EMI & PCI can also be clocked from external pads, STBus side will be synchronized to SYSTEM_CLOCK
	PCI_CLOCK	CLK_PCI	A	33/66 MHz	
	DEVICE_CLK_IN	EMI_FLASHCLK (PAD)		50 MHz	EMI SS clock when in EMI clock slave mode or PCI clock when in PCI clock slave mode.
GPLMI0	MCLK	MCLK		400 MHz	From GPLMI0 padlogic after divider and DLL
GPLMI0PL	LMI_PL_MCLK	LMI_PL_MCLK	D	800 MHz	From PLL
RESERVED	RESERVED	RESERVED			
COMMS					
COMMs	CLK_IC	CLK_IC_IF_100	A	100 MHz	Type 1 & 2 interconnect clock
	LP_CLOCK	CLK_LPC	B	46.875 kHz	Low power clock
	CLK_DAA	CLK_DAA	B	32.768 MHz	DAA clock
	CLK_DSS	CLK_DSS	B	36.864 MHz	Smart card clock

13.3 CPUs and interconnect clock generation (ClockGen A)

The reference clock can be either an internal 30 MHz clock signal or a clock connected to the SYSCLKINALT pin. The reset value is defined by mode pin[0] value.

This ClockGen is responsible for clocking the following units.

Table 65. ClockGen A mapping

Channel		30	900	450	800	
div#	**STi7197 Clk name**	**OSC**	**PLL0 HS**	**PLL0 LS**	**PLL1**	**Comment**
CLK_DIV_HS[0]	CLK_IC_STNOC	-	/3=300		/3=266 /2=400	-
CLK_DIV_HS[1]	CLK_FDMA0	-	/3=300		/3=266 /2=400	-
CLK_DIV_HS[2]	CLK_FDMA1	-				-
CLK_DIV_HS[3]	NOT USED	-	-		/3=266 /4=200	-
CLK_DIV_LS[4]	CLK_SH4_ICK	/32=0.95		/1=450		-
CLK_DIV_LS[5]	CLK_IC_IF_100	-		-	/8=100	-
CLK_DIV_LS[6]	CLK_LX_DMU_CPU	-		/1=450	/2=400	-
CLK_DIV_LS[7]	CLK_LX_AUD_CPU	-		/1=450	/2=400	-

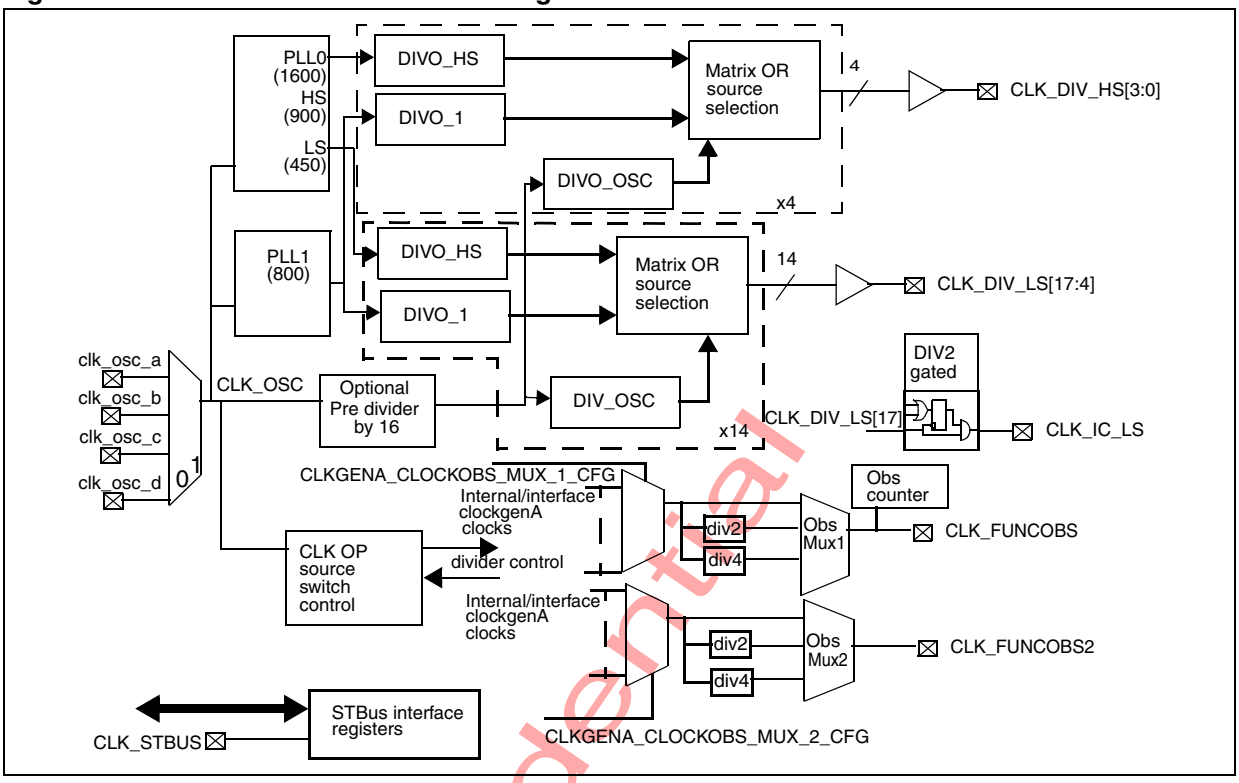
Table 65. ClockGen A mapping (continued)

Channel		30	900	450	800	
div#	**STi7197 Clk name**	**OSC**	**PLL0 HS**	**PLL0 LS**	**PLL1**	**Comment**
CLK_DIV_LS[8]	CLK_IC_DISP_200	-		-	/4=200	-
CLK_DIV_LS[9]	CLK_IC_BDISP_200	-		-	/4=200	-
CLK_DIV_LS[10]	CLK_IC_TS_200	-		-	/4=200	-
CLK_DIV_LS[11]	CLK_DISP_PIPE_200	-		-	/4=200	-
CLK_DIV_LS[12]	CLK_BLIT_PROC	-		-	/3=266	DeltaMu IC at 266 MHz
CLK_DIV_LS[13]	CLK_ETHERNET_PHY	-		/6=75 /9=50 /18=25		-
CLK_DIV_LS[14]	CLK_PCI	-		-	/12=66 /24=33	-
CLK_DIV_LS[15]	CLK_EMI_MASTER	-		-	-	-
CLK_DIV_LS[16]	CLK_IC_COMPO_200	-		-	-	-
CLK_DIV_LS[17]	CLK_IC_IF_200	-		-	-	two outputs; full speed and half speed
CLK_IC_LS	not used	-		-	-	

13.3.1 Block diagram

At POR, all clocks are output at 30 MHz (×1 from USB/SATA osc). The *Figure 26* shows the STi7197 ClockGen A block diagram.

Figure 26. STi7197 ClockGen A block diagram



13.3.2 Clock–off and reduced power

Clocks in group A can be slowed to less than 1 MHz, through register programming or low power signal from LPC, or stopped.

13.3.3 Clock observability

All the clocks of the ClockGen A can be observed on the TRIGGEROUT pad.

The CLOCK_OUT_SEL[5:0] bits of the CLKGNA_CLKOBS_MUX_X_CFG (where X = 1 and 2) configuration register is provided to select the clock which will be routed to the pad.

13.4 Video decoder, display, and Comms clock generation (ClockGen B)

This ClockGen is mainly responsible for generating the clocks used by the video display pipeline. This includes the following units:

- SD and HD displays
- compositor
- video output stage (formatters, HDMI, and DENC)
- HD and SD video DACs

In addition, ClockGen B also generates some processing clocks for the following units:

- comms—LPC/PWM

ClockGen B comprises two digitally controlled frequency synthesizers (FS0 and FS1). The reference clock can be either an internal 30 MHz clock (USB) signal or a clock connected to the SYSCLKINALT pin. The reset value is the SATA Phy clock.

The ClockGen B also includes a digital clock recovery module to recover the encoder clock.

The block diagram of ClockGen B is shown in *Figure 28*.

13.4.1 Clock signals

The *Table 66* lists the group B clocks with their maximum frequency.

Table 66. Clock generator B

Clock name	Maximum frequency (MHz)	Description
CLK_PIX_HD	148.5	HD pixel clock
CLK_PIX_SD	148.5	SD pixel clock (support HD format)
CLK_DISP_HD	148.5	HD display clock
CLK_DISP_ID	13.5	SD display clock
CLK_GDP3	148.5	GDP3 pixel clock (HD or SD)
CLK_656	148.5	DVO0 pixel clock
CLK_PP	150	Delta Preprocessors
CLK_DAA	32.768	DAA clock
CLK_DSS	36.864	DSS clock
CLK_LPC	46.875	Low Power Controller clock
CLK_TTXT	27	Teletext clock
CLK_SERLZR_HDMI	148.5	HDMI serializer clock
CLK_BCH_HDMI	148.5	HDMI BCH clock
CLK_TMDS_HDMI	148.5	HDMI TMDS clock
CLK_656_1	148.5	DVO1 pixel clock

The frequency of all the clocks is programmable. Especially, the video clocks must be set up with respect to the display standard in use.

The *Table 67* gives some programming examples with respect to the targeted application.

Table 67. Video clock domains by applications

Application			CLK_PIXEL_HD	CLK_DISP_HD	CLK_PIXEL_SD	CLK_DISP_ID	CLK_656	CLK_TMDS_HDMI	CLK_GDP3
Main (1080p60) & Aux	Main 1080p/60Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	148.5	148.5	27	13.5	148.5	148.5	148.5
		GDP3 on aux	148.5	148.5	27	13.5	148.5	NA	13.5

Table 67. Video clock domains by applications (continued)

Application			CLK_PIXEL_HD	CLK_DISP_HD	CLK_PIXEL_SD	CLK_DISP_ID	CLK_656	CLK_TMDS_HDMI	CLK_GDP3
Main (HD) & Aux (HD)	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 1080i/30 Hz or 720p/60Hz(HD) (no DACs outputs)	GDP3 on main	148.5	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	148.5	148.5	74.25	148.5	NA	74.25
Main & Aux	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	148.5	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	74.25	27	13.5	148.5	NA	13.5
Main & Aux	Main 480p/576p (ED) Aux: 480i / 576i (SD)	GDP3 on main	108	27	27	13.5	54	27	27
		GDP3 on aux	108	27	27	13.5	54	NA	13.5
Alternate (main to denc)	Main 480i/576i (SD) Aux: 480i / 576i (SD)	GDP3 on main	108	13.5	27	NA	27	27	13.5
Main & Aux SCART	Main 1080i/30Hz or 720p/60Hz (HD) Aux: 480i / 576i (SD)	GDP3 on main	108 (from FS0)	74.25	27	13.5	148.5	74.25	74.25
		GDP3 on aux	148.5	74.25	27	13.5	148.5	NA	13.5
Main & Aux pseudo-SCART	Main 480i/ 576i (SD) - TV (video + gfx) Aux: 480i / 576i (SD) - VCR (video only)	GDP3 on main	108	13.6	27	13.6	NA	NA	13.5
		GDP3 on aux	108	13.5	27	13.5	NA	NA	13.5

13.4.2 Clock generator B startup configuration

After the reset phase, the ClockGen B is by default configured with a 13.5 MHz display clock on both the Main and Auxiliary video outputs.

Table 68. Clock generator B default configuration

Clock name	Frequency (MHz)	Description
clk_pix_hd	148.5	HD pixel clock
clk_pix_sd	148.5	SD pixel clock
clk_disp_hd	13.5	HD display clock
clk_disp_id	13.5	SD display clock
clk_gdp3	148.5	GDP3 pixel clock (HD or SD)
clk_656	148.5	DVO pixel clock
clk_dvp	27	DVP clock
clk_daa	32.768	DAA clock

Table 68. Clock generator B default configuration (continued)

Clock name	Frequency (MHz)	Description
clk_dss	36.864	DSS clock
clk_lpc	46.875	Low Power Controller clock
clk_pp	27	DeltaMu Preprocessor clock must be re-programmed for 150 MHz frequency.
clk_fso_chan0	108	Clock to HDMI PII rejection
clk_tmds_hdmi	27	HDMI TMDS clock
clk_656_1	13.5	DVO1 pixel clock

13.4.3 Clock frequency change

The clock generator always starts with the default configuration as defined in *Table 68*. Nevertheless, the frequency synthesizers FS0 and FS1 can be re-configured to produce different frequencies.

Clock generator programming—lock/unlock

To prevent any unwanted ClockGen reprogramming, a protection mechanism is provided using the CKGB_LOCK register. This register must be written first with the keyword 0xC0DE to authorize any ClockGen registers update. Writing another data to the CKGB_LOCK register locks all the ClockGen registers.

Clock ratio change without changing FS0 and FS1 programming

The clocks clk_bch_hdmi, clk_tmds_hdmi, clk_656_1, clk_pix_hd, clk_disp_hd, clk_656, clk_gdp2, clk_disp_id, and clk_pix_sd are generated from a master clock (from FS0 and FS1), which is then divided by programmable dividers (by 2, 4, 8, or 1024). These dividers can be redefined using the register CKGB_DISP_CFG without changing the FS0 and FS1 setup. The clock generator design ensures a glitch-free frequency change.

FS0 and FS1 frequency definition

The frequencies generated by FS0 and FS1 are defined by the registers CKGB_FS0/1_MDx, CKGB_FS0/1_PEx and CKGB_FS0/1_SDIVx and is given by the following formula:

$$f_{OUT} = \frac{2^7 \times f_{IN}}{2^{SDIV} \times (1 + MD - PE \times 2^{-15})}$$

where f_{IN} is the frequency of the reference clock (27 or 30 MHz).

13.4.4 Clock frequency reduction

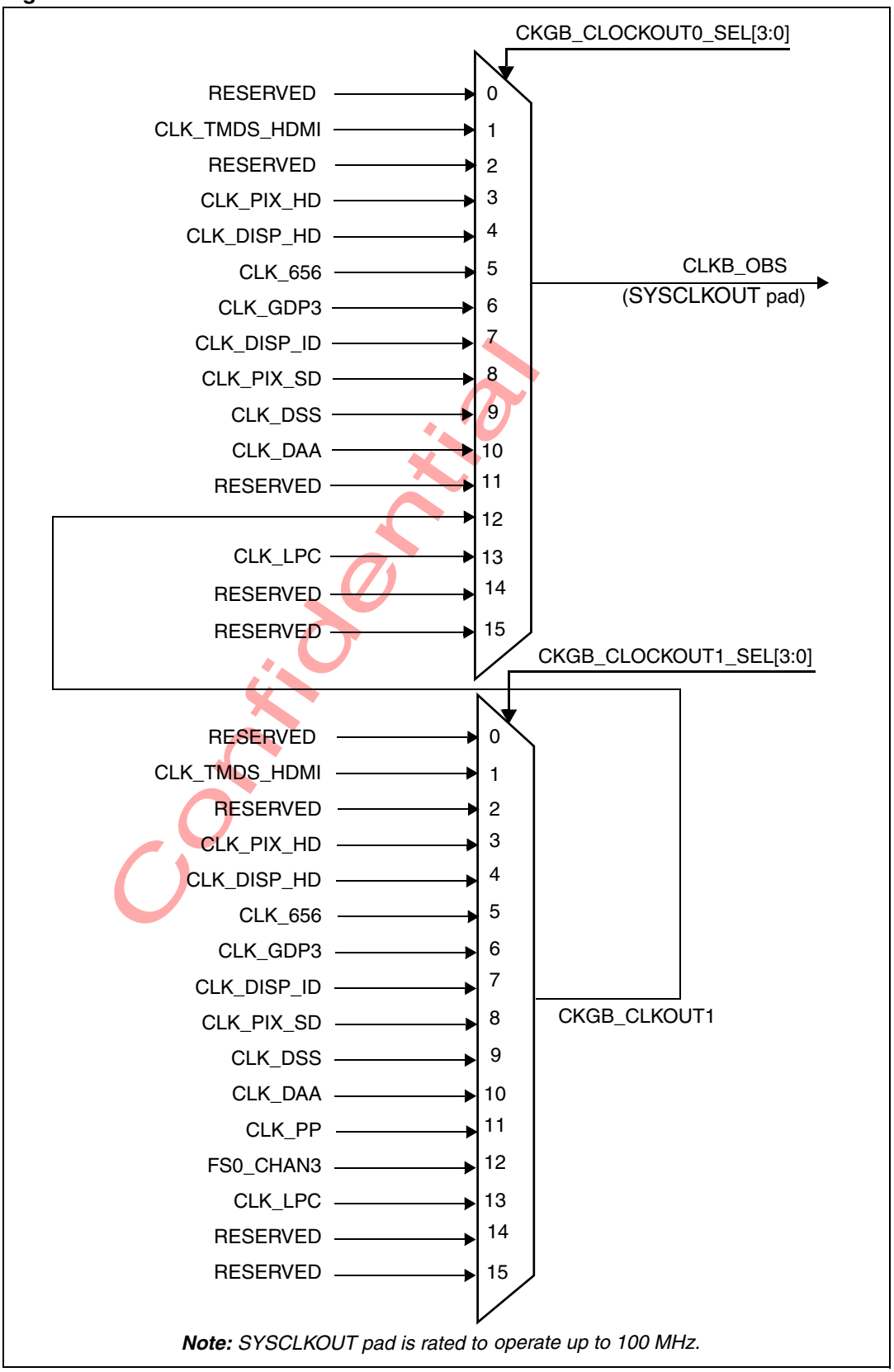
Most of the group B clocks can be divided to reduce the power consumption with the register CKGB_CLK_DIV without stopping the clocks.

13.4.5 Clocks observation

Any group B clock can be routed and observed on the SYSCLKOUT pad.

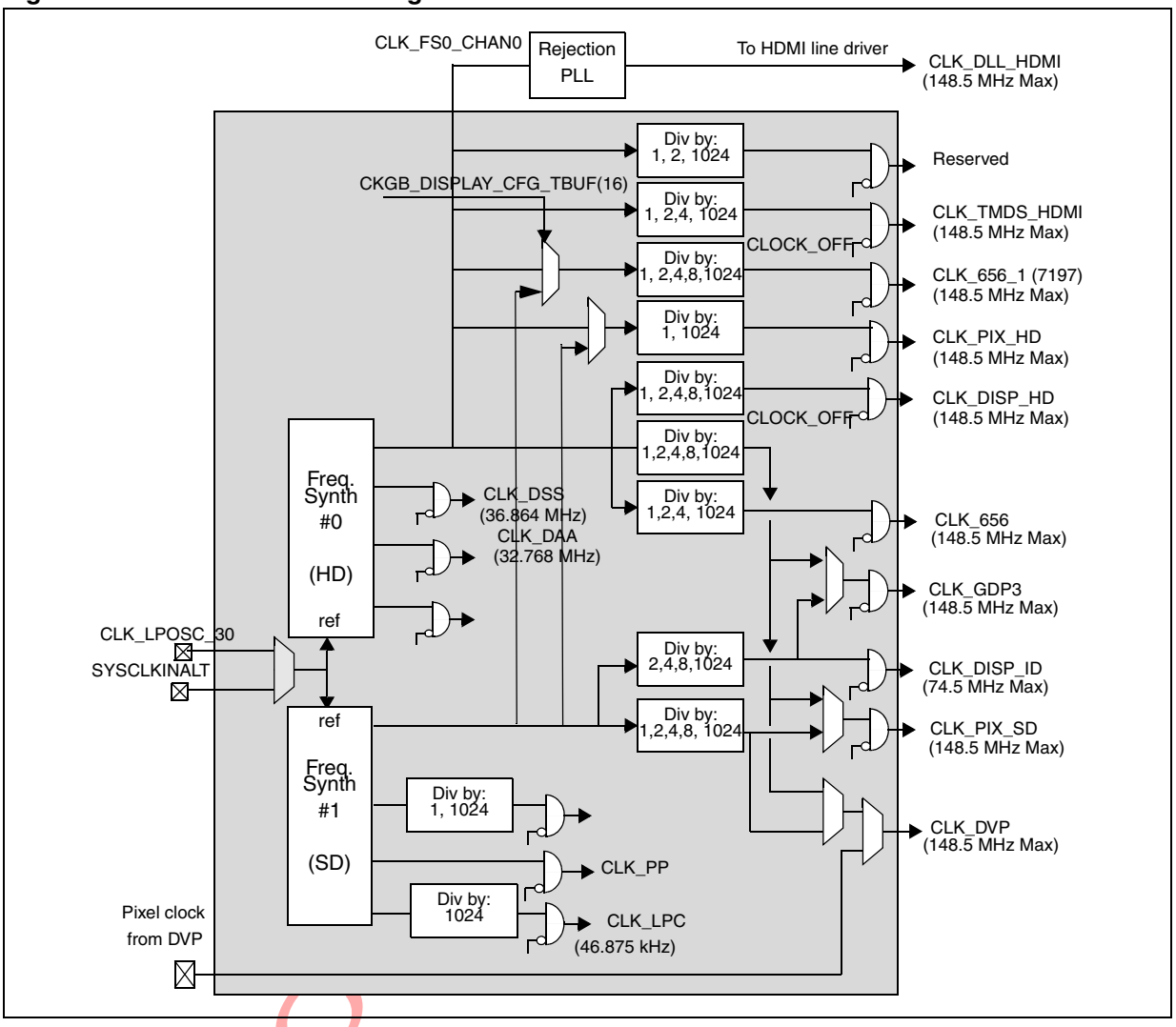
The configuration register CKGB_CLKOUT_SEL is provided to select the clock which will be routed to the pad.

Figure 27. FS0 and FS1 clocks observation



Note: *SYSCLKOUT pad is rated to operate up to 100 MHz.*

Figure 28. ClockGen B block diagram



13.4.6 Frequency synthesizers reference clock

The reference clock of two frequency synthesizers is selectable and can be chosen between the 30 MHz clock coming from the SATA Phy or from the pad SYSCLKINALT.

13.5 Audio clock generation (ClockGen C)

The ClockGen C is responsible for clocking the following units:

- multichannel PCM Player 0 (CLK_PCM0) connected to HDMI or external DACs (stereo)
- stereo PCM Player 1 (CLK_PCM1) connected to internal audio DACs and to HDMI stereo channels
- S/PDIF Player
- stereo audio DAC

The audio clock generator is a quad-frequency synthesizer which generates the 256 x Fs (audio sampling frequency) from which the I²S serial clock, left-right clock and DAC oversampling clocks are derived.

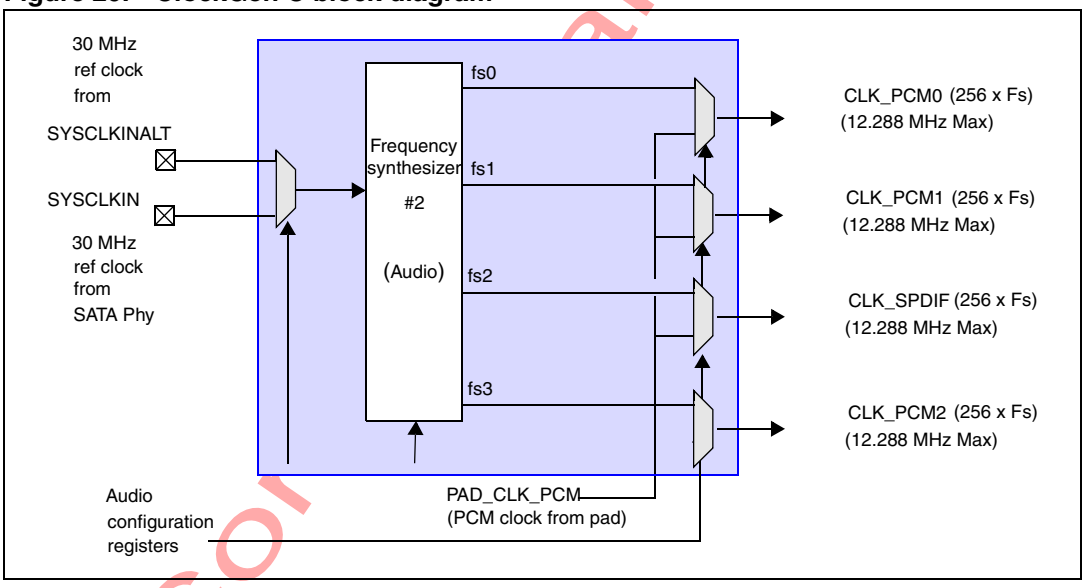
Typical audio sampling frequencies are: 32 kHz, 44.1 kHz, and 48 kHz for Set-top box applications, and can be up to 192 or 96 kHz for DVD applications.

The three audio players have independent clock generators issued from the same quad-frequency synthesizer. The frequency synthesizer channel#0 clocks the PCM player#0, the channel#1 clocks the PCM player#1, and the channel#2 clocks the S/PDIF player.

Refer to *Section 3.13: Audio subsystem on page 28* for a full overview of the Audio system clocking.

The *Figure 29* shows the block diagram of ClockGen C.

Figure 29. ClockGen C block diagram



13.5.1 Frequency synthesizer reference clock

The reference clock of the frequency synthesizer is selectable and can be chosen between the 30 MHz clock coming from the SATA Phy or from the pad SYSCLKINALT. The reset value is the SATA Phy clock.

13.6 LMI memory clocks (ClockGen D)

The ClockGen D supplies clocks to the LMI memory interface(s). This is a simple ClockGen with a PLL only, the dividing function, to generate the GPLMI IP Mclk, is done inside the LMI padlogic.

13.6.1 Clock signals

The *Table 69* lists group D clocks with their maximum and reset frequency.

Table 69. Clock Generator D

Clock name	Maximum frequency (MHz)	Reset frequency (MHz)	Description
CLK_LMI_PL	800	0	-
CLK_LMI	400	0	Phase altered and divided by 2 version of CLK_LMI_PL

13.6.2 Reference clock

The reference clock can be either an internal 30 MHz clock signal or a clock connected to the SYSCLKINALT pin. The reset value is SYSCLKALTIN.

13.6.3 Clock frequency reduction

Flexible, CPU can reprogram the PLL controls.

13.7 MPEG clock recovery

The MPEG clock recovery is a mechanism to adjust the locally generated clocks with the encoder clock referenced in the program counter reference (PCR) located in the adaptation field of the incoming transport stream.

The STi7197 generates three local clocks from internal frequency synthesizers using a fixed and stable 27 MHz reference clock produced by a crystal.

These three clocks are:

- clk_pix_sd used for standard definition display
- clk_pix_hd used for high definition display
- clk_pcm (256 × Fs, where Fs can take several possible values, such as 32 kHz, 44.1 kHz, and 48 kHz) used for audio output

13.7.1 Clock recovery principle

The mechanism assumes that these three clocks are related to each other.

The recovery is done as usual for the CLK_PIX_SD (generated by the frequency synthesizer FS#0) by comparing the 42 bits PCR value located in the adaptation field of the stream with the local system timer counter (STC) value when a packet arrives. This generates a potential correction that is applied to the CLK_PIX_SD frequency synthesizer. The frequency synthesizer is programmed with new setup values to slow or accelerate the clock.

Regarding the Audio PCM clock recovery, two counters are used.

- A PCM free-running counter, clocked by the PCM Audio frequency synthesizer FS#2.
- A reference counter, clocked by the SD video frequency synthesizer FS#0. The maximum value of this counter is programmable defining the time interval between two consecutive resets. This counter is used as a time-base.

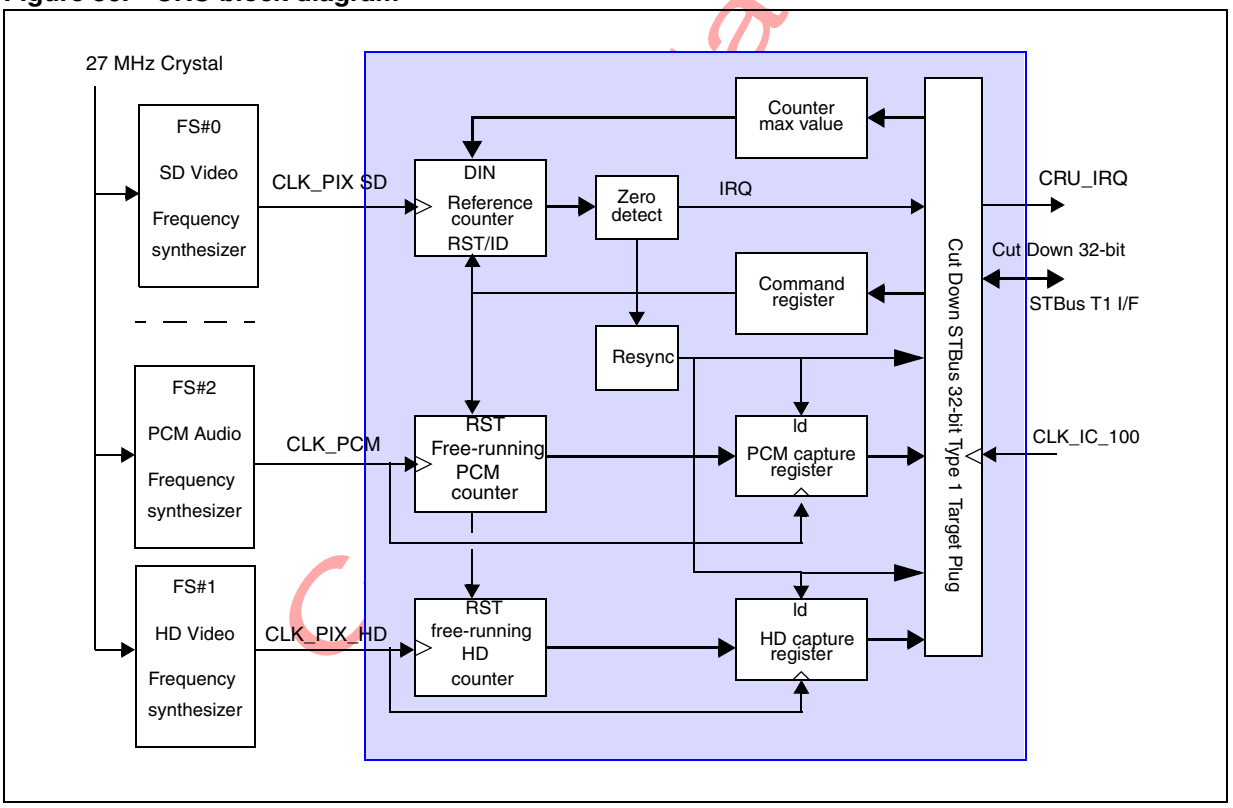
When the reference counter resets, the values of the free-running counter clocked off CLK_PCM is captured into a readable register. This event generates an interrupt to the CPU (CRU_IRQ). The CPU reads the value and compares it with the previously captured value. The difference between two adjacent values gives an indication of the correction to apply to the PCM audio frequency synthesizer FS#2.

The decision to correct the frequency synthesizer's setup is under the control of the software.

The same principle applies for the recovery of the CLK_PIX_HD. A free-running counter is clocked with the HD video frequency synthesizer FS#1. The same reference counter is used. When this counter resets then the output of the free-running counter clocked at CLK_PIX_HD is captured into a readable register.

The *Figure 30* shows the block diagram of clock recovery unit (CRU).

Figure 30. CRU block diagram



14 Power-on-reset and system reset

14.1 Reset sources

The different reset sources are:

- Power-on-reset (POR) signal, which is applied on the RESETN pad (with glitch suppression using a Schmitt type pad)
- Watchdog reset generated by the ST40 internal Watchdog Timer (WDT)
- UDI reset sent through the ST40 debug port
- Software reset from the ST40 to the ST231 CPU through the ST231 reset filters
- Smartcard insertion

The ST40 manual reset is not used, only the PMU_PRESET_N POR reset is used.

14.2 POR reset (cold reset) vs. system reset (warm reset)

In the POR sequence (cold reset), everything is reset including the clock generators and captured mode pins values.

In the system reset (warm reset) sequence, everything is reset except clock generators and a part of system configuration. The system reset sequence is executed when the reset source is watchdog, UDI, long-time-out reset, or smartcard insertion.

The long-time-out reset can be performed with an interrupt generated from a PIO. The CPU can use this interrupt to identify a long-time-out reset, and then use the WDT to generate a system reset.

14.3 Reset test mode

The reset generator includes a test mode that allows to bypass all the stretchers, and to directly apply a reset signal simultaneously to all the units.

15 Mode pins

The *mode pins* are a group of pads configured in the input mode, and are dedicated to capture values during the power-on-reset sequence that are used to configure certain defined functionalities. The captured values are viewed in the *SYSTEM_STATUS1*[22:0] register.

The mode pins are captured at the rising-edge of the NOTRESETIN signal during the reset phase with setup and hold constraints defined in the *Chapter 20.1: System timing interface*, and are made available to the system to define operating modes, such as ClockGen boot configuration. The *Table 70* describes the mapping of the mode pins on PIO pads.

Table 70. Mode pins mapping

Bit	Bit field	Controlled unit	Controlling Pad
MODE[0]	**Ref clock selection for Clockgen A** 0: SYSCLKINALT (Ext) 1: Osc (SATA)	ClockGen A	MII_MDIO [PIO8(3)]
MODE[2:1]	**PLL0 startup configuration**(1) 00: Fin/Fout–27/900 MHz 01: Fin/Fout–27/604.8 MHz 10: Fin/Fout–30/900 MHz 11: Fin/Fout–30/600 MHz	ClockGen A	[PIO16(1,0)]
MODE[4:3]	**PLL1 startup configuration**(1) 00: Fin/Fout–27/799.2 MHz 01: Fin/Fout–27/399.6 MHz 10: Fin/Fout–30/800 MHz 11: Fin/Fout–30/400 MHz	ClockGen A	MII_MDINT: MII_MDC [PIO9(6):PIO8(4)]
MODE[6:5]	**Reset bypasses**(2) CPU_RST_OUT_BYPASS[1]: bypass of (LX_Audio+LXDelphi) reset loop back CPU_RST_OUT_BYPASS[0]: bypass of (SH4+LX_Audio+LXDelphi) reset loop back	Reset generator	[PIO16(3:2)]
MODE[7]	**Resetout mode** (see SYSTEM_CONFIG9, long_reset_mode bit)(3)	Reset generator	MII_TXEN [PIO8(2)]
MODE[9:8]	**BOOT mode selection**: 00: SH4-300 boot first 01: ST231 DeltaMu boot first 10: ST231 Audio boot first	ST40, ST231 Audio, ST231 DeltaMu, request filtering	MII_RXD[3:2] [PIO9(1:0)]
MODE[10]	**Reserved** (Do not connect)	Reserved	MII_RXDV [PIO7(4)]
MODE[11]	**nand_addr_short_not_long**(4)	Nand Controller	MII_RXER [PIO7(5)]
MODE[12]	**Serial Flash usage**: 0: ATMEL 1: ST Flash	EMI4	MII_RXD[0] PIO8(6)
MODE[13]	**Boot device port size at boot:** (4) 0: 16 bits 1: 8 bits	EMI4 and Nand Controller	[PIO16(4)]

Table 70. Mode pins mapping (continued)

Bit	Bit field	Controlled unit	Controlling Pad
MODE[14]	**emiss_slave_not_master**	EMI subsystem	MII_RXD[1] [PIO8(7)]
MODE[16:15]	**Boot Device**: 00: NOR Flash (EMI controller) 01: NAND Flash (NAND Controller) 10: Serial Flash (SPI controller) 11: Reserved	EMI subsystem	MII_TXD[1:0] [PIO7(7:6)]
MODE[17]	**emiss_clock_slave_not_master**	EMI subsystem	MII_TXD[2] [PIO8(0)]
MODE[18]	**nand_page_large_not_small**(4)	Nand Controller	MII_TXD[3] [PIO8(1)]

1. Allows set up of ClockGen A PLL0 and PLL1 configurations (frequency input/frequency output) without relying on software. The ClockGen A registers CLKGENA_CLKOPSRC_SWITCH_CFG/CFG2 have to be configured to switch the source of STi7197 clocks from oscillator (default mode after reset) to PLL. The use of mode pins speeds up the configuration of ClockGen A. By the time the software changes the CLKGENA_CLKOPSRC_SWITCH_CFG/CFG2 setting, the PLL may already be locked (normally, this makes it possible to mask the PLL lock time). For more details, please contact your local ST representative to access ClockGen A functional specifications.
2. Allows bypass of the CPUs handshake in the chain of the reset generator. After boot, the modepin value can be bypassed by using the *SYSTEM_CONFIG9*[28:27] register. (This register is not reset in the case of a Watchdog reset, and takes the value of the two modepins at reset.) A typical use of this system config bit is to bypass the ST231 resetout. The ST40 may change the boot address of the ST231 (by default 0x0). To allow the ST231 to take into account this new boot address it must be reset again through a config register (*SYSTEM_CONFIG29*). In that case, the ST231 resetout is NOT propagated to the other IPs, which may have already been configured.
3. This bitfield selects the resetout mode (WDOGRSTOUT pin):

   In Long ResetOut mode, the reset value guarantees a 200 ms reset out for the resetout.

   In Short ResetOut mode, resetout lasts 100 µs.

   The resetout period is loaded during reset (RST_CONF) on the *SYSTEM_CONFIG9*[25:0] register (being the resetout period value depending on the mode pin 7 value). This register is not reset in the case of a Watchdog reset and can be reprogrammed after reset to allow for a resetout period of 2.48 s.
4. The NAND controller selects among the different memory types based on the three input signals: NAND_PAGE_LARGE_NOT_SMALL, NAND_ADD_SHORT_NOT_LONG, AND NAND_DATA_8_NOT_16. Refer to *Table 71*.

Table 71. Memory type based on static input pins

Type select signal			Type	Comment
NAND_PAGE_LARGE_NOT_SMALL	**NAND_ADD_SHORT_NOT_LONG**	**NAND_DATA_8_NOT_16**		
0	0	1	3	Small page devices
0	0	0	4	
0	1	1	1	
0	1	0	2	
1	0	1	7	Large page devices
1	0	0	8	
1	1	1	5	
1	1	0	6	

System configuration registers reset

Some system configuration registers are not affected by a system reset. They keep the value which was written either during the POR reset or by the software.

These registers are:

- mode pins value captured during the POR sequence
- reset generator configuration—resetout duration, CPUresetout bypass(1:0)
- boot mode
- boot size—boot Flash bus width (8 or 16 bits)

16 Low power control

Power down mode in the STi7197 consists of having some or almost all clocks running at 1/1024 of their normal speed. This reduces power consumption dramatically and still enables some software to be running, also, it enables the chip to be woken up fairly quickly without having to reboot the application.

Note: Certain precautions must be taken to achieve this: In particular, the DDR SDRAM must be put into self-refresh mode prior to entering this mode, and at wake up there must be no access to DDR until the DDR and associated PadLogic have been restored to their normal mode of operation. If the LMI clock is slowed down (to less than 100 MHz), the DDL of the LMI padlogic will no longer be operational. It will also be necessary to update the refresh interval.

Additionally, a Standby mode is provided whereby some clocks can be completely switched off. This can be a power saving feature for applications where functionalities clocked by a dedicated clock will never be needed.

The standby mode includes different mechanisms: switch-off clocks by programming the ClockGen or some bits of the system configuration module (for the EMI and DDR self-refresh), standby, and sleep modes in the ST40.

The ST40 also supports two main low power modes: sleep and standby (see *ST40 sleep and standby modes overview on page 269*).

The EMI clock cannot be switched off with the ClockGen. Both IPs support the power-down protocol: this is managed by a simple hand-shake between the system configuration register (under control of the CPU) and the two IPs. This mechanism allows the EMI clock to be switched off selectively.

The same mechanism is used to send the DDR into self-refresh mode (power-down protocol between the LMI core and the system configuration module).

16.1 Entering low power modes

Method 1.1: by programming configuration bits in the ClockGen

Using configuration bits of the ClockGen, some clocks can selectively be slowed down (divided by 1024) to enter power down mode whilst others keep their nominal speed. Refer to the ClockGen specifications.

Note: Standby mode (clocks halted) is also controllable through configuration bits of the ClockGen.

Method 1.2: using the low power controller (LPC) module

A global power down command can be issued by using the low power alarm (LPA) timer of the LPC module (part of STi7197 COMMs). Refer to *Figure 31 on page 268*.

All clocks, for which the 1024 divider ratio is available inside the two ClockGens, will be slowed down: the 1024 division is not currently implemented for the following clocks:

- In the ClockGen A:
  - CLK_EMI_MASTER_A (EMI clock @ 100 MHz)
  - CLK_ETHERNET_A (Ethernet clock @ 100 MHz)
- In the ClockGen B:
  - CLK_DSS (DSS clock @ 36.768 MHz)
  - CLK_DAA (DAA clock @ 32.768 MHz)
  - CLK_EMI_MASTER_B (EMI clock @ 100 MHz)
  - CLK_ETHERNET_B (Ethernet clock @ 100 MHz)

Power-down mode is entered upon programming of the LPA timer.

Note: 1 Use of the LPA Counter is not compatible with use as a WatchDog Timer. Refer to the LPC specification for details.

2 Standby mode (clocks completely switched off) cannot be entered through the LPC.

3 The only way to slow down the clocks for which the 1024 divider ratio is not implemented inside the ClockGen, is to bypass the PLL (By doing this it is possible to reach frequencies in the range of a few MHz), or to use the clockgen configuration registers to reduce the clock frequency generated by the PLL. Refer to clockgen specifications for details.

Method 1.3: using a global power down control bit

A global power down command (all clocks slowed down) can be issued by setting the appropriate configuration bit located in the CONF block register (refer to the System Configuration bit, *SYSTEM_CONFIG7*[23]). Global standby mode (clocks completely switched off) cannot be entered this way.

16.2 Exiting low power modes

Method 2.1: through configuration bits in the ClockGen

If power down is entered by Method 1.1 above, it can clear the bits that are already set in ClockGen while exiting.

Note: This is also valid for standby mode (that is, when clocks were halted through ClockGen configuration).

Method 2.2: through the LPC

If power down is entered by Method 1.2 above: when the LPA counter reaches zero, the LPC releases the global power down command and the ClockGen exits power down mode. The duration of the countdown is user programmable, and can be programmed from a few milliseconds to up to 271 days after LPA has been programmed (LPA counter is 40 bits clocked at 46.87 kHz).

Method 2.3: upon detection of activity on the UHF or IRB inputs

This generates an interrupt (IRB_WAKEUP_INTERRUPT) to the ILC3, which, assuming it has first been programmed accordingly, treats it as a wake up request that it routes to the LPC and also to the CONF module (to clear the global power-down bit). Refer to *Figure 31 on page 268*.

Note: ***IMPORTANT****: The IRB_WAKE_UP interrupt routed to the ILC3 is generated only if the global power down command is received by the wake-up interrupt generator module. This implies that the LPC must be programmed (METH 1.2). This also has the effect of slow down the clocks to 1/1024 of their normal frequency.*

If power down is entered by method 1.2: the LPC, when it receives the wake up request from the ILC, clears the global power down command that goes to the ClockGen and normal speed is restored.

If power down is entered by method 1.3: the global power-down control bit in the CONF block, when it receives the wake up request from the ILC, clears the global power down command that goes to the ClockGen and normal speed is restored.

If power down is entered by method 1.1: the configuration bits in the ClockGen must be set back to their normal value. This can be done by an interrupt routine. However, if DDR is not operational (because it was sent in self-refresh) this means the interrupt servicing routine is stored in the ST40 cache or stored in external Flash, if EMI is not switched off.

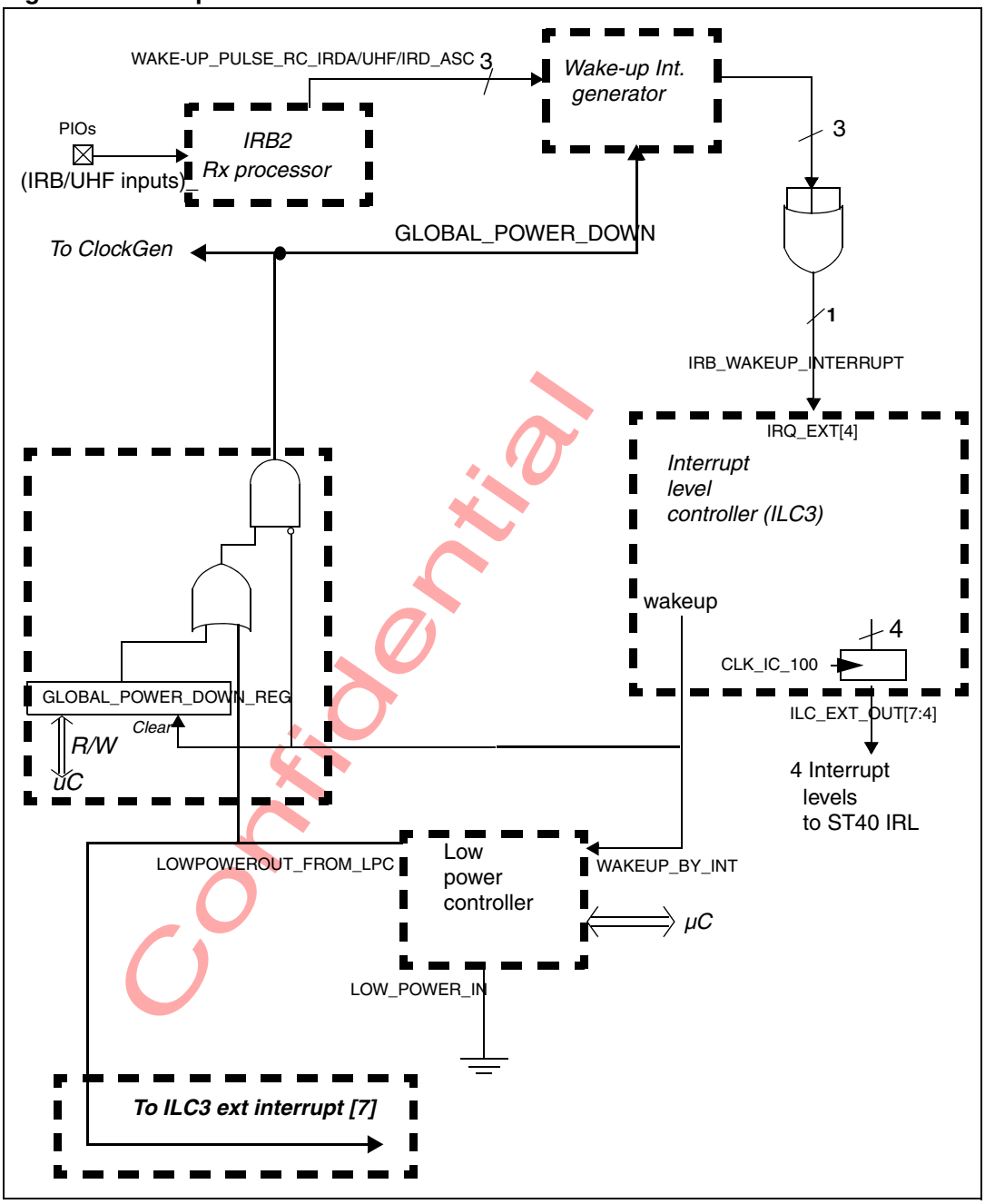
In case that the interrupt going to the ILC3 upon detection of IRB/UHF activity can be treated as a normal interrupt, servicing it then consists of restoring the ClockGen configuration bits.

Note: *The same interrupt can be also used to wake-up the ST40 from sleep or standby mode since four interrupt levels provided by the ILC3 are connected to the ST40 IRL.*

Method 2.4: upon firing of any selected interrupt

This is just an extension of the latter case. In fact if the condition that the relevant interrupt handler is not located in DDR is fulfilled, then any source can be programmed to trigger the interrupt routine that will clear configuration bits in the ClockGen if power down was entered in that way (method 1.1), or clear the LPA counter to restore normal operation if power down was controlled from the LPC (method 1.2).

Figure 31. Low power mode control hardware



16.3 DDR self-refresh

To send the DDR in self-refresh the CPU needs to write a bit in the system configuration register:

- GP-LMI/LMI padlogic configuration *SYSTEM_CONFIG11*:LMIPL_PLL_POWERDOWN

  This write operation activates the power-down protocol for the LMI Core (a power-down request is received by the LMI). The LMI core completes all of the outstanding operations, it puts the DDR in self-refresh mode and then answers with a power-down

grant. This can be monitored by means of a status bit in the system configuration register:

- LMI padlogic status register *SYSTEM_STATUS4*:LMI_PWRD_ACK

  As soon the acknowledge is received the LMI clock can be switched off or slowed down using the methods described before.

  After exiting from low power mode the DLLs inside the LMI padlogic must be reset by means of a soft reset using the system configuration bit and the lock condition must be reached:

  GP-LMI / LMI padlogic configuration *SYSTEM_STATUS4*:RST_N_LMI (active low)

  Note: This procedure has the effect of resetting the LMI core. This implies that the LMI core configuration must be re-done.

  The software needs to guarantee that no access is performed to the LMI during power-down and until LMI and padlogic are restored to the normal mode of operation.

16.4 EMI and PCI clocks stopping

The clocks of these three IPs can be switched off with the same mechanism used to put the DDR into self-refresh (that is, by means of the power-down protocol executed between the system configuration and the two IPs). For that case the system configuration bits to be used are:

- Power down configuration register *SYSTEM_CONFIG12*:
  - bit[1] EMI_POWER_DOWN_REQ: Power-down request for EMI module
  - bit[2] PCI_POWER_DOWN_REQ: Power-down request for PCI module
- Power down status register *SYSTEM_STATUS15*:
  - bit[1] POWER_DOWN_ACK_EMI: EMI power-down acknowledge
  - bit[2] POWER_DOWN_ACK_PCI: PCI power-down acknowledge

16.5 ST40 sleep and standby modes overview

The ST40-300 ISA includes a sleep instruction that can be used to suspend operation of the core to the point where the clocks can be stopped. The ST40-300 top also provides signals to inform an SoC level power or clock controller when it is safe to remove the clock and to determine whether the CSP clock should be stopped or not.

Note: The STi7197 ClockGenA does not allow the ST40 clocks to be switched off because of the missing hand-shake with the ST40. ST40 clocks can only be slowed-down.

Sleep mode

On executing the sleep instruction the ST40-300 core will flush the instructions in the pipeline and complete all outstanding STBus transactions on the initiator port. Once this has been completed the CPU will assert the EXT_ST40_CORE_PDACK signal to indicate that the clock to the core can be removed.

The actual gating of the clock provided to the core is expected to be performed at the SoC level from the clock controller itself in response to the EXT_ST40_CORE_PDACK signal being asserted. This is done to allow the entire clock tree to be stopped and therefore to maximize the dynamic power-saving.

Note: The STi7197 ClockGenA does not allow the ST40_ICK clock to be switched off because of the missing handshake with the ST40.

The CSP also provides a mechanism to enter sleep mode as directed by a system level clock or power controller. In this case the CSP is instructed to enter sleep mode by the system level assertion of the EXT_ST40_CSP_PDREQ signal. At this point the CSP will complete all outstanding STBus requests that it has received. Once the CSP is idle it will internally switch the relevant wake-up control signals to operate correctly with the CSP clock removed and will then assert EXT_ST40_CSP_PDACK to indicate that it is safe to stop the clock to the CSP.

The actual gating of the clock provided to the CSP is expected to be performed at the SoC level from the clock controller itself in response to the EXT_ST40_CSP_PDACK signal being asserted. This is done to allow the entire clock tree to be stopped and therefore to maximize the dynamic power-saving.

Note: 1 Neither the core nor the CSP will signal readiness to have their clocks removed until all outstanding transactions are completed. Consequently, a pending access to a non-responding peripheral will prevent the ST40-300 entering sleep mode. The system designer must ensure that other initiators and targets in the system are shut down in a manner that ensures all transactions can be completed safely.

2 The STi7197 ClockGenA does not allow the ST40_PCK clock to be switched off because of the missing hand-shake with the ST40.

Exiting sleep mode

Two conditions will cause the ST40 core to exit sleep mode.

- An interrupt on the NMI, IRL, through the interrupt expansion interface or generated by one of the CSP peripherals (if the CSP is still being clocked).
- Either a manual or power-on reset. This can be applied either through the relevant pins on the core, through the user debug interface (UDI), or by the watchdog timer.

De-asserting EXT_ST40_CSP_PDREQ will not cause the CSP or core to resume from sleep and will be ignored. When a return from sleep mode is requested the CSP de-asserts the EXT_ST40_CSP_PDACK signal to indicate to the system level clock controller that it is ready for its clock to be started.

Note: Before starting the CSP clock the system-level clock controller should de-assert EXT_ST40_CSP_PDREQ to prevent the CSP from re-entering sleep mode.

Once the CSP has started to receive a clock it will return to functional mode and will assert the STBus default grant signal to indicate it can start to accept transactions from the STBus.

The CSP also signals internally to the core that it is to wake-up from sleep mode, at which point the core de-asserts its EXT_ST40_CORE_PDACK and waits until the core clock is re-started by the clock controller, therefore allowing the core to continue with execution of instructions.

Note: There is no mechanism in place to prevent the CSP from transitioning into sleep even if the CPU is in functional mode. An operation where the core is being clocked and the CSP is powered down is not supported and should be avoided except during the transitions to and from sleep mode.

17 System config module

17.1 Brief overview

The System Config is a module that holds general purpose configuration registers. It can also be used to read back some system configurations.

Register addresses are shown as *SystemConfigBaseAddress* + Offset

The *SystemConfigBaseAddress* is: 0xFE00 1000

17.1.1 Register summary

Table 72. Register summary

Address offset	Register	Description	Reference
0x0000	*DEVICE_ID*	Device identifier	*on page 274*
0x0004	*EXTRA_DEVICE_ID*	Reserved	*on page 274*
Status registers			
0x0008	*SYSTEM_STATUS0*	USB/SATA PHY status register	*on page 275*
0x000C	*SYSTEM_STATUS1*	Mode pin status captured during power-on-reset	*on page 275*
0x0010	*SYSTEM_STATUS2*	OSC status register	*on page 276*
0x0014	*SYSTEM_STATUS3*	LMI-PADLOGIC (LMI_SYS) status register	*on page 276*
0x0018	*SYSTEM_STATUS4*	LMI-PADLOGIC (LMI_SYS) status register	*on page 277*
0x001C	*SYSTEM_STATUS5*	ClockGen D Jitter estimator capture pattern monitor	*on page 277*
0x0020	*SYSTEM_STATUS6*	ClockGen D Jitter estimator beat edge monitor	*on page 278*
0x0024	*SYSTEM_STATUS7*	Compensation status registers	*on page 278*
0x0028	*SYSTEM_STATUS8*	ClockGenD Jitter estimator beat edge counter monitor	*on page 279*
0x002C	*SYSTEM_STATUS9*	HDMI PLL status register	*on page 279*
0x0030	*SYSTEM_STATUS10*	USB/LMI PLI Bist counter status register	*on page 280*
0x0034	*SYSTEM_STATUS11*	Reserved	*on page 280*
0x0038	*SYSTEM_STATUS12*	Thermal sensor status register	*on page 281*
0x003C	*SYSTEM_STATUS13*	Reserved	*on page 281*
0x0040	*SYSTEM_STATUS14*	Reserved	*on page 281*
0x0044	*SYSTEM_STATUS15*	Power down status register	*on page 282*
Configuration registers			
0x0100	*SYSTEM_CONFIG0*	Transport configuration register	*on page 283*
0x0104	*SYSTEM_CONFIG1*	HDMI PHY compensation code register	*on page 284*

Table 72. Register summary (continued)

Address offset	Register	Description	Reference
0x0108	SYSTEM_CONFIG2	HDMI PHY configuration register	on page 285
0x010C	SYSTEM_CONFIG3	DAC /HDMI configuration register	on page 286
0x0110	SYSTEM_CONFIG4	USB / Delta -Mu configuration register	on page 287
0x0114	SYSTEM_CONFIG5	EMI/PCI configuration register	on page 288
0x0118	SYSTEM_CONFIG6	Vidout configuration register	on page 290
0x011C	SYSTEM_CONFIG7	COMMS /Ethernet configuration register	on page 291
0x0120	SYSTEM_CONFIG8	SH4 boot control configuration register	on page 293
0x0124	SYSTEM_CONFIG9	ResetGen configuration register (only sensitive to preset)	on page 294
0x0128	SYSTEM_CONFIG10	ITRQ pads control pin configuration register	on page 295
0x012C	SYSTEM_CONFIG11	LMI padlogic configuration register	on page 295
0x0130	SYSTEM_CONFIG12	LMI padlogic configuration register	on page 297
0x0134	SYSTEM_CONFIG13	LMI padlogic configuration register	on page 299
0x0138	SYSTEM_CONFIG14	LMI padlogic configuration register	on page 300
0x13C	SYSTEM_CONFIG15	Key scan / FDMA configuration register	on page 300
0x0140	SYSTEM_CONFIG16	Comms SSC configuration register	on page 301
0x0144	SYSTEM_CONFIG17	CPXM configuration control register	on page 302
0x0148	SYSTEM_CONFIG18	pad state configuration control register	on page 303
0x014C	SYSTEM_CONFIG19	PIO 0 alternate function control register	on page 303
0x0150	SYSTEM_CONFIG20	PIO 1 alternate function control register	on page 304
0x0154	SYSTEM_CONFIG21	PIO 2 alternate function control register	on page 304
0x0158	SYSTEM_CONFIG22	Compensation configuration registers	on page 305
0x015C	SYSTEM_CONFIG23	Compensation configuration registers	on page 306
0x0160	SYSTEM_CONFIG24	Osc configuration register	on page 307
0x0164	SYSTEM_CONFIG25	PIO 3 alternate function control register	on page 308
0x0168	SYSTEM_CONFIG26	ST230 Lx - AUDIO boot	on page 309
0x016C	SYSTEM_CONFIG27	ST230 Lx - AUDIO reset control and periph address	on page 310
0x0170	SYSTEM_CONFIG28	ST230 DELTA - MU boot	on page 311
0x0174	SYSTEM_CONFIG29	ST230 DELTA -MU reset control and periph address	on page 311
0x0178	SYSTEM_CONFIG30	Reserved	on page 312
0x017C	SYSTEM_CONFIG31	EMI configuration register	on page 312
0x0180	SYSTEM_CONFIG32	Power Down configuration register	on page 313

Table 72. Register summary (continued)

Address offset	Register	Description	Reference
0x0184	*SYSTEM_CONFIG33*	SOFT_JTAG register for the USB2.0 tap controller	*on page 314*
0x0188	*SYSTEM_CONFIG34*	PIO 4 alternate function control register	*on page 315*
0x018C	*SYSTEM_CONFIG35*	PIO 5 alternate function control register	*on page 315*
0x0190	*SYSTEM_CONFIG36*	PIO 6 alternate function control register	*on page 316*
0x0194	*SYSTEM_CONFIG37*	PIO 7 alternate function control register	*on page 316*
0x0198	*SYSTEM_CONFIG38*	LMI configuration register	*on page 317*
0x019C	*SYSTEM_CONFIG39*	Reserved	*on page 318*
0x01A0	*SYSTEM_CONFIG40*	Clock select configuration register	*on page 318*
0x01A4	*SYSTEM_CONFIG41*	Thermal sensor configuration register	*on page 319*
0x01A8	*SYSTEM_CONFIG42*	LMI configuration register	*on page 319*
0x01AC	*SYSTEM_CONFIG43*	LMI configuration register	*on page 320*
0x01B0	*SYSTEM_CONFIG44*	Reserved	*on page 320*
0x01B4	*SYSTEM_CONFIG45*	Reserved	*on page 321*
0x01B8	*SYSTEM_CONFIG46*	PIO 8 alternate function control register	*on page 321*
0x01BC	*SYSTEM_CONFIG47*	PIO 9 alternate function control register	*on page 322*
0x01C0	*SYSTEM_CONFIG48*	PIO 12 alternate function control register	*on page 322*
0x01C4	*SYSTEM_CONFIG49*	PIO 13 alternate function control register	*on page 323*
0x01C8	*SYSTEM_CONFIG50*	PIO 15 alternate function control register	*on page 324*
0x01CC	*SYSTEM_CONFIG51*	LMI configuration register	*on page 325*
0x01D0	*SYSTEM_CONFIG52*	LMI configuration register	*on page 326*
0x01D4	*SYSTEM_CONFIG53*	Reserved	*on page 326*
0x01D8	*SYSTEM_CONFIG54*	Reserved	*on page 327*
0x01DC	*SYSTEM_CONFIG55*	LMI configuration	*on page 327*
INTC2 registers			
0x0300	*INTC2_PRIORITY00*	Reserved	*on page 328*
0x0304	*INTC2_PRIORITY04*	Reserved	*on page 328*
0x0308	*INTC2_PRIORITY08*	Reserved	*on page 329*
0x0320	*INTC2_REQUEST00*	Reserved	*on page 329*
0x0324	*INTC2_REQUEST04*	Reserved	*on page 329*
0x0328	*INTC2_REQUEST08*	Reserved	*on page 330*
0x0340	*INTC2_MASK00*	Reserved	*on page 330*
0x0344	*INTC2_MASK04*	Reserved	*on page 330*
0x0348	*NTC2_MASK08*	Reserved	*on page 331*

Table 72. Register summary (continued)

Address offset	Register	Description	Reference
0x0360	*INTC2_MASK_CLEAR00*	Reserved	*on page 331*
0x0364	*INTC2_MASK_CLEAR04*	Reserved	*on page 331*
0x0368	*INTC2_MASK_CLEAR08*	Reserved	*on page 332*
0x0380	*INTC2_MODE*	Reserved	*on page 332*

17.1.2 Device ID register descriptions

DEVICE_ID — Device ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VERSION				GROUP_ID						DEVICE_ID															MANUFACTURER_ID							JTAG_BIT

Address: *SystemConfigBaseAddress* + 0x0000

Type: R

Reset: 0x2D43 E041

Description: JTAG device ID

[31:28] **VERSION**

[27:22] **GROUP_ID**

[21:12] **DEVICE_ID**

[11:1] **MANUFACTURER_ID**

[0] **JTAG_BIT**

EXTRA_DEVICE_ID — Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0004

Type: R

Reset: 0xXXXX

Description: Reserved

[31:0] RESERVED

17.1.3 System status register description

SYSTEM_STATUS0 USB/SATA PHY status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																												BISTOK	TDO_USB	TDO_SATA	RESERVED

Address: *SystemConfigBaseAddress* + 0x0008

Type: R

Reset: 0x0000

Description: USB/SATA Phy status

[31:4] RESERVED

[3] **BISTOK**: High level means that bist is running into USB PHY device and no error is detected.

[2] **TDO_USB**: USB2 PHY TDO signal.

[1] **TDO_SATA**: SATA PHY TDO signal.

[0] RESERVED

SYSTEM_STATUS1 Mode pins values

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED													MODE_PIN																		

Address: *SystemConfigBaseAddress* + 0x000C

Type: R

Reset: Undefined[b]

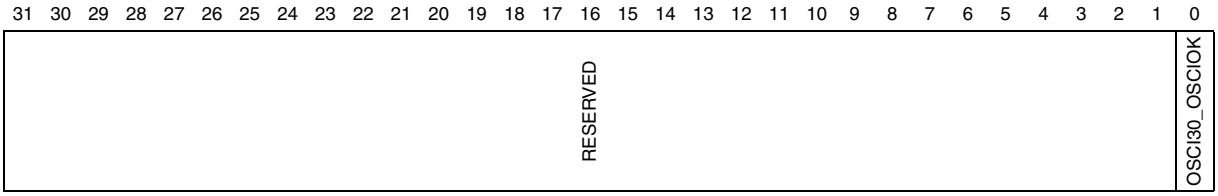
Description: Mode pins values

[31:19] RESERVED

[18:0] **MODE_PIN**: Mode pins are captured during the power-on-reset period.

b. Reset value depends on modepins value

SYSTEM_STATUS2 OSC status



Address: *SystemConfigBaseAddress* + 0x0010

Type: R

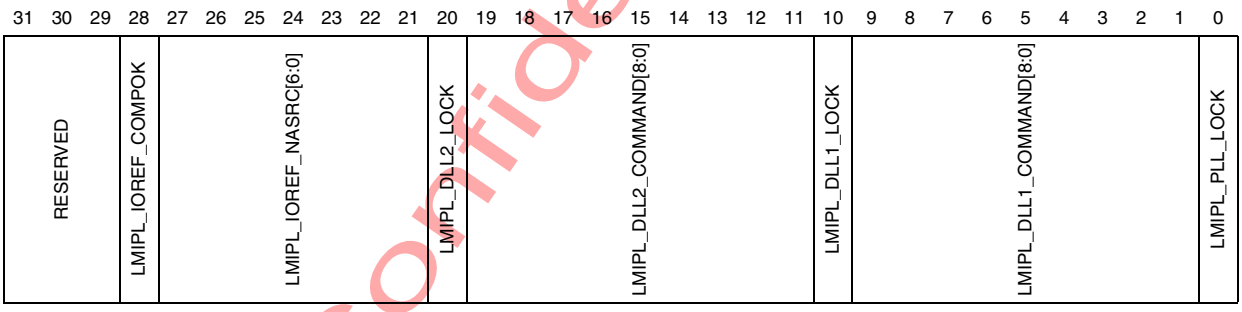
Reset: 0x0000 0000

Description: OSC status

[31:1] RESERVED

[0] **OSCI30_OSCIOK**:
1: OSCI 30 MHz oscillation stable (ZI output enabled)
0: OSCI 30 MHz oscillation unstable

SYSTEM_STATUS3 LMI status



Address: *SystemConfigBaseAddress* + 0x0014

Type: R

Reset: 0xXXXX(c)

Description: LMI status

[31:29] RESERVED

[28] **LMIPL_IOREF_COMPOK**: Can be high only in normal mode and when a new measured code is available on the ASRC lines. When macrocell turns from any other mode to normal mode, delay constraints are applied to COMPOK signal.

[27:21] **LMIPL_IOREF_NASRC[6:0]**: Input code to be copied on the AxSRC lines by the compensation cell in Read mode.

c. From LMI Padlogic

[20] **LMIPL_DLL2_LOCK**: DLL2 lock:
0: DDL2 is unlocked 1: DDL2 is locked

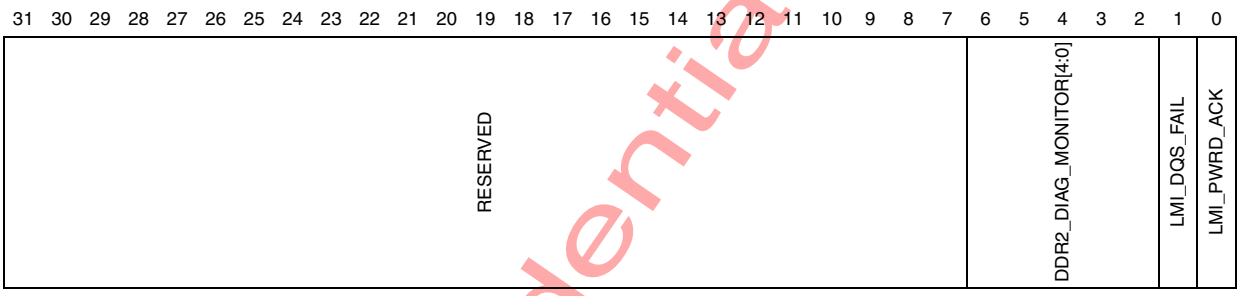
[19:11] **LMIPL_DLL2_COMMAND[8:0]**: DLL2 command. Reports the command currently being generated by DLL2.

[10] **LMIPL_DLL1_LOCK**: DLL1 lock.
0: DDL1 is unlocked 1: DDL1 is locked

[9:1] **LMIPL_DLL1_COMMAND[8:0]**: DLL1 command. Reports the command currently being generated by DLL1.

[0] **LMIPL_PLL_LOCK**: LMIPL PLL lock signal.
0: LMI PLL is unlocked 1: LMI PLL is locked

SYSTEM_STATUS4 LMI padlogic status



Address: *SystemConfigBaseAddress* + 0x0018

Type: R

Reset: 0x00000000

Description: LMI padlogic configuration status

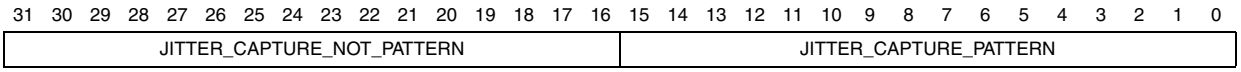
[31:7] RESERVED

[6:2] **DDR2_DIAG_MONITOR[4:0]**: For future development.

[1] **LMI_DQS_FAIL**:
1: Notification for DQS spurious/missing behavior

[0] **LMI_PWRD_ACK**:
1: LMI power acknowledge

SYSTEM_STATUS5 Clockgen D Jitter estimator capture pattern monitor



Address: *SystemConfigBaseAddress* + 0x001C

Type: R

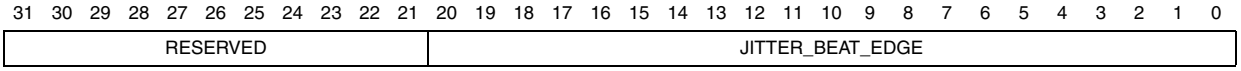
Reset: 0x00000000

Description: ClockGenD Jitter estimator capture pattern monitor

[31:16] JITTER_CAPTURE_NOT_PATTERN

[15:0] JITTER_CAPTURE_PATTERN

SYSTEM_STATUS6 Clockgen D Jitter estimator beat edge monitor



Address: *SystemConfigBaseAddress* + 0x0020

Type: R

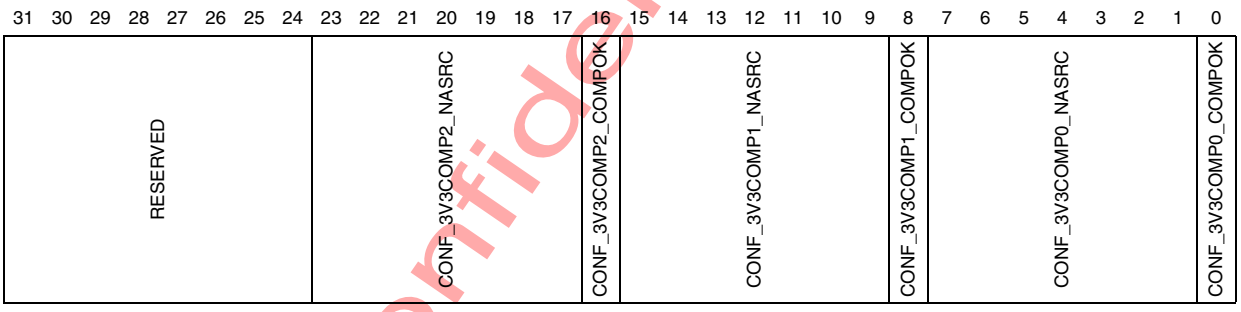
Reset: 0x00000000

Description: ClockGenD Jitter estimator beat edge monitor

[31:21] RESERVED

[20:0] **JITTER_BEAT_EDGE**

SYSTEM_STATUS7 Compensation status



Address: *SystemConfigBaseAddress* + 0x0024

Type: R

Reset: 0x00000000

Description: Compensation status

[31:24] RESERVED

[23:17] **CONF_3V3COMP2_NASRC**: 3V3 compensation 2: NASRC code

[16] **CONF_3V3COMP2_COMPOK**: 3V3 compensation 2: COMPOK signal

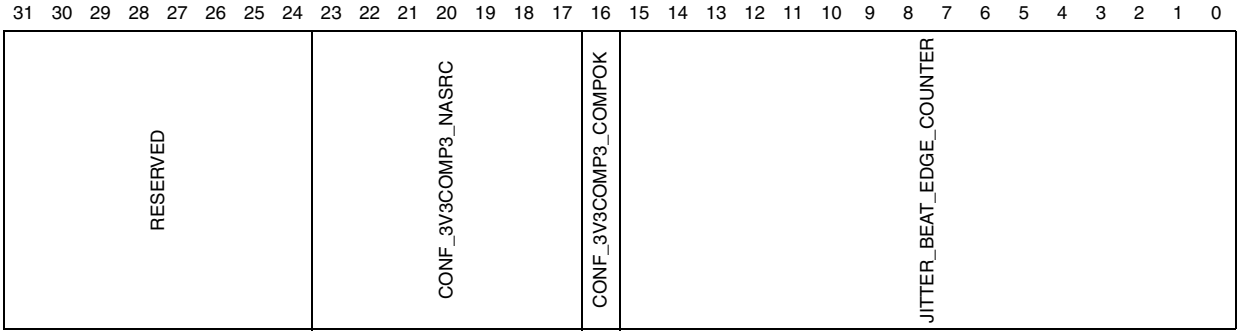
[15:9] **CONF_3V3COMP1_NASRC**: 3V3 compensation 1: NASRC code

[8] **CONF_3V3COMP1_COMPOK**: 3V3 compensation 1: COMPOK signal

[7:1] **CONF_3V3COMP0_NASRC**: 3V3 compensation 0: NASRC code

[0] **CONF_3V3COMP0_COMPOK**: 3V3 compensation 0: COMPOK signal

SYSTEM_STATUS8 ClockGenD Jitter estimator beat edge counter monitor



Address: *SystemConfigBaseAddress* + 0x0028

Type: R

Reset: 0x00000000

Description: ClockGenD Jitter estimator beat edge pattern monitor

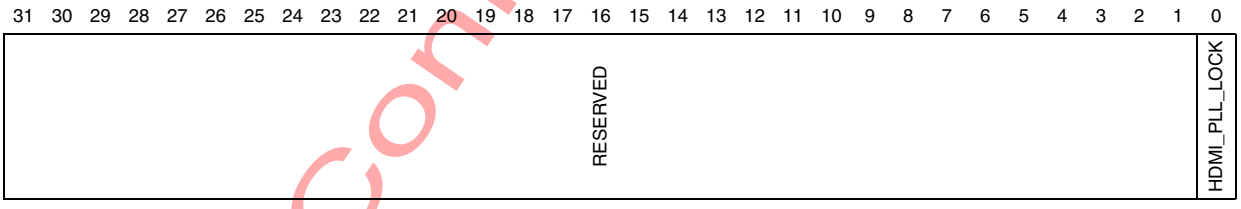
[31:24] RESERVED

[23:17] **CONF_3V3COMP3_NASRC**: 3V3 compensation 3: NASRC code

[16] **CONF_3V3COMP3_COMPOK**: 3V3 compensation 3: COMPOK signal

[15:0] JITTER_BEAT_EDGE_COUNTER

SYSTEM_STATUS9 HDMI PLL status



Address: *SystemConfigBaseAddress* + 0x002C

Type: R

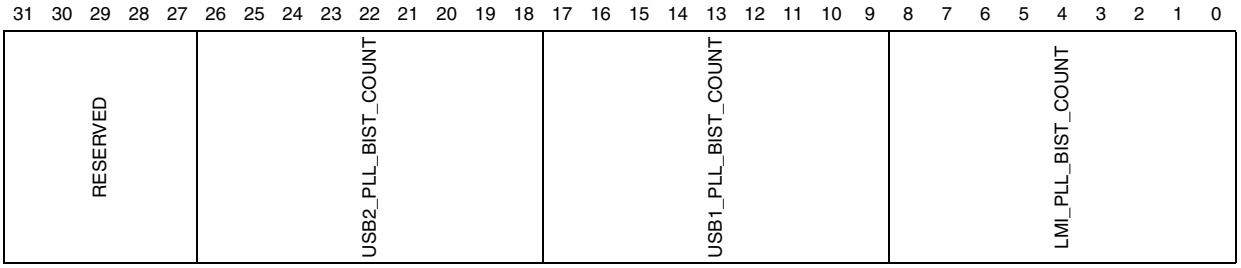
Reset: 0x00000000

Description: HDMI PLL status

[31:1] RESERVED

[0] **HDMI_PLL_LOCK**: Used to check lock condition of HDMI rejection PLL.
0: HDMI rejection PLL is unlocked 1: HDMI rejection PLL is locked

SYSTEM_STATUS10 USB/LMI PLI Bist counter status



Address: *SystemConfigBaseAddress* + 0x0030

Type: R

Reset: 0x00000000

Description: Reserved

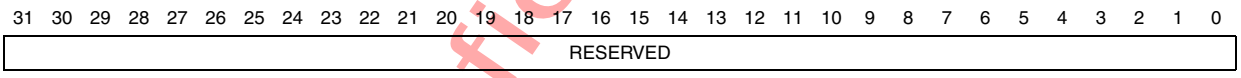
[31:27] RESERVED

[26:18] **USB2_PLL_BIST_COUNT**: Value of USB2 PLL Bist counter value

[17:9] **USB1_PLL_BIST_COUNT**: Value of USB1 PLL Bist counter value

[8:0] **LMI_PLL_BIST_COUNT**: Value of LMI PLL Bist counter value

SYSTEM_STATUS11 Reserved



Address: *SystemConfigBaseAddress* + 0x0034

Type: R

Reset: 0xXXXX

Description: Reserved

[31:0] RESERVED

SYSTEM_STATUS12 Thermal sensor status

31:18	17	16:10	9	8	7:1	0
RESERVED	VOBS	DATA	DATAREADY	OVERFLOW	INTREG	COMPOUT

Address: *SystemConfigBaseAddress* + 0x0038

Type: R

Reset: 0x00000000

Description: Thermal sensor status

[31:18] RESERVED

[17] **VOBS**: Reserved to debug - not connected in application.

[16:10] **DATA**: Output data.

[9] **DATAREADY**: Set to '1' every 32 clock cycles when conversion is over, valid for 1 clock period, held at '0' as long as the bandgap has not started.

[8] **OVERFLOW**: Overflow of digital adder, corresponds to the upper limit of the temperature range after calibration.

[7:1] **INTREG**: Reserved to debug - not connected in application.

[0] **COMPOUT**: Reserved to debug - not connected in application.

SYSTEM_STATUS13 Reserved

31:0
RESERVED

Address: *SystemConfigBaseAddress* + 0x003C

Type: R

Reset: 0x00000000

Description: Reserved

[31:0] RESERVED

SYSTEM_STATUS14 Reserved

31:0
RESERVED

Address: *SystemConfigBaseAddress* + 0x0040

Type: R

Reset: 0x00000000

Description: Reserved

[31:0] RESERVED

SYSTEM_STATUS15 Power-down status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																								POWER_DOWN_ACK_SATA1	RESERVED	POWER_DOWN_ACK_USB2	POWER_DOWN_ACK_USB1	POWER_DOWN_ACK_KEY_SCAN	POWER_DOWN_ACK_PCI	POWER_DOWN_ACK_EMI	RESERVED

Address: *SystemConfigBaseAddress* + 0x0044

Type: R

Reset: 0x00000000

Description: Power down status

[31:8] RESERVED

[7] **POWER_DOWN_ACK_SATA1**:
1: SATA host power down acknowledge

[6] RESERVED

[5] **POWER_DOWN_ACK_USB2**:
1: USB2 host power down acknowledge.

[4] **POWER_DOWN_ACK_USB1**:
1: USB1 host power down acknowledge

[3] **POWER_DOWN_ACK_KEY_SCAN**:
1: Key scanner power down acknowledge

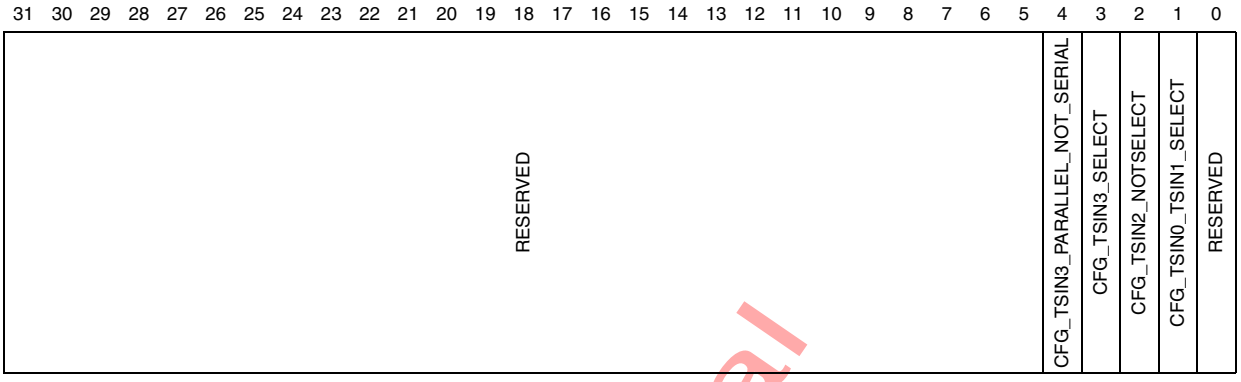
[2] **POWER_DOWN_ACK_PCI**:
1: PCI power down acknowledge

[1] **POWER_DOWN_ACK_EMI**:
1: EMI power down acknowledge

[0] RESERVED

17.1.4 System configuration register description

SYSTEM_CONFIG0 **Transport stream configuration**



Address: *SystemConfigBaseAddress* + 0x0100

Type: RW

Reset: 0x00000000

Description: Transport stream configuration

[31:5] RESERVED

[4] **CFG_TSIN3_PARALLEL_NOT_SERIAL**:
0: TSIN3 is in serial mode 1: TSIN3 is in parallel mode

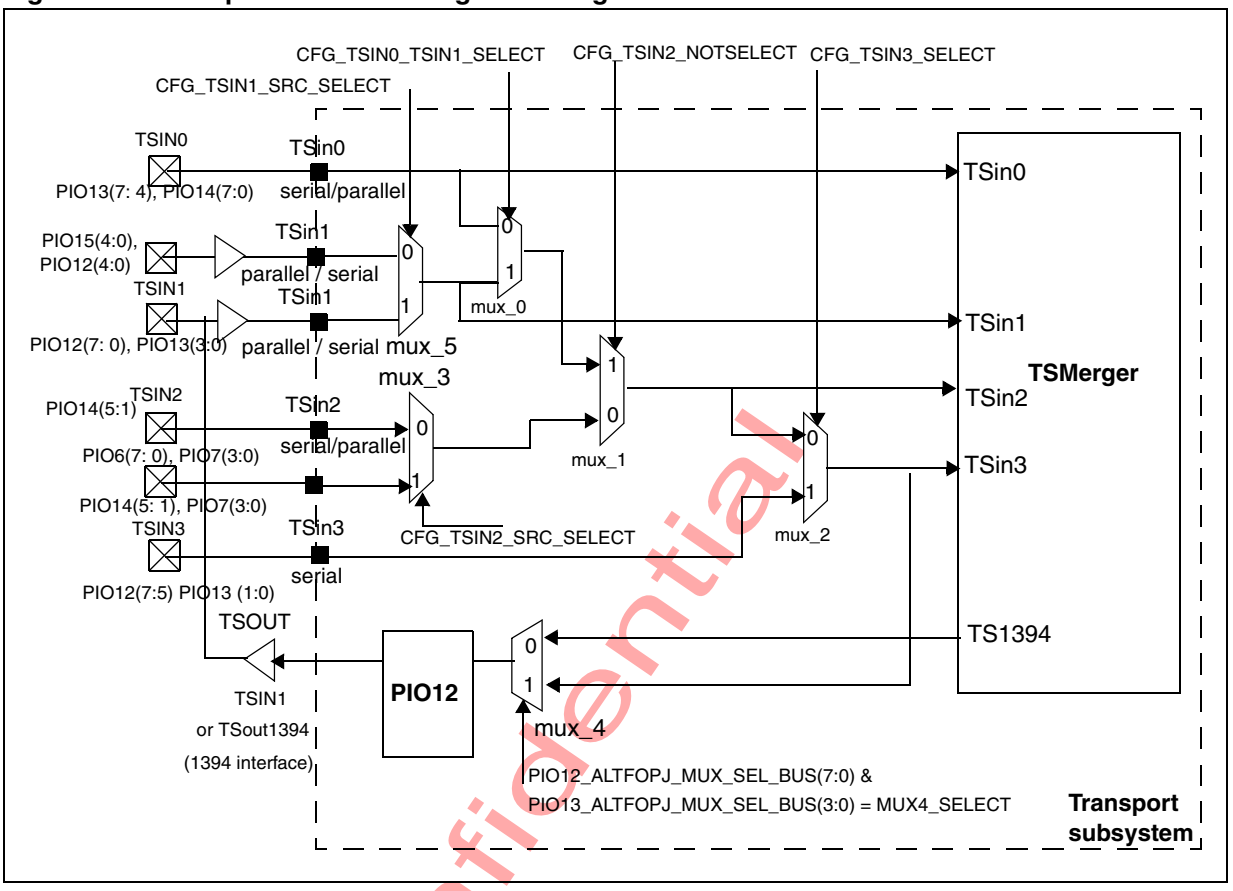
[3] **CFG_TSIN3_SELECT**:
0: TSIN3 of TS_Merger receives output of mux_1 (that is, TSIN0, TSIN1, OR TSIN2 depending upon CFG_TSIN0_TSIN1_SELECT and CFG_TSIN2_NOTSELECT)
1: TSIN3 of TS_Merger receives TSIN3

[2] **CFG_TSIN2_NOTSELECT**:
0: Input TSIN2 of TSMerger receives TSIN2
1: Input TSIN2 of TSMerger receives output of mux_0 (i.e. TSIN0 or TSIN1 depending of CFG_TSIN0_TSIN1_SELECT)

[1] **CFG_TSIN0_TSIN1_SELECT**:
0: TSIN0 routed through mux_0 to input 1 of mux_1
1: TSIN1 routed through mux_0 to input 1 of mux_1

[0] RESERVED

Figure 32. Transport stream routing to TSMerger



Note: CFG_TSIN3_PARALLEL_NOT_SERIAL is an extra programming required to select parallel mode. On reset, the TSIN3 stream by default is in serial mode. Since, on PIO TSIN3 can be selected both in parallel and serial mode, therefore, to receive TSIN3 in parallel mode this bit must be first programmed to 1. Then, serial not parallel configuration inside TSmerger will also be required to process TSIN3 in serial/parallel mode.

SYSTEM_CONFIG1 HDMI PHY compensation configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USER_COMP																															

Address: *SystemConfigBaseAddress* + 0x0104

Type: RW

Reset: 0x00000000

Description: HDMI PHY compensation configuration

[31:0] **USER_COMP**: External compensation code command to be applied to the HDMI phy.

SYSTEM_CONFIG2 HDMI / HDMI phy configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	HDMI_AUDIO_SRC_SEL	HDMI_CEC_RX_ENABLE	CLK_BCH_HDMI_DIVSEL	HDMI_HOT_PLUG_ENABLE	HDMI_POFF_ENABLE	HDMI_PHY_PREEMPWDTHEXT	HDMI_PHY_PREEMPWDTH[2:0]			HDMI_PHY_PREEMPSTR[1:0]		HDMI_PHY_PREEMPON	PROG[1:0]		COMPENSATION_BYPASS	USER_COMP[47:32]																

Address: *SystemConfigBaseAddress* + 0x0108

Type: RW

Reset: 0x0000

Description: HDMI PHY configuration

[31] RESERVED

[30] **HDMI_AUDIO_SRC_SEL**:
0: Audio SRC is 2-channel stereo 1: Audio SRC is 8-channel PCM out

[29] **HDMI_CEC_RX_ENABLE**:
0: Indicates disabled
1: Indicates usage of HDMI_CEC_RX is enabled

[28] CLK_BCH_HDMI_DIVSEL

[27] **HDMI_HOT_PLUG_ENABLE**:
1: Enables mapping of HDMI_HOT_PLUG_IN on PIO

[26] **HDMI_POFF_ENABLE**:
0: Disables power off (POFF) on HDMI 1: Enables POFF on HDMI

[25] HDMI_PHY_PREEMPWDTHEXT

[24:22] HDMI_PHY_PREEMPWDTH[2:0]

[21:20] HDMI_PHY_PREEMPSTR[1:0]

[19] HDMI_PHY_PREEMPON

[18:17] **PROG[1:0]**: Programs the output buffer speed for PROGB/PROGA.
x0: Speed set up to 1.6 Gbps 01: Speed set up to 800 Mbps
1x: Speed set up to 400 Mbps

[16] **COMPENSATION_BYPASS**: Selects internally generated compensation bits or external compensation code.
0: Provides external bits generated by USER_COMP to compensation cell
1: Provides compensation bits generated by Pivot compensation cell

[15:0] **USER_COMP[47:32]**: External compensation command bit.

SYSTEM_CONFIG3 Video DAC / HDMI configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL_S_HDMI_MDIV								PLL_S_HDMI_NDIV								PLL_S_HDMI_PDIV			PLL_S_HDMI_ENABLE	S_HDMI_RST_N	DVONOTPAD_DVP_MAIN	TST_DAC_HD_CMDR	TST_DAC_HD_CMDS	TST_DAC_SD_CMDR	TST_DAC_SD_CMDS	DAC_HD_HZU	DAC_HD_HZV	DAC_HD_HZW	DAC_SD_HZU	DAC_SD_HZV	DAC_SD_HZW

Address: *SystemConfigBaseAddress* + 0x010C

Type: RW

Reset: 0x32644000

Description: DAC configuration

[31:24] **PLL_S_HDMI_MDIV[7:0]**: Sets the dividing factor of the 8-bit programmable input divider.

[23:16] **PLL_S_HDMI_NDIV[7:0]**: Sets the dividing factor of the 8-bit programmable loop divider.

[15:13] **PLL_S_HDMI_PDIV[2:0]**: Sets the dividing factor of the 3-bit programmable output divider.

[12] **PLL_S_HDMI_ENABLE**: This signal determines the mode of operation of the rejection PLL.
0: PLL is powered down 1: Rejection PLL is powered up

[11] **S_HDMI_RST_N**:
0: HDMI serializer reset is asserted 1: HDMI serializer is de-asserted

[10] **DVONOTPAD_DVP_MAIN**:
0: DVP video input coming from pads 1: DVP video input coming from DVO

[9] **TST_DAC_HD_CMDR**: Functions with CMDR signals. Can be used to force DAC HD O/P.

[8] **TST_DAC_HD_CMDS**: Functions with CMDS signal. Can be used to force DAC HD O/P.

[7] **TST_DAC_SD_CMDR**: Functions with CMDR signals. Can be used to force DAC SD O/P.

[6] **TST_DAC_SD_CMDS**: Functions with CMDS signal. Can be used to force DAC SD O/P.

[5] **DAC_HD_HZU**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[4] **DAC_HD_HZV**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[3] **DAC_HD_HZW**:
1: Disables the DAC HD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[2] **DAC_SD_HZU**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[1] **DAC_SD_HZV**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

[0] **DAC_SD_HZW**:
1: Disables the DAC SD output current and puts the O/P in high impedance mode, but leaves the reference circuitry powered for fast recovery to active mode.

SYSTEM_CONFIG4 STBus / USB configuration control

31:17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	USBPHY_INEDGECTRL2	USB_INDCSHIFT2	USBPHY_INEDGECTRL1	USB_INDCSHIFT1	CFG_USB2_OVRCURR_ENABLE	CFG_USB1_OVRCURR_ENABLE	CFG_TSIN2_SRC_SELECT	CFG_TSIN1_SRC_SELECT	RESERVED	USB_PHY_XTAL_VALID	USB2_PRT_OVCURR_SEL	USB1_PRT_OVCURR_SEL	USB2_PRT_OVCURR_POL	USB1_PRT_OVCURR_POL	PLL_CLOCK_STOP	USB_HOST_SOFT_RESET_ENABLE	ENABLE_TID_DELTAMU

Address: *SystemConfigBaseAddress* + 0x0110

Type: RW

Reset: 0x00000126

Description: STBus/ USB Configuration

[31:17] RESERVED

[16] **USBPHY_INEDGECTRL2**:
0: USBPHY_INEDGECTRL2 is inactive 1: USBPHY_INEDGECTRL2 is active

[15] **USB_INDCSHIFT2**
0: USBPHY_INDCSHIFT2 is inactive 1: USBPHY_INDCSHIFT2 is active

[14] **USBPHY_INEDGECTRL1**:
0: USBPHY_INEDGECTRL1 is inactive 1: USBPHY_INEDGECTRL1 is active

[13] **USB_INDCSHIFT1**:
0: USBPHY_INDCSHIFT1 is inactive 1: USBPHY_INDCSHIFT1 is active

[12] **CFG_USB2_OVRCURR_ENABLE**:
0: Disabled 1: USB2_overcurrent is enabled

[11] **CFG_USB1_OVRCURR_ENABLE**:
0: Disabled 1: USB1_overcurrent is enabled

[10] **CFG_TSIN2_SRC_SELECT**:
0: TSin2 is from PIO6 1: TSin2 is from PIO14

[9] **CFG_TSIN1_SRC_SELECT:**
0: TSin1 is from PIO12 1: TSin1 is selected from PIO15

[8] RESERVED

[7] **USB_PHY_XTAL_VALID**:
0: OSC input is invalid 1: OSC input to USB PHY is stable

[6] **USB2_PRT_OVCURR_SEL**:
0: From PIO4[6] 1: USB2_PRT_OVCURR_IN is from PIO14[6]

[5] **USB1_PRT_OVCURR_SEL**:
0: From PIO4[4] 1: USB1_PRT_OVCURR_IN is from PIO12[5]

[4] **USB2_PRT_OVCURR_POL**:
0: USB2_PRT_OVCURR is sensed active low 1: USB2_PRT_OVCURR is active high

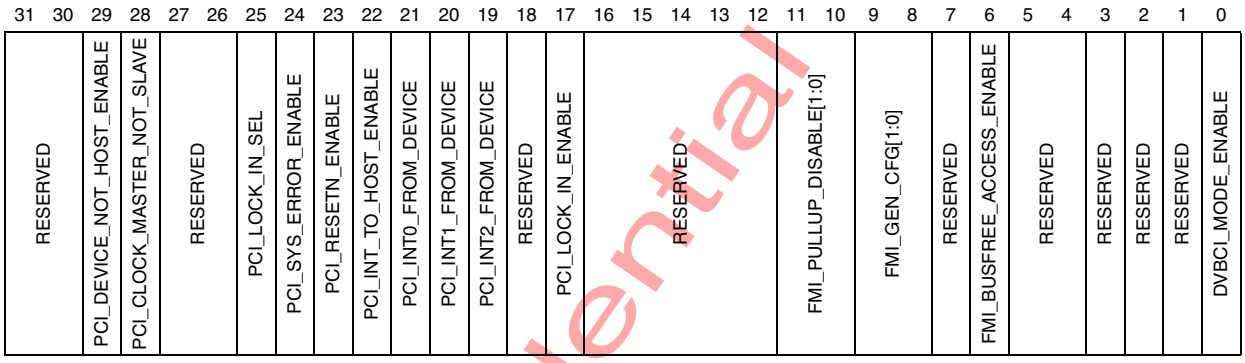
[3] **USB1_PRT_OVCURR_POL**:
0: USB1_PRT_OVCURR is sensed active low 1: USB1_PRT_OVCURR is active high

[2] **PLI_CLOCK_STOP**:
1: Stops the PLL1600 clock output to LMI padlogic

[1] **USB_HOST_SOFT_RESET_ENABLE**:
1: Allows soft reset of USB host (active low)

[0] **ENABLE_TID_DELTAMU**:
1: Enables TID[3:0] generation for DeltaMu Rasta STBUS plug2

SYSTEM_CONFIG5 EMI / PCI configuration



Address: *SystemConfigBaseAddress* + 0x0114

Type: RW

Reset: 0x04000040

Description: EMI / PCI configuration

[31:30] RESERVED

[29] **PCI_DEVICE_NOT_HOST_ENABLE**:
0: PCI is a host 1: PCI is a device

[28] **PCI_CLOCK_MASTER_NOT_SLAVE**:
0: PCI clock is slave 1: PCI clock is master

[27:26] RESERVED

[25] **PCI_LOCK_IN_SEL**:
0: PCI_LOCK_IN is from PIO7[0] 1: PCI_LOCK_IN is from PIO15[5]

[24] **PCI_SYS_ERROR_ENABLE**:
0: ISs disabled 1: Indicates PCI_SYSTEM_ERROR enabled

[23] **PCI_RESETN_ENABLE**:
0: Indicates PCI_RESETN_FROM_HOST_TO_DEVICE is disabled
1: Indicates PCI_RESETN_FROM_HOST_TO_DEVICE is enabled

[22] **PCI_INT_TO_HOST_ENABLE**:
0: Indicates INT_PCI_TO_HOST is disabled 1: Indicates INT_PCI_TO_HOST enabled

[21] **PCI_INT0_FROM_DEVICE**:
0: Indicates disabled
1: Indicates PCI_INT_FROM_DEVICE[0] is enabled

[20] **PCI_INT1_FROM_DEVICE**:
0: Indicates disabled
1: Indicates PCI_INT_FROM_DEVICE[1] is enabled

[19] **PCI_INT2_FROM_DEVICE**:
0: Indicates disabled
1: Indicates PCI_INT_FROM_DEVICE[2] is enabled

[18] RESERVED

[17] **PCI_LOCK_IN_ENABLE**:
0: indicates disabled 1: Indicates usage of PCI_LOCK_IN is enabled

[16:12] RESERVED

[11:10] **FMI_PULLUP_DISABLE[1:0]**:
0: Pullup is enabled 1: Pullup is disabled

[9:8] **FMI_GEN_CFG[1:0]**: Decides whether re-timing stages are used or not in FMI padlogic

[7] RESERVED

[6] **FMI_BUSFREE_ACCESS_ENABLE**:
0: Indicates disabled
1: EMI_BUS_FREE_ACCESSPENDING_IN enabled

[5:1] RESERVED

[0] **DVBCI_MODE_ENABLE:**
0: DVBCI mode is disabled 1: Indicates DVB-CI mode is enabled

SYSTEM_CONFIG6 Video-out configuration control

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																OLD_FASHIONED_DVO1	AUX_NOT_MAIN_DVO1	REF_NO_SYNCH_DVO1	H_NOT_V_DVO1	SPDIF_CHANNEL_SEL		PCMPLYR0_OUT_SEL			OLD_FASHIONED_DVO0	AUX_NOT_MAIN_DVO0	REF_NO_SYNCH_DVO0	H_NOT_V_DVO0	BOT_NOT_TOP_INVERSION	AUDIO_SYNC_MAIN_NOT_AUX	PIP_MODE

Address: *SystemConfigBaseAddress* + 0x0118

Type: RW

Reset: 0x0000

Description: Video-out configuration

[31:16] RESERVED

[15] **OLD_FASHIONED_DVO1**:
0: H/V reference and synch are from VTG1 1: H/V reference and synch are from main

[14] **AUX_NOT_MAIN_DVO1**:
0: H/V reference is taken from main channel 1: H/V reference is taken from AUX channel

[13] **REF_NO_SYNCH_DVO1**:
0: Input is H/V sync for DVO1 1: Input from pad is H/V reference

[12] **H_NOT_V_DVO1**:
0: V ref/sync is selected for DVO1 1: H ref/sync is selected

[11:10] **SPDIF_CHANNEL_SEL**:
00: SPDIF_CH0 is selected 01: SPDIF_CH1 is selected
10: SPDIF_CH2 is selected 11: SPDIF_CH3 is selected

[9:7] **PCMPLYR0_OUT_SEL**:
000: PCM channel 0 is routed to PCM_READER

[6] **OLD_FASHIONED_DVO0**:
0: H/V reference and synch are from VTG0 1: H/V reference and synch are from main

[5] **AUX_NOT_MAIN_DVO0**:
0: H/V reference is taken from main channel 1: H/V reference is taken from AUX channel

[4] **REF_NO_SYNCH_DVO0**:
0: Input is H/V sync for DVO0 1: Input from pad is H/V reference

[3] **H_NOT_V_DVO0**:
0: V ref/sync is selected for DVO0 1: H ref/sync is selected

[2] **BOT_NOT_TOP_INVERSION**:
0: Inversion is disabled 1: Inversion is enabled

[1] **AUDIO_SYNC_MAIN_NOT_AUX**:
0: Audio synch is taken from VTG_AUX 1: Audio synch is taken from VTG_MAIN

[0] **PIP_MODE**:
1: Video2 plug of compositor is routed to main mixer else on AUX mixer

SYSTEM_CONFIG7 Comms/Ethernet configuration control

31:28	27	26:25	24	23	22	21	20	19	18	17	16	15:13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	ENMII	PHY_INTF_SELECT	RESERVED	GLOBAL_POWER_DOWN	DAA_CONFIG_CTRL	RESERVED	MAC_SPEED_SEL	RESERVED	RMII_MODE	MIIM_DIO_SELECT	ETHERNET_INTERFACE_ON	RESERVED	DAA_SERIAL_MODE	SC1_COND_VCC_ENABLE	SC_DETECT_VPP_POL	IRB_DATA_OUT_POL_OD	SC0_DETECT_VCC_POL	SC0_COND_VCC_ENABLE	SC0_NOT_SC1_SELECT	SCCLK1_NOT_CLKDSS	SCCLK0_NOT_CLKDSS	SC1_DETECT_VCC_POL	UART2_CTS_SRC_SELECT	UART2_RXD_SRC_SELECT	SCIF_PIO_OUTEN

Address: *SystemConfigBaseAddress* + 0x011C

Type: RW

Reset: 0x08081000

Description: COMMS/Ethernet configuration

[31:28] RESERVED

[27] **ENMII**:
0: Reverse MII mode 1: MII mode

[26:25] **PHY_INTF_SELECT**: Selects the type of Ethernet mode
00: MII mode (Default) 01: Reserved
1x: Reserved

[24] RESERVED

[23] **GLOBAL_POWER_DOWN**:
0: Normal mode 1: Activate low power

[22] **DAA_CONFIG_CTRL**: DAA configuration control

[21] RESERVED

[20] **MAC_SPEED_SEL**:
0: Indicates that the MAC is running at 10 Mbps speed
1: Indicates that the MAC is running at 100 Mbps speed
Remark: Useless if RMII interface is not activated (*SYSTEM_CONFIG7*[18]). MAC speed does not need to be specified in MII mode.

[19] RESERVED

[18] **RMII_MODE**:
0: MII interface activated 1: RMII interface activated

[17] **MIIM_DIO_SELECT**:
1: MIIM_DIO from external input, else from GMAC

[16] **ETHERNET_INTERFACE_ON**:
0: All MII pads in input mode
1: Ethernet on (pads enables controlled by MAC)

[15:13] RESERVED

[12] **DAA_SERIAL_MODE**: DAA serial interface mode select pin
0: Sets a low level on FSYNC at the beginning of the transition
1: Sets a start pulse on FSYNC at the beginning of the transition

[11] **SC1_COND_VCC_ENABLE:** Enables control of smart card VCC upon detection of smart card removal or insertion.This bit is overridden by PDES_SC_MUXOUT, which is driven by a configuration bit in the PDES.

0: Alternate PIO output pin SC_NOT_SETVCC is driven permanently low
1: Alternate PIO output pin SC_NOT_SETVCC is controlled according to input SC_DETECT

[10] **SC_DETECT_VPP_POL**:

0: Output pin SC_NOT_SETVPP is PDES_SC_SETVPP
1: Output pin SC_NOT_SETVPP is inverted of PDES_SC_SETVPP

[9] **IRB_DATA_OUT_POL_OD**: Selection of polarity of IRB output signal routed as alternate function

IRB_DATA_OUT_OD to PIO_3[6] (normally configured as open-drain)

1: Polarity of IRB_DATA_OUT_OD is inverted
0: IRB_DATA_OUT_OD has same polarity as IRB_DATA_OUT

[8] **SC0_DETECT_VCC_POL**:

0: Output pin SC_NOT_SETVPP is not inverted
1: Output pin SC_NOT_SETVPP is inverted

[7] **SC0_COND_VCC_ENABLE:** Enables control of smart card VCC upon detection of smart card removal or insertion.This bit is overridden by PDES_SC_MUXOUT, which is driven by a configuration bit in the PDES.

0: Alternate PIO output pin SC_NOT_SETVCC is driven permanently low
1: Alternate PIO output pin SC_NOT_SETVCC is controlled according to input SC_DETECT

[6] **SC0_NOT_SC1_SELECT**:

0: Smartcard1 is selected 1: Smartcard 0 is selected

[5] **SCCLK1_NOT_CLKDSS**: Smartcard clock muxing selection.

0: Smartcard clock sourced from CLK_DSS (CLKgen B)
1: Smartcard clock sourced from smartcard clock generator (COMMS): SCCLKGEN1_CLK_OUT

[4] **SCCLK0_NOT_CLKDSS**: Smartcard clock muxing selection.

0: Smartcard clock sourced from CLK_DSS (CLKgen B)
1: Smartcard clock sourced from smartcard clock generator (COMMS): SCCLKGEN0_CLK_OUT

[3] **SC1_DETECT_VCC_POL**:

0: Output pin SC1_NOT_SETVCC is not inverted
1: Output pin SC1_NOT_SETVCC is inverted

[2] **UART2_CTS_SRC_SELECT**:

0: From PIO4[2] 1: UART2_CTS is from PIO12[2]

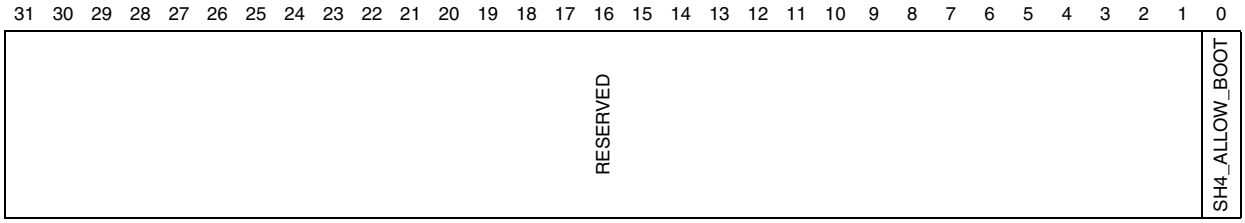
[1] **UART2_RXD_SRC_SELECT**:

0: From PIO4[1] 1: UART2_RXD is from PIO12[1]

[0] **SCIF_PIO_OUTEN**:

0: Used as regular PIO 1: SCIF output enable

SYSTEM_CONFIG8 SH4 boot configuration control



Address: *SystemConfigBaseAddress* + 0x0120

Type: RW

Reset: 0x01[d]

Description: This register configures the ST40 boot process. Bit 0 controls the ST40 boot request upon reset. Its value depends on the mode_pins (9:8) captured during the reset period.

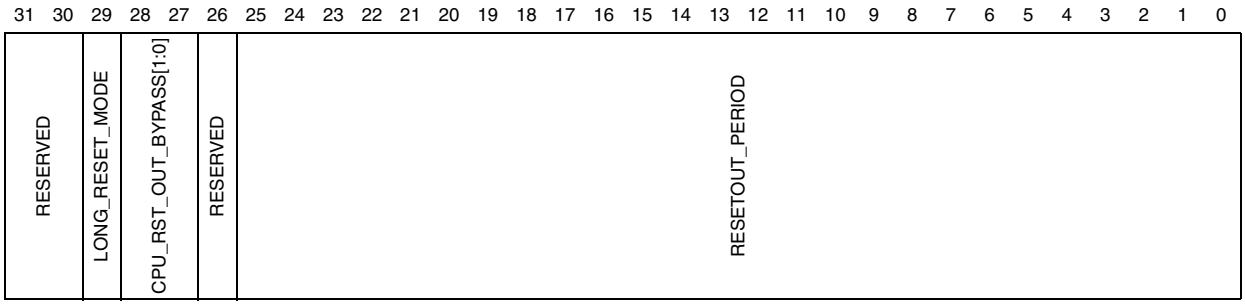
[31:1] RESERVED

[0] **SH4_ALLOW_BOOT**: ST40 request filter control.

0: Request bypassed 1: Request enabled

d. 0x01 when MODE[9:8]=00; ST40 boots, 0x00 for other values of MODE[9:8].

SYSTEM_CONFIG9 Reset Gen configuration control



Address: *SystemConfigBaseAddress* + 0x0124

Type: RW

Reset: 0xXXXX[e]

Description: Reset Gen configuration

[31:30] RESERVED

[29] **LONG_RESET_MODE**: ResetOut mode. Reset value from mode pin (7)

[28:27] **CPU_RST_OUT_BYPASS[1:0]**:
CPU_RST_OUT_BYPASS (1): bypass of (LX_Audio+LXDelphi) reset loop back
CPU_RST_OUT_BYPASS (0): bypass of (SH4+LX_Audio+LXDelphi) reset loop back
Reset value from mode pin (6:5).

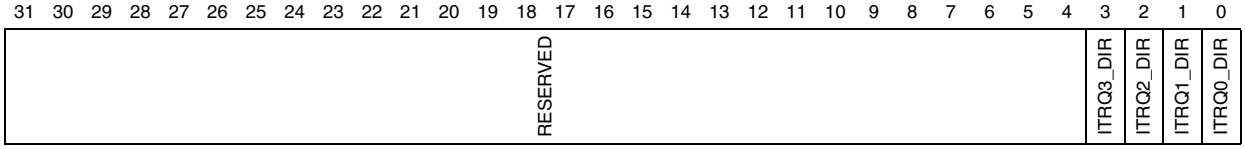
[26] RESERVED

[25:0] **RESETOUT_PERIOD**: Period of ResetOut in 27MHz cycles.
In Long ResetOut mode, the reset value guarantees a 200 ms reset out.
In short ResetOut mode, reset out lasts 100 µs.
This dynamic of this register allows for a max reset out of 2.48 s.
Reset value: 0x5265C0 in long ResetOut mode(1), 0x000A8C in short ResetOut mode

1. Long ResetOut mode is selected when the CONF input mode_pin(7) is set to 1.

e. Depends on mode pin

SYSTEM_CONFIG10 ITRQ pins configuration control



Address: *SystemConfigBaseAddress* + 0x0128

Type: RW

Reset: 0x000F

Description: ITRQ pins configuration

[31:4] RESERVED

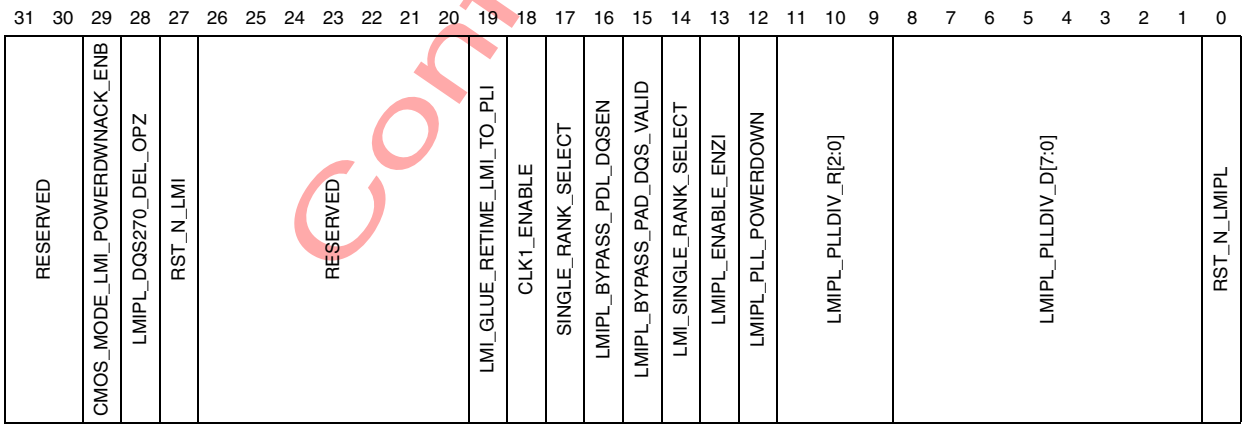
[3] **ITRQ3_DIR**:
0: ITRQ3 is configured as output 1: ITRQ3 is configured as input

[2] **ITRQ2_DIR**:
0: ITRQ2 is configured as output 1: ITRQ2 is configured as input

[1] **ITRQ1_DIR**:
0: ITRQ1 is configured as output 1: ITRQ1 is configured as input

[0] **ITRQ0_DIR**: ITRQ0 pin direction:
0: ITRQ0 configured as output 1: ITRQ0 configured as input

SYSTEM_CONFIG11 GP-LMI / LMI padlogic configuration control



Address: *SystemConfigBaseAddress* + 0x012C

Type: RW

Reset: 0x00000D28

Description: LMI padlogic configuration

[31:30] RESERVED

[29] **CMOS_MODE_LMI_POWERDWNACK_ENB**
0: CMOS mode power mode is disabled
1: CMOS mode power mode is enabled

[28] **LMIPL_DQS270_DEL_OPZ**: Selects dqs270_del as 3T/4 or T/2 (1=T/2)

[27] **RST_N_LMI**:
1: LMI sub system reset. Active Low.

[26:20] RESERVED

[19] **LMI_GLUE_RETIME_LMI_TO_PLI**:
0: No re-time 1: Re-time is done

[18] **CLK1_ENABLE**:
0: clk1 is disabled 1: clk1 is enabled

[17] **SINGLE_RANK_SELECT**:
0: Dual rank (default) 1: Single rank is selected

[16] **LMIPL_BYPASS_PDL_DQSEN**:
1: Bypasses PDL component of DQS_EN_DEL timing.

[15] **LMIPL_BYPASS_PAD_DQS_VALID**:
1: Bypasses dummy pad component of DQS_EN_DEL timing.

[14] LMI_SINGLE_RANK_SELECT:
0: Dual rank is selected 1: Single rank is selected

[13] **LMIPL_ENABLE_ENZI**:
1: Overrides ENZI disable when MODEZI = 0 (differential input mode).

[12] **LMIPL_PLL_POWERDOWN**: PLL power down
0: Normal mode 1: Power down mode

[11:9] **LMIPL_PLLDIV_R[2:0]**: Default values for PLL output clock at 666 MHz
Values for PLL output clock at 800 MHz:
LMIPL0_PLLDIV_R(2:0) = 100

[8:1] **LMIPL_PLLDIV_D[7:0]**: Default values for PLL output clock at 666 MHz
Values for PLL output clock at 800 MHz:
LMIPL0_PLLDIV_R[2:0] = 100

[0] **RST_N_LMIPL**: LMISYS_PL reset. Active low.

SYSTEM_CONFIG12 GP-LMI / LMI padlogic configuration control

31	30	29	28	27	26	25	24	23	22	21 20 19 18 17 16 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_LMIPL_FUNC_OTHERS_PD	CONF_LMIPL_FUNC_OTHERS_PU	CONF_LMIPL_FUNC_CMDDQSNCKN_PD	CONF_LMIPL_FUNC_CMDDQSNCKN_PU	LMIPL_IOREF_TQ	LMIPL_IOREF_DDR_COMP	LMIPL_IOREF_ACCURATE	LMIPL_IOREF_FREEZE	LMIPL_IOREF_COMPTQ	LMIPL_IOREF_COMPEN	LMIPL_IOREF_RASRC[6:0]	LMIPL_FUNC_TQ_VREF	LMIPL_FUNC_USEPAD_VREF	LMIPL_FUNC_ODTB	LMIPL_FUNC_ODTA	LMIPL_FUNC_MODEZI	LMIPL_FUNC_ZOUTPROGA_CMD	LMIPL_FUNC_ZOUTPROGA_CK	LMIPL_FUNC_ZOUTPROGA_DQDQSDM	LMIPL_FUNC_PROGB_CMD	LMIPL_FUNC_PROGB_CK	LMIPL_FUNC_PROGB_DQDQSDM	LMIPL_FUNC_PROGA_CMD	LMIPL_FUNC_PROGA_CK	LMIPL_FUNC_PROGA_DQDQSDM	LMIPL_FUNC_DDR

Address: *SystemConfigBaseAddress* + 0x0130

Type: RW

Reset: 0xA200180F

Description: GP-LMI / LMI padlogic configuration

[31] **CONF_LMIPL_FUNC_OTHERS_PD**: (func_pdn_active_hi) Other pads than CMD, DQSN, CKN pulldown command.

[30] **CONF_LMIPL_FUNC_OTHERS_PU**: (func_pu_active_high) Other pads than CMD, DQSN, CKN pullup command.

[29] **CONF_LMIPL_FUNC_CMDDQSNCKN_PD**: (func_pdn_active_lo)CMD, DQSN, CKN pad pulldown command.

[28] **CONF_LMIPL_FUNC_CMDDQSNCKN_PU**: (func_pu_active_lo) CMD, DQSN, CKN pad pullup command.

[27] **LMIPL_IOREF_TQ**:
1: IDDQ mode select.

[26] **LMIPL_IOREF_DDR_COMP**:
1: Controls PSW compensation signal.

[25] **LMIPL_IOREF_ACCURATE**:
1: Accurate mode select.

[24] **LMIPL_IOREF_FREEZE**:
1: Freezes compensation code.

[23] **LMIPL_IOREF_COMPTQ**: Operating mode.

[22] **LMIPL_IOREF_COMPEN**: Operating mode.

[21:15] **LMIPL_IOREF_RASRC[6:0]**: Input code.

[14] **LMIPL_FUNC_TQ_VREF**: TQ setting for VREFIN pad control.

[13] **LMIPL_FUNC_USEPAD_VREF**: Use PAD setting for VREFIN pad.

[12] **LMIPL_FUNC_ODTB**:

[11] **LMIPL_FUNC_ODTA**: ODTA / ODTB controlling On Die Termination
00: Disabled 01: RTT2 = 150 Ω
10: RTT2 = 150 Ω 11: RTT1 = 75 Ω

[10] **LMIPL_FUNC_MODEZI**: Receiver mode select (I/O MODEZI)
0: Differential 2.5 V receiver for DDR1 or Differential 1.8 V receiver for DDR2
1: 2.5 V Digital CMOS receiver for DDR1 or 1.8 V Digital CMOS receiver for DDR2

[9] **LMIPL_FUNC_ZOUTPROGA_CMD**: (func_zoutproga_abc) Outputs buffer impedance (I/O ZOUTPROGA).

[8] **LMIPL_FUNC_ZOUTPROGA_CK**: (func_zoutproga_k) Outputs buffer impedance (I/O ZOUTPROGA).

[7] **LMIPL_FUNC_ZOUTPROGA_DQDQSDM**: (func_zoutproga_d) Outputs buffer impedance(I/O ZOUTPROGA).
0: 25 Ω (Strong SSTL2)
1: 40 Ω (Weak SSTL2)

[6] **LMIPL_FUNC_PROGB_CMD**: (func_progb_abc) PROGB for CMD pads.

[5] **LMIPL_FUNC_PROGB_CK**: (func_progb_k) PROGB for CK/CKN pads.

[4] **LMIPL_FUNC_PROGB_DQDQSDM**: (func_progb_d) PROGB for DQ/DQS/DQSN/DM pads.

[3] **LMIPL_FUNC_PROGA_CMD**: (func_proga_abc) PROGA for CMD pads.

[2] **LMIPL_FUNC_PROGA_CK**: (func_proga_k) PROGA for CK/CKN pads.

[1] **LMIPL_FUNC_PROGA_DQDQSDM** (func_proga_d): PROGA for DQ/DQS/DQSN/DM pads.

[0] **LMIPL_FUNC_DDR**: DDR mode
0: DDR1 operation mode (2.5 V) 1: DDR2 operation mode (1.8 V)

SYSTEM_CONFIG13 GP-LMI / LMI padlogic configuration control

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									LMIPL_FORCE_DQS_VALID_MINUS_HALF	LMIPL_FORCE_ODT_INT_MINUS_HALF	RESERVED			LMIPL0_SEL_OEN_DEL	LMIPL0_DLL1_USR_CMD[8:0]								LMIPL0_DLL1_LOCK_CON[3:0]				LMIPL0_DLL1_INT_CMD_CON	LMIPL0_DLL1_EXT_CMD_CON	LMIPL0_PDL_CLK_OPZ_DLL1	LMIPL0_DLL1_SOFT_RST		

Address: *SystemConfigBaseAddress* + 0x0134

Type: RW

Reset: 0x00000000

Description: LMI padlogic configuration

[31:23] RESERVED

[22] **LMIPL_FORCE_DQS_VALID_MINUS_HALF**: Utilizes negative shift of DDR 0.5 CAS latency in DDR2 mode for dqs270_valid timing.
0: Aligned 1: T/2

[21] **LMIPL_FORCE_ODT_INT_MINUS_HALF**: Utilizes negative shift of DDR 0.5 CAS latency in DDR2 mode for odt_int timing.
0: Aligned 1: T/2

[20:18] RESERVED

[17] **LMIPL0_SEL_OEN_DEL**: DATA/DM output enable timing options (T/4 resolution).

[16:8] **LMIPL0_DLL1_USR_CMD**[8:0]: Allows user control of DLL1 delay.

[7:4] **LMIPL0_DLL1_LOCK_CON**[3:0]: Defines lock condition for DLL1.

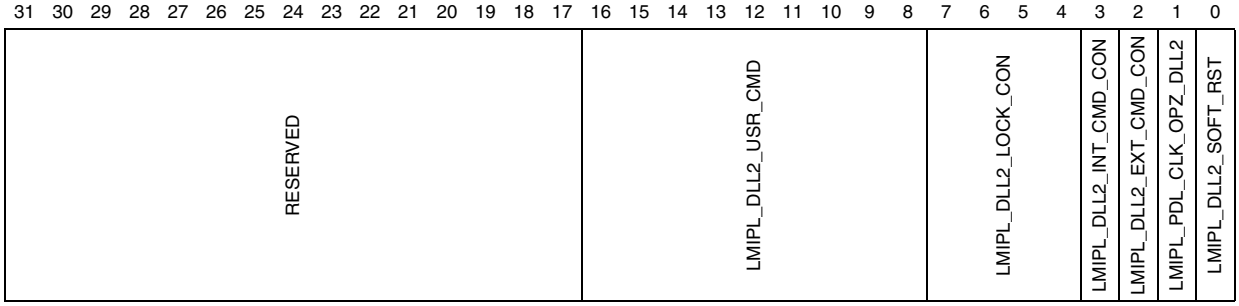
[3] **LMIPL0_DLL1_INT_CMD_CON**: Controls which internal delay command is used for DLL1.

[2] **LMIPL0_DLL1_EXT_CMD_CON**: Controls which external delay command is used for DLL1.

[1] **LMIPL0_PDL_CLK_OPZ_DLL1**: Selects CLK_COMMAND inputs for DLL1 PDLs (LOW = PDL output, HIGH = DLL output).

[0] **LMIPL0_DLL1_SOFT_RST**: DLL1 soft reset.

SYSTEM_CONFIG14 LMI padlogic configuration control



Address: *SystemConfigBaseAddress* + 0x0138

Type: RW

Reset: 0x0000

Description: LMI Padlogic configuration

[31:17] RESERVED

[16:8] **LMIPL_DLL2_USR_CMD**: Allows user control of DLL2 delay.

[7:4] **LMIPL_DLL2_LOCK_CON**: Defines lock condition for DLL2.

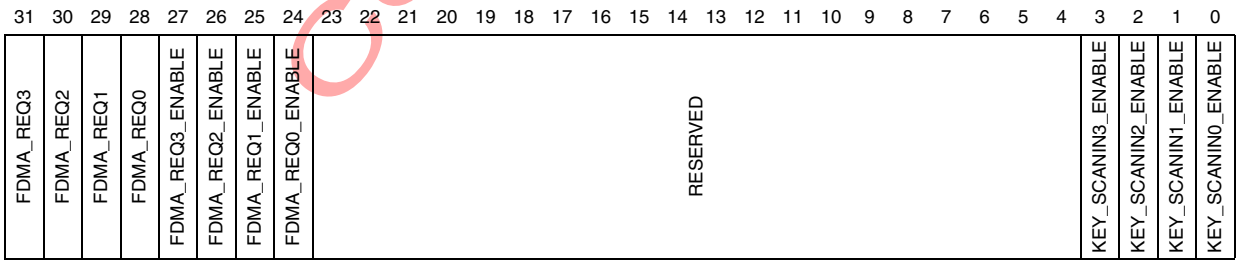
[3] **LMIPL_DLL2_INT_CMD_CON**: Controls which internal delay command is used for DLL2.

[2] **LMIPL_DLL2_EXT_CMD_CON**: Controls which external delay command is used for DLL2.

[1] **LMIPL_PDL_CLK_OPZ_DLL2**: Selects CLK_COMMAND inputs for DLL2 PDLs (LOW = PDL output, HIGH = DLL output).

[0] **LMIPL_DLL2_SOFT_RST**: DLL2 soft reset.
0: DLL2 soft reset is inactive 1: DLL2 soft reset is active

SYSTEM_CONFIG15 FDMA and key scan configuration



Address: *SystemConfigBaseAddress* + 0x013C

Type: RW

Reset: 0x000000

Description: FDMA and key scan configuration

[31] **FDMA_REQ3**: Internal FDMA req 3 ORed with external FDMA req 3

[30] **FDMA_REQ2**: Internal FDMA req 2 ORed with external FDMA req 2

[29] **FDMA_REQ1**: Internal FDMA req 1ORed with external FDMA req 1

[28] **FDMA_REQ0**: Internal FDMA req 0 ORed with external FDMA req 0

[27] **FDMA_REQ3_ENABLE**: External FDMA req 3 enable

[26] **FDMA_REQ2_ENABLE**: External FDMA req 2 enable

[25] **FDMA_REQ1_ENABLE**: External FDMA req 1 enable

[24] **FDMA_REQ0_ENABLE**: External FDMA req 0 enable

[23:4] RESERVED

[3] **KEY_SCANIN3_ENABLE**:
0: Indicates key_scanin3 disabled 1: Indicates key_scanin3 enabled

[2] **KEY_SCANIN2_ENABLE**:
0: Indicates key_scanin2 disabled 1: Indicates key_scanin2 enabled

[1] **KEY_SCANIN1_ENABLE**:
0: Indicates key_scanin1 disabled 1: Indicates key_scanin1 enabled

[0] **KEY_SCANIN0_ENABLE**:
0: Indicates key_scanin0 disabled 1: Indicates key_scanin0 enabled

SYSTEM_CONFIG16 Comms SSC configuration

31–20	19–18	17–16	15–14	13	12–11	10–9	8–7	6–5	4	3	2–1	0
RESERVED	SSC3_SCLK_IN	SSC3_MTSR_IN_SEL[1:0]	SSC3_MRST_IN_SEL[1:0]	RESERVED	SSC2_SCLK_IN[1:0]	SSC2_MTSR_IN_SEL[1:0]	SSC2_MRST_IN_SEL[1:0]	RESERVED		SSC1_MRST_IN_SEL	RESERVED	SSC0_MRST_IN_SEL

Address: *SystemConfigBaseAddress* + 0x0140

Type: RW

Reset: 0x000000

Description: Comms SSC configuration

[31:20] RESERVED

[19:18] **SSC3_SCLK_IN**:
00: ssc3_sclk_in from PIO3[6] 01: ssc3_sclk_in from PIO13[2]
1x: ssc3_sclk_in from PIO13(6)

[17:16] **SSC3_MTSR_IN_SEL[1:0]**:
00: ssc3_mtsr_in from PIO3[7] 01: ssc3_mtsr_in from PIO13[3]
1x: ssc3_mtsr_in from PIO13[7]

[15:14] **SSC3_MRST_IN_SEL[1:0]**:
00: ssc3_mrst_in from PIO2[1] 01: ssc3_mrst_in from PIO3(7)
10: ssc3_mrst_in from PIO13[3] 11: ssc3_mrst_in from PIO13(7)

[13] RESERVED

[12:11] **SSC2_SCLK_IN[1:0]**:
0x: ssc2_sclk_in from PIO3[4] 10: ssc2_sclk_in from PIO12[0]
11: ssc2_sclk_in from PIO13[4]

[10:9] **SSC2_MTSR_IN_SEL[1:0]**:
00: ssc2_mtsr_in from PIO3[5] 01: ssc2_mtsr_in from PIO12[1]
1x: ssc2_mtsr_in from PIO13[5]

[8:7] **SSC2_MRST_IN_SEL[1:0]**:
00: ssc2_mrst_in from PIO2[0] 01: ssc2_mrst_in from PIO3[5]
10: ssc2_mrst_in from PIO12[1] 11: ssc2_mrst_in from PIO13[5]

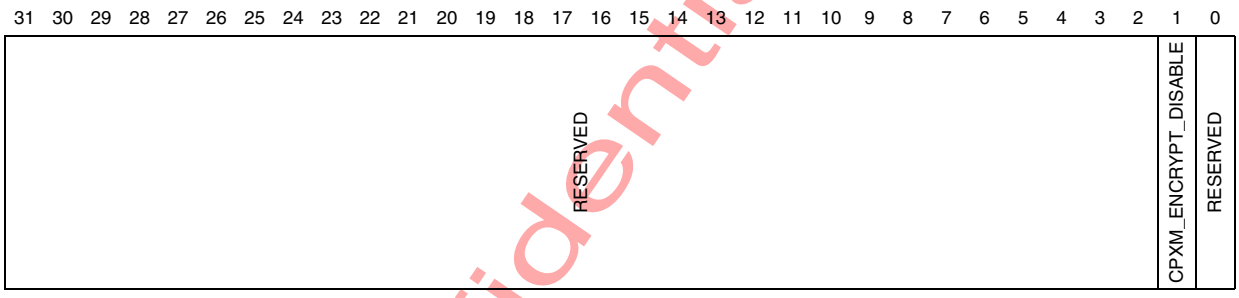
[6:4] RESERVED

[3] **SSC1_MRST_IN_SEL**:
0: ssc1_mrst_in is from PIO2[6] 1: ssc1_mrst_in is from PIO2[7]

[2:1] RESERVED

[0] **SSC0_MRST_IN_SEL**:
0: ssc0_mrst_in is from PIO2[3] 1: ssc0_mrst_in is from PIO2[4]

SYSTEM_CONFIG17 CPXM CPRM enable configuration



Address: *SystemConfigBaseAddress* + 0x0144

Type: RW

Reset: 0x00000002

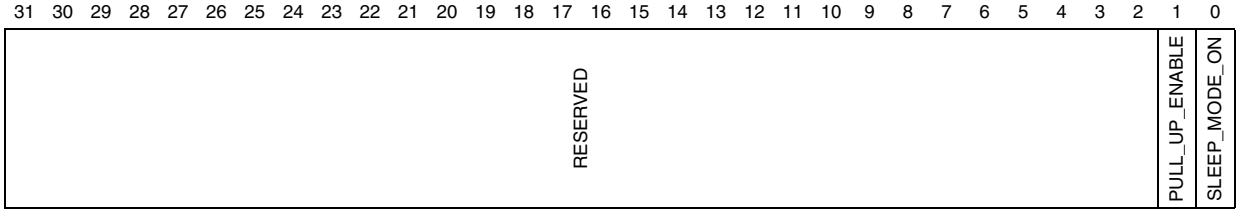
Description: CPXM CPRM encode enable configuration

[31:2] RESERVED

[1] **CPXM_ENCRYPT_DISABLE**:
0: Enabled only if CPXM feature is enabled 1: CPXM_ENCRYPT is disabled

[0] RESERVED

SYSTEM_CONFIG18 PAD State control



Address: *SystemConfigBaseAddress* + 0x0148

Type: RW

Reset: 0x0000

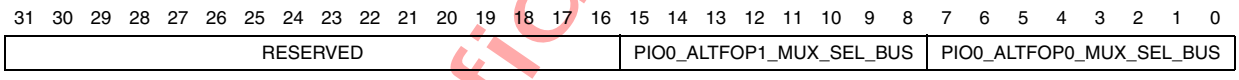
Description: Pad state configuration

[31:2] RESERVED

[1] **PULL_UP_ENABLE**:
0: Indicates pull up is de-active 1: Indicates pad pullup is active

[0] **SLEEP_MODE_ON**:
0: Indicates switched off 1: Indicates sleep mode control switched on

SYSTEM_CONFIG19 Alternate function output control for PIO 0



Address: *SystemConfigBaseAddress* + 0x014C

Type: RW

Reset: 0x0000

Description: PIO0 alternate function output configuration

[31:16] RESERVED

[15:8] **PIO0_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO0_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO0_ALTFOPJ_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG20 Alternate function output control for PIO 1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO1_ALTFOP1_MUX_SEL_BUS								PIO1_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0150

Type: RW

Reset: 0x00000000

Description: Alternate Function PIO1 Output Control

[31:16] RESERVED
[15:8] **PIO1_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO1_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO1_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0)]

SYSTEM_CONFIG21 Alternate function output control for PIO 2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO2_ALTFOP1_MUX_SEL_BUS								PIO2_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0154

Type: RW

Reset: 0x00000000

Description: PIO2 alternate function output configuration

[31:16] RESERVED
[15:8] **PIO2_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO2_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO2_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG22 Compensation configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CONF_3V3COMP2_RASRC							CONF_3V3COMP2_FREEZE	CONF_3V3COMP2_COMPTQ	CONF_3V3COMP2_COMPEN	CONF_3V3COMP1_RASRC							CONF_3V3COMP1_FREEZE	CONF_3V3COMP1_COMPTQ	CONF_3V3COMP1_COMPEN	CONF_3V3COMP0_RASRC						CONF_3V3COMP0_FREEZE	CONF_3V3COMP0_COMPTQ	CONF_3V3COMP0_COMPEN

Address: *SystemConfigBaseAddress* + 0x0158

Type: RW

Reset: 0x00000000

Description: Compensation configuration

[31:30] RESERVED

[29:23] **CONF_3V3COMP2_RASRC**: 3V3 COMPENSATION 2: Input code

[22] **CONF_3V3COMP2_FREEZE**: 3V3 COMPENSATION 2: Freezes ASRC code to its last value

[21] **CONF_3V3COMP2_COMPTQ**:

[20] **CONF_3V3COMP2_COMPEN**: 3V3 COMPENSATION 2: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

[19:13] **CONF_3V3COMP1_RASRC**: 3V3 COMPENSATION 1: Input code

[12] **CONF_3V3COMP1_FREEZE**: 3V3 COMPENSATION 1: Freezes ASRC code to its last value

[11] **CONF_3V3COMP1_COMPTQ**:

[10] **CONF_3V3COMP1_COMPEN**: 3V3 COMPENSATION 1: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

[9:3] **CONF_3V3COMP0_RASRC**: 3V3 COMPENSATION 0: Input code

[2] **CONF_3V3COMP0_FREEZE**: 3V3 COMPENSATION 0: Freezes ASRC code to its last value

[1] **CONF_3V3COMP0_COMPTQ**:

[0] **CONF_3V3COMP0_COMPEN**: 3V3 COMPENSATION 0: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

SYSTEM_CONFIG23 Compensation configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CONF4_3V3COMP_TQ	CONF_3V3COMP4_FREEZE	CONF_3V3COMP4_COMPTQ	CONF_3V3COMP4_COMPEN		CONF_3V3COMP4_RASRC									CONF3_3V3COMP_TQ	CONF_3V3COMP3_RASRC								CONF_3V3COMP3_FREEZE	CONF_3V3COMP3_COMPTQ	CONF_3V3COMP3_COMPEN

Address: *SystemConfigBaseAddress* + 0x015C

Type: RW

Reset: 0x00000000

Description: Compensation configuration

[31:25] RESERVED

[24] **CONF4_3V3COMP_TQ**: Drives the 4 compensations TQ pin 1 to put the cells in IDDQ mode

[23] **CONF_3V3COMP4_FREEZE**: 3V3 COMPENSATION 4: Freezes ASRC code to its last value

[22] **CONF_3V3COMP4_COMPTQ**:

[21:20] **CONF_3V3COMP4_COMPEN**: 3V3 COMPENSATION 4: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

[19:11] **CONF_3V3COMP4_RASRC**: 3V3 COMPENSATION 4: Input code

[10] **CONF3_3V3COMP_TQ**: Drives the 4 compensations TQ pin
1: Puts the cells in IDDQ mode

[9:3] **CONF_3V3COMP3_RASRC**: 3V3 COMPENSATION 3: Input code

[2] **CONF_3V3COMP3_FREEZE**: 3V3 COMPENSATION 3: Freeze ASRC code to its last value

[1] **CONF_3V3COMP3_COMPTQ**:

[0] **CONF_3V3COMP3_COMPEN**: 3V3 COMPENSATION 3: Operating mode (comptq/compen)
00: Normal mode 01: HZ mode
11: Read mode

SYSTEM_CONFIG24 OSC configuration

31:6	5	4	3	2	1:0
RESERVED	CLKGENA_OBSCLK_ENABLE	SYSCLKOUT_ENABLE	RESERVED	OSCI_BYPASS	RESERVED

Address: *SystemConfigBaseAddress* + 0x0160

Type: RW

Reset: 0x0000000C

Description: Oscillator configuration

[31:6] RESERVED

[5] **CLKGENA_OBSCLK_ENABLE**:
0: Disabled 1: ClockGenA clk output is enabled

[4] **SYSCLKOUT_ENABLE**:
0: Disabled 1: ClockGenB clk output is enabled

[3] RESERVED

[2] **OSCI_BYPASS**:
0: OSC is bypassed 1: OSC is not bypassed

[1:0] RESERVED

SYSTEM_CONFIG25 Alternate function output control for PIO 3

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO3_ALTFOP1_MUX_SEL_BUS								PIO3_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0164

Type: RW

Reset: 0x0000

Description: PIO3 alternate function output

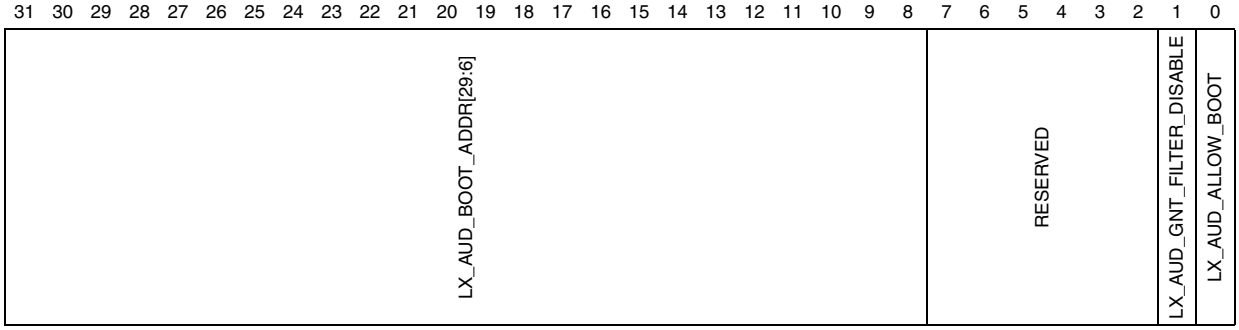
[31:16] RESERVED

[15:8] **PIO3_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO3_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4: PIO3_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG26 LX audio configuration



Address: *SystemConfigBaseAddress* + 0x0168

Type: RW

Reset: 0xXXXX(f)

Description: LX Audio configuration

[31:8] **LX_AUD_BOOT_ADDR[29:6]**: ST230 AUDIO boot address.

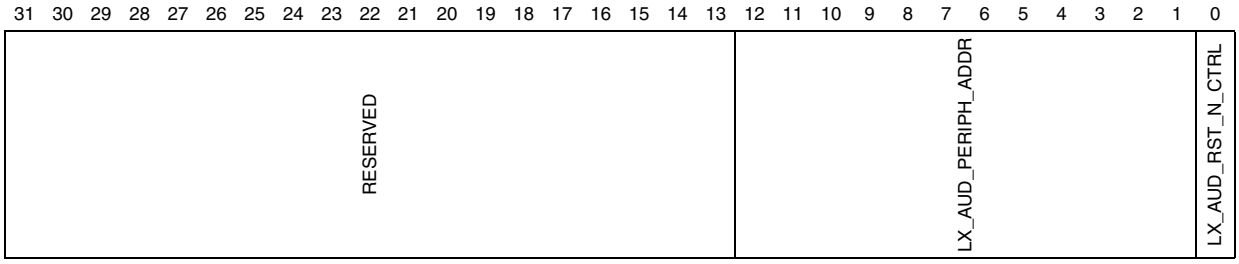
[7:2] RESERVED

[1] **LX_AUD_GNT_FILTER_DISABLE**:
1: Filter is disabled

[0] **LX_AUD_ALLOW_BOOT**: ST230 AUDIO request filter.
0: Request bypassed 1: Request enabled

f. Depends on mode pins; reset value is:
0 for other values of MODE[9:8] and LX_AUDIO_BOOT_ENABLE
1 when MODE[9:8]=10 AND LX_AUDIO_BOOT_ENABLE=1

SYSTEM_CONFIG27 LX audio configuration



Address: *SystemConfigBaseAddress* + 0x016C

Type: RW

Reset: 0x1FD0

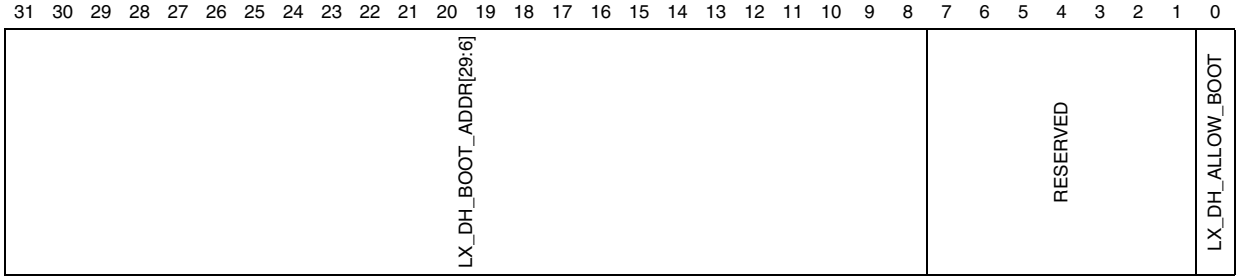
Description: LX Audio configuration

[31:13] RESERVED

[12:1] **LX_AUD_PERIPH_ADDR**: ST230 AUDIO peripheral address.

[0] **LX_AUD_RST_N_CTRL**: ST230 AUDIO reset active low control bit.
0: Reset of ST230 driven by hardware reset 1: Reset of ST230 fixed to active state

SYSTEM_CONFIG28 LX Delta Rasta configuration



Address: *SystemConfigBaseAddress* + 0x0170

Type: RW

Reset: 0xXXXX(g)

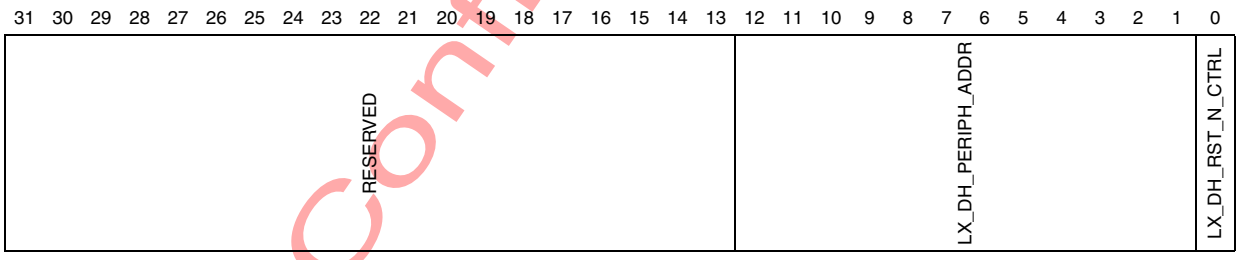
Description: LX Delta Rasta configuration

[31:8] **LX_DH_BOOT_ADDR[29:6]**: ST230 DELPHI boot address.

[7:1] RESERVED

[0] **LX_DH_ALLOW_BOOT**:
ST230 DELPHI request filter:
0: Request bypassed 1: Request enabled

SYSTEM_CONFIG29 LX Delta Rasta configuration



Address: *SystemConfigBaseAddress* + 0x0174

Type: RW

Reset: 0x1FCC

Description: LX Delta Rasta configuration

g. Depends on mode pins; reset value is:
0: For other values of MODE[9:8] and LX_DELTA_BOOT_ENABLE
1: When MODE[9:8]=01 AND LX_DELTA_BOOT_ENABLE=1

[31:13] RESERVED

[12:1] **LX_DH_PERIPH_ADDR**: ST230 DELPHI peripheral address.

[0] **LX_DH_RST_N_CTRL**: ST230 DELPHI reset active low control bit.
0: Reset of ST230 driven by hardware reset 1: Reset of ST230 fixed to active state

SYSTEM_CONFIG30 Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0178

Type: RW

Reset: 0x0000

Description: Reserved

[31:0] RESERVED

SYSTEM_CONFIG31 EMI configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED											EMI_PAD_MODE	RESERVED																	DMA_SRC_ID[3:0]			

Address: *SystemConfigBaseAddress* + 0x017C

Type: RW

Reset: 0x0000

Description: EMI configuration

[31:21] RESERVED

[20] **EMI_PAD_MODE**:
0: TTL bi-directional mode (EMI) 1: PCI mode

[19:4] RESERVED

[3:0] **DMA_SRC_ID[3:0]**: DMA source ID.

SYSTEM_CONFIG32 Power down configuration

31:12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	SATA_HC_POWER_DOWN_REQ	RESERVED	SATA_PHY_POWER_DOWN_REQ	RESERVED	USB2_PHY_POWER_DOWN_REQ	USB1_PHY_POWER_DOWN_REQ	USB2_HC_POWER_DOWN_REQ	USB1_HC_POWER_DOWN_REQ	KEY_SCAN_POWER_DOWN_REQ	PCI_POWER_DOWN_REQ	EMI_POWER_DOWN_REQ	RESERVED

Address: *SystemConfigBaseAddress* + 0x0180

Type: RW

Reset: 0x0B35

Description: Power down configuration

[31:12] RESERVED

[11] **SATA_HC_POWER_DOWN_REQ**:
0: SATA host power up 1: SATA host power down

[10] RESERVED

[9] **SATA_PHY_POWER_DOWN_REQ**:
1: Power down request for SATA PHY module

[8] RESERVED

[7] **USB2_PHY_POWER_DOWN_REQ**:
0: USB2 phy is power up 1: USB2 phy is in power down

[6] **USB1_PHY_POWER_DOWN_REQ**:
0: USB1 phy is power up 1: USB1 phy is in power down

[5] **USB2_HC_POWER_DOWN_REQ**:
1: Power down request for USB2 HC module

[4] **USB1_HC_POWER_DOWN_REQ**:
1: Power down request for USB1 HC module

[3] **KEY_SCAN_POWER_DOWN_REQ**:
1: Power down request for Key scanner module

[2] **PCI_POWER_DOWN_REQ**:
1: Power down request for PCI module is active

[1] **EMI_POWER_DOWN_REQ**:
1: Power down request for EMI module is active

[0] RESERVED

Note: 1 Due to the reset value of bit 0, 2 ,4,5,9, and 11 the PCI and USB PHY's and SATA HC+PHY are switched off by default.

2 USB PHY's power down are active low.

SYSTEM_CONFIG33 SOFT_JTAG register (USB) configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXTERNAL_DAA_SEL	RESERVED																								SOFT_JTAG_EN	TMS_SATA	TRSTN_SATA	TMS_USB	TRSTN_USB	TDI	TCK

Address: *SystemConfigBaseAddress* + 0x0184

Type: RW

Reset: 0x00000000

Description: SOFT_JTAG register (USB) configuration

[31] EXTERNAL_DAA_SEL

[30:7] RESERVED

[6] **SOFT_JTAG_EN**: High level means that USB2.0 or SATA TAP is managed by SOFT_JTAG register; Low level means JTAG is through PAD.

[5] **TMS_SATA**: TEST mode select for SATA TAP only

[4] **TRSTN_SATA**: Asynchronous reset for SATA TAP only.

[3] **TMS_USB**: Test mode select USB2.0 TAP only.

[2] **TRSTN_USB**: Asynchronous reset USB2.0 TAP only.

[1] **TDI**: Test data input for the USB2.0 TAP or SATA TAP.

[0] **TCK**: Test clock for the USB2.0 TAP or SATA TAP.

SYSTEM_CONFIG34 Alternate function PIO output control for PIO 4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO4_ALTFOP1_MUX_SEL_BUS								PIO4_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0188

Type: RW

Reset: 0x00000000

Description: PIO4 alternate function output configuration

[31:16] RESERVED

[15:8] **PIO4_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO4_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4 : PIO4_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG35 Alternate function PIO output control for PIO 5

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO5_ALTFOP1_MUX_SEL_BUS								PIO5_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x018C

Type: RW

Reset: 0x0000

Description: PIO5 alternate function output configuration

[31:16] RESERVED

[15:8] **PIO5_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO5_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4 : PIO5_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG36 Alternate Function PIO Output Control for PIO 6

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO6_ALTFOP1_MUX_SEL_BUS								PIO6_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0190

Type: RW

Reset: 0x0000

Description: PIO6 alternate function output configuration

[31:16] RESERVED
[15:8] **PIO6_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO6_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4 : PIO6_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG37 Alternate function PIO output control for PIO 7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO7_ALTFOP1_MUX_SEL_BUS								PIO7_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x0194

Type: RW

Reset: 0x00000000

Description: PIO7 alternate function output configuration

[31:16] RESERVED
[15:8] **PIO7_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO7_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 10 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 4 : PIO7_ALTFOPj_MUX_SEL_BUS(n) = 11 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG38 LMI / LMI padlogic configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED							CONF_LMI_SEL_SYNC_FLOP_NB[1:0]		CONF_LMI_SEL_SYNC_FLOP_HALF	CONF_LMI_SEL_CLK_PHASE	CONF_LMI_PWRD_REQ	CONF_LMI_HP_EN_AP[1:0]		CONF_LMI_LP_EN_AP[1:0]		RESERVED									CONF_LMI_MEM_BASE_ADDR[7:0]							

Address: *SystemConfigBaseAddress* + 0x0198

Type: RW

Reset: 0x0000000C

Description: LMI / LMI padlogic configuration

[31:25] RESERVED

[24:23] **CONF_LMI_SEL_SYNC_FLOP_NB[1:0]**: Selection of the number of flops used in the synchronizer to prevent metastability.

00: Two flops are used
01: Three flops are used
10 : Four flops are used
11: One flop is used; For test/characterization only

[22] **CONF_LMI_SEL_SYNC_FLOP_HALF**: Selection of the CLK_M clock or CLK_M180 used for the first resync. flop used to prevent metastability:

0: Both rising and falling edges of CLK_M are used
1: Only rising edge of CLK_M is used

[21] **CONF_LMI_SEL_CLK_PHASE**: Selection of the clock edges used in FIFO control:

0: Both rising and falling edges of CLK_M are used
1: Only rising edges of CLK_M is used

[20] **CONF_LMI_PWRD_REQ**: LMI power down request.

[19:18] **CONF_LMI_HP_EN_AP[1:0]**: Enables read with autoprecharge on lmi0 high priority port.

[17:16] **CONF_LMI_LP_EN_AP[1:0]**: Enables read with autoprecharge on lmi0 low priority port.

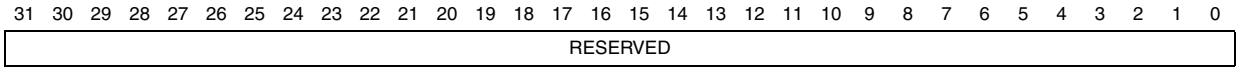
[15:8] RESERVED

[7:0] **CONF_LMI_MEM_BASE_ADDR[7:0]**: LMI memory base address.

29-bit LMI base address: 0x0C

32-bit LMI base address: 0x40

SYSTEM_CONFIG39 Reserved



Address: *SystemConfigBaseAddress* + 0x019C

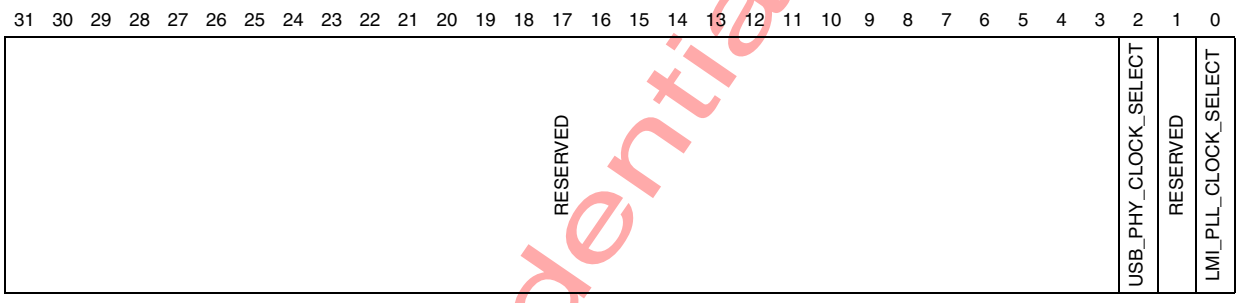
Type: RW

Reset: 0x0000

Description: Reserved

[31:0] RESERVED

SYSTEM_CONFIG40 Clock select configuration



Address: *SystemConfigBaseAddress* + 0x01A0

Type: RW

Reset: 0x00000004

Description: Clock select configuration

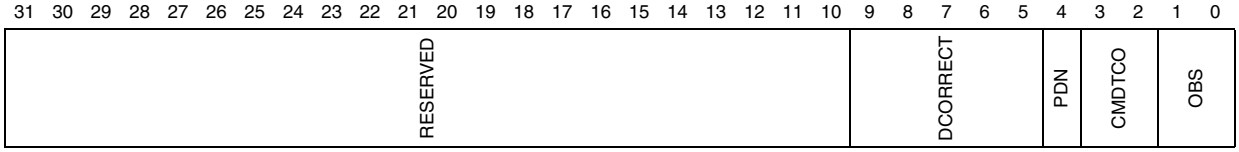
[31:3] RESERVED

[2] **USB_PHY_CLOCK_SELECT**: Select clock for USB PHY.
0: Clock from SATA OSC 1: Clock from alternate pad

[1] RESERVED

[0] **LMI_PLL_CLOCK_SELECT**: Select clock for LMI Pll input.
0: Clock from alternate pad 1: Clock from SATA OSC

SYSTEM_CONFIG41 Thermal sensor configuration



Address: *SystemConfigBaseAddress* + 0x01A4

Type: RW

Reset: 0x00000008

Description: Thermal sensor configuration

[31:10] RESERVED

[9:5] **DCORRECT**: Digital code to correct systematic offset by addition to the digital output.

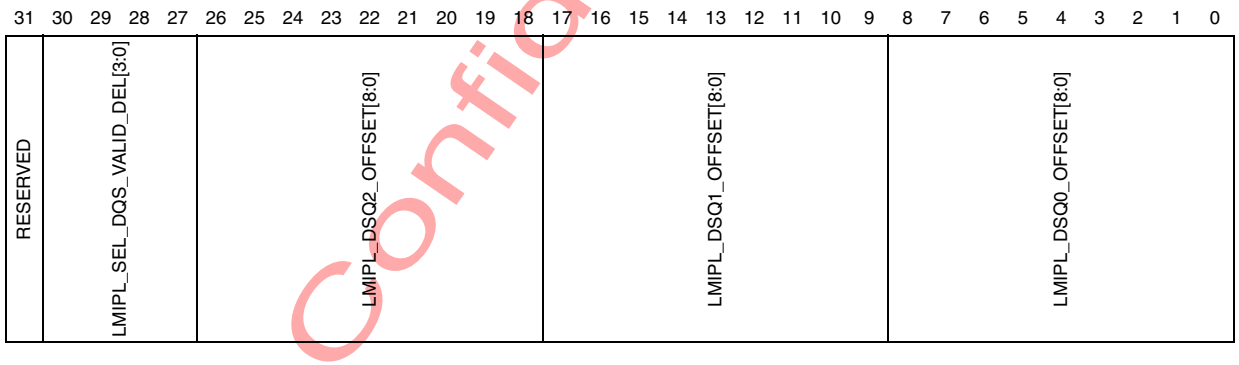
[4] **PDN**: Power Down

0: Power down mode 1: Normal mode; asynchronous

[3:2] **CMDTCO:** Reserved to debug. To be fixed to 10 in application.

[1:0] **OBS:** Reserved to debug. To be fixed to 00 in application.

SYSTEM_CONFIG42 LMI / LMI padlogic configuration



Address: *SystemConfigBaseAddress* + 0x01A8

Type: RW

Reset: 0x0000

Description: LMI padlogic configuration

[31] RESERVED

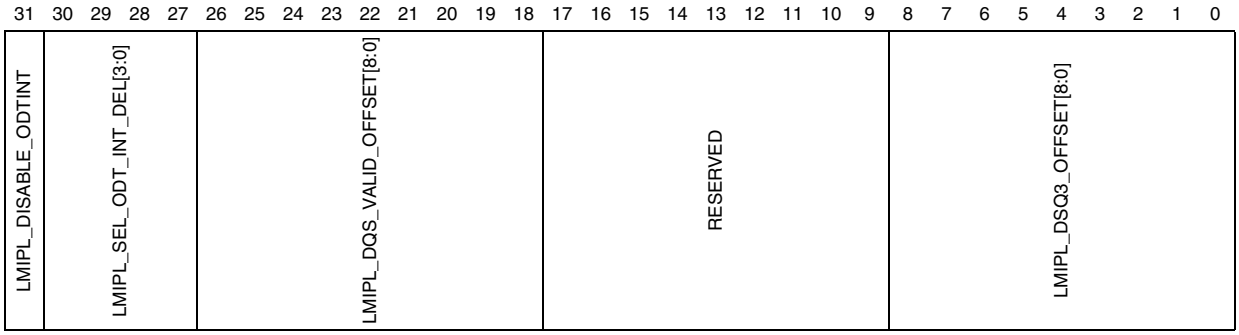
[30:27] **LMIPL_SEL_DQS_VALID_DEL[3:0]**: 'dqs_valid' timing options (T/4 resolution).

[26:18] **LMIPL_DSQ2_OFFSET[8:0]**: Offset command for DQS[2] PDL.

[17:9] **LMIPL_DSQ1_OFFSET[8:0]**: Offset command for DQS[1] PDL.

[8:0] **LMIPL_DSQ0_OFFSET[8:0]**: Offset command for DQS[0] PDL.

SYSTEM_CONFIG43 LMI / LMI Padlogic configuration



Address: *SystemConfigBaseAddress* + 0x01AC

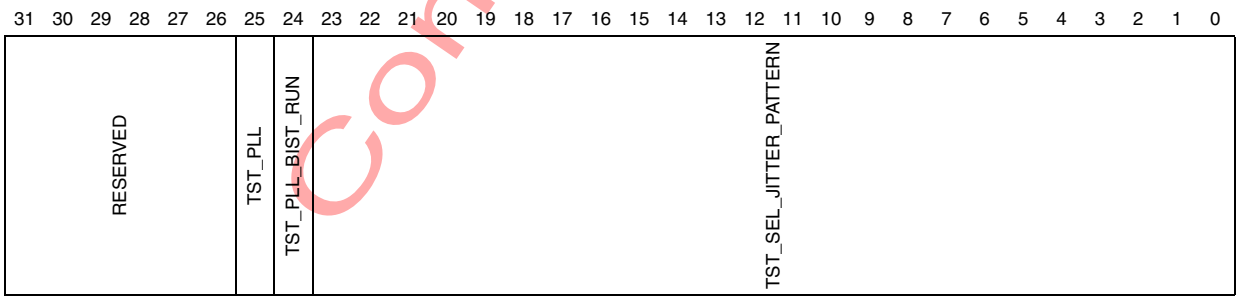
Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic configuration

[31] **LMIPL_DISABLE_ODTINT**: Disables Internal ODT function (as in DDR1 mode).
[30:27] **LMIPL_SEL_ODT_INT_DEL[3:0]**: Internal ODT timing options (T/4 resolution).
[26:18] **LMIPL_DQS_VALID_OFFSET[8:0]**: Offset command for 'dqs_en_del' PDL.
[17:9] RESERVED
[8:0] **LMIPL_DSQ3_OFFSET[8:0]**: Offset command for DQS[3] PDL.

SYSTEM_CONFIG44 ClockgenD Jitter estimator



Address: *SystemConfigBaseAddress* + 0x01B0

Type: RW

Reset: 0x00000000

Description: ClockGen D Jitter estimator configuration

[31:26] RESERVED
[25] **TST_PLL**
[24] **TST_PLL_BIST_RUN**
[23:0] **TST_SEL_JITTER_PATTERN**

SYSTEM_CONFIG45 Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x01B4

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] RESERVED

SYSTEM_CONFIG46 Alternate function PIO output control for PIO 8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO8_ALTFOP1_MUX_SEL_BUS								PIO8_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01B8

Type: RW

Reset: 0x0000

Description: PIO8 alternate function output configuration

[31:16] RESERVED

[15:8] **PIO8_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO8_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO8_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG47 Alternate function PIO output control for PIO 9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO9_ALTFOP1_MUX_SEL_BUS								PIO9_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01BC

Type: RW

Reset: 0x0000

Description: PIO9 alternate function output configuration

[31:16] RESERVED
[15:8] **PIO9_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO9_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO9_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG48 Alternate function PIO output control for PIO 12

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								PIO12_ALTFOP2_MUX_SEL_BUS								PIO12_ALTFOP1_MUX_SEL_BUS								PIO12_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01C0

Type: RW

Reset: 0x0000

Description: PIO12 alternate function output configuration

[31:24] RESERVED
[23:16] **PIO12_ALTFOP2_MUX_SEL_BUS**
[15:8] **PIO12_ALTFOP1_MUX_SEL_BUS**
[7:0] **PIO12_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 000 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]
Alternate 2 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 001 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]
Alternate 3 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 010 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]
Alternate 4 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 011 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]
Alternate 5 : PIO12_ALTFOPj_MUX_SEL_BUS(n) = 1xx [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG49 Alternate function PIO output control for PIO 13

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
RESERVED	PIO13_ALTFOP2_MUX_SEL_BUS	PIO13_ALTFOP1_MUX_SEL_BUS	PIO13_ALTFOP0_MUX_SEL_BUS

Address: *SystemConfigBaseAddress* + 0x01C4

Type: RW

Reset: 0x0000

Description: PIO13 alternate function output configuration

[31:24] RESERVED

[23:16] **PIO13_ALTFOP2_MUX_SEL_BUS**

[15:8] **PIO13_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO13_ALTFOP0_MUX_SEL_BUS**

Note: Alternate 1 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 000 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 001 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 010 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 4 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 011 [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

Alternate 5 : PIO13_ALTFOPj_MUX_SEL_BUS(n) = 1xx [(j = 0,1,2); (n = 0,1,2,3,4,5,6,7)]

SYSTEM_CONFIG50 Alternate function PIO output control for PIO 15

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																PIO15_ALTFOP1_MUX_SEL_BUS								PIO15_ALTFOP0_MUX_SEL_BUS							

Address: *SystemConfigBaseAddress* + 0x01C8

Type: RW

Reset: 0x00000400

Description: PIO15 alternate function output configuration

[31:16] RESERVED

[15:8] **PIO15_ALTFOP1_MUX_SEL_BUS**

[7:0] **PIO15_ALTFOP0_MUX_SEL_BUS**

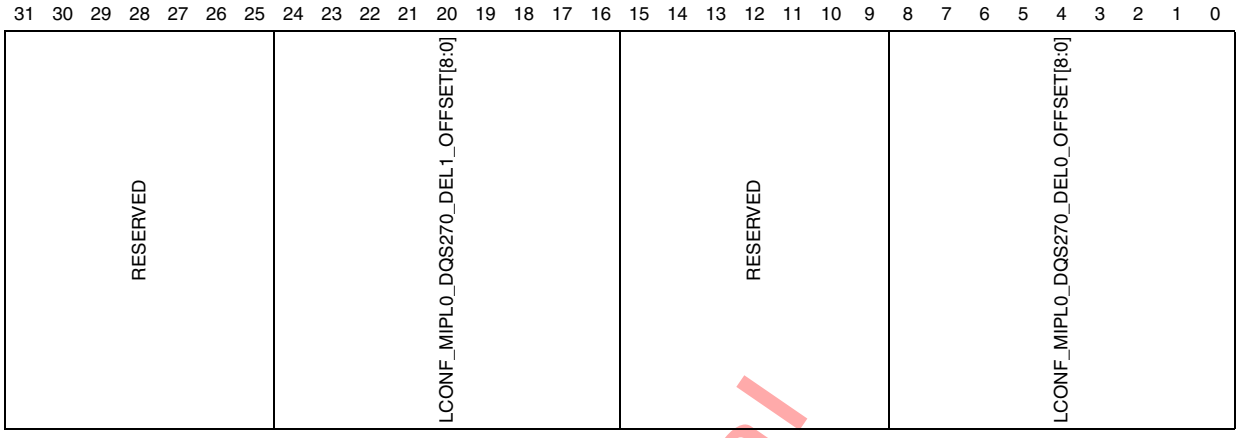
Note: Alternate 1 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 00 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 2 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 01 [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Alternate 3 : PIO15_ALTFOPj_MUX_SEL_BUS(n) = 1x [(j = 0,1); (n = 0,1,2,3,4,5,6,7)]

Note: PIO10, PIO11 and PIO14 do not require any alternate function output muxing as they are dedicated.

SYSTEM_CONFIG51 LMI / LMI Padlogic configuration



Address: *SystemConfigBaseAddress* + 0x01CC

Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic configuration

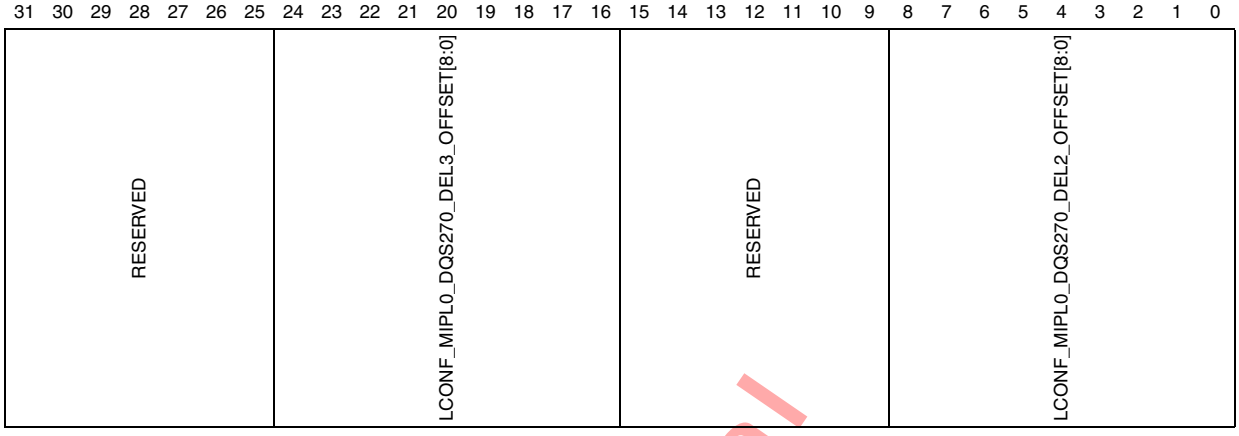
[31:25] RESERVED

[24:16] **LCONF_MIPL0_DQS270_DEL1_OFFSET[8:0]**: Offset command for ‘dqs270_del1’ PDL.

[15:9] RESERVED

[8:0] **LCONF_MIPL0_DQS270_DEL0_OFFSET[8:0]**: Offset command for ‘dqs270_del0’ PDL.

SYSTEM_CONFIG52 LMI / LMI Padlogic configuration



Address: *SystemConfigBaseAddress* + 0x01D0

Type: RW

Reset: 0x0000

Description: LMI / LMI Padlogic configuration

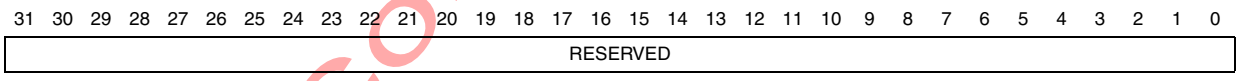
[31:25] RESERVED

[24:16] **LCONF_MIPL0_DQS270_DEL3_OFFSET[8:0]**: Offset command for ‘dqs270_del1’ PDL.

[15:9] RESERVED

[8:0] **LCONF_MIPL0_DQS270_DEL2_OFFSET[8:0]**: Offset command for ‘dqs270_del0’ PDL.

SYSTEM_CONFIG53 Reserved



Address: *SystemConfigBaseAddress* + 0x01D4

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] RESERVED

SYSTEM_CONFIG54 Reserved

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x01D8

Type: RW

Reset: 0x00000000

Description: Reserved

[31:0] RESERVED

SYSTEM_CONFIG55 LMI / LMI Padlogic configuration

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		LMIPL_USERMODE_PDL_DQS_VALID	LMIPL_USERMODE_PDL_DQS270_DEL	LMIPL_USERMODE_PDL_DQS	LMIPL_USER_COMMAND_DQS_VALID									RESERVED				LMIPL_RETIME_PLI_LMI	LMIPL_PHASE_SHIFT[1:0]		LMIPL_LOWER_16BIT_ONLY	LMIPL_FILTER_SHIFT_PARAM[2:0]			LMIPL_DUMMY_PCB_TRACE	LMIPL_DOUBLE_WIDTH	LMIPL_DDR2_DIAG_CONTROL[4:0]				

Address: *SystemConfigBaseAddress* + 0x01DC

Type: RW

Reset: 0x00002000

Description: LMI / LMI Padlogic configuration

[31:30] RESERVED

[29] **LMIPL_USERMODE_PDL_DQS_VALID**:
0: T/4 DLL1 command routed to dqs_valid PDL
1: user_command_dqs_valid<8:0> routed to dqs_valid PDL

[28] **LMIPL_USERMODE_PDL_DQS270_DEL**:
0: 3T/4 (or T/2) DLL2 command routed to dqs270_del<3:0> PDLs
1: dll2_usr_cmd<8:0> routed to dqs270_del<3:0> PDLs

[27] **LMIPL_USERMODE_PDL_DQS**:
0: T/4 DLL command routed to dqs<3:0> PDLs
1: dll1_usr_cmd<8:0> routed to dqs<3:0> PDLs

[26:18] **LMIPL_USER_COMMAND_DQS_VALID**: User command for forcing delay of dqs_valid PDL(also diagnostics).

[17:14] RESERVED

[13] **LMIPL_RETIME_PLI_LMI**: Active high retiming stage enable for lmisys_pl.

[12:11] **LMIPL_PHASE_SHIFT[1:0]**: Shift padlogic clock in T/4 increments; needs clk_pll stopped when rst_n released.

[10] **LMIPL_LOWER_16BIT_ONLY**: 16/32-bit mode switch; High = 16-bit mode.

[9:7] **LMIPL_FILTER_SHIFT_PARAM[2:0]**: Programmable filter characteristic.

[6] **LMIPL_DUMMY_PCB_TRACE**: Active high to enable dummy PCB trace option.

[5] **LMIPL_DOUBLE_WIDTH**: Enable half speed LMI-PLI interface.

[4:0] **LMIPL_DDR2_DIAG_CONTROL[4:0]**: For future development. Tied off.

17.1.5 INTC2 registers description

INTC2_PRIORITY00 — INTC2 priority 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0300

Type: RW

Reset: 0

Description: INTC2 priority 00

[31:0] RESERVED

INTC2_PRIORITY04 — INTC2 priority 04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0304

Type: RW

Reset: 0

Description: INTC2 priority 04

[31:0] RESERVED

INTC2_PRIORITY08 INTC2 priority 08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0308

Type: RW

Reset: 0

Description: INTC2 priority 08

[31:0] RESERVED

INTC2_REQUEST00 INTC2 request 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0320

Type: RW

Reset: 0

Description: INTC2 request 00

[31:0] RESERVED

INTC2_REQUEST04 INTC2 request 04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0324

Type: RW

Reset: 0

Description: INTC2 request 04

[31:0] RESERVED

INTC2_REQUEST08 INTC2 request 08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0328

Type: RW

Reset: 0

Description: INTC2 request 08

[31:0] RESERVED

INTC2_MASK00 INTC2 mask 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0340

Type: RW

Reset: 0

Description: INTC2 mask 00

[31:0] RESERVED

INTC2_MASK04 INTC2 mask 04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0344

Type: RW

Reset: 0

Description: INTC2 mask 04

[31:0] RESERVED

NTC2_MASK08 INTC2 mask 08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0348

Type: RW

Reset: 0

Description: INTC2 mask 08

[31:0] RESERVED

INTC2_MASK_CLEAR00 INTC2 mask clear 00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0360

Type: RW

Reset: 0

Description: INTC2 mask clear 00

[31:0] RESERVED

INTC2_MASK_CLEAR04 INTC2 mask clear 04

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0364

Type: RW

Reset: 0

Description: INTC2 mask clear 04

[31:0] RESERVED

INTC2_MASK_CLEAR08 INTC2 mask clear 08

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0368

Type: RW

Reset: 0

Description: INTC2 mask clear 08

[31:0] RESERVED

INTC2_MODE INTC2 mode

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED																															

Address: *SystemConfigBaseAddress* + 0x0380

Type: RW

Reset: 0

Description: INTC2 mode

[31:0] RESERVED

18 External circuitry recommendations

18.1 Power supplies

18.1.1 Decoupling recommendations

It is recommended to:

- connect all balls of the same group (with the same names) together
- add decoupling capacitors between each VDD and GND group, respectively:
  - VDD3V3 group and GND3V3 group
  - AVDD2V5 group and AGND2V5 group
  - VDD1V8_2V5 group and LMI_GND1V8 group
  - DVDD1V2 group and DGND1V2 group

The decoupling capacitor values must be carefully considered and fully simulated prior to the board design cycle.

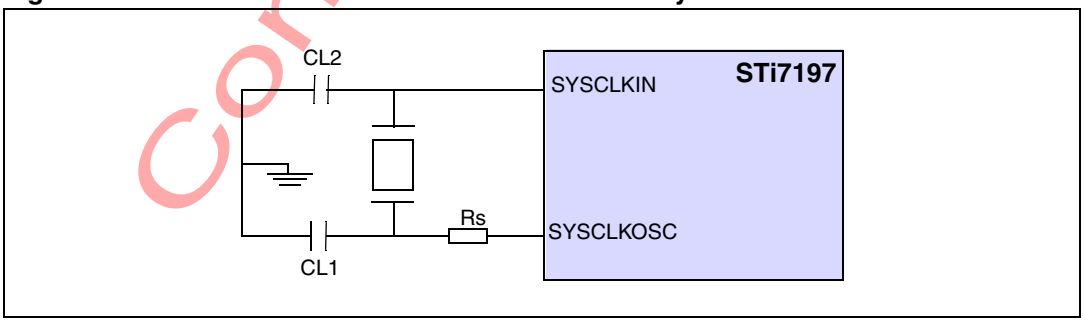
18.1.2 Power-up recommendations

There is no specific recommendation for power-up sequence.

18.2 System

The SYS oscillator recommended external circuitry is shown in *Figure 33*.

Figure 33. Oscillator recommended external circuitry



For the electrical specifications, please contact your local ST representative to access SATA application notes describing oscillators' electrical specifications.

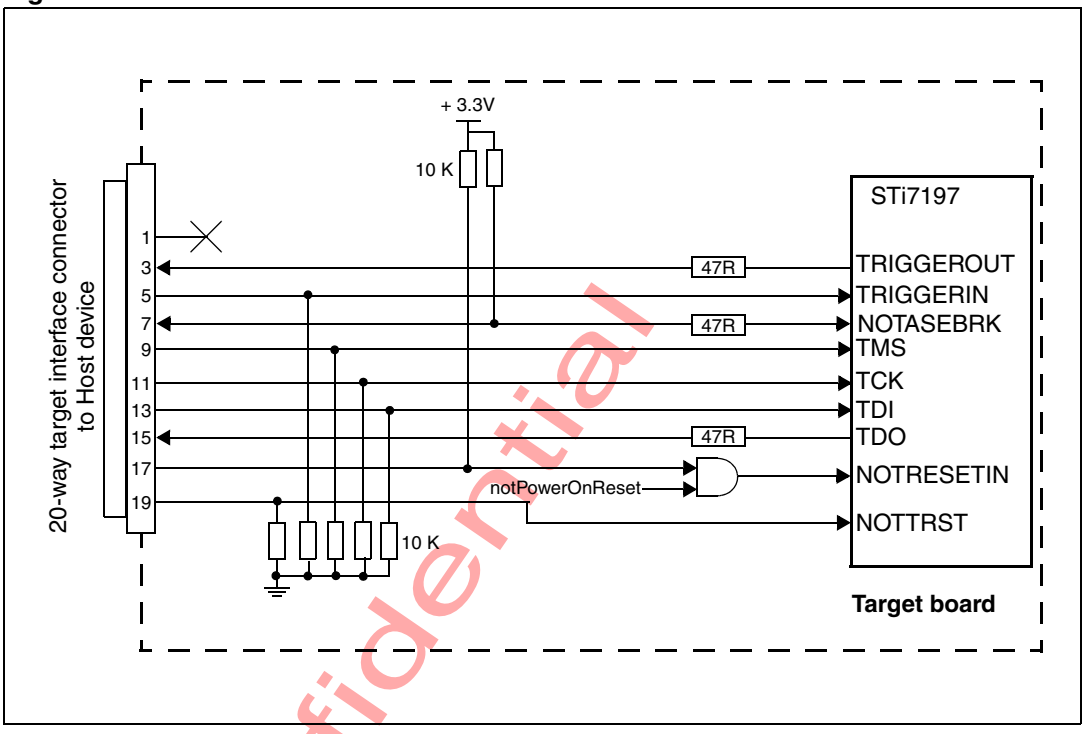
Two differential signals (VDDSENSE and GNDSENSE) are used to provide loopback information on the core supply voltage to an external voltage regulator.

Most of the signals have internal pull-up or pull-down, and do not require an external resistor when not in use. Refer to the 'I/O value' field of *Table 36* for details.

18.3 JTAG

The JTAG recommended connections are shown in *Figure 34.*

Figure 34. Recommended connections



Note: If there is a lot of noise on the clock line, a capacitor in the range 10 to 100 pF can be fitted between TCK and ground near the target STi7197. However, this may limit the maximum TAP clock rate.

18.4 Display analog output interface

18.4.1 Video DACs description

There are two identical sets of triple video DACs for HD and SD output. Both are triple high performance 10-bit digital-to-analog converters, and consist of three 10-bit DAC modules joined together. A reference circuit controlled by one external resistor sets the full-scale output for each DAC set. Each DAC is able to drive 10 mA.

The blocks are powered by 2.5 V analog and 1.2 V digital supplies, with separate analog and digital grounds.

The blocks require an external precision resistor (Rref) to provide a bandgap reference. The Rref optimum value is 7.81 kΩ ±1%.

The blocks' analog current sources provide a voltage output range of 1.4 V with an optimum linearity through an external precision resistor (Rload). The Rload optimum value is 140 Ω ±1%.

The calculation for the voltage output range is:

Vout = Din * 0.0625 * [(Rext-Mass_quiet)/Rref]*Rload

where:

- Din is the Code value in decimal
- Rext-Mass_quiet is VbandGap(=1.2214 V)
- Rref is the reference resistor; optimum value is 7.81 kΩ
- Rload is the load resistor (=140 Ω)

18.4.2 Power mode

Each DAC has two power modes—normal mode and high-impedance mode—that are controlled by the *SYSTEM_CONFIG3* system configuration register.

The high impedance mode allows fast recovery from the low power consumption state, and can be used to reduce power during line and frame refresh.

Each DAC takes 100 ns time interval to switch from normal mode to high-impedance mode, and *vice-versa*.

18.4.3 Video DACs output-stage adaptation and amplification

Please contact your local ST representative to access application notes describing video DACs output stage adaptation and amplification.

18.5 HDMI interface

Please contact your local ST representative to access application notes describing HDMI PCB design guidelines.

18.6 Audio digital interface

Please contact your local ST representative to access application notes describing audio digital interface.

18.7 Audio analog interface

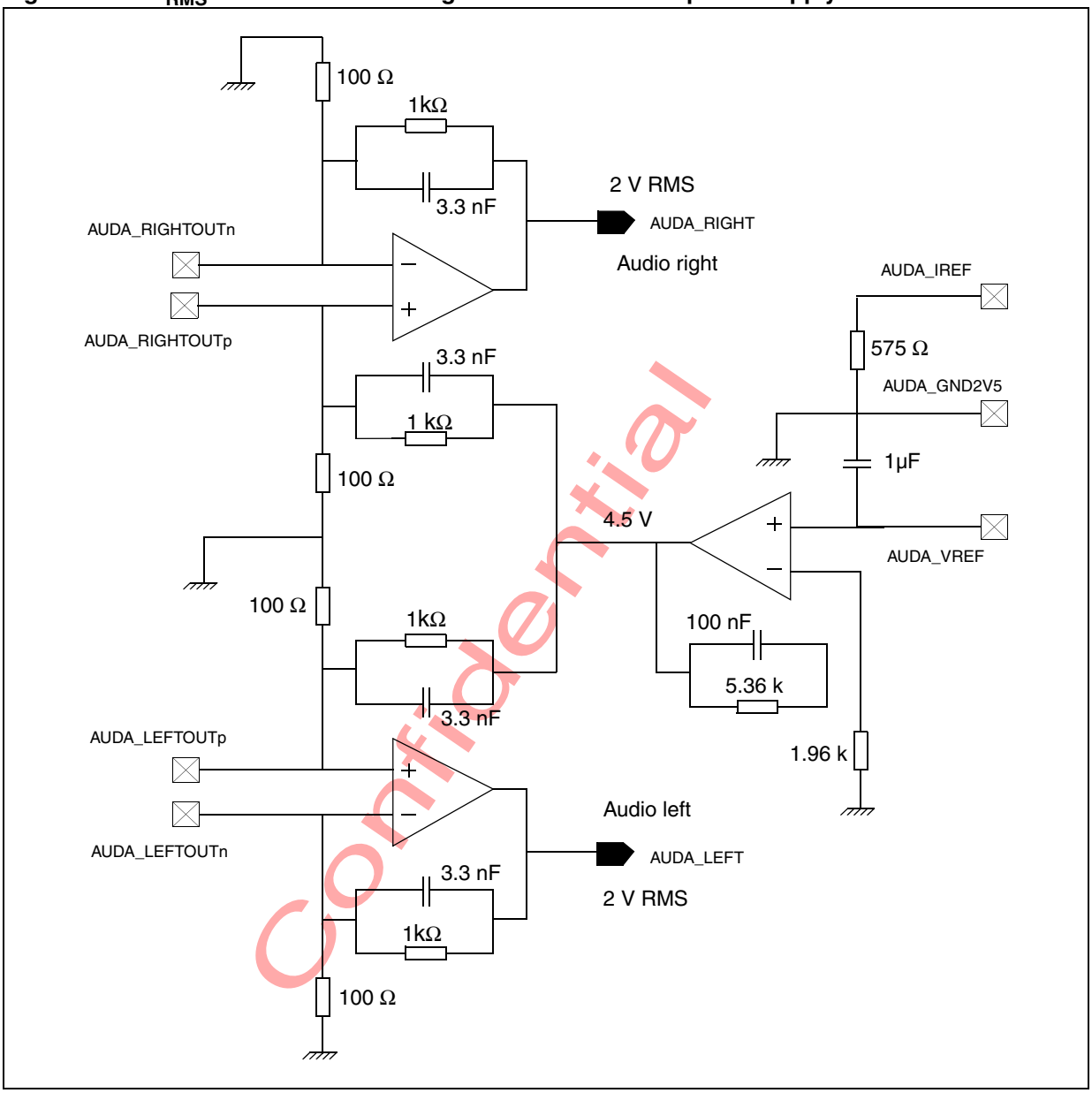
The audio DAC provides differential current source outputs for each channel. The use of a differential mode interface circuit is recommended to achieve the best signal to noise ratio performance. A single-ended mode interface circuit can be used, by grounding pins AUDA_LEFTOUTN and AUDA_RIGHTOUTN, but this is not recommended as the resulting signal to noise ratio is less than 90 dB.

An external 1% resistor R_{REF} should be connected between AUDA_IREF and AUDA_GND2V5. A typical value for R_{REF} is 575 Ω, to get proper band gap functionality.

An external 10 µF capacitance should be connected between AUDA_VREF and AUDA_GND2V5.

Figure 35 describes an audio output stage to deliver a 2 V RMS signal.

Figure 35. $2V_{RMS}$ external audio analog schematic with +9V power supply



18.8 Programmable inputs/outputs

There is no specific external circuitry recommendations for this interface.

18.9 External memory interface (EMI)

The EMI is designed to be connected to up to:

- 1 PCI/33 MHz slot + 4 TTL/100 MHz/40 pF slots
- 1 PCI/66 MHz slot + 3 TTL/100 MHz/30 pF slots

Please contact your local ST representative to access application notes describing PCI interface implementation.

18.10 Local memory interface

Apart from the direct signal connections between the LMI and the DDR memories (refer to *Figure 36* and *Figure 37* for details), several extra connections are required.

An external resistor of 121 kΩ +/- 1% is to be connected between LMI_COMP_REF AND LMI_COMP_GND to enable the internal pad drive compensation mechanism.

The two voltage reference signals LMIVREF[0]/LMIVREF[1] are to be connected together to the memories' VREF signals and to a resistor pair whose pedestal is connected to VDD1V8_2V5 and LMI_GND1V8.

The LMIDUMMY[0]/LMIDUMMY[1] signals act as a PCB track delay estimator, and have to be connected through a dummy PCB trace. If all signal lengths are equal to an ideal TL_{signal}, TL_{dummy} is also equal to this TL_{signal}. If this is not the case, the ideal TL_{dummy} length is defined by the following equation:

$$TL_{dummy} = 0.5 \times \{(TL_{LMICLK[0]} + TL_{NOTLMICLK[0]} + TL_{LMICLK[1]} + TL_{NOTLMICLK[1]}) / 4 + (TL_{LMIDQS[0]} + TL_{LMIDQSN[0]} + TL_{LMIDQS[1]} + TL_{LMIDQSN[1]} + TL_{LMIDQS[2]} + TL_{LMIDQSN[2]} + TL_{LMIDQS[3]} + TL_{LMIDQSN[3]}) / 8\}$$

For further information on LMI PCB design guidelines, please contact your local ST representative.

Figure 36. LMI: connections to a (single rank/2 x16 devices) DDR 32-bit configuration

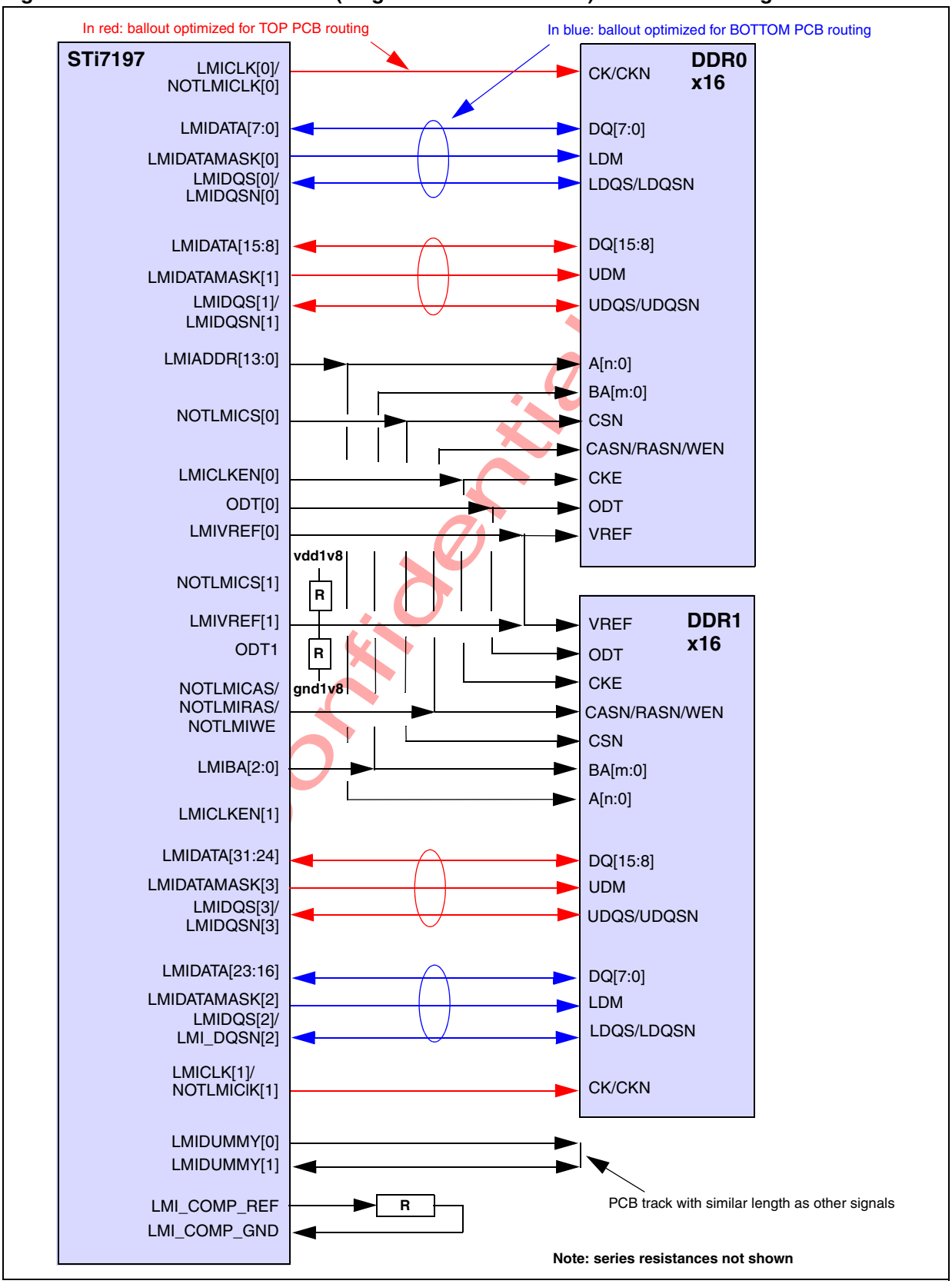
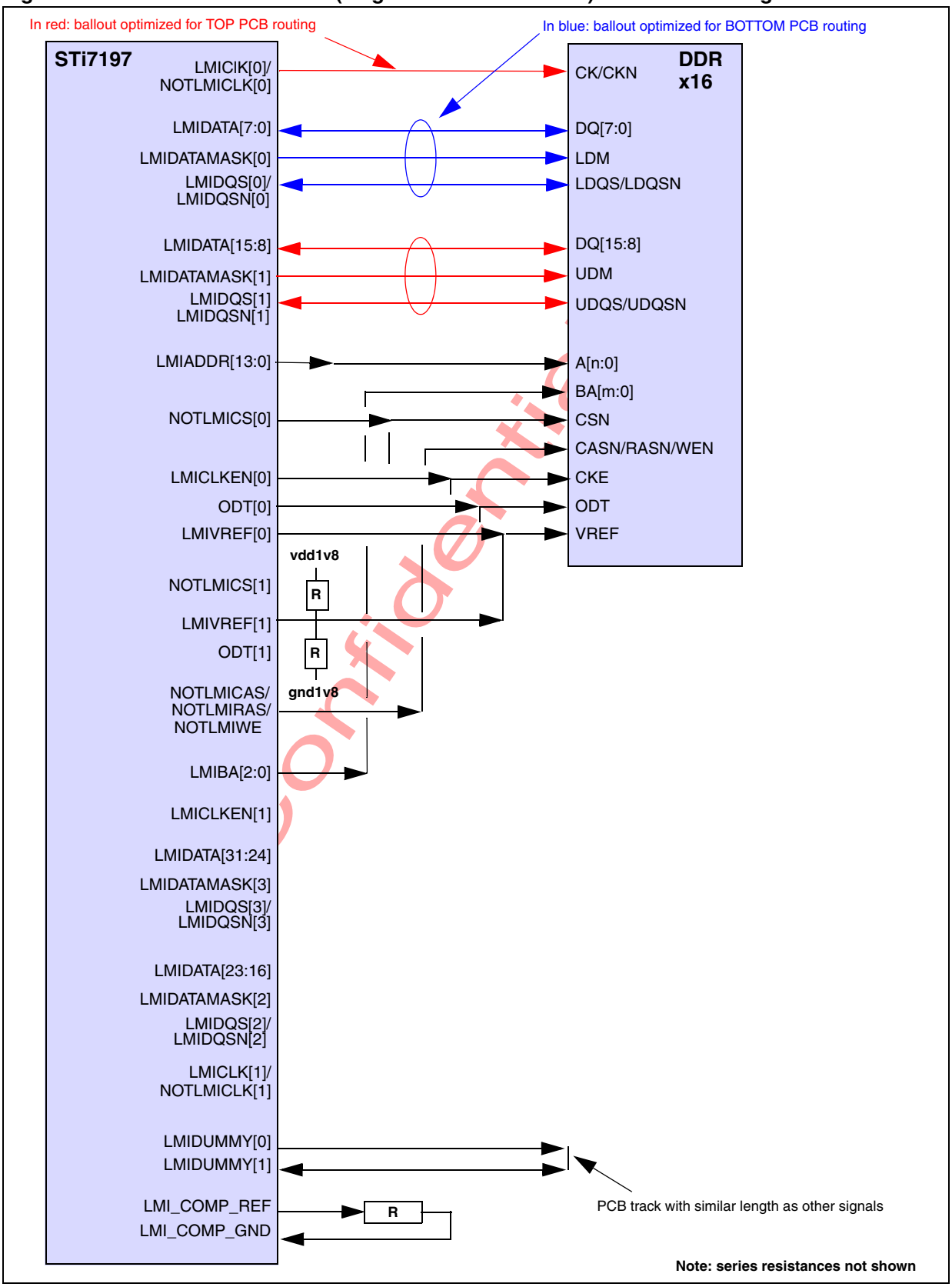


Figure 37. LMI: connections to a (single rank/1 x16 devices) DDR 16-bit configuration



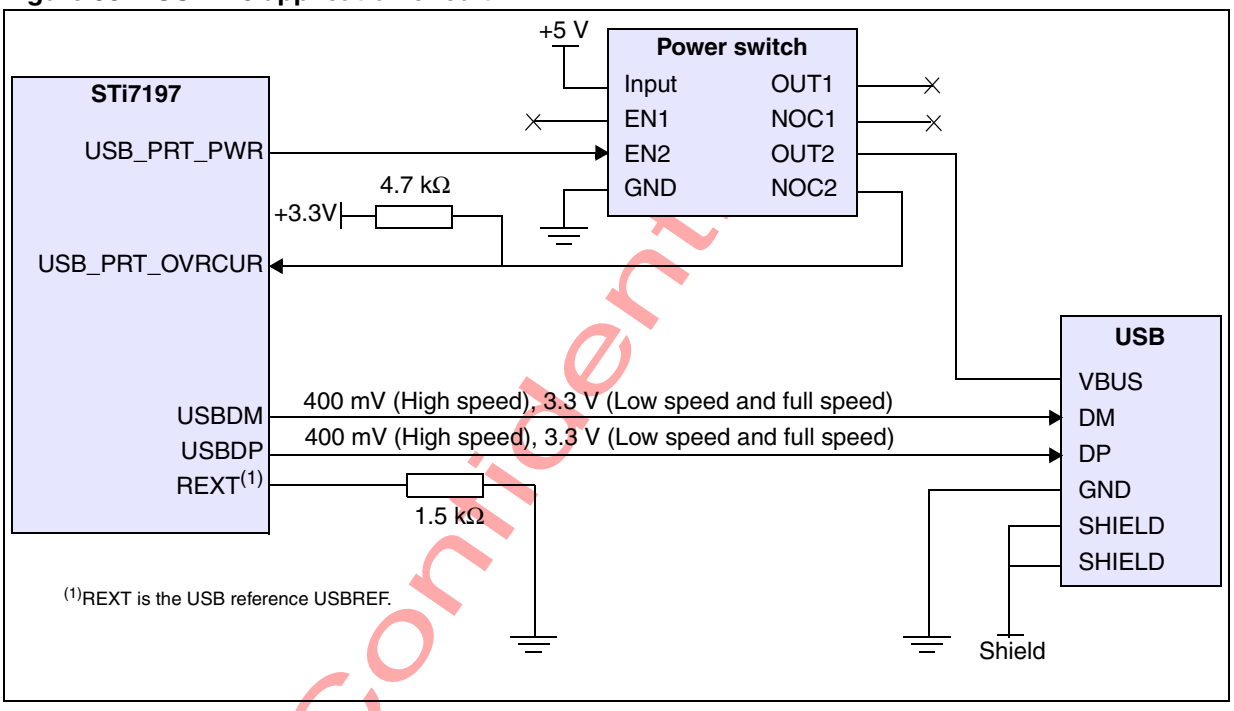
18.11 Ethernet interface

Some mode pins are mapped on some Ethernet interface signals. Pull-up or pull-down resistors have to be added depending upon the chosen reset configuration. Refer to *Mode pins* for details.

18.12 USB interface

The USB external recommended connections are shown in *Figure 38.*

Figure 38. USB 2.0 application circuit



For PCB design guidelines, refer to the 'USB PCB design guidelines' specific document (7991152). For access to this ST internal document please contact your local ST representative.

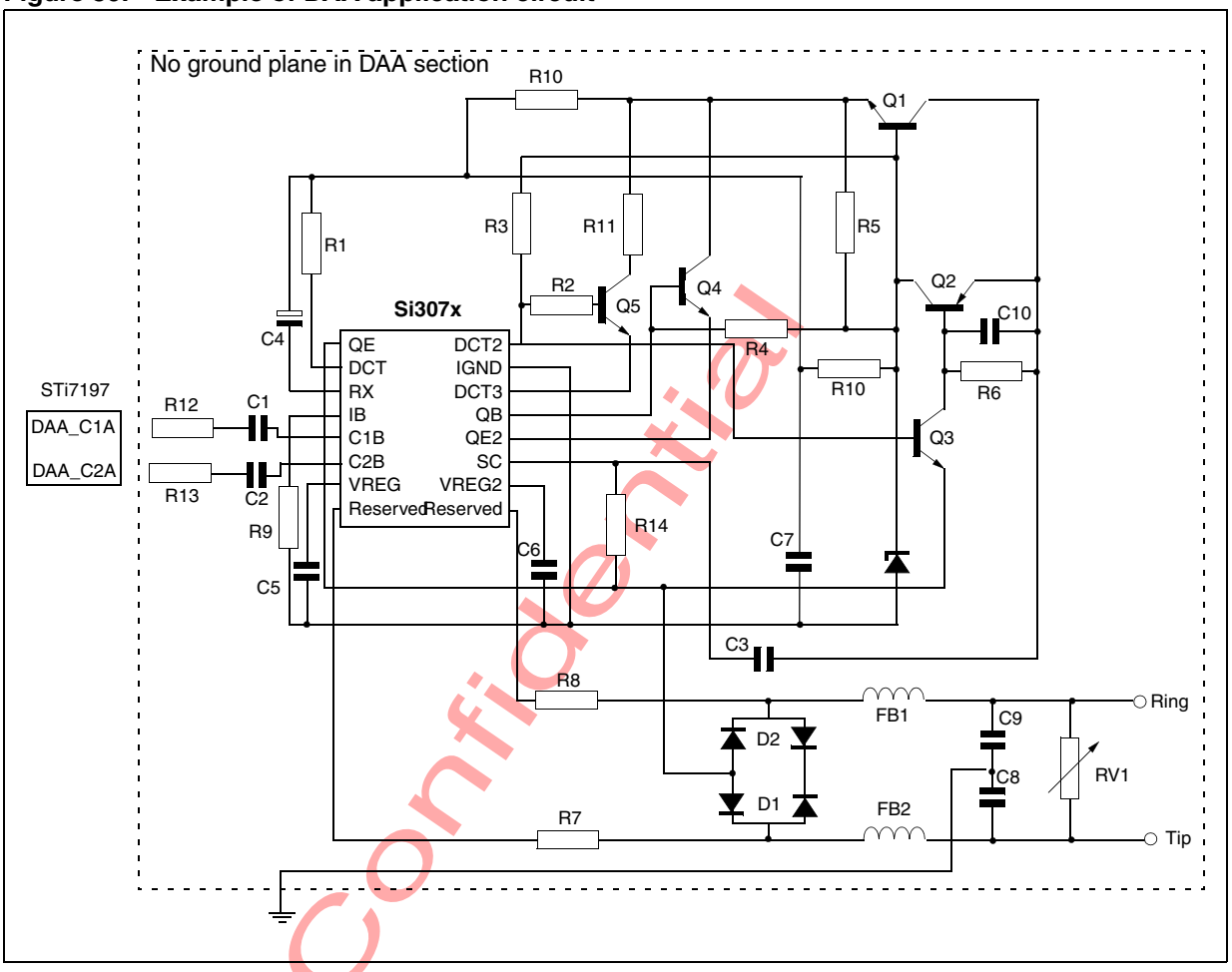
18.13 SATA

Please contact your local ST representative to access application notes describing SATA PCB design guidelines.

18.14 Peripherals

The DAA external recommended connections are shown in *Figure 39.*

Figure 39. Example of DAA application circuit



Note: The ISO-Link capacitors C1 and C2, (33 pF) should be as close to the line-side device as possible.They should also be as close to the embedded system-side DAA module as possible and no further than 6 inches away.

19 Electrical specifications

19.1 Absolute maximum ratings

Table 73. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Units
$VDD3V3_{max}$	Digital 3.3 V maximum voltage	-0.5	-	4.0	V
$VDD2V5_{max}$	Analog 2.5 V maximum voltage	-0.5	-	4.5	V
$VDD1V8\_2V5_{max}$	Digital 1.8 V maximum voltage	-0.5	-	2.5	V
$VDD1V2_{max}$	Digital 1.2 V maximum voltage	-0.5	-	1.9	V
V_{ESD_HBM}	Electrostatic discharge voltage (HBM)(1) JESD22-A114 - Class 1C	-	-	-	-
V_{ESD_RCDM}	Electrostatic discharge voltage (RCDM)(1) JESD22-C101- Class II	-	-	-	-
T_{STG}	Storage temperature	- 40	-	150	°C

1. For a definition of the ESD classes, see the relevant JEDEC standards, or contact STMicroelectronics customer support.

Note: 1 These are maximum limits. Exceeding them may result in permanent damage to the device. Operation at these limits is not intended.

2 These AMR values are applicable to all pins powered to the given voltage.

19.2 Operating conditions

Table 74. Normal operating conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD3V3	Digital 3.3 V operating voltage	3.00	3.30	3.60	V
VDD2V5	Analog 2.5 V operating voltage	2.25	2.50	2.75	V
VDD1V8	Digital 1.8 V operating voltage	1.70	1.80	1.90	V
VDD1V2	Digital 1.2 V operating voltage	1.17	1.20	1.26	V
I_{3V3}	Digital 3.3 V current	-	0.03(1)	0.04(2)	A
I_{2V5}	Analog 2.5 V current	-	0.15(1)	0.16(2)	A
I_{1V8}	Digital 1.8 V current	-	0.38(1)	0.40(2)	A
I_{1V2}	Digital 1.2 core current	-	1.15(1)	1.49(2)	A
C_L	Load capacitance per pin	-	-	100	pF
TA	Operating ambient temperature	0	-	70	°C
T_{j_max}	Maximum junction temperature	-	-	125(3)	°C

Table 74. Normal operating conditions

Symbol	Parameter	Min	Typ	Max	Units
PD	Power dissipation	-	2.54(1)	3.22(2)	W
R_{thJA}(4)	Junction-to-ambient thermal resistance (mounted on recommended PCB)	-	16.8	-	°C/W

1. Typical values correspond to normal process/voltage/temperature.
2. Maximal values correspond to worse-case process/voltage/temperature.
3. Maximal value corresponds to the estimated Tjunction with worse- case process/voltage/temperature.
4. The RthJA has been measured using an FR4 board without heatsink. The value must be considered only as an indication. The thermal performance of the electronic package can vary significantly depending on board design, size, thickness, material and other physical factors.

Note: The power consumption is dependant for the chip activation (chip activity and chip temperature) and silicon temperature which is PCB dependant. The values given in this table are measured on ST application environment and may vary from one application to another.

19.3 Audio DAC

19.3.1 Electrical characteristics

Absolute maximum ratings

The *Table 75* describes absolute maximum ratings for audio DAC.

Table 75. Absolute maximum ratings

Symbol	Parameter	Min	Typ	Max	Units
ANA1_VDD2V5	Analog power supply	-	-	4	V

Operating conditions

The *Table 76* describes operating conditions for audio DAC.

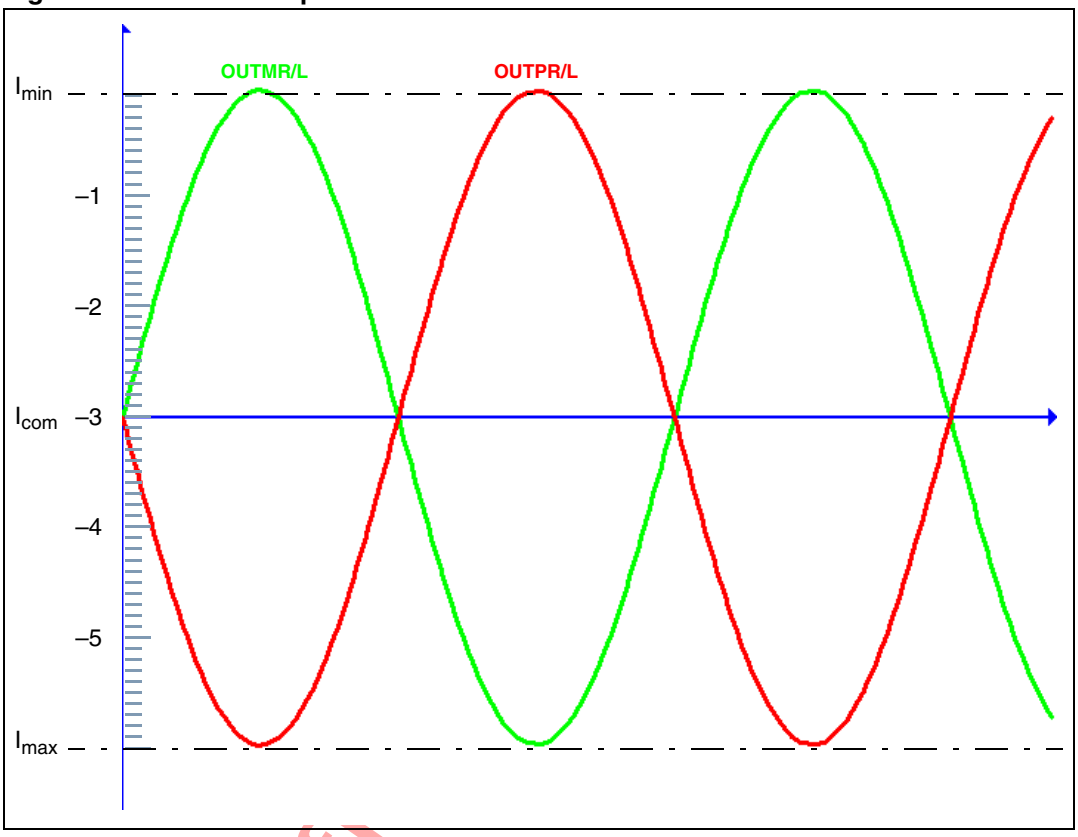
Table 76. Operating conditions

Symbol	Parameter	Min	Typ	Max	Units
ANA1_VDD2V5	Analog power supply	2.25	2.5	2.75	V
I_{PD}	Supply Current in Power Down Mode	-	-	10	µA

Output current

In case of no input data, the DAC provides a common mode output current (Icom), as shown in *Figure 40*.

Figure 40. Current output



The output current is fixed by internal reference current or can be fixed externally.

Table 77. Audio DAC output current

Parameter	Imin	Icom	Imax	Unit
Output current	0	$-\frac{0.8}{Rext}$	$-\frac{1.613}{Rext}$	A

19.4 Triple HD video DACs

The *Table 78* describes absolute maximum ratings for triple video DACs.

Table 78. Absolute maximum rating

Symbol	Parameter	Min	Typ	Max	Unit
VIDA1_VCCA1/ VIDA2_VCCA1	Analog power supply for current matrix & bias blocks 2.75 V	-	-	2.75	V
VIDA1_VCCA2/ VIDA2_VCCA2	Analog power supply for level shifters	-	-	2.75	V

The *Table 79* describes operating conditions for triple video DACs.

Table 79. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VIDA1_VCCA1/ VIDA2_VCCA1	Analog power supply for current matrix & bias blocks 2.75 V	2.25	2.5	2.75	V
VIDA1_VCCA2/ VIDA2_VCCA2	Analog power supply for level shifters	2.25	2.5	2.75	V

The *Table 80* describes static electrical performance of TriDAC.

Table 80. Static electrical performance Rref = 7.81 kΩ; Rload = 140 Ω

Symbol	Parameter	Min	Typ	Max	Unit
Nb	DAC resolution	-	10	-	bits
PonAnalog	Power consumption analog/ active(1)	-	110	133	mW
PonDigital	Power consumption digital/ active(2)	-	3.0	3.9	mW
PHZ	Power consumption / HZ mode(3)	-	12.7	15.6	mW
POFF	Power consumption / Off mode(4)	-	2.5	102.0	µW
INL	Integral non linearity	-	± 0.4	± 1.0	LSB
DNL	Differential non linearity	-	± 0.2	± 0.5	LSB
DAC to DAC matching	DAC to DAC matching(5)	-	± 0.5	± 3	
Compliance	Output compliance 0 V < Vout < 1.4 V	-	-	0.03	LSB
Iout Rref = 7.81 kΩ	DAC output current	0 (code min)	-	10.0 (code max)	mA
Full scale Gain Error	Full scale gain error (6)	-	-	±7	%
Rout	DAC output resistance @ DC	100	-	-	kΩ

1. Typical consumption at 2.5 V/1.2 V supply; and Max. at 2.75 V/1.32 V supply
2. Typical consumption at 2.5 V/1.2 V supply; and Max. at 2.75 V/1.32 V supply
3. Independent of clock activity
4. Transistor off-stage leakage only
5. Under ideal supply conditions
6. This value includes the 1% variation of reference resistor (Rref) and 1% of load resistor (Rload)

The *Table 81* describes dynamic electrical performance of video DACs.

Table 81. Dynamic electrical performance Rref = 7.81 kΩ; Rload = 140 Ω

Symbol	Parameter	Min	Typ	Max	Unit
F_CLK	Clock speed	-	-	160	MHz
BDW	Output 3 dB bandwidth @ Fclk=160 MHz	DC to 30	-	-	MHz
THD	Total harmonic distortion Fin =4 MHz, F_clk =160 MHz	-44.27	-46.47	-	dB
SFDR	Spurious free dynamic range Fin=4 MHz, Fclk=160 MHz Output full scale	-44.88	-47.79	-	dB
PSRR (dVout/dVvcca)	Power supply rejection ratio @ 1 Hz (full scale)	-50	-55	-	dB
	Power supply rejection ratio @1 MHz(full scale)	-22	-25	-	dB

19.5 DAA electrical characteristics

The *Table 82* describes absolute maximum ratings for DAA.

Table 82. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max	Units
V_1	Input voltage on IO pin with respect to GND		–	3.6	V

19.6 DDR electrical characteristics

19.6.1 Limiting values

The *Table 83* describes the limiting values for DDR.

Table 83. DDR limiting values

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDE	1.8 V pad supply voltage	DDR II mode	1.7	1.8	1.9	V
		DDR I mode	2.25	2.5	2.75	V
VREF(DC)	Input reference voltage connected on REFSSTL (corresponding to supply VDDE)	(1)	(0.49 * VDDE)	(0.5 * VDDE)	(0.51 * VDDE)	V
VTT	Termination voltage	(2)	VREF - 0.04	VREF	VREF +0.04	V

1. The value of VREF is expected to be (0.49-0.51) x VDDE of the transmitting device and VREF is expected to track variations in VDDE.
2. Peak to peak AC noise on VREF may not exceed ± 2% of VREF(DC). VTT of transmitting device must track VREF of receiving device.

19.6.2 Output buffer DC characteristics

Table 84. Output buffer DC characteristics

Symbol	Mode of I/O buffer	Parameter	Conditions	Min	Typ	Max	Unit
Iol	DDRI	Output minimum DC current sink	Vol = 0.36V(1)	16.2	-	-	mA
Ioh		Output minimum DC current source	Voh = VDDE - 0.36V	-16.2	-	-	mA
Iol	DDRII	Output minimum DC current sink	Vol = 0.28V	13.4	-	-	mA
Ioh		Output minimum DC current source	Voh = VDDE - 0.28V(2)	-13.4	-	-	mA

1. SSTL2 classII specification with ZOUTPROGA set low.
2. SSTL_18 specification with ZOUTPROGA set low.

19.6.3 Input buffer DC specifications

Table 85. Input buffer DC characteristics for DDRI

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Voltage reference	-	0.49 * VDDE = 1.1	0.5 * VDDE = 1.25	0.51 * VDDE = 1.4	V
Vil (DC)	DC input logic low	-	-0.3	-	VREF - 0.15	V
Vih (DC)	DC input logic high	-	VREF + 0.15	-	VDDE + 0.3	V
Vil (AC)	AC input logic low	-	-	-	VREF - 0.31	V
Vih(AC)	AC input logic high	-	VREF + 0.31	-	-	V

Table 86. Input buffer DC characteristics for DDRII

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREF	Voltage reference	-	0.49 * VDDE = 0.833	0.5 * VDDE = 0.9	0.51 * VDDE = 0.969	V
Vil (DC)	DC input logic low	-	-0.3	-	VREF - 0.125	V
Vih (DC)	DC input logic high	-	VREF + 0.125	-	VDDE + 0.3	V
VTT (DC)	Termination voltage		VREF - 0.04	-	VREF + 0.04	V
Vil (AC)	AC input logic low	-	-	-	VREF - 0.25	V
Vih(AC)	AC input logic high	-	VREF + 0.25	-	-	V

19.7 SATA PHY electrical characteristics

19.7.1 Absolute maximum ratings

Table 87 describes the absolute maximum ratings.

Table 87. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
SATAVDDR	Supply Voltage (1.2 V nom.)	-	1.35	V
SATAVDDT				
SATAVDD_PLL				
SATAVDD2_PLL	Supply Voltage (2.5 V)	-	2.75	V
V_{INH1}	Input high level (oscillator and PLL 2v5 inputs)	-	2.75	V
V_{INH2}	Input high level (all other inputs)	-	1.35	V

19.7.2 Operating conditions

Table 88 describes the operating conditions.

Table 88. Operating conditions

Symbol	Parameter	Min	Typ	Max	Units
SATAVDDR	1v2 supply voltage range	1.08	1.20	1.32	V
SATAVDDT					
SATAVDD_PLL					
SATAVDD2_PLL	Supply Voltage (2.5 V)	2.25	2.50	2.75	V
	Supply ripple (1MHz to 3GHz)	-	-	50	mV(pk-pk)

19.7.3 General electrical specifications

Table 89 describes the general electrical specifications.

Table 89. General electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit
Rref	External reference resistor (from refers pin to the VDD_PLL pin)	-1%	475	+1%	Ohm
$TUI_{SATASAS1}$	Unit Interval for SATA/SAS gen1 (1.5 Gbps)	-	666.67	-	ps
F_{SSC}	Spread spectrum modulation frequency	30	-	33	kHz
SSC_{TOL}	Spread spectrum modulation deviation	-5000	-	+0	ppm
Z_{diff}	Nominal differential impedance	-	100	-	

19.8 External memory interface (EMI)

The EMI pads are TTL/PCI dual-mode. TTL electrical specifications are shown in *Table 90* and PCI electrical specifications in *Table 91*.

Table 90. TTL-mode 3V3 EMI pads DC specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{IH}	Input logic 1 voltage	2.0	-	VDD3V3 + 0.5	V	
V_{IL}	Input logic 0 voltage	-0.5	-	0.8	V	
V_{OH}	Output logic 1 voltage	VDD3V3 - 0.2	-	-	V	(1)
V_{OL}	Output logic 0 voltage	-	-	0.2	V	(2)
R_{PU}	Equivalent pull-up resistance	-	50	-	kΩ	
R_{PD}	Equivalent pull-down resistance	-	50	-	kΩ	
I_{IN}	Input leakage current (input pin)	-	-	4	µA	(3)
C_{IN}	Input capacitance	-	-	10	pF	

1. I_{OUT} = -8 mA
2. I_{OUT} = 8 mA
3. 0 ≤V_{in} ≤VDD3V3

Table 91. PCI-mode 3V3 EMI pads DC specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{IH}	Input logic 1 voltage	0.5*VDD3V3	-	VDD3V3 + 0.5	V	
V_{IL}	Input logic 0 voltage	-0.5	-	0.3*VDD3V3	V	
V_{OH}	Output logic 1 voltage	0.9*VDD3V3	-		V	(1)
V_{OL}	Output logic 0 voltage	-	-	0.1*VDD3V3	V	(2)
R_{PU}	Equivalent pull-up resistance	-	50	-	kΩ	
R_{PD}	Equivalent pull-down resistance	-	50	-	kΩ	
I_{IN}	Input leakage current (input pin)	-	-	4	µA	(3)
C_{IN}	Input capacitance	-	-	10	pF	

1. I_{OUT} = -0.5 mA
2. I_{OUT} = 1.5 mA
3. 0 ≤V_{in} ≤VDD3V3

19.9 USB

Table 92 describes the operating conditions of USB.

Table 92. USB operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
USB1_VDD3V3	Analog supply voltage	3.0	3.3	3.6	V
USB2_VDD3V3					
USB_VDD1V2	Digital supply voltage	1.1	1.2	1.3	V
USB_VDD2V5	Analog supply voltage	2.3	2.5	2.7	V
V_{LFS-cm}	Low and full speed mode input common mode level	800	-	2500	mV
V_{HS-cm}	High speed mode input common mode level	-50	200	500	mV
$V_{chirp-cm}$	Chirp mode input common mode level	-50	-	600	mV
V_{diff}	Differential input signal amplitude	100	400	1100	mV

19.10 3V3 IO pads

Table 93 describes the electrical specifications for the 3V3 IO pads.

Table 93. 3V3 electrical specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IH}	High level input voltage	2	-	-	V	
V_{IL}	Low level input voltage	-	-	0.8	V	
V_{HYST}	Input hysteresis voltage	300	-	-	mV	
V_{OH}	High level output voltage	VDDE3V3 - 0.3	-	-	V	(1)
V_{OL}	Low level output voltage	-	-	0.3	V	(2)
I_{PU}	Pull-up current (conditions Vi = 0 V)	39	66	101	µA	
I_{pd}	Pull-down current (conditions Vi=VDDE3V3)	33	66	120	µA	
R_{PU}	Equivalent pull-up resistance (conditions Vi = 0 V)	36	50	76	kΩ	
R_{PD}	Equivalent pull-down resistance (conditions Vi = VDDE3V3)	30	50	90	kΩ	

1. I_{OUT} = -6mA
2. I_{OUT} = 6mA

19.11 Crystal oscillator specifications

Table 94. Crystal oscillator specifications

Symbol	Parameter	Min	Typ	Max	Unit
$Xtal_I$	Amplitude at pin XTAL_I (ball AK8)	0.5		2.0	V_{pp}
$Xtal_O$	Amplitude at pin XTAL_O (ball AL8)	0.5		2.2	V_{pp}
	Oscillation start-up time			2	ms
G_{mO}	Oscillation transductance		28.5		mA/V
R_{neg}	Negative impedance		288		Ω
	Oscillator gain	10			dB

20 Timing interfaces

20.1 System timing interface

Figure 41. Reset timing

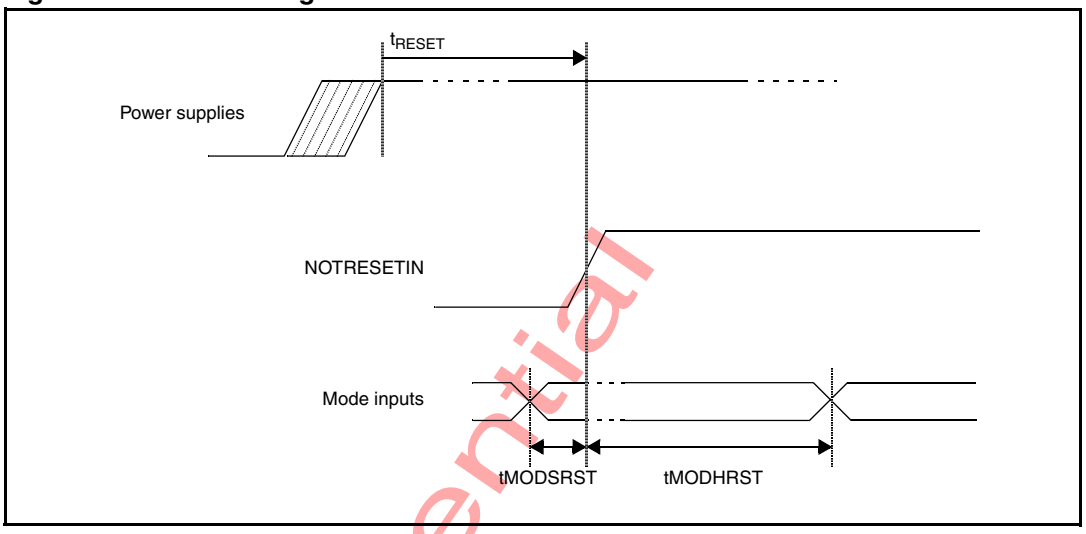


Table 95. System input/output port timing parameters

Symbol	Parameter	Min	Max	Units
t_{RESET}	Power supply stabilization to NOTRESETIN signal deassertion	1	-	ms
$t_{MODSRST}$	Inputs setup to NOTRESETIN	5	-	ns
$t_{MODHRST}$	Inputs hold from NOTRESETIN	1.2	-	ms

20.2 Digital audio interface

20.2.1 Digital PCM reader input interface

Digital PCM reader timing waveform

The *Figure 42* shows the timing waveforms of the digital Audio PCM input to the PCM reader.

Figure 42. Digital PCM audio input timing waveforms

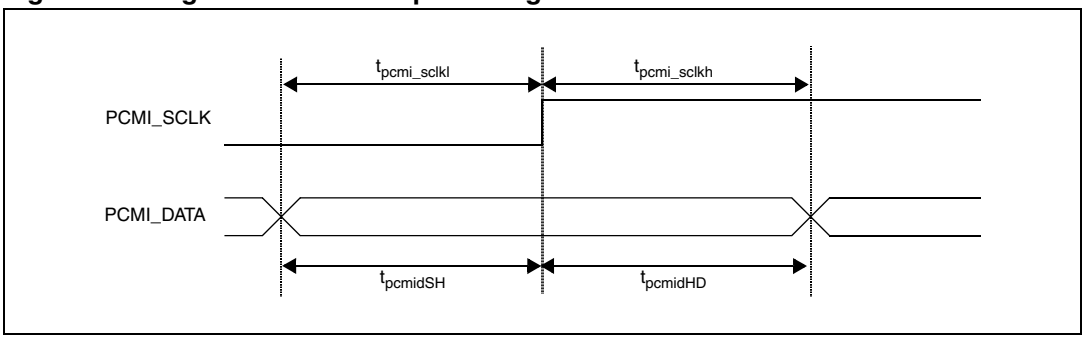


Table 96. Digital audio PCM input timing parameters

Symbol	Parameter	Min	Max	Units
f_{pcmi_sclk}	PCMI_SCLK max frequency	--	32	MHz
t_{pcmi_sclkl}	PCMI_SCLK low pulse	12	--	ns
t_{pcmi_sclkh}	PCMI_SCLK high pulse	12	--	ns
$t_{pcmidSH}$	PCMI_data setup time to PCMI_SCLK rising edge	5	--	ns
$t_{pcmidHD}$	PCMI_data hold time from PCMI_SCLK rising edge	5	--	ns

20.3 Digital PCM player output interface

20.3.1 PCM player output timing waveform

The *Figure 43* shows the timing waveforms of the PCM player output interface.

Figure 43. PCM player timing output waveforms

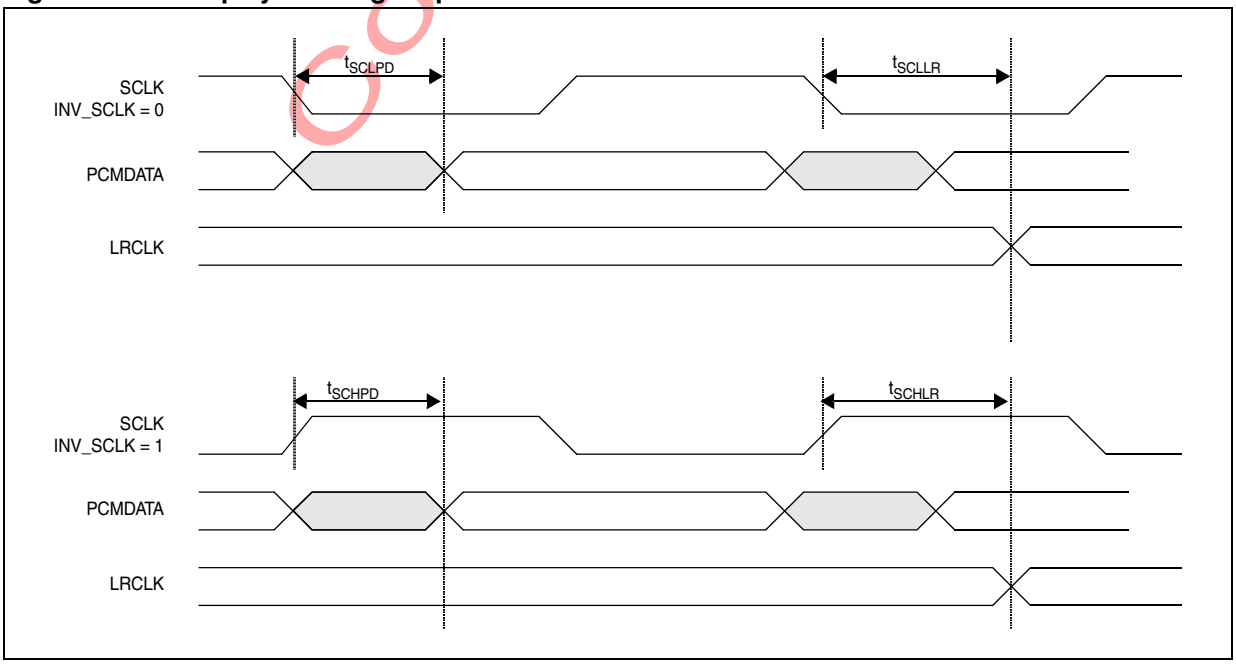


Table 97. PCM player output timing parameters

Symbol	Parameter	Min	Max	Units
t_{SCLPD}	SCLK low to PCMDATA valid	--	10	ns
t_{SCLLR}	SCLK low to LRCLK	--	10	ns
t_{SCHPD}	SCLK high to PCMDATA valid	--	50	ns
t_{SCHLR}	SCLK high to LRCLK	--	50	ns

20.4 Transport stream input AC specification

20.4.1 Parallel transport stream input interface

The *Figure 44* shows the timing waveforms of parallel transport stream input interface.

Figure 44. Parallel transport stream input timing waveform

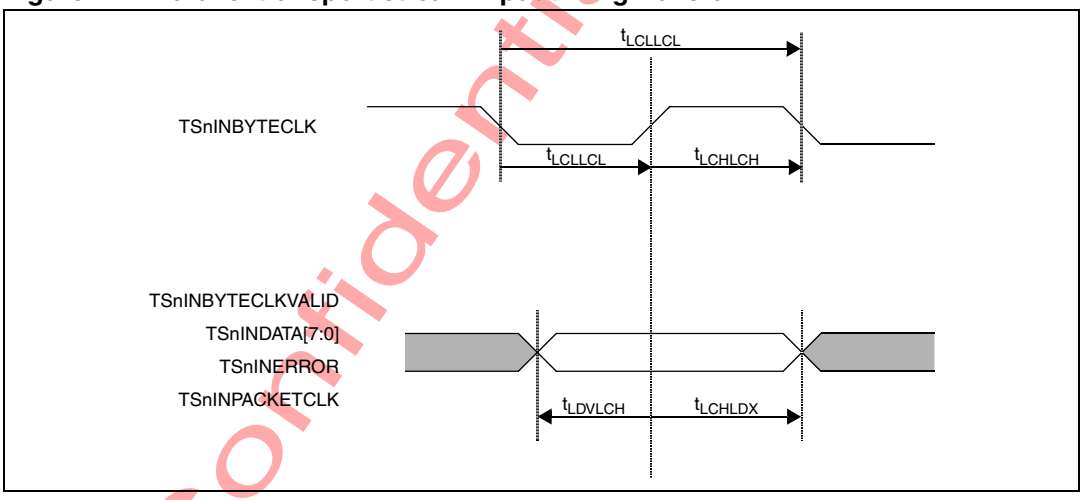


Table 98. Parallel transport stream input timing parameter

Symbol	Parameter	Min	Max	Units
t_{LCLLCL}	TSnINBYTECLK period	37	--	ns
t_{LCHLCH}	TSnINBYTECLK pulse width high	10	--	ns
t_{LCLLCL}	TSnINBYTECLK pulse width low	10	--	ns
t_{LDVLCH}	TSnIN signals valid to TSnINBYTECLK high	4	--	ns
t_{LCHLDX}	TSnIN signals hold after TSnINBYTECLK high	2	--	ns

20.4.2 Serial transport stream input interface

The *Figure 45* shows the timing waveforms of serial transport stream input interface.

Figure 45. Serial transport stream input timing waveform

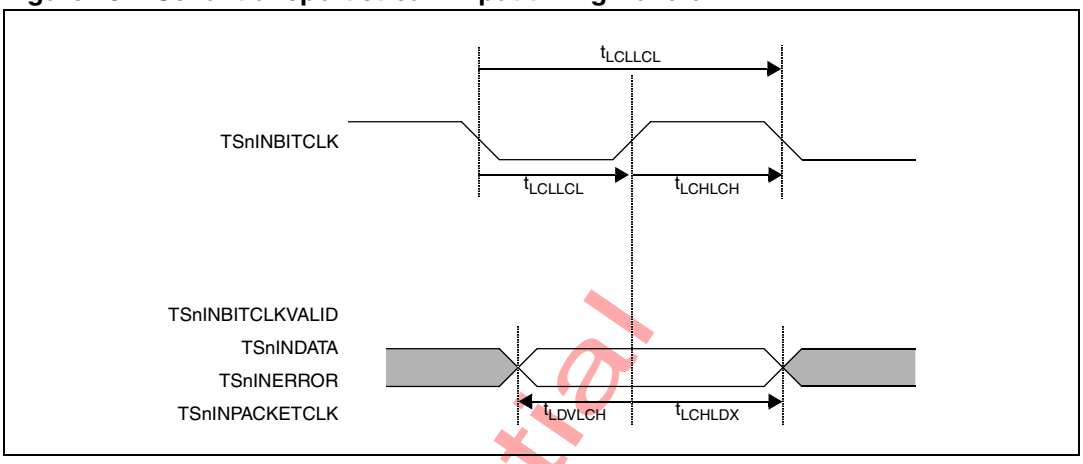


Table 99. Serial transport stream input timing parameter

Symbol	Parameter	Min	Max	Units
t_{LCLLCL}	TSnINBITCLK period	10	--	ns
t_{LCHLCH}	TSnINBITCLK pulse width high	3	--	ns
t_{LCLLCL}	TSnINBITCLK pulse width low	3	--	ns
t_{LDVLCH}	TSnIN signals valid to TSnINBITCLK high	3	--	ns
t_{LCHLDX}	TSnIN signals hold after TSnINBITCLK high	2	--	ns

20.5 Transport stream output AC specification

The *Figure 46* shows the timing waveforms of transport stream output interface.

Figure 46. Transport stream output timing

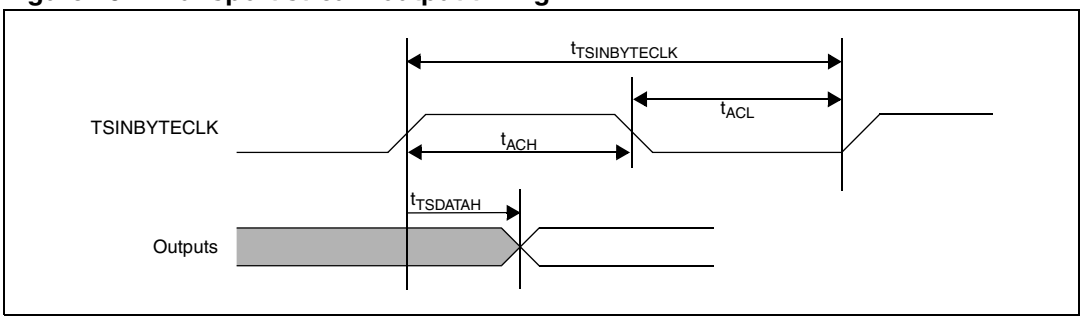


Table 100. Transport stream output port timings

Symbol	Parameter	Min	Max	Units
$t_{TSINBYTECLK}$	TSINBYTECLK clock period	10(1)	33.3(2)	ns
$t_{TSDATAH}$	Output delay to TSINBYTECLK	-	0	ns
t_{ACH}	TSINBYTECLK pulse width high	4	-	ns
t_{ACL}	TSnINBYTECLK pulse width low	4	-	ns

1. Minimum clock period in case of serial mode.
2. Maximum clock period in case of parallel mode.

20.6 JTAG interfaces AC specification

Input clocks: TCK (rising edge)

Inputs: TDI, TMS

Figure 47. JTAG interface timing

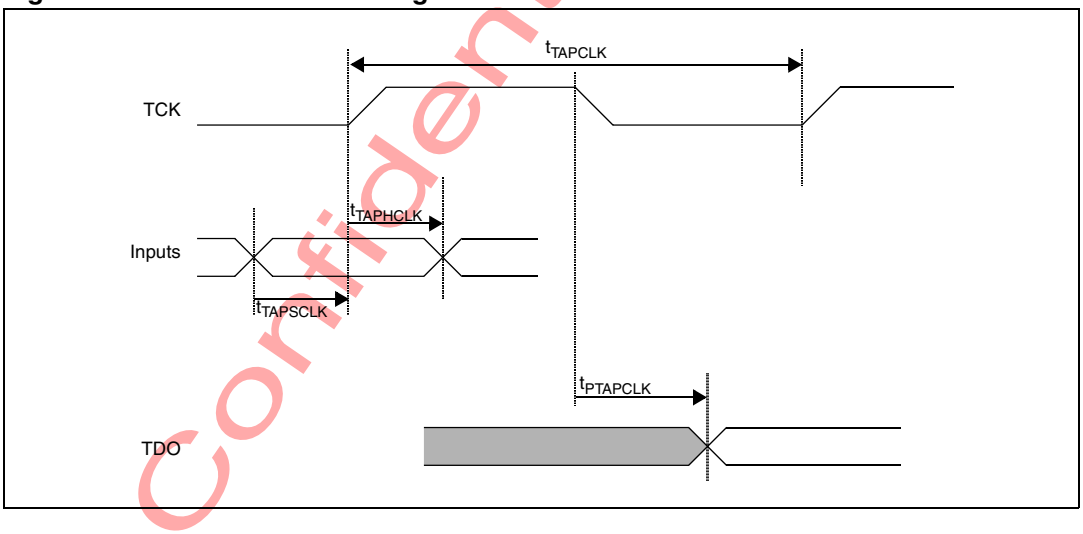


Table 101. JTAG input/output port timings

Symbol	Parameter	Min	Max	Units
Input clock	TCK period	20		ns
tTAPHCLK	Inputs setup to TCK rising edge	5		ns
tTAPSCLK	Inputs hold to TCK rising sdge	5		ns
tPTAPCLK	Output delay to TCK falling edge		15	ns

20.7 EMI timings

All of the outputs come from a multiplexer controlled by the clock. It is assumed that the EMI will be programmed so that all the outputs will be changed on the falling edge of the clock.

Following tables assume an external load of 25 pF on every EMI pad.

20.7.1 Synchronous devices

All synchronous transactions originate and terminate at flip flops within the padlogics. Outputs are generated with respect to the falling edge of the bus clock, and inputs are sampled with respect to the rising edge.

EMI-Clock: EMISFLASH

EMI-outputs: EMIADDR[*], EMIDATA[*], NOTEMICS*, NOTEMIBE, NOTEMIOE, NOTEMILBA, NOTEMIBAA, EMIRDNOTWR

EMI-inputs: EMIDATA[*], EMIREADYORWAIT

Figure 48. EMI synchronous device timing

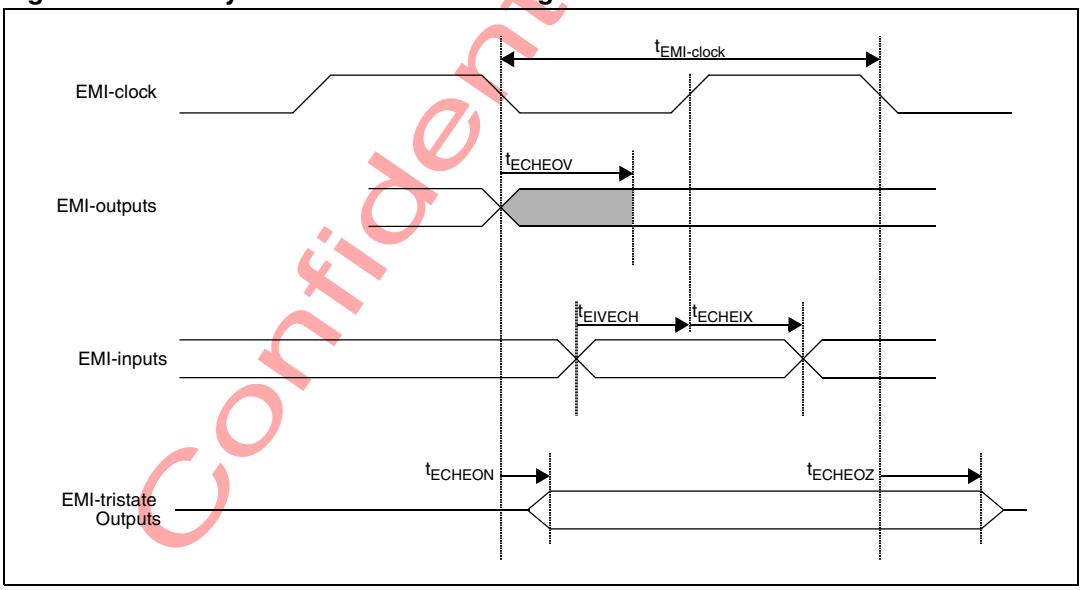


Table 102. EMI / SFLASH synchronous interface parameters

Symbol	Parameter	Min	Max	Units
Input clock	EMISFLASHCLK period	33		ns
t_{ECHEOV}	Bus clock falling edge to valid data	0	4	ns
t_{EIVECH}	Input valid to rising clock edge (input setup time)	5.5		ns
t_{ECHEIX}	Rising clock edge to input invalid (input hold time)	0		ns
t_{ECHEON}	Falling clock edge to data valid (after tristate output)	2		ns
t_{ECHEOZ}	Falling clock edge to data valid (before tri-state output)		-3	ns

These values are static offsets within a bus cycle, they should be read in conjunction with the waveforms in *external memory interface* (EMI), which are cycle accurate only.

Asynchronous memory/peripherals

The EMI strobes are programmed in terms of internal clock phases, that is to say with half cycle resolution. The clock to output delay for all outputs (address, data, strobes) are closely matched with a skew tolerance of ±3 ns (assuming an external load of 25 pF on pads).

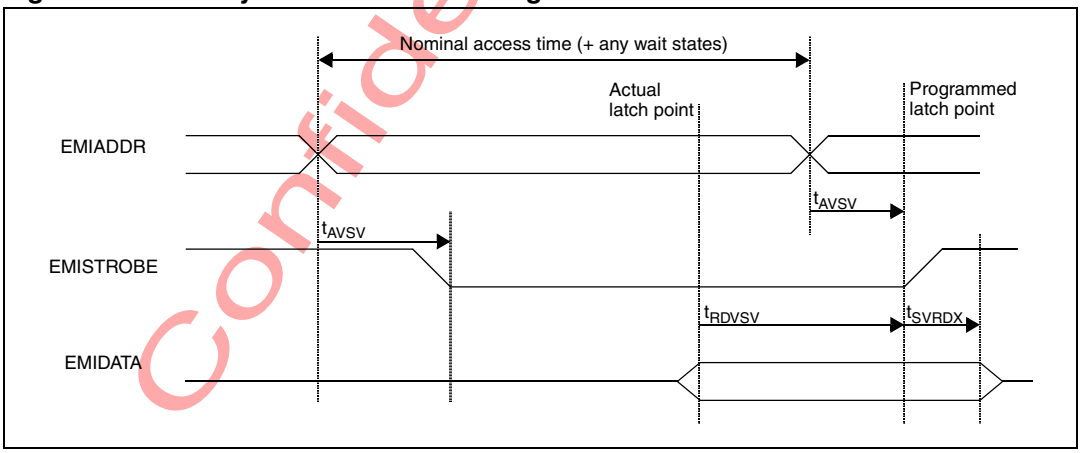
The input latch point for a read access is determined by the number of programmed EMI subsystem clock cycles for the latch point. The correction allows the latch point to be measured from the edge of an active chip select, that has been programmed to rise at the programmed read latch point.

Time between the address bus switching and a chip select or data bus output switching is n programmed phases ±3 ns. That is, worst case, the chip select or data is maximum of 3 ns after the address, or worst case the chip select or data is 3 ns before the address.

For a read cycle, the data is latched by the STi7197 at the programmed number of EMI subsystem clock cycles from the end of the access plus a latch point correction time, which is effectively the read setup time. The latch point correction time (read setup time) is a minimum of 5 ns + skew tolerance correction of the output signal used as a reference. This is 5 ± 3 ns, thus the minimum read setup time relative to a strobe is 8 ns. This ensures the read hold time is always a minimum of 0 ns, guaranteed by design.

Asynchronous access - READ

Figure 49. EMI asynchronous read timing



Asynchronous access - WRITE

Figure 50. EMI asynchronous write timing

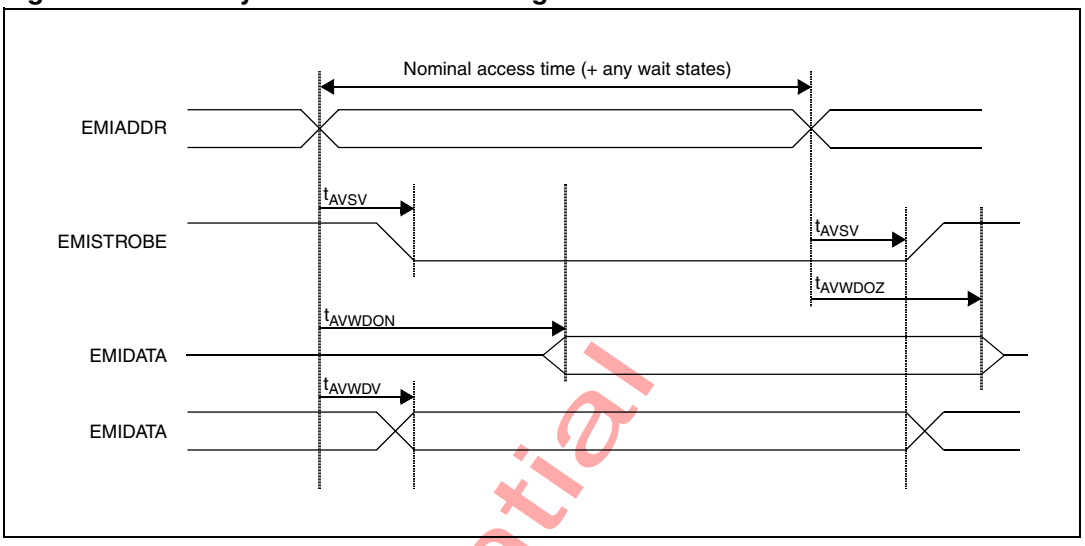


Table 103. EMI / Asynchronous memory/peripherals interface parameters

Symbol	Parameter	Min	Max	Units	Note
t_{AVSV}	Address valid to output strobe valid	-1.5	3	ns	(1)
t_{RDVSV}	Read data valid to strobe valid (read setup time)	8		ns	(2)
t_{SVRDX}	Read data hold time after strobe valid (read hold time)	0		ns	(3)
t_{AVWDON}	Address valid to write data valid (after tristate output)	3		ns	(4)
t_{AVWDOZ}	Address valid to write data valid (before tristate output)		-4.5	ns	
t_{AVWDV}	Address valid to write data valid	-2	2	ns	

1. Skew plus nominal N programmed EMI subsystem clock cycles of strobe delay.
2. Skew from nominal programmed read latch point.
3. Minimum values are guaranteed by design.
4. Skew from nominal programmed phases of data drive delay.

Table 103 assumes an external load of 25 pF on EMI pads.

20.8 LMI DDR2-SDRAM timings

The DDR2 interface is compliant to the Jedec DDR2 specs (DDR2-800 grade).

20.9 PIO output AC specification

Reference clock in this case means the last transition of any PIO signal.

Note: There are two different sets of PIO timings, one for the SSC (I²C) outputs and one for all other PIO outputs.

Figure 51. PIO timing

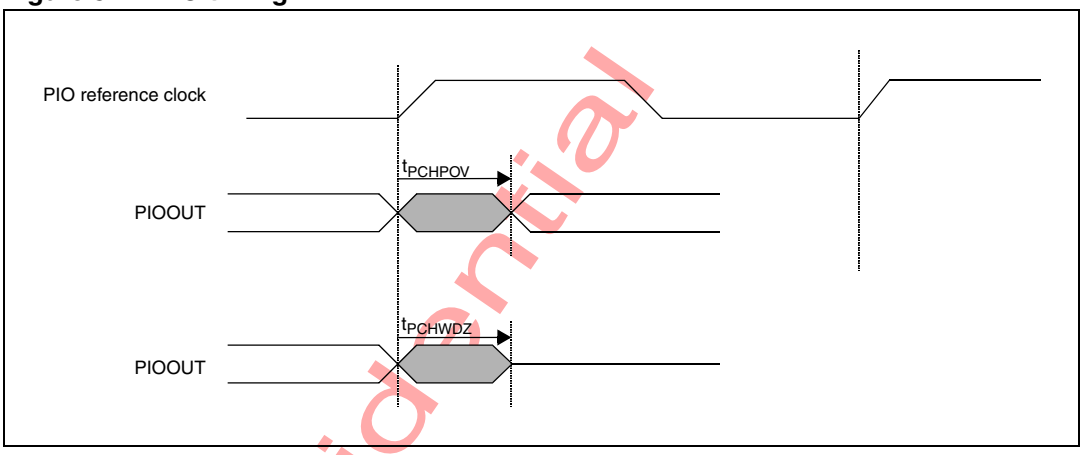


Table 104. PIO timings: SSC (I²C bus)

Symbol	Parameter	Min	Max	Units
t_{PCHPOV}	PIO_REFCLOCK high to PIO output valid	-20.0	0.0	ns
t_{PCHWDZ}	PIO tristate after PIO_REFCLOCK high	-20.0	5.0	ns
t_{PIOr}	Output rise time	3.0	30.0	ns
t_{PIOf}	Output fall time	3.0	30.0	ns

20.10 Ethernet interface

20.10.1 MII interface

MII receive interface

The *Figure 52* shows the timing waveform for the Receive MII interface.

Figure 52. Receive signal timing relationship at the MII PHY interface

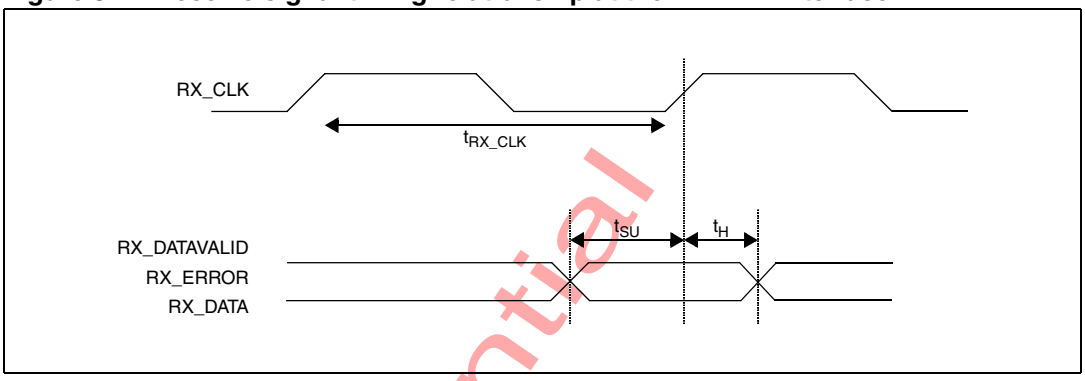


Table 105. Receive MII interface timings

Symbol	Parameter	Min	Max	Units
t_{RX_CLK}	RX_CLK time period	20		ns
t_{SU}	Input signals (RX_DATAVALID, RX_ERROR, RX_DATA) setup time	10		ns
t_H	Input signals (RX_DATAVALID, RX_ERROR, RX_DATA) hold time	10		ns

MII transmit interface

The *Figure 53* shows the timing waveform for the Transmit MII interface.

Figure 53. Transmit signal timing relationship at the MII PHY interface

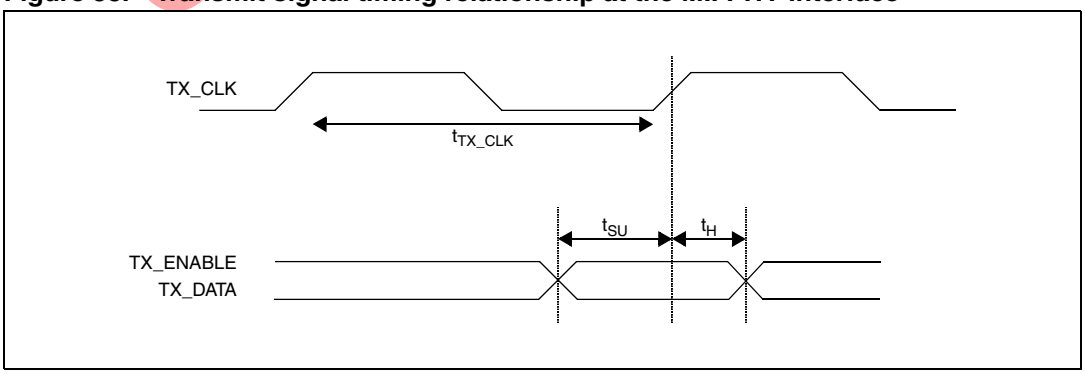


Table 106. Transmit MII interface timings

Symbol	Parameter	Min	Max	Units
t_{TX_CLK}	TX_CLK time period	20		ns
t_{SU}	Output signals (TX_ENABLE, TX_DATA) setup time	10		ns
t_H	Output signals (TX_ENABLE, TX_DATA) hold time	0	25	ns

MII control interface

The *Figure 54* shows the timing waveform for the MII control interface.

Figure 54. Control signal timing relationship at the MII PHY interface

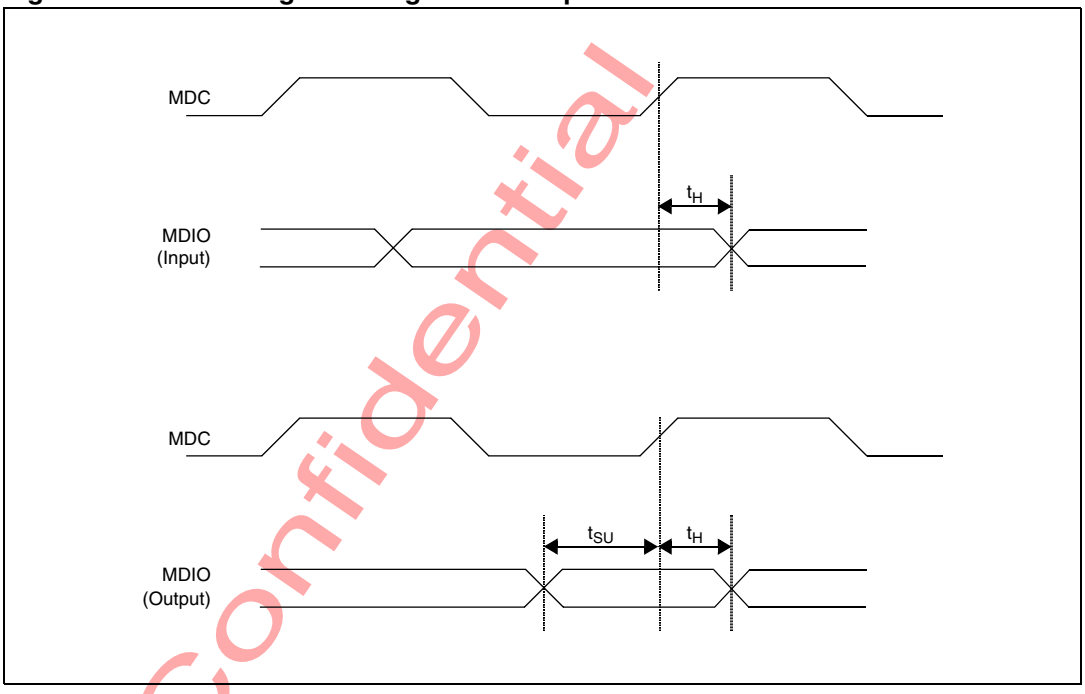
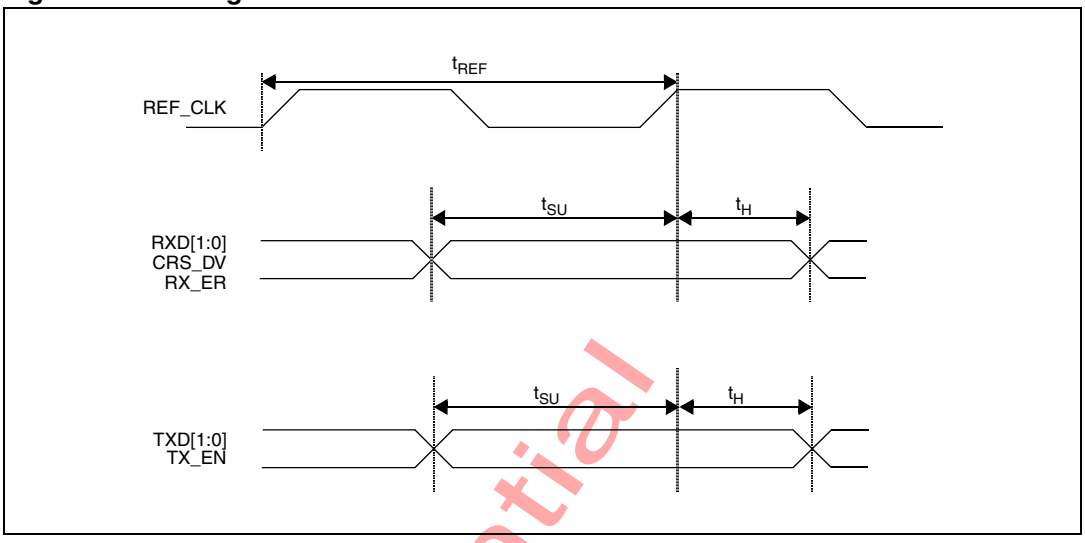


Table 107. MII control interface timings

Symbol	Parameter	Min	Max	Units
Input signal (MDIO)				
t_H	Input signal (MDIO) hold time	0	300	ns
Output signal (MDIO)				
t_{SU}	Output signal (MDIO) setup time	10		ns
t_H	Output signal (MDIO) hold time	10		ns

20.10.2 RMII interface

Figure 55. Timing waveform for the RMII interface



The *Table 108* describes RMII timings parameters.

Table 108. RMII timing parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{REF}	REF_CLK Frequency	-	50	-	MHz
	REF_CLK Duty Cycle	35	-	65	%
t_{SU}	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER (Data Setup to REF_CLK rising edge)	4	-	-	ns
t_H	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER (Data hold from REF_CLK rising edge)	2	-	-	ns

21 Alternate functions on PIO

21.1 Alternate functions

To improve flexibility and to allow the STi7197 to fit into different set-top box application architectures, the input and output signals from some of the peripherals and functions are not directly connected to the pins of the device. Instead, they are assigned to the alternate function inputs and outputs of a PIO port bit, or an I/O pin. This allows the pins to be configured with their default function if the associated input or output is not required in that particular application.

Some pins have several alternate functions, for inputs and outputs, or both. *Table 109* to *Table 125* list the different alternate functions.

Inputs connected to the alternate function input are permanently connected to the input pin. The output signal from a peripheral is only connected when the PIO bit is configured into either push-pull or open drain driver alternate function mode.

Some alternate function signals are available on more than one PIO port.

The STi7197 uses seven PIO banks (PIO#0 to PIO#6) that are controlled by the COMMS IP and 10 banks that are driven by a standalone PIO module called STD_PIO.

The STi7197 embeds two types of PIOs alternate functions.

- Functions that are enabled by a register located inside the COMMS (or STD_PIO module).
- Functions that are enabled by a register located inside the system config module. This configuration is required for the pins where the alternate functions are enabled already at reset (by default the pins controlled by the COMMS are in the PIO mode and not alternate).

In addition to the multiplexing on the PIO pins, the STi7197 uses other pin multiplexing to provide different signal options depending upon the device application. For these other multiplexing options see *Section 9: Basic chip operating modes and multiplexing scenarios on page 192*.

Figure 56. I/O port pins (alternate functions controlled by COMMS or STD_PIO)

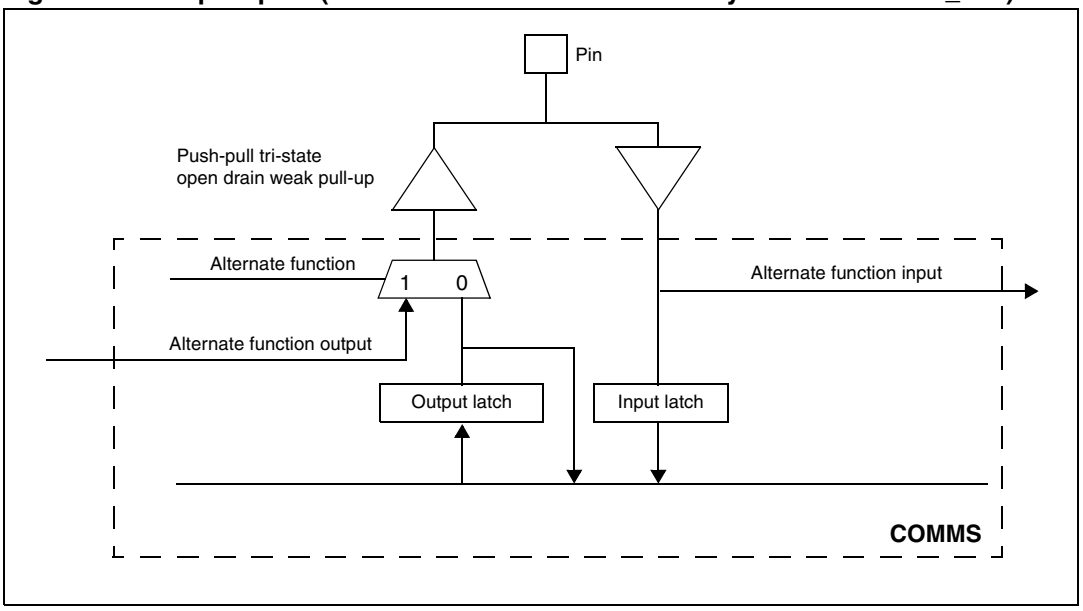
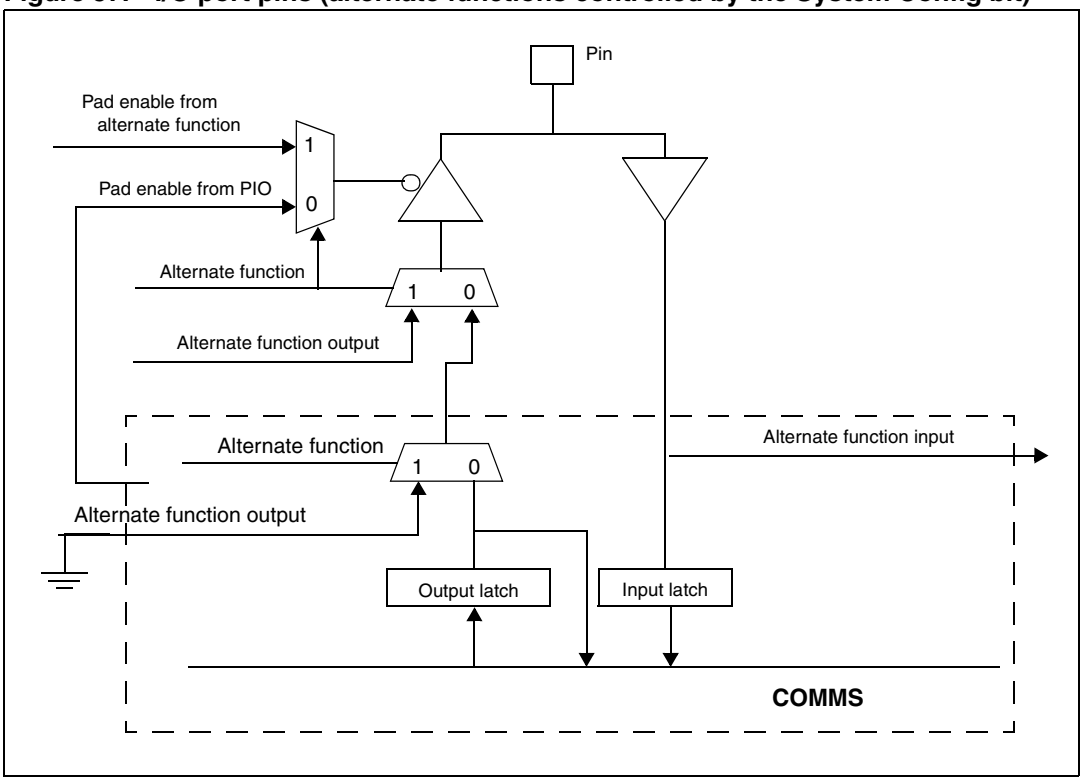


Figure 57. I/O port pins (alternate functions controlled by the System Config bit)



Note: In case of alternate functions controlled by the System Config bit, the enabling of the pad is driven by the alternate function itself when in the alternate mode or by the COMMS (or STD_PIO) signals when in the PIO mode.

21.2 PIO0 alternate functions

PIO0 is on COMMS block. It provides:

- first digital video output (DVO0) extension (8 to 16-bit)
- second digital video output (DVO1)(24-bit)
- Smartcard interfaces (SC0 and SC1)
- UART0 interfaces

Table 109. PIO0 alternate functions

PIO0	Config register: SYSTEM_CONFIG19[15:0]					
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		DVO1	**DVO 0**	**SC 0**	**UART 0**	**Reserved**
PIO0[0]	Name	DVO1[0]	DVO0[16]	SC0_DATAOUT	UART0_TXD	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	O	RESERVED
	Configuration	SYSTEM_CONFIG19[8,0]=00	SYSTEM_CONFIG19[8,0]=01	SYSTEM_CONFIG19[8,0]=10	SYSTEM_CONFIG19[8,0]=11	RESERVED
PIO0[1]	Name	DVO1[1]	DVO0[17]	SC0_DATAIN	UART0_RXD	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	I	I	RESERVED
	Configuration	SYSTEM_CONFIG19[9,1]=00	SYSTEM_CONFIG19[9,1]=01	Not required	Not required	RESERVED
PIO0[2]	Name	DVO1[2]	DVO0[18]	SC0_EXTCLKIN	UART0_NOT_OE	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	I	O	RESERVED
	Configuration	SYSTEM_CONFIG19[10,2]=00	SYSTEM_CONFIG19[10,2]=01	Not required	SYSTEM_CONFIG19[10,2]=11	RESERVED
PIO0[3]	Name	DVO1[3]	DVO0[19]	SC0_CLKOUT	UART0_RTS	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	O	RESERVED
	Configuration	SYSTEM_CONFIG19[11,3]=00	SYSTEM_CONFIG19[11,3]=01	SYSTEM_CONFIG19[11,3]=10	SYSTEM_CONFIG19[11,3]=11	RESERVED

Table 109. PIO0 alternate functions (continued)

PIO0	Config register: SYSTEM_CONFIG19[15:0]					
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		DVO1	**DVO 0**	**SC 0**	**UART 0**	**Reserved**
PIO0[4]	Name	DVO1[4]	DVO0[20]	SC0_RESET	UART0_CTS	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	UART 0	RESERVED
	Direction	O	O	O	I	RESERVED
	Configuration	SYSTEM_CONFIG19[12,4]=00	SYSTEM_CONFIG19[12,4]=01	SYSTEM_CONFIG19[12,4]=10	Not required	RESERVED
PIO0[5]	Name	DVO1[5]	DVO0[21]	SC0_COND_VCC	-	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	-	RESERVED
	Direction	O	O	O	-	RESERVED
	Configuration	SYSTEM_CONFIG19[13,5]=00	SYSTEM_CONFIG19[13,5]=01	SYSTEM_CONFIG19[13,5]=10	-	RESERVED
PIO0[6]	Name	DVO1[6]	DVO0[22]	SC0_COND_VPP	-	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	-	RESERVED
	Direction	O	O	O	-	RESERVED
	Configuration	SYSTEM_CONFIG19[14,6]=00	SYSTEM_CONFIG19[14,6]=01	SYSTEM_CONFIG19[14,6]=10	-	RESERVED
PIO0[7]	Name	DVO1[7]	DVO0[23]	SC0_DETECT	-	RESERVED
	Description	Second DVO output	First DVO output	Smartcard 0	-	RESERVED
	Direction	O	O	I	-	RESERVED
	Configuration	SYSTEM_CONFIG19[15,7]=00	SYSTEM_CONFIG19[15,7]=01	Not required	-	RESERVED

21.3 PIO1 alternate functions

PIO1 is on COMMS block. It provides:

- DVO1 (24-bit)
- Smartcard interface (SC1)
- MAFE interface
- UART interfaces

Table 110. PIO1 alternate functions

PIO1	Config register: SYSTEM_CONFIG20[15:0]				
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1	**MAFE I/F**	**SC 1**	**UART 1**
PIO1[0]	Name	DVO1[8]	MAFE_DIN	SC1_DATAOUT	UART1_TXD
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	I	O	O
	Configuration	SYSTEM_CONFIG20[8,0]=00	Not required	SYSTEM_CONFIG20[8,0]=10	SYSTEM_CONFIG20[8,0]=11
PIO1[1]	Name	DVO1[9]	MAFE_SCLK	SC1_DATAIN	UART1_RXD
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	I	I	I
	Configuration	SYSTEM_CONFIG20[9,1]=00	Not required	Not required	Not required
PIO1[2]	Name	DVO1[10]	MAFE_HC1	SC1_EXTCLKIN	-
	Description	Second DVO output	MAFE	Smartcard 1	-
	Direction	O	O	I	-
	Configuration	SYSTEM_CONFIG20[10,2]=00	SYSTEM_CONFIG20[10,2]=01	Not required	-
PIO1[3]	Name	DVO1[11]	MAFE_DOUT	SC1_CLKOUT	UART1_RTS
	Description	Second DVO output	MAFE	Smartcard 1	UART 1
	Direction	O	O	O	O
	Configuration	SYSTEM_CONFIG20[11,3]=00	SYSTEM_CONFIG20[11,3]=01	SYSTEM_CONFIG20[11,3]=10	SYSTEM_CONFIG20[11,3]=11

Table 110. PIO1 alternate functions (continued)

PIO1	Config register: SYSTEM_CONFIG20[15:0]				
	Config bus: PIO0_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1	**MAFE I/F**	**SC 1**	**UART 1**
PIO1[4]	Name	DVO1[12]	-	SC1_RESET	UART1_CTS
	Description	Second DVO output	-	Smartcard 1	UART 1
	Direction	O	-	O	I
	Configuration	SYSTEM_CONFIG20[12,4]=00	-	SYSTEM_CONFIG20[12,4]=10	Not required
PIO1[5]	Name	DVO1[13]	MAFE_FS	SC1_COND_VCC	-
	Description	Second DVO output	MAFE	Smartcard 1	-
	Direction	O	I	O	-
	Configuration	SYSTEM_CONFIG20[13,5]=00	Not required	SYSTEM_CONFIG20[13,5]=00	-
PIO1[6]	Name	DVO1[14]	-	SC1_COND_VPP	-
	Description	Second DVO output	-	Smartcard 1	-
	Direction	O	-	O	-
	Configuration	SYSTEM_CONFIG20[14,6]=00	-	SYSTEM_CONFIG20[14,6]=10	-
PIO1[7]	Name	DVO1[15]	-	SC1_DETECT	-
	Description	Second DVO output	-	Smartcard 1	-
	Direction	O	-	I	-
	Configuration	SYSTEM_CONFIG20[15,7]=00	-	Not required	-

21.4 PIO2 alternate functions

PIO2 is on COMMS block. It provides:

- DVO1 (24-bit)
- SSC0 and SSC1 interfaces with I²C half-duplex/full-duplex modes selectable by the ssc0_mux_sel and ssc1_mux_sel bits
- SSC2 and SSC3 interfaces with I²C half-duplex modes selectable

Table 111. PIO2 alternate functions

PIO2	Config register: SYSTEM_CONFIG21[15:0]				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1		**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[0]	Name	DVO1[16]	-	SSC2_MTSR	SSC2_MRST
	Description	Second DVO output	-	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[8,0]=00	-	In: Not required Out: SYSTEM_CONFIG21[8,0]=10	In: SYSTEM_CONFIG16[8,7]=00 Out: SYSTEM_CONFIG21[8,0]=11
PIO2[1]	Name	DVO1[17]	-	SSC3_MTSR	SSC3_MRST
	Description	Second DVO output	-	SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[9,1]=00	-	In: Not required Out: SYSTEM_CONFIG21[9,1]=10	In: SYSTEM_CONFIG16[15,14]=00 Out: SYSTEM_CONFIG21[9,1]=11
PIO2[2]	Name	DVO1[18]	-	SSC0_SCL	SSC0_SCL
	Description	Second DVO output	-	SSC0 serial clock in/out	SSC0 serial clock in/out
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[10,2]=00	-	In: Not required Out: SYSTEM_CONFIG21[10,2]=10	In: Not required Out: SYSTEM_CONFIG21[10,2]=11

Table 111. PIO2 alternate functions (continued)

PIO2	Config register: SYSTEM_CONFIG21[15:0]				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1		**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[3]	Name	DVO1[19]	-	SSC0_MTSR	SSC0_MRST
	Description	Second DVO output	-	SSC0 Data bit: master transmit/slave receive, full duplex	SSC0 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[11,3]=00	-	In: Not required Out: SYSTEM_CONFIG21[11,3]=10	In: SYSTEM_CONFIG16[0]=0 Out: SYSTEM_CONFIG21[11,3]=11
PIO2[4]	Name	DVO1[20]	-	SSC0_MRST	SSC0_MRST
	Description	Second DVO output	-	SSC0 Data bit: master receive/slave transmit, full duplex	SSC0 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[12,4]=00	-	SYSTEM_CONFIG21[12,4]=10	In: SYSTEM_CONFIG16[0]=1 Out: SYSTEM_CONFIG21[12,4]=11
PIO2[5]	Name	DVO1[21]	-	SSC1_SCL	SSC1_SCL
	Description	Second DVO output	-	SSC1 Serial Clock	SSC1 Serial Clock
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[13,5]=00	-	In: Not required Out: SYSTEM_CONFIG21[13,5]=10	In: Not required Out: SYSTEM_CONFIG21[13,5]=11
PIO2[6]	Name	DVO1[22]	-	SSC1_MTSR	SSC1_MRST
	Description	Second DVO output	-	SSC1 Data bit: master transmit/slave receive, full duplex	SSC1 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[14,6]=00	-	In: Not required Out: SYSTEM_CONFIG21[14,6]=10	In: SYSTEM_CONFIG16[3]=0 Out: SYSTEM_CONFIG21[14,6]=11

Table 111. PIO2 alternate functions (continued)

PIO2	Config register: SYSTEM_CONFIG21[15:0]				
	Config bus: PIO2_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1		**SSC 0,1,2,3**	**SSC 0,1,2,3**
PIO2[7]	Name	DVO1[23]	-	SSC1_MRST	SSC1_MRST
	Description	Second DVO output	-	SSC1 Data bit: master receive/slave transmit, full duplex	SSC1 Data bit: master receive/slave transmit, full duplex
	Direction	O	-	I/O	I/O
	Configuration	SYSTEM_CONFIG21[15,7]=00	-	In: Not required Out: SYSTEM_CONFIG21[15,7]=10	In: SYSTEM_CONFIG16[3]=1 Out: SYSTEM_CONFIG21[15,7]=11

21.5 PIO3 alternate functions

PIO3 is on COMMS block. It provides:

- DVO0 (16-bit)
- DVO1 (24-bit)
- digital video port extension (DVP0) (16-bit)
- SSC2 and SSC3 interfaces with I2C half-duplex modes selectable
- infra red blaster (IRB) interface
- auxiliary VTG synchronizations

Table 112. PIO3 alternate functions

PIO3	Config register: SYSTEM_CONFIG25[15:0]				
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1	**IRB, DVP 0, SSC 2,3**	**IRB, SSC 2,3**	**AUX video timing h/v refs**
PIO3[0]	Name	DVO1HS	-	IRB_IR_IN	VTG_AUX_HS
	Description	DVO horizontal sync	-	IRB IR data input	Aux video
	Direction	O	-	I	O
	Configuration	SYSTEM_CONFIG25[8,0]=00	-	Not required	SYSTEM_CONFIG25[8,0]=11
PIO3[1]	Name	DVO1_CLK	-	IRB_UHF_IN	-
	Description	DVO clock	-	IRB UHF data input	-
	Direction	O	-	I	-
	Configuration	SYSTEM_CONFIG25[9,1]=00	-	Not required	-
PIO3[2]	Name	DVO1VS	IRB_IR_DATA_OUT	IRB_IR_DATA_OUT	VTG_AUX_VS
	Description	DVO vertical sync	IRB IR data output	IRB IR data output	Aux video
	Direction	O	O	O	O
	Configuration	SYSTEM_CONFIG25[10,2]=00	SYSTEM_CONFIG25[10,2]=01	SYSTEM_CONFIG25[10,2]=10	SYSTEM_CONFIG25[10,2]=11

Table 112. PIO3 alternate functions (continued)

PIO3	Config register: SYSTEM_CONFIG25[15:0]				
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 1	**IRB, DVP 0, SSC 2,3**	**IRB, SSC 2,3**	**AUX video timing h/v refs**
PIO3[3]	Name	DVO1DE	IRB_DATA_OUT_OD	IRB_DATA_OUT_OD	VTG_AUX_BOTNOTTOP
	Description	Second DVO output	IRB data output open drain	IRB data output open drain	Aux video
	Direction	O	O	O	O
	Configuration	SYSTEM_CONFIG25[11,3]=00	SYSTEM_CONFIG25[11,3]=01	SYSTEM_CONFIG25[11,3]=10	SYSTEM_CONFIG25[11,3]=11
PIO3[4]	Name	DVO0[0]	DVP0[8]/SSC2_SCL	SSC2_SCL	-
	Description	First DVO output	DVP input/SSC2 SCL out	SSC2 SCL out	-
	Direction	O	I/O	I/O	-
	Configuration	SYSTEM_CONFIG25[12,4]=00	In: Not required Out: SYSTEM_CONFIG25[12,4]=01	In: SYSTEM_CONFIG16[12,11]=00/01 Out: SYSTEM_CONFIG25[12,4]=10	-
PIO3[5]	Name	DVO0[1]	DVP0[9]/SSC2_MTSR	SSC2_MTSR	SSC2_MRST	-
	Description	First DVO output	DVP input/SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex	-
	Direction	O	I/O	I	I/O	-
	Configuration	SYSTEM_CONFIG25[13,5]=00	In: Not required Out: SYSTEM_CONFIG25[13,5]=01	SYSTEM_CONFIG16[10,9]=00	In: SYSTEM_CONFIG16[8,7]=01 Out: SYSTEM_CONFIG25[13,5]=10	-
PIO3[6]	Name	DVO0[2]	DVP0[10]/SSC3_SCL	SSC3_SCL	-
	Description	First DVO output	DVP input/SSC3 SCL out	SSC3 SCL in/SSC3 SCL out	-
	Direction	O	I/O	I/O	-
	Configuration	SYSTEM_CONFIG25[14,6]=00	In: Not required Out: SYSTEM_CONFIG25[14,6]=01	In: SYSTEM_CONFIG16[19,18]=00 Out: SYSTEM_CONFIG25[14,6]=10	-

Table 112. PIO3 alternate functions (continued)

PIO3	Config register: SYSTEM_CONFIG25[15:0]					
	Config bus: PIO3_ALTFOP[1:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**		**Alternate 4**
		DVO 1	**IRB, DVP 0, SSC 2,3**	**IRB, SSC 2,3**		**AUX video timing h/v refs**
PIO3[7]	Name	DVO0[3]	DVP0[11]/SSC3_MTSR	SSC3_MTSR	SSC3_MRST	-
	Description	First DVO output	DVP input/ SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex	-
	Direction	O	I/O	I	I/O	-
	Configuration	SYSTEM_CONFIG25[15,7]=00	In: Not required Out: SYSTEM_CONFIG25[15,7]=01	In: SYSTEM_CONFIG16[17,16]=00	In: SYSTEM_CONFIG16[15,14]=01 Out: SYSTEM_CONFIG25[15,7]=10	-

21.6 PIO4 alternate functions

PIO4 is on COMMS block. It provides:

- DVO0 (16-bit)
- DVP0 (16-bit)
- UART2 interface
- pulse width modulator (PWM) interface
- USB power control

Table 113. PIO4 alternate functions

PIO4	Config register: SYSTEM_CONFIG34[15:0]				
	Config bus: PIO4_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 0	**DVP 0**	**UART 2, PWM 0,1**	**PWM 0, USB 1,2 Power ctrl**
PIO4[0]	Name	DVO0[4]	DVP0[12]	UART2_TXD	-
	Description	First DVO output	DVP input	UART	-
	Direction	O	I	O	-
	Configuration	SYSTEM_CONFIG34[8,0]=00	Not required	SYSTEM_CONFIG34[8,0]=10	-
PIO4[1]	Name	DVO0[5]	DVP0[13]	UART2_RXD	-
	Description	First DVO output	DVP input	UART	-
	Direction	O	I	I	-
	Configuration	SYSTEM_CONFIG34[9,1]=00	Not required	Not required	-
PIO4[2]	Name	DVO0[6]	DVP0[14]	UART2_CTS	-
	Description	First DVO output	DVP input	UART	-
	Direction	O	I	I	-
	Configuration	SYSTEM_CONFIG34[10,2]=00	Not required	Not required	-

Table 113. PIO4 alternate functions (continued)

PIO4	Config register: SYSTEM_CONFIG34[15:0]				
	Config bus: PIO4_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 0	**DVP 0**	**UART 2, PWM 0,1**	**PWM 0, USB 1,2 Power ctrl**
PIO4[3]	Name	DVO0[7]	DVP0[15]	PWM_CAPTURE_IN0/UART2_RTS	-
	Description	First DVO output	DVP input	PWM 0 capture input/UART	-
	Direction	O	I	I/O	-
	Configuration	SYSTEM_CONFIG34[11,3]=00	Not required	In: Not required Out: SYSTEM_CONFIG34[11,3]=10	-
PIO4[4]	Name	DVO0[8]	-	PWM_OUT0	USB1_PRT_OVCUR
	Description	First DVO output	-	PWM 0 output	USB 1 PRT overcurrent
	Direction	O	-	O	I
	Configuration	SYSTEM_CONFIG34[12,4]=00	-	SYSTEM_CONFIG34[12,4]=10	SYSTEM_CONFIG4[5]=0
PIO4[5]	Name	DVO0[9]	-	PWM_OUT1	USB1_PRT_PWR
	Description	First DVO output	-	PWM 1 output	USB 1 PRT power
	Direction	O	-	O	O
	Configuration	SYSTEM_CONFIG34[13,5]=00	-	SYSTEM_CONFIG34[13,5]=10	SYSTEM_CONFIG34[13,5]=11
PIO4[6]	Name	DVO0[10]	-	PWM_COMPARE_OUT1	USB2_PRT_OVCUR
	Description	First DVO output	-	PWM 1 compare output	USB 2 PRT overcurrent
	Direction	O	-	O	I
	Configuration	SYSTEM_CONFIG34[14,6]=00	-	SYSTEM_CONFIG34[14,6]=10	SYSTEM_CONFIG4[6]=0
PIO4[7]	Name	DVO0[11]	-	PWM_CAPTURE_IN1	USB2_PRT_PWR
	Description	First DVO output	-	PWM 1 compare output	USB 2 PRT power
	Direction	O	-	I	O
	Configuration	SYSTEM_CONFIG34[15,7]=00	-	Not required	SYSTEM_CONFIG34[15,7]=11

21.7 PIO5 alternate functions

PIO5 is on COMMS block. It provides:

- DVO0
- key scanner interface (KEY SCAN)
- UART3 interface
- main VTG synchronization signals

Table 114. PIO5 alternate functions

PIO5	Config register: SYSTEM_CONFIG35[15:0]				
	Config bus: PIO5_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 0	**Key SCAN I/F, UART 3**	**UART 3**	**Key scanning, Main video timing h/v refs**
PIO5[0]	Name	DVO0[12]	UART3_TXD	-	KEY_SCAN_OUT[0]
	Description	First DVO output	UART 3	-	Key scanning
	Direction	O	O	-	O
	Configuration	SYSTEM_CONFIG35[8,0]=00	SYSTEM_CONFIG35[8,0]=01	-	SYSTEM_CONFIG35[8,0]=11
PIO5[1]	Name	DVO0[13]	-	UART3_RXD	KEY_SCAN_OUT[1]
	Description	First DVO output	-	UART 3	Key scanning
	Direction	O	-	I	O
	Configuration	SYSTEM_CONFIG35[9,1]=00	-	Not required	SYSTEM_CONFIG35[9,1]=11
PIO5[2]	Name	DVO0[14]	UART3_RTS	-	KEY_SCAN_OUT[2]
	Description	First DVO output	UART 3	-	Key scanning
	Direction	O	O	-	O
	Configuration	SYSTEM_CONFIG35[10,2]=00	SYSTEM_CONFIG35[10,2]=01	-	SYSTEM_CONFIG35[10,2]=11

Table 114. PIO5 alternate functions (continued)

PIO5	Config register: SYSTEM_CONFIG35[15:0]				
	Config bus: PIO5_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVO 0	**Key SCAN I/F, UART 3**	**UART 3**	**Key scanning, Main video timing h/v refs**
PIO5[3]	Name	DVO0[15]	-	UART3_CTS	KEY_SCAN_OUT[3]
	Description	First DVO output	-	UART 3	Key scanning
	Direction	O	-	I	O
	Configuration	SYSTEM_CONFIG35[11,3]=00	-	Not required	SYSTEM_CONFIG35[11,3]=11
PIO5[4]	Name	DVO0_HSYNC	KEY_SCAN_IN[0]	-	VTG_MAIN_HS
	Description	First DVO output	Key scanning	-	VTG main
	Direction	O	I	-	O
	Configuration	SYSTEM_CONFIG35[12,4]=00	Not required	-	SYSTEM_CONFIG35[12,4]=11
PIO5[5]	Name	DVO0CLK	KEY_SCAN_IN[1]	-	
	Description	First DVO output	Key scanning	-	
	Direction	O	I	-	
	Configuration	SYSTEM_CONFIG35[13,5]=00	Not required	-	
PIO5[6]	Name	DVO0_VSYNC	KEY_SCAN_IN[2]	-	VTG_MAIN_VS
	Description	First DVO output	Key scanning	-	VTG main
	Direction	O	I	-	O
	Configuration	SYSTEM_CONFIG35[14,6]=00	Not required	-	SYSTEM_CONFIG35[14,6]=11
PIO5[7]	Name	DVO0_DATA_EN	KEY_SCAN_IN[3]	-	VTG_MAIN_BOTNOTTOP
	Description	First DVO output	Key scanning	-	VTG main
	Direction	O	I	-	O
	Configuration	SYSTEM_CONFIG35[15,7]=00	Not required	-	SYSTEM_CONFIG35[15,7]=11

21.8 PIO6 alternate functions

PIO6 is on COMMS block. It provides:

- DVP0 (8-bit)
- third transport input (TSIN2) interface
- second PCMCIA interface
- input VTG synchronization signals
- EMI SS arbiter signals/PCI support
- EMI SS arbiter signals

Table 115. PIO6 alternate functions

PIO6	Config register: SYSTEM_CONFIG36[15:0]				
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVP 0, PCMCIA 2 I/F	**TSIN 2**	**PCI I/F, PCMCIA 2 I/F, Video input timing h/v refs**	**PCI I/F, EMI I/F**
PIO6[0]	Name	DVP0[0]/PCMCIA2_OE	TSIN2SER/DATA[7]	PCI_INT_TO_HOST	PCI_INT_FROM_DEVICE[0]
	Description	DVP input/ PCMCIA 2 I/F	TS2 input	PCI host	PCI device
	Direction	I/O	I	O	I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[8,0]=00	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG36[8,0]=10	SYSTEM_CONFIG5[27]=0
PIO6[1]	Name	DVP0[1]/PCMCIA2_WE	TSIN2BYTECLK	-	PCI_INT_FROM_DEVICE[1]
	Description	DVP input/ PCMCIA 2 I/F	TS2 input	-	PCI device
	Direction	I/O	I	-	I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[9,1]=00	SYSTEM_CONFIG4[10]=0	-	Not required

Table 115. PIO6 alternate functions (continued)

PIO6	Config register: SYSTEM_CONFIG36[15:0]				
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVP 0, PCMCIA 2 I/F	**TSIN 2**	**PCI I/F, PCMCIA 2 I/F, Video input timing h/v refs**	**PCI I/F, EMI I/F**
PIO6[2]	Name	DVP0[2]/PCMCIA2_IORD	TSIN2BYTECLKVALID	-	PCI_INT_FROM_DEVICE[2]
	Description	DVP input/PCMCIA 2 i/F	TS2 input	-	PCI Host/device
	Direction	I/O	I	-	I
	Configuration	In: Not required Out: SYSTEM_CONFIG36[10,2]=00	SYSTEM_CONFIG4[10]=0	-	Not required
PIO6[3]	Name	DVP0[3]/PCMCIA2_IOWR	TSIN2ERROR	-	-
	Description	DVP input/PCMCIA 2 I/F	TS2 input	-	-
	Direction	I/O	I	-	-
	Configuration	In: Not required Out: SYSTEM_CONFIG36[11,3]=00	SYSTEM_CONFIG4[10]=0	-	-
PIO6[4]	Name	DVP0[4]	TSIN2PACKETCLK	PCMCIA2_WAIT	-
	Description	DVP input	TS2 input	PCMCIA 2 I/F	-
	Direction	I	I	I	-
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required	-
PIO6[5]	Name	DVP0[5]	TSIN2DATA[6]	PCMCIA_INT	PCI_BUS_REQ[1]
	Description	DVP input	TS2 input	PCMCIA 2 I/F	PCI Host/device
	Direction	I	I	I	I
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required	Not required

Table 115. PIO6 alternate functions (continued)

PIO6	Config register: SYSTEM_CONFIG36[15:0]				
	Config bus: PIO6_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVP 0, PCMCIA 2 I/F	**TSIN 2**	**PCI I/F, PCMCIA 2 I/F, Video input timing h/v refs**	**PCI I/F, EMI I/F**
PIO6[6]	Name	DVP0[6]	TSIN2DATA[5]	VTG_IN_HS	PCI_BUS_REQ[2]
	Description	DVP input	TS2 input	VTG input lock	PCI Host/device
	Direction	I	I	I	I
	Configuration	Not Required	In: SYSTEM_CONFIG4[10]=0	Not required	Not required
PIO6[7]	Name	DVP0[7]	TSIN2DATA[4]	VTG_IN_VS	-
	Description	DVP input	TS2 input	VTG	-
	Direction	I	I	I	-
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=0	Not required	-

21.9 PIO7 alternate functions

PIO7 is PIO0 on GPIO standalone block. It provides:

- DVP0 (8-bit)
- third transport input interface (TSIN2)
- MII and RMII interfaces
- KEY SCAN
- EMI SS arbiter signals/PCI support
- EMI SS arbiter signals

Note: During reset PIO7[7:4] are in input mode for mode pin capture.

Table 116. PIO7 alternate functions

PIO7	Config register: SYSTEM_CONFIG37[15:0]				
	Config bus: PIO7_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVP 0	**TSIN 2**	**Key scanning**	**PCI I/F**
PIO7[0]	Name	DVP0_HSYNC	TSIN2DATA[3]	KEY_SCAN_OUT[0]	PCI_LOCK_IN
	Description	DVP input	TS2 input	Key scanning	PCI Host/device
	Direction	I	I	O	I
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[8,0]=10	SYSTEM_CONFIG5[25]=0
PIO7[1]	Name	DVP0_VSYNC	TSIN2DATA[2]	KEY_SCAN_OUT[1]	PCI_BUS_GNT[1]
	Description	DVP input	TS2 input	Key scanning	PCI Host/device
	Direction	I	I	O	O
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[9,1]=10	Out: SYSTEM_CONFIG37[9,1]=11
PIO7[2]	Name	DVP0_CLK	TSIN2DATA[1]	KEY_SCAN_OUT[2]	PCI_BUS_GNT[2]
	Description	DVP input	TS2 input	Key scanning	PCI Host/device
	Direction	I	I	O	O
	Configuration	Not required	SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[10,2]=10	Out: SYSTEM_CONFIG37[10,2]=11

Table 116. PIO7 alternate functions (continued)

PIO7	Config register: SYSTEM_CONFIG37[15:0]				
	Config bus: PIO7_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		DVP 0	**TSIN 2**	**Key scanning**	**PCI I/F**
PIO7[3]	Name		TSIN2DATA[0]	KEY_SCAN_OUT[3]	-
	Description		TS2 input	Key scanning	-
	Direction		I	O	-
	Configuration		SYSTEM_CONFIG4[10]=0	SYSTEM_CONFIG37[11,3]=10	-
PIO7[4]	Name	MII_RXDV/MII_EXCRS	RMII_CRSDV	-	-
	Description	MII receive data valid	RMII receive data valid	-	-
	Direction	I/O	I	-	-
	Configuration	In: Not required Out: SYSTEM_CONFIG37[12,4]=00	SYSTEM_CONFIG4[10]=0	-	-
PIO7[5]	Name	MII_RXER/MII_EXCOL	RMII_RXER	-	-
	Description	MII receive error	RMII receive error	-	-
	Direction	I/O	I	-	-
	Configuration	In: Not required Out: SYSTEM_CONFIG37[13,5]=00	SYSTEM_CONFIG4[10]=0	-	-
PIO7[6]	Name	MII_TXD[0]	RMII_TXD[0]	-	-
	Description	MII transmit data	RMII transmit data	-	-
	Direction	O	O	-	-
	Configuration	SYSTEM_CONFIG37[14,6]=00	SYSTEM_CONFIG37[14,6]=01	-	-
PIO7[7]	Name	MII_TXD[1]	RMII_TXD[1]	-	-
	Description	MII transmit data	RMII transmit data	-	-
	Direction	O	O	-	-
	Configuration	SYSTEM_CONFIG37[15,7]=00	SYSTEM_CONFIG37[15,7]=01	-	-

21.10 PIO8 alternate functions

PIO8 is PIO1 on GPIO standalone block. It provides:

- MII and RMII interfaces
- DVO1 ALPHA coefficient output

Note: During reset PIO8[7:0] are in input mode for mode pin capture.

Table 117. PIO8 alternate functions

PIO8	Config register: SYSTEM_CONFIG46[15:0]			
	Config bus: PIO8_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	**-**
PIO8[0]	Name	MII_TXD[2]	DVO1_ALPHA[0]	-
	Description	MII transmit data	Second DVO/Alpha output	-
	Direction	O	O	-
	Configuration	SYSTEM_CONFIG46[8,0]=00	SYSTEM_CONFIG46[8,0]=01	-
PIO8[1]	Name	MII_TXD[3]	DVO1_ALPHA[1]	-
	Description	MII transmit data	Second DVO/Alpha output	-
	Direction	O	O	-
	Configuration	SYSTEM_CONFIG46[9,1]=00	SYSTEM_CONFIG46[9,1]=01	-
PIO8[2]	Name	MII_TXEN	RMII_TXEN	-
	Description	MII TX Enable	RMII TX Enable	-
	Direction	O	O	-
	Configuration	SYSTEM_CONFIG46[10,2]=00	SYSTEM_CONFIG46[10,2]=01	-

Table 117. PIO8 alternate functions (continued)

PIO8	Config register: SYSTEM_CONFIG46[15:0]			
	Config bus: PIO8_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	**-**
PIO8[3]	Name	MII_MDIO	RMII_MDIO	-
	Description	MII mgmt data	RMII mgmt data	-
	Direction	I/O	I/O	-
	Configuration	In: Not required Out: SYSTEM_CONFIG46[11,3]=00	In: Not required Out: SYSTEM_CONFIG46[11,3]=01	-
PIO8[4]	Name	MII_MDCI/MII_MDCO	RMII_MDC	-
	Description	MII Mgmg Clock input/output	RMII Mgmg Clock	-
	Direction	I/O	O	-
	Configuration	In: Not required Out: SYSTEM_CONFIG46[12,4]=00	SYSTEM_CONFIG46[12,4]=01	-
PIO8[5]	Name	MII_RXCLK	DVO1_ALPHA[2]	-
	Description	MII receive clock for RXD	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG46[13,5]=01	-
PIO8[6]	Name	MII_RXD[0]	RMII_RXD[0]	-
	Description	MII receive data	RMII receive data	-
	Direction	I	I	-
	Configuration	Not required	Not required	-
PIO8[7]	Name	MII_RXD[1]	RMII_RXD[1]	-
	Description	MII receive data	RMII receive data	-
	Direction	I	I	-
	Configuration	Not required	Not required	-

21.11 PIO9 alternate functions

PIO9 is PIO2 on GPIO standalone block. It provides:

- MII and RMII interfaces
- DVO1 ALPHA coefficient output

Note: During reset PIO9[6, 1:0] are in input mode for mode pin capture.

Table 118. PIO9 alternate functions

PIO9	Config register: SYSTEM_CONFIG47[15:0]			
	Config bus: PIO9_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	**-**
PIO9[0]	Name	MII_RXD[2]	DVO1_ALPHA[3]	-
	Description	MII receive data	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG47[8,0]=01	-
PIO9[1]	Name	MII_RXD[3]	DVO1_ALPHA[4]	-
	Description	MII receive data	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG47[9,1]=01	-
PIO9[2]	Name	MII_TXCLK	DVO1_ALPHA[5]	-
	Description	MII Transmit clock for TXD	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG47[10,2]=01	-
PIO9[3]	Name	MII_COL	DVO1_ALPHA[6]	-
	Description	MII collision detected	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG47[11,3]=01	-

Table 118. PIO9 alternate functions (continued)

PIO9	Config register: SYSTEM_CONFIG47[15:0]			
	Config bus: PIO9_ALTFOP[1:0]_MUX_SEL_BUS[7:0]			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		MII I/F	**RMII I/F, Digital video output 1**	**-**
PIO9[4]	Name	MII_CRS	DVO1_ALPHA[7]	-
	Description	MII carrier sense detected	Second DVO/Alpha output	-
	Direction	I	O	-
	Configuration	Not required	SYSTEM_CONFIG47[12,4]=01	-
PIO9[5]	Name	MII_PHYCLK	RMII_REFCLK	-
	Description	Clock to PHY	RMII REF CLOCK	-
	Direction	O	I/O	-
	Configuration	SYSTEM_CONFIG47[13,5]=00	In: Not required Out: SYSTEM_CONFIG47[13,5]=01	-
PIO9[6]	Name	MII_MDINT	RMII_MDINT	-
	Description	Mgmt data interrupt	RMII Mgmt data interrupt	-
	Direction	I	I	-
	Configuration	Not required	Not required	-
PIO9[7]	Name	HDMI_PLUGIN/MDO_EN	-	-
	Description	HDMI, MDO	-	-
	Direction	I/O	-	-
	Configuration	In: Not required Out: SYSTEM_CONFIG47[15,7]=00	-	-

21.12 PIO10 alternate functions

PIO10 is PIO3 on GPIO standalone block. It provides:

- multichannel digital audio PCM output (AUDDIG1PCMOUT)
- audio S/PDIF output S/PDIF
- stereo digital Audio PCM input (AUDDIG)

Table 119. PIO10 alternate functions

PIO10	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio output 0, SPDIF I/F, Audio digital input 0	**-**	**-**
PIO10[0]	Name	AUDDIG0_PCM_OUT_DATA0	-	-
	Description	PCMOUT 0 - data 0	-	-
	Direction	O	-	-
	Configuration	Not required	-	-
PIO10[1]	Name	AUDDIG0_PCM_OUT_DATA1	-	-
	Description	PCMOUT 0 - data 1	-	-
	Direction	O	-	-
	Configuration	Not required	-	-
PIO10[2]	Name	PCI_IDSEL/AUDDIG0_PCM_OUT_DATA2	-	-
	Description	PCI, PCMOUT 0 - data 2	-	-
	Direction	I/O	-	-
	Configuration	Not required	-	-
PIO10[3]	Name	AUDDIG0_PCM_OUT_CLKIN/CLK	-	-
	Description	PCMOUT 0 - clock	-	-
	Direction	I/O	-	-
	Configuration	Not required	-	-

Table 119. PIO10 alternate functions (continued)

PIO10	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio output 0, SPDIF I/F, Audio digital input 0	**-**	**-**
PIO10[4]	Name	AUDDIG0_PCM_OUT_LRCLK	-	-
	Description	PCMOUT0 - LRCLK	-	-
	Direction	O	-	-
	Configuration	Not required	-	-
PIO10[5]	Name	AUDDIG0_PCM_OUT_SCLK	-	-
	Description	PCMOUT0 - SCLK	-	-
	Direction	O	-	-
	Configuration	Not required	-	-
PIO10[6]	Name	AUD_SPDIF_OUT	-	-
	Description	SPDIF out	-	-
	Direction	O	-	-
	Configuration	Not required	-	-
PIO10[7]	Name	AUDDIG0_PCM_DATAIN/AUDDIG1_PCM_OUT_DATA0	-	-
	Description	PCMIN0/PCMOUT1 - data	-	-
	Direction	I/O	-	-
	Configuration	Not required	-	-

21.13 PIO11 alternate functions

PIO11 is PIO4 on GPIO standalone block. It provides:

- stereo digital audio PCM input (AUD0PCMIN)
- stereo digital audio PCM output (AUD1PCMOUT)

Note: PIO11 alternate function is controlled by SYS_CFG5[29]

Table 120. PIO11 alternate functions

PIO11	**Config register: Not required**			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio input 0	**Genlock**	**-**
PIO11[0]	Name	AUDDIG0_PCM_STRBIN/AUDDIG1_PCM_OUT_LRCLK	-	-
	Description	PCMIN0 - SCLK/PCMOUT1 - LRCLK	-	-
	Direction	I/O	-	-
	Configuration	Not required	-	-
PIO11[1]	Name	AUDDIG0_PCM_LRCLKIN/AUDDIG1_PCM_OUT_SCLK	-	-
	Description	PCMIN0 - LRCLK/PCMOUT1 - SCLK	-	-
	Direction	I/O	-	-
	Configuration	Not required	-	-
PIO11[2]	Name	-	-	-
	Description	-	-	-
	Direction	-	-	-
	Configuration	-	-	-
PIO11[3]	Name	-	-	-
	Description	-	-	-
	Direction	-	-	-
	Configuration	-	-	-

Table 120. PIO11 alternate functions (continued)

PIO11	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		Digital audio input 0	**Genlock**	**-**
PIO11[4]	Name	-		-
	Description	-		-
	Direction	-		-
	Configuration	-		-
PIO11[5]	Name	-	PIXCLK_FROM_PAD	-
	Description	-	Genlock	-
	Direction	-	I	-
	Configuration	-	Not required	-
PIO11[6]	Name	-	VSYNC_FROM_PAD	-
	Description	-	Genlock	-
	Direction	-	I	-
	Configuration	-	Not required	-
PIO11[7]	Name	-	HSYNC_FROM_PAD	-
	Description	-	Genlock	-
	Direction	-	I	-
	Configuration	-	Not required	-

21.14 PIO12 alternate functions

PIO12 is PIO5 on GPIO standalone block. It provides:

- second transport input (TSIN1)
- transport output (TSOUT)
- SSC2 interface with I2C half-duplex modes selectable
- UART2 interface
- USB1 power control
- fourth transport input (TSIN3) (serial only)

Table 121. PIO12 alternate functions

PIO12	Config register: SYSTEM_CONFIG48[23:0]						
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**		**Alternate 4**	**Alternate 5**
		TSIN 1	**TSOUT**	**SSC 2, USB 1 power ctrl**		**TSIN3, UART2, SSC2**	**UART2**
PIO12[0]	Name	TSIN1SER/DATA[7]	TSOUTSER/DATA[7]	SSC2_SCL		SSC2_SCL	UART2_TXD
	Description	TS1 input	TS output	SSC2 serial clock in/out		SSC2 serial clock out	UART
	Direction	I	O	I/O		O	O
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[16,8,0]=001	In: SYSTEM_CONFIG16[12,11]=10 Out: SYSTEM_CONFIG48[16,8,0]=010		SYSTEM_CONFIG48[16,8,0]=011	SYSTEM_CONFIG48[16,8,0]=100
PIO12[1]	Name	TSIN1BYTECLK	TSOUTBYTECLK	SSC2_MTSR	SSC2_MRST	UART2_RXD	-
	Description	TS1 input	TS output	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex	UART	-
	Direction	I	I/O	I/O	I	I	-
	Configuration	SYSTEM_CONFIG4[9]=0	In: Not required Out: SYSTEM_CONFIG48[17,9,1]=001	In: SYSTEM_CONFIG16[10,9]=01 Out: SYSTEM_CONFIG48[17,9,1]=010	SYSTEM_CONFIG16[8,7]=10	Not required	-

Table 121. PIO12 alternate functions (continued)

PIO12	Config register: SYSTEM_CONFIG48[23:0]					
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 1	**TSOUT**	**SSC 2, USB 1 power ctrl**	**TSIN3, UART2, SSC2**	**UART2**
PIO12[2]	Name	TSIN1BYECLKVALID	TSOUTBYTECLKVALID	-	UART2_CTS	-
	Description	TS1 input	TS output	-	UART	-
	Direction	I	O	-	I	-
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[18,10,2]=001	-	Not required	-
PIO12[3]	Name	TSIN1ERROR	TSOUTERROR	-	-	UART2_RTS
	Description	TS1 input	TS output	-	-	UART
	Direction	I	O	-	-	O
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[19,11,3]=001	-	-	SYSTEM_CONFIG48[19,11,3]=100
PIO12[4]	Name	TSIN1PACKETCLK	TSOUTPACKETCLK	-	-	-
	Description	TS1 input	TS output	-	-	-
	Direction	I	O	-	-	-
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[20,12,4]=001	-	-	-
PIO12[5]	Name	TSIN1DATA[6]	TSOUTDATA[6]	USB1_PRT_OVCUR	TSIN3SER/DATA[7]	-
	Description	TS1 input	TS output	USB 1 PRT overcurrent	TS3 input	-
	Direction	I	O	I	I	-
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[21,13,5]=001	SYSTEM_CONFIG4[5]=1	Not required	-
PIO12[6]	Name	TSIN1DATA[5]	TSOUTDATA[5]	USB1_PRT_PWR	TSIN3BYTECLK	-
	Description	TS1 input	TS output	USB 1 PRT power	TS3 input	-
	Direction	I	O	O	I	-
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[22,14,6]=001	SYSTEM_CONFIG48[22,14,6]=010	Not required	-

Table 121. PIO12 alternate functions (continued)

PIO12	Config register: SYSTEM_CONFIG48[23:0]					
	Config bus: PIO12_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 1	**TSOUT**	**SSC 2, USB 1 power ctrl**	**TSIN3, UART2, SSC2**	**UART2**
PIO12[7]	Name	TSIN1DATA[4]	TSOUTDATA[4]	-	TSIN3BYTECLKVALID	-
	Description	TS1 input	TS output	-	TS3 input	-
	Direction	I	O	-	I	-
	Configuration	SYSTEM_CONFIG4[9]=0	SYSTEM_CONFIG48[23,15,7]=001	-	Not required	-

21.15 PIO13 alternate functions

PIO13 is PIO6 on GPIO standalone block. It provides:

- TSIN1
- TSIN0
- fourth transport input (TSIN3) (serial only)
- TSOUT
- PWM
- SSC2 and SSC3 interfaces with I²C half-duplex modes selectable

Table 122. PIO13 alternate functions

PIO13	Config register: SYSTEM_CONFIG49[23:0]					
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 0,1	**TSOUT, SSC 2,3**	**TSOUT, SSC 3**	**TSIN 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[0]	Name	TSIN1DATA[3]	TSOUTDATA[3]	TSOUTDATA[3]	TSIN3ERROR/PWM_OUT0	PWM_OUT0
	Description	TS1 input	TS output	TS output	TS3 input/PWM out	PWM out
	Direction	I	O	O	I/O	O
	Configuration	Not required	SYSTEM_CONFIG49[16,8,0]=001	SYSTEM_CONFIG49[16,8,0]=010	In: Not required Out: SYSTEM_CONFIG49[16,8,0]=011	SYSTEM_CONFIG49[16,8,0]=100
PIO13[1]	Name	TSIN1DATA[2]	TSOUTDATA[2]	TSOUTDATA[2]	TSIN3PACKETCLK/PWM_OUT1	PWM_OUT1
	Description	TS1 input	TS output	TS output	TS3 input	PWM out
	Direction	I	O	O	I/O	O
	Configuration	Not required	SYSTEM_CONFIG49[17,9,1]=001	SYSTEM_CONFIG49[17,9,1]=010	In: Not required Out: SYSTEM_CONFIG49[17,9,1]=011	SYSTEM_CONFIG49[17,9,1]=100

Table 122. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]					
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]					
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 0,1	**TSOUT, SSC 2,3**	**TSOUT, SSC 3**	**TSIN 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[2]	Name	TSIN1DATA[1]	TSOUTDATA[1]	SSC3_SCL/TSOUTDATA[1]	SSC3_SCL	SSC3_SCL
	Description	TS1 input	TS output	SSC3 input/TS output	SSC3 output	SSC3 output
	Direction	I	O	I/O	O	O
	Configuration	Not required	SYSTEM_CONFIG49[18,10,2]=001	In: Not required Out: SYSTEM_CONFIG49[18,10,2]=010	SYSTEM_CONFIG49[18,10,2]=011	SYSTEM_CONFIG49[18,10,2]=100
PIO13[3]	Name	TSIN1DATA[0]	TSOUTDATA[0]	SSC3_MTSR/SSC3_MRST/TSOUTDATA[0]	SSC3_MTSR	SSC3_MTSR
	Description	TS1 input	TS output	SSC3 Data bit: master transmit/slave receive, full duplex/TS output	SSC3 Data bit: master receive/slave transmit, full duplex	
	Direction	I	O	I/O	O	O
	Configuration	Not required	SYSTEM_CONFIG49[19,11,3]=001	In: SYSTEM_CONFIG16[17,16]=01/ SYSTEM_CONFIG16[15,14]=10 Out: SYSTEM_CONFIG49[19,11,3]=010	SYSTEM_CONFIG49[19,11,3]=011	SYSTEM_CONFIG49[19,11,3]=100
PIO13[4]	Name	TSIN0SER/DATA[7]	SSC2_SCL	SSC2_SCL	-	-
	Description	TS0 input	SSC2 serial clock in/out	SSC2 serial clock out	-	-
	Direction	I	I/O	O	-	-
	Configuration	Not required	In: SYSTEM_CONFIG16[12,11]=11 Out: SYSTEM_CONFIG49[20,12,4]=001	SYSTEM_CONFIG49[20,12,4]=010	-	-

Table 122. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]						
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**		**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 0,1	**TSOUT, SSC 2,3**		**TSOUT, SSC 3**	**TSIN 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[5]	Name	TSIN0BYTECLK	SSC2_MTSR	SSC2_MRST	SSC2_MRST	-	-
	Description	TS input	SSC2 Data bit: master transmit/slave receive, full duplex	SSC2 Data bit: master receive/slave transmit, full duplex		-	-
	Direction	I/O	I/O	I	O	-	-
	Configuration	In: Not required Out: SYSTEM_CONFIG49[21,13,5]=000	In SYSTEM_CONFIG16[10,9]=10/11 Out: SYSTEM_CONFIG49[21,13,5]=001	SYSTEM_CONFIG16[8,7]=11	SYSTEM_CONFIG49[21,13,5]=010	-	-
PIO13[6]	Name	TSIN0BYTECLKVALID	SSC3_SCL		SSC3_SCL	-	-
	Description	TS0 input	SSC3 serial clock in/out		SSC3 serial clock out	-	-
	Direction	I	I/O		O	-	-
	Configuration	Not required	In: SYSTEM_CONFIG16[19,18]=10/11 Out: SYSTEM_CONFIG49[22,14,6]=001		SYSTEM_CONFIG49[22,14,6]=010	-	-

Table 122. PIO13 alternate functions (continued)

PIO13	Config register: SYSTEM_CONFIG49[23:0]						
	Config bus: PIO13_ALTFOP[2:0]_MUX_SEL_BUS[7:0]						
PIN	**Parameter**	**Alternate 1**	**Alternate 2**		**Alternate 3**	**Alternate 4**	**Alternate 5**
		TSIN 0,1	**TSOUT, SSC 2,3**		**TSOUT, SSC 3**	**TSIN 3, PWM 0,1**	**PWM 0,1, SSC3**
PIO13[7]	Name	TSIN0ERROR	SSC3_MTSR	SSC3_MRST	SSC3_MRST	-	-
	Description	TS0 input	SSC3 Data bit: master transmit/slave receive, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex	SSC3 Data bit: master receive/slave transmit, full duplex	-	-
	Direction	I	I/O	I	O	-	-
	Configuration	Not required	In: SYSTEM_CONFIG16[17,16]=10/11 Out: SYSTEM_CONFIG49[23,15,7]=001	SYSTEM_CONFIG16[15,14]=11	SYSTEM_CONFIG49[23,15,7]=010	-	-

21.16 PIO14 alternate functions

PIO14 is PIO7 on GPIO standalone block. It provides:

- TSIN0
- TSIN2 (serial only)
- USB2 power control

Table 123. PIO14 alternate functions

PIO14	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		TSIN 0	**TSIN 2, USB 2 power ctrl**	**-**
PIO14[0]	Name	TSIN0PACKETCLK	-	-
	Description	TS 0 input	-	-
	Direction	I	-	-
	Configuration	Not required	-	-
PIO14[1]	Name	TSIN0DATA[6]	TSIN2SER/DATA[7]	-
	Description	TS 0 input	TS 2 input	-
	Direction	I	I	-
	Configuration	Not required	SYSTEM_CONFIG4[10]=1	-
PIO14[2]	Name	TSIN0DATA[5]	TSIN2BYTECLK	-
	Description	TS 0 input	TS 2 input	-
	Direction	I	I	-
	Configuration	Not required	In: SYSTEM_CONFIG4[10]=1	-
PIO14[3]	Name	TSIN0DATA[4]	TSIN2BYTECLKVALID	-
	Description	TS 0 input	TS 2 input	-
	Direction	I	I	-
	Configuration	Not required	SYSTEM_CONFIG4[10]=1	-

Table 123. PIO14 alternate functions (continued)

PIO14	Config register: Not required			
	Config bus: Not required			
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**
		TSIN 0	**TSIN 2, USB 2 power ctrl**	**-**
PIO14[4]	Name	TSIN0DATA[3]	TSIN2ERROR	-
	Description	TS 0 input	TS 2 input	-
	Direction	I	I	-
	Configuration	Not required	SYSTEM_CONFIG4[10]=1	-
PIO14[5]	Name	TSIN0DATA[2]	TSIN2PACKETCLK	-
	Description	TS 0 input	TS 2 input	-
	Direction	I	I	-
	Configuration	Not required	SYSTEM_CONFIG4[10]=1	-
PIO14[6]	Name	TSIN0DATA[1]	USB2_PRT_OVCUR	-
	Description	TS 0 input	USB2 PRT overcurrent	-
	Direction	I	I	-
	Configuration	Not required	SYSTEM_CONFIG4[10]=1	-
PIO14[7]	Name	TSIN0DATA[0]	USB2_PRT_PWR	-
	Description	TS 0 input	USB2 PRT power	-
	Direction	I	O	-
	Configuration	Not required	Not required	-

21.17 PIO15 alternate functions

PIO15 is PIO8 on GPIO standalone block. It provides:

- SPI boot interface
- EMI SS arbiter signals/PCI support
- PCI interface

Table 124. PIO15 alternate functions

PIO15	Config register: SYSTEM_CONFIG50[15:0]				
	Config bus: PIO15_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Serial peripheral I/F	**Transport stream input 1**	**PCI I/F, EMI I/F**	**-**
PIO15[0]	Name	SPIBOOT_CLOCK	TSIN1PACKETCLK	-	-
	Description	SPI	TS1 input	-	-
	Direction	O	I	-	-
	Configuration	SYSTEM_CONFIG50[8,0]=00	SYSTEM_CONFIG4[9]=1	-	-
PIO15[1]	Name	SPIBOOT_DATA_OUT	TSIN1BYTECLK	-	-
	Description	SPI	TS1 input	-	-
	Direction	O	I	-	-
	Configuration	SYSTEM_CONFIG50[9,1]=00	SYSTEM_CONFIG4[9]=1	-	-
PIO15[2]	Name	SPIBOOT_CS	TSIN1BYTECLKVALID	EMI_SS_BUS_FREE_ACCESSPEND/EMI_SS_BUS_FREE_OUT	EMI_SS_BUS_FREE_OUT
	Description	SPI	TS1 input	EMI I/F	EMI I/F
	Direction	O	I	I/O	O
	Configuration	SYSTEM_CONFIG50[10,2]=00	SYSTEM_CONFIG4[9]=1	In: Not required Out: SYSTEM_CONFIG50[10,2]=10	SYSTEM_CONFIG50[10,2]=11

Table 124. PIO15 alternate functions (continued)

PIO15	Config register: SYSTEM_CONFIG50[15:0]				
	Config bus: PIO15_ALTFOP[1:0]_MUX_SEL_BUS[7:0]				
PIN	**Parameter**	**Alternate 1**	**Alternate 2**	**Alternate 3**	**Alternate 4**
		Serial peripheral I/F	**Transport stream input 1**	**PCI I/F, EMI I/F**	**-**
PIO15[3]	Name	SPIBOOT_DATA_IN	TSIN1ERROR	PCI_INT_FROM_DEVICE[0]/PCI_INT_TO_HOST	PCI_INT_TO_HOST
	Description	SPI	TS1 input	PCI host/device	PCI Host
	Direction	I	I	I/O	O
	Configuration	Not required	SYSTEM_CONFIG4[9]=1	In: SYSTEM_CONFIG5[27]=1 Out: SYSTEM_CONFIG50[11,3]=10	SYSTEM_CONFIG50[11,3]=11
PIO15[4]	Name	-	TSIN1SER/DATA[7]	PCI_SYSTEM_ERROR	PCI_SYSTEM_ERROR
	Description	-	TS1 input	PCI Host/device	PCI Host/device
	Direction	-	I	I/O	O
	Configuration	-	SYSTEM_CONFIG4[9]=1	In: Not required Out: SYSTEM_CONFIG50[12,4]=10	SYSTEM_CONFIG50[12,4]=11
PIO15[5]	Name	-	-	PCI_LOCK_IN	-
	Description	-	-	PCI Host/device	-
	Direction	-	-	I	-
	Configuration	-	-	SYSTEM_CONFIG5[25]=1	-
PIO15[6]	Name	-	-	PCI_PME_IN	-
	Description	-	-	PCI Host/device	-
	Direction	-	-	I	-
	Configuration	-	-	Not required	-
PIO15[7]	Name	-	-	PCI_RESETN_FROM_HOST_TO_DEVICE	-
	Description	-	-	PCI Host/device	-
	Direction	-	-	I	-
	Configuration	-	-	Not required	-

21.18 PIO16 alternate functions

PIO16 is PIO9 on GPIO standalone block. It provides:

- MPEG recovered clock

Note: During reset PIO16[6:0] is in input mode for mode pin capture.

Table 125. PIO16 alternate functions

PIO16	Config register: Not required		
	Config bus: Not required		
		Alternate 1	Alternate 2
PIO16[0]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[1]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[2]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[3]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[4]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED

Table 125. PIO16 alternate functions (continued)

PIO16	Config register: Not required		
	Config bus: Not required		
		Alternate 1	**Alternate 2**
PIO16[5]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[6]	Name	RESERVED	RESERVED
	Description	RESERVED	RESERVED
	Direction	RESERVED	RESERVED
	Configuration	RESERVED	RESERVED
PIO16[7]	Name	MPEG_RECOVERY_CLOCK	
	Description	MPEG recovered clock	
	Direction	O	
	Configuration	Not required	

22 Licenses

Supply of this product does not convey a license under the relevant intellectual property of the companies mentioned in this chapter nor imply any right to use this intellectual property in any finished end-user or ready to use final product. An independent license for such use is required and can be obtained by contacting the company or companies concerned.

Once the license is obtained, a copy must be sent to STMicroelectronics.

The details of all the features requiring licenses are not provided within the datasheet and register manual. They are provided only after a copy of the license has been received by STMicroelectronics.

The features requiring licenses include:

CSS

CSS DVD Copy Protection is intellectual property of Matsushita Electronics Industrial Co. The CSS DVD Copy Protection license allows the use of the CSS decryption cell embedded in the STi7197.

For all details, contact Matsushita at:
Matsushita Electronics Industrial Co. LTD, CSS Interim License Organization, 1006 Kadoma, Kadoma-Shi, Osaka 571-8503 JAPAN

Dolby® Digital EX, Pro Logic® II, MLP Lossless™

Dolby Digital, Pro Logic and MLP Lossless are intellectual properties of Dolby Labs. The Dolby Digital, Pro Logic or MLP Lossless license allows the use of the corresponding decoder embedded in the STi7197.

Two types of license exist: S license must be obtained for samples (up to 25 units). P license must be obtained for production.

For all details, contact Dolby Labs at:
Dolby Labs, 100 Potrero Avenue, San Francisco, CA 94103, USA

Rovi™

Compliant Devices can only be sold or distributed to Authorized Buyers.

In the event that the Rovi variant of this Device is supplied, attention is drawn to the following notice:

This device is protected by U.S. patent numbers 6,516,132; 5,583,936; 6,836,549; and 7,050,698 and other intellectual property rights. The use of Rovi Corporation's copy protection technology in the device must be authorized by Rovi Corporation and is intended for home and other limited pay-per-view uses only, unless otherwise authorized in writing by Rovi Corporation. Reverse engineering or disassembly is prohibited.

Dwight Cavendish

The STi7197 is enabled with the Dwight Cavendish copy protection process. Activation of the Dwight Cavendish copy protection is subject to Dwight Cavendish Intellectual Property Rights and is not permitted otherwise than with an express written licence from Dwight Cavendish.

For more details, click *www.dwightcav.com*

TruSurround XT™, CircleSurround™ II

The CircleSurround II, TruSurround XT and SRS technology rights incorporated in this chip are owned by SRS Labs, a U.S. corporation and licensed to ST Microelectronics. Purchasers of this chip, who use the SRS technology incorporated herein, must sign a license for use of the chip and display of the SRS trademarks. Any product using the SRS technology incorporated in this chip must be sent to SRS Labs for review. Circle Surround II, TruSurround XT and SRS are protected under U.S. and foreign patents issued and/or pending.

Neither the purchase of this chip, nor the corresponding sale of audio enhancement equipment conveys the right to sell commercialized recordings made with any SRS technology. SRS requires all set makers to comply with all rules and regulations as outlined in the SRS Trademark Usage Manual.

For all details, contact SRS Labs at:
SRS Labs Inc., 2909 Daimler Street, Santa Ana, CA 92705 USA

DTS® (ES, 96/24, Neo)

DTS ES, DTS 96/24 and DTS Neo are intellectual properties of Digital Theater Systems Inc. The DTS licenses allow the use of the corresponding decoder executed in the STi7197.

For all details, contact Digital Theater Systems Inc at:
DTS, 5171 Clareton Drive, Agoura Hills, CA 91301, USA

CPRM/CPPM

CPRM/CPPM technology is intellectual property of 4C Entity. The CPRM/CPPM license allows the use of the CPRM/CPPM technology embedded in the STi7197.

For all details, contact 4C Entity at:
4C Entity, LLC, 225 B Cochrane Circle, Morgan Hill, CA 95037, USA

Windows Media® (audio [WMA] and video [WMV])

Windows Media is intellectual property of Microsoft Corporation. The Windows Media license allows the use of the Windows Media audio and video decoders executed in the STi7197.

For all details, contact Microsoft at:
Microsoft Corporation, One Microsoft Way, Redmond, WA 98052-6399, USA

USB (Universal Serial Bus)

USB is intellectual property of USB-IF. The USB license gives the right to display the certified USB logo with a product when the product has passed USB-IF compliance testing for product quality.

For all details, contact USB-IF:
USB Implementers Forum, Inc., 5440 SW Westgate Drive, Suite 217, Portland, OR 97221, USA

HDMI™ (High-definition multimedia interface™)

HDMI and High-definition multimedia interface are intellectual properties of HDMI Licensing, LLC. The HDMI license allows the use of HDMI in the STi7197.

For all details, contact HDMI Licensing, LLC at:
1060 E. Arques Avenue, Suite 100, Sunnyvale, CA 94085, USA

HDCP

HDCP is an intellectual property of Digital Content Protection, LLC. The HDCP license allows the use of HDCP in the STi7197.

For all details, contact Digital Content Protection, LLC at:
C/O Intel Corporation, Stephen Balogh, JF2-55, 2111 NE 25th Ave, Hillsboro, OR 97124

AACS

AACS is an intellectual property of Koninklijke Philips Electronics N.V.

For all details, contact AACS LA, LLC at:
c/o AACS Administration, 5440 SW Westgate Drive, Suite 217, Portland, Oregon 97221

AAC

AAC is an intellectual property of Fraunhofer Institut Integrierte Schaltungen.
For all details, contact Fraunhofer Institute IIS, Am Wolfsmantel 33, 91058 Erlangen, Germany.

23 Revision history

Table 126. Document revision history

Date	Revision	Changes
13-Aug-2010	A	Initial release.
26-Jul-2011	2	– Updated *Section 2.8: Audio/video outputs on page 12* regarding HDMI. – Added *Section 2.13: HDMI interface on page 14*. – Updated equation in *Section 13.4.3: Clock frequency change on page 254*. – Updated *Figure 4: Transport subsystem block diagram on page 18* for TSOUT. – Updated the ESD values. Updated the $VDD3V3_{max}$ minimum and maximum voltages to -0.5 V and 4.0 V, respectively, in *Table 73 on page 342*. – Updated the operating condition values in *Table 74 on page 342*. – Updated frequency in extended operating mode to 600 MHz and DMIPS to 1100 on *page 13*. – Updated the MII interface pin names in *Table 24: MII interface pin mapping on page 182*. – Updated the RMII interface pin names in *Table 25: RMII interface pin mapping on page 183*. – Updated the MII and RMII interface names in *Table 39: STi7197 Ethernet muxing details (in standard mode) on page 204*. – Updated the MII and RMII interface names in *Table 70: Mode pins mapping on page 262*. – Updated the MII and RMII interface pin names in *Chapter 21: Alternate functions on PIO on page 364*. – Added *Chapter 5: Ordering information on page 37*. – Updated AK16, AK17, AM16 and AL16 pin names in *Figure 15* and *Figure 16*, Table 5 on *page 151* and *page 152*, and Table 14 on *page 169*.

CONFIDENTIALITY OBLIGATIONS:

This document contains sensitive information.
Its distribution is subject to the signature of a Non-Disclosure Agreement (NDA).
It is classified "**CONFIDENTIAL**".

At all times you should comply with the following security rules
(Refer to NDA for detailed obligations):

Do not copy or reproduce all or part of this document
Keep this document locked away

Further copies can be provided on a "need to know basis", please contact your local ST sales office.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com