



N-Channel 30-V (D-S), 175°C MOSFET PWM Optimized

CHARACTERISTICS

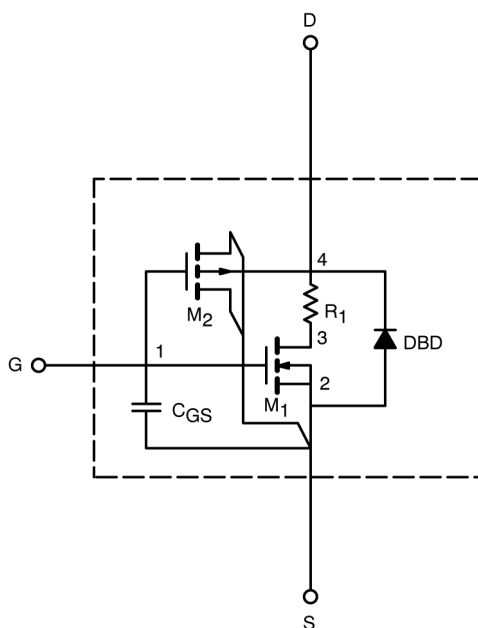
- N-Channel Vertical DMOS
- Macro Model (Model Subcircuit Schematic)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model schematic is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-to-5V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPICE Device Model SUP/ SUB70N03-09P

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SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1.67	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	621	A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 30\ \text{A}$	0.007	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 20\ \text{A}$	0.011	
		$V_{GS} = 10\ \text{V}$, $I_D = 30\ \text{A}$, 125°C	0.0108	
		$V_{GS} = 10\ \text{V}$, $I_D = 30\ \text{A}$, 175°C	0.0127	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 30\ \text{A}$	51	S
Diode Forward Voltage ^a	V_{SD}	$I_F = 70\ \text{A}$, $V_{GS} = 0\ \text{V}$	0.92	V
Dynamic^b				
Input Capacitance	C_{iss}	$V_{GS} = 0\ \text{V}$, $V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$	2681	pf
Output Capacitance	C_{oss}		664	
Reverse Transfer Capacitance	C_{rss}		310	
Total Gate Charge ^c	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 70\ \text{A}$	46	nC
Gate-Source Charge ^c	Q_{gs}		8.5	
Gate-Drain Charge ^c	Q_{gd}		11	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 0.21\ \Omega$ $I_D \equiv 70\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 2.5\ \Omega$	13	ns
Rise Time ^c	t_r		11	
Turn-Off Delay Time ^c	$t_{d(off)}$		35	
Fall Time ^c	t_f		12	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	35	

Notes

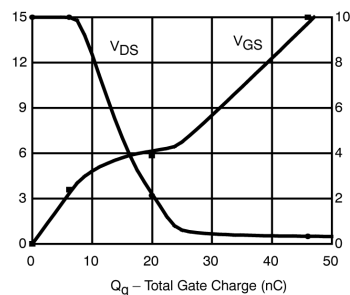
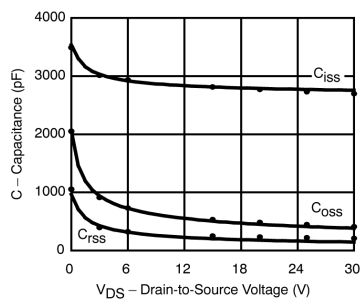
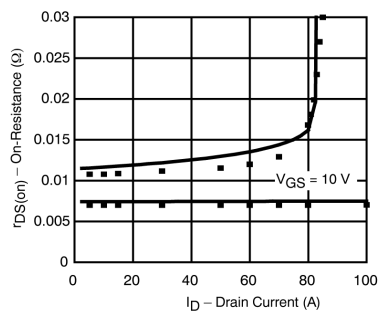
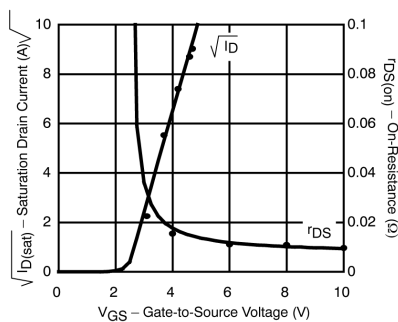
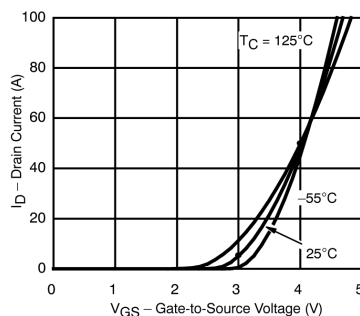
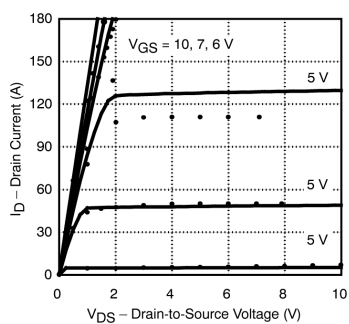
- Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature



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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.