

## N-Channel 30-V (D-S) MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a, e</sup>	$Q_g$ (Typ)
30	0.0038 at $V_{GS} = 10$ V	98	82 nC
	0.0044 at $V_{GS} = 4.5$ V	98	

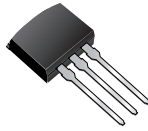
### FEATURES

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested
- Compliant to RoHS Directive 2011/65/EU

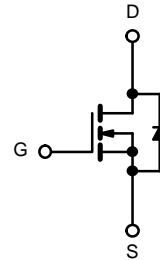

**RoHS**  
 COMPLIANT

### APPLICATIONS

- OR-ing
- Server
- DC/DC

 I<sup>2</sup>PAK  
 (TO-262)

**VBNC1303**

 D<sup>2</sup>PAK  
 (TO-263)

**VBL1303**


N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	98 <sup>a, e</sup>	A
	$T_C = 70$ °C		98 <sup>e</sup>	
	$T_A = 25$ °C		28.8 <sup>b, c</sup>	
	$T_A = 70$ °C		27 <sup>b, c</sup>	
Pulsed Drain Current		$I_{DM}$	300	
Avalanche Current Pulse		$I_{AS}$	36	
Single Pulse Avalanche Energy		$E_{AS}$	64.8	V
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	90 <sup>a, e</sup>	A
	$T_A = 25$ °C		3.13 <sup>b, c</sup>	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	250 <sup>a</sup>	W
	$T_C = 70$ °C		175	
	$T_A = 25$ °C		3.75 <sup>b, c</sup>	
	$T_A = 70$ °C		2.63 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

### THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>b, d</sup>	$t \leq 10$ sec	$R_{thJA}$	32	40	°C/W
Maximum Junction-to-Case	Steady State	$R_{thJC}$	0.5	0.6	

Notes:

 a. Based on  $T_C = 25$  °C.

b. Surface mounted on 1" x 1" FR4 board.

 c.  $t = 10$  sec.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

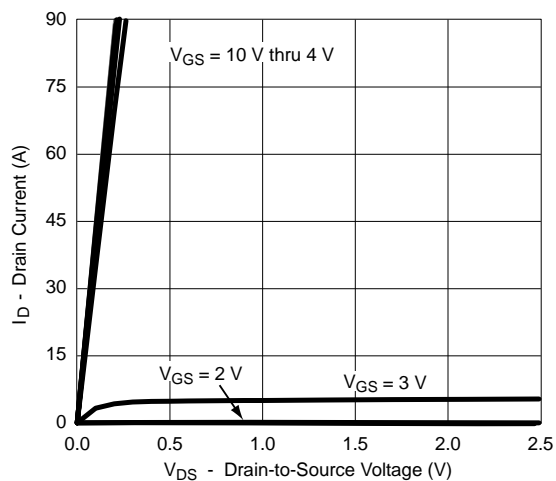
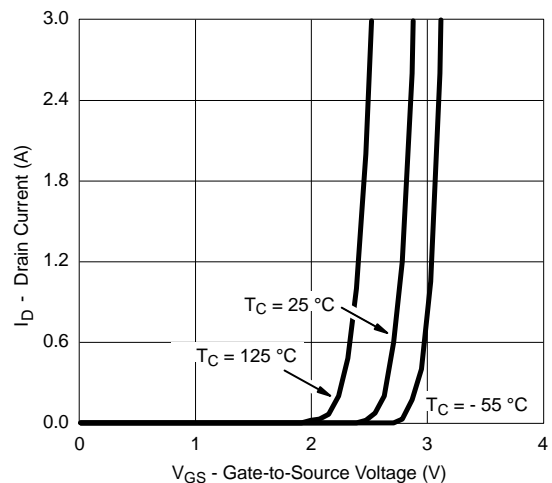
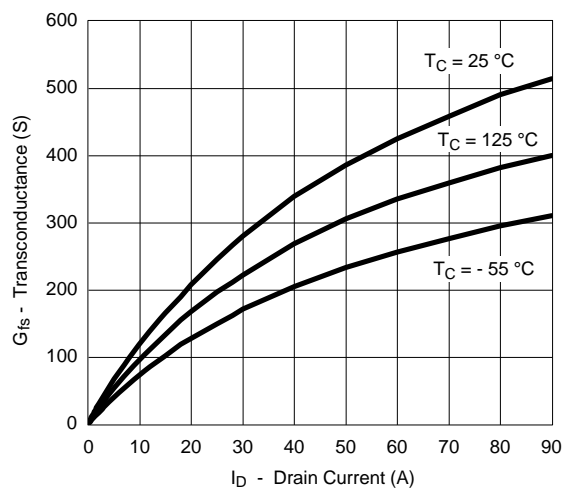
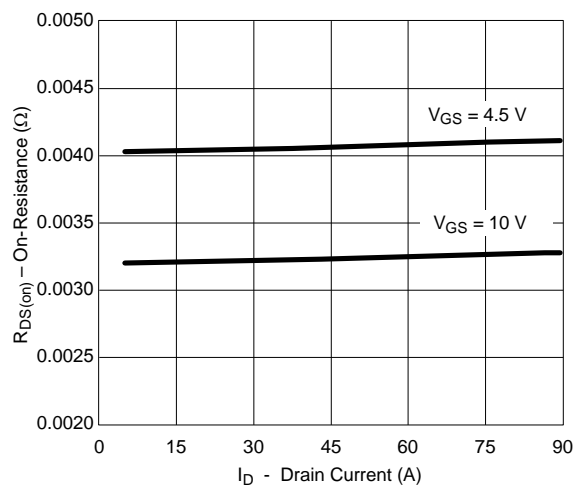
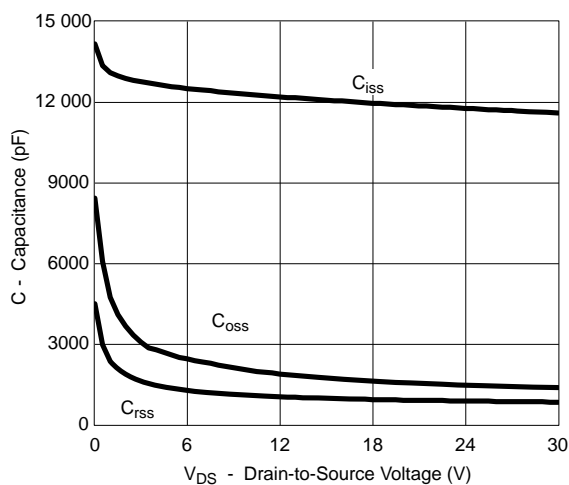
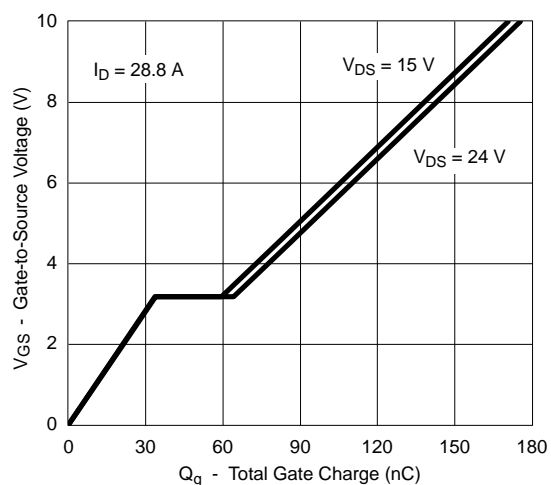
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA		35		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 7.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5		2.5	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	90			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 28.8 A		0.0024	0.0038	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 27 A		0.0027	0.0044	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 28.8 A		160		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 0 V, f = 1 MHz		12065		pF
Output Capacitance	C <sub>oss</sub>			1725		
Reverse Transfer Capacitance	C <sub>rss</sub>			970		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 28.8 A		171	257	nC
		V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 28.8 A		81.5	123	
Gate-Source Charge	Q <sub>gs</sub>			34		
Gate-Drain Charge	Q <sub>gd</sub>			29		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.4	2.1	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.625 Ω I <sub>D</sub> ≅ 24 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		18	27	ns
Rise Time	t <sub>r</sub>			11	17	
Turn-Off Delay Time	t <sub>d(off)</sub>			70	105	
Fall Time	t <sub>f</sub>			10	15	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.67 Ω I <sub>D</sub> ≅ 22.5 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		55	83	
Rise Time	t <sub>r</sub>			180	270	
Turn-Off Delay Time	t <sub>d(off)</sub>			55	83	
Fall Time	t <sub>f</sub>			12	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			90	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				90	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 22 A		0.8	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C		52	78	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			70.2	105	nC
Reverse Recovery Fall Time	t <sub>a</sub>			27		ns
Reverse Recovery Rise Time	t <sub>b</sub>			25		

Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

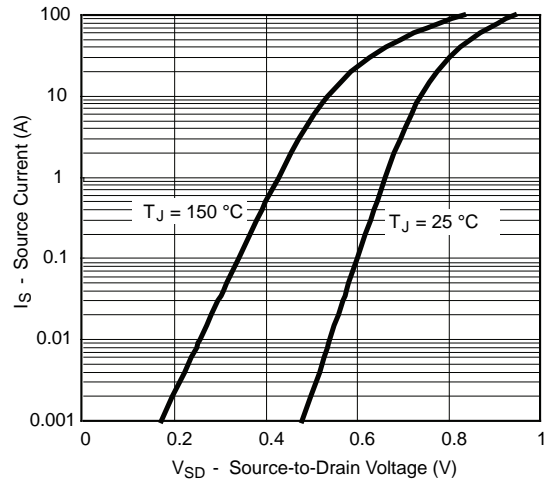
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**Transconductance**

 **$R_{DS(on)}$  vs. Drain Current**

**Capacitance**

**Gate Charge**

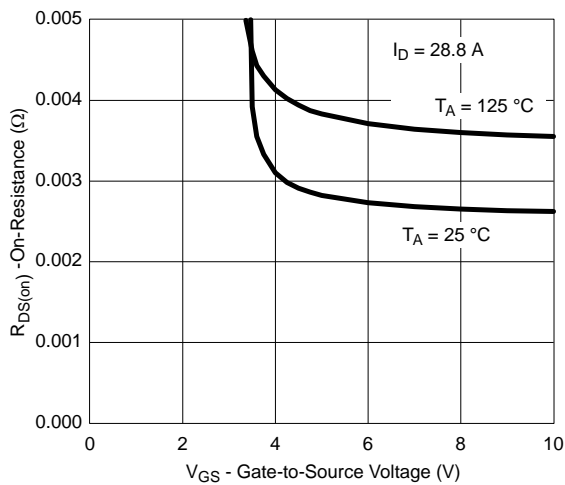
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



On-Resistance vs. Junction Temperature



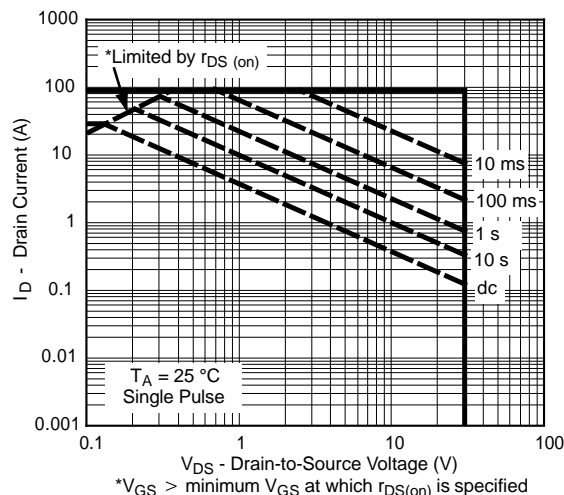
Forward Diode Voltage vs. Temperature



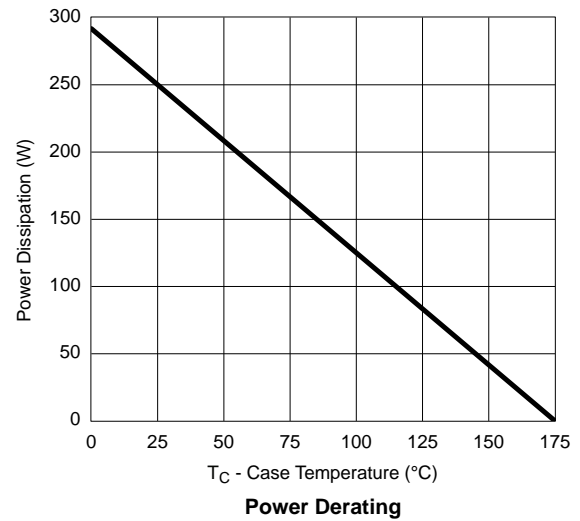
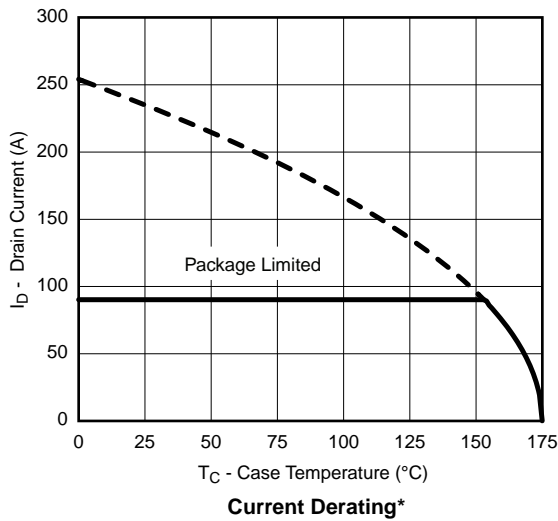
$R_{DS(on)}$  vs.  $V_{GS}$  vs. Temperature



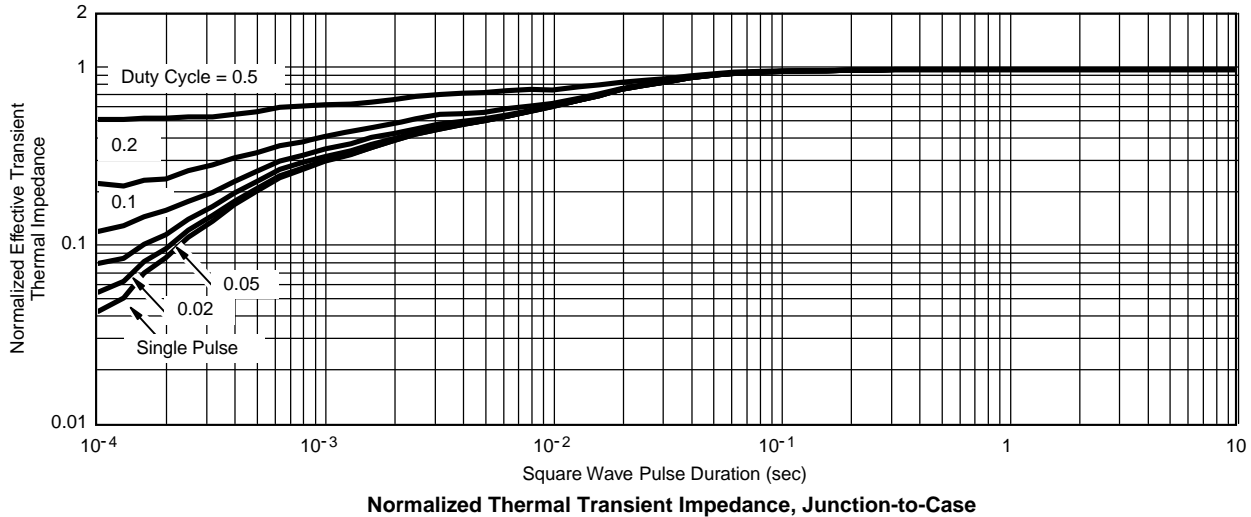
Threshold Voltage

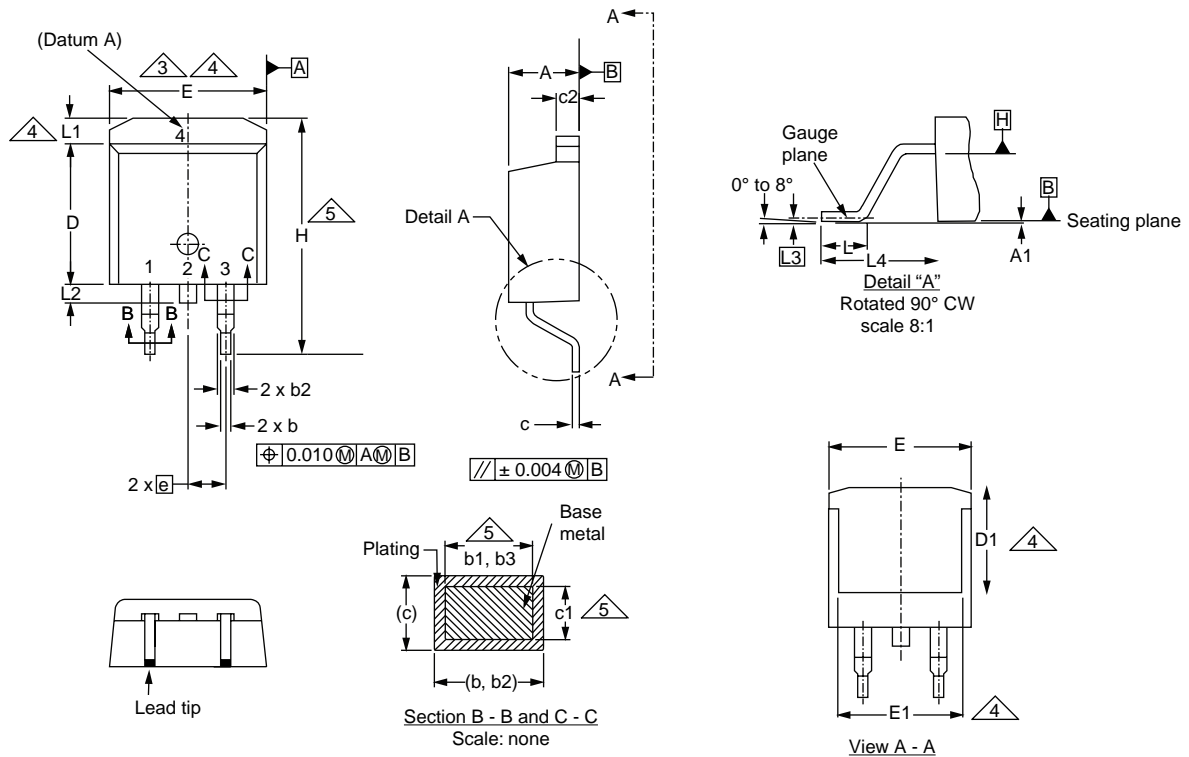


\* $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified  
**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)


\*The power dissipation  $P_D$  is based on  $T_{J(max)} = 175$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

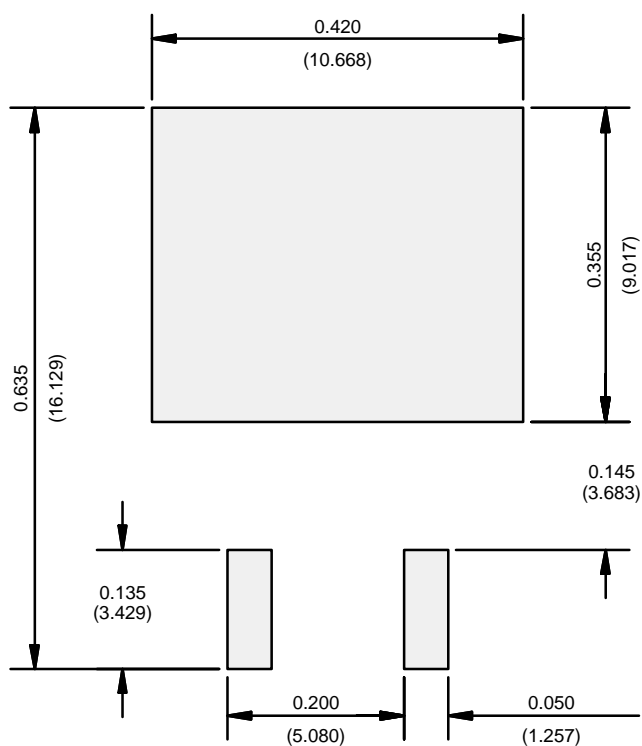


**TO-263AB (HIGH VOLTAGE)**

ECN: S-82110-Rev. A, 15-Sep-08  
 DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**

Recommended Minimum Pads  
Dimensions in Inches/(mm)

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