



New Product

SUD50N03-06AP

Vishay Siliconix

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ)
30	0.0057 @ $V_{GS} = 10$ V	90	30
	0.0078 @ $V_{GS} = 4.5$ V	77	

FEATURES

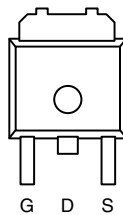
- TrenchFET® Power MOSFET
- Optimized for Low-Side Synchronous Rectifier Operation
- 100% R_g Tested



APPLICATIONS

- DC/DC Converters
- Synchronous Rectifiers

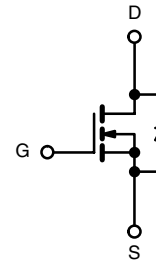
TO-252



Top View

Drain Connected to Tab

Ordering Information: SUD50N03-06AP—E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	90 ^{a, e}	A
	$T_C = 70^\circ\text{C}$		75 ^{a, e}	
	$T_A = 25^\circ\text{C}$		30 ^{b, c}	
	$T_A = 70^\circ\text{C}$		25 ^{b, c}	
Pulsed Drain Current		I_{DM}	100	
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	I_S	55 ^{a, e}	
	$T_A = 25^\circ\text{C}$		6.7 ^{b, c}	
Avalanche Current Pulse		I_{AS}	45	mJ
Single Pulse Avalanche Energy		E_{AS}	101	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	83	W
	$T_C = 70^\circ\text{C}$		58	
	$T_A = 25^\circ\text{C}$		10 ^{b, c}	
	$T_A = 70^\circ\text{C}$		7 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	$t \leq 10$ sec	R_{thJA}	12	15	$^\circ\text{C/W}$
Maximum Junction-to-Case	Steady State	R_{thJC}	1.5	1.8	

Notes:

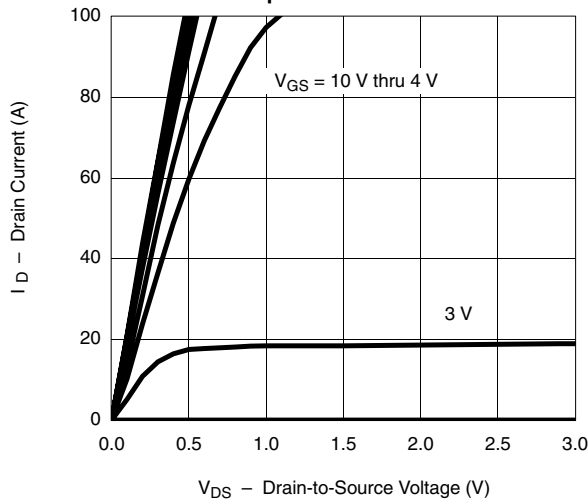
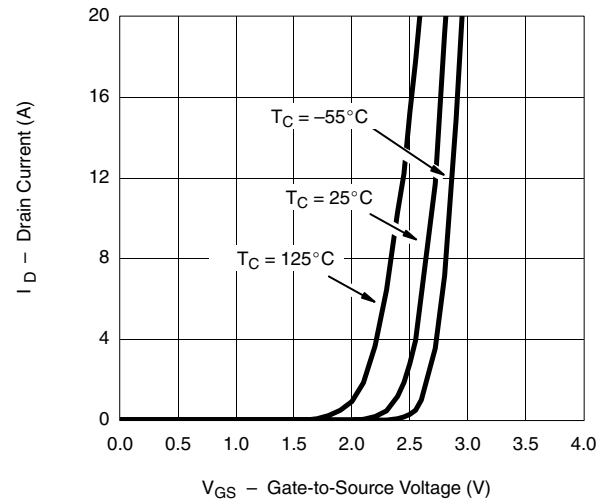
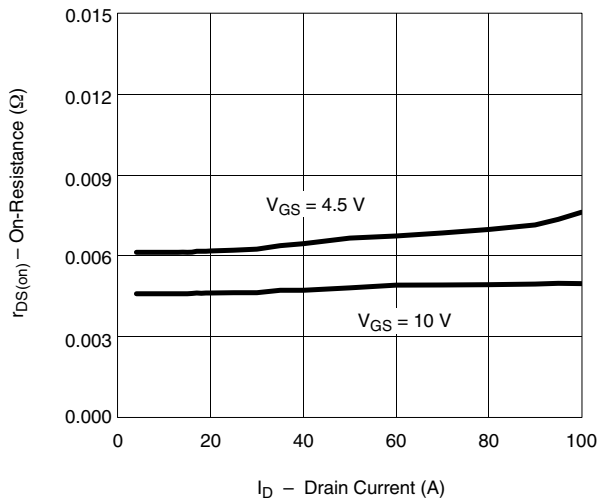
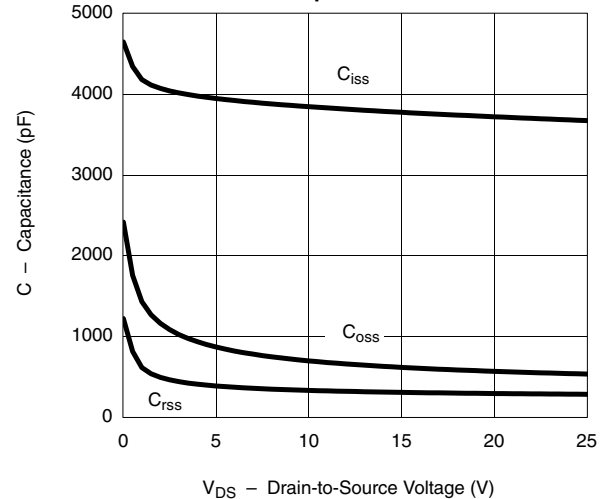
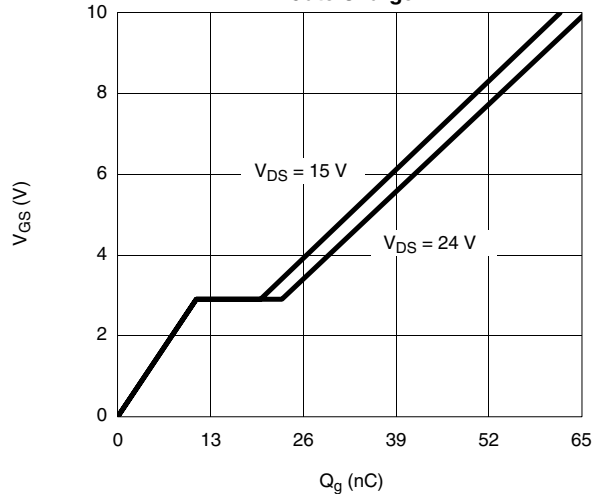
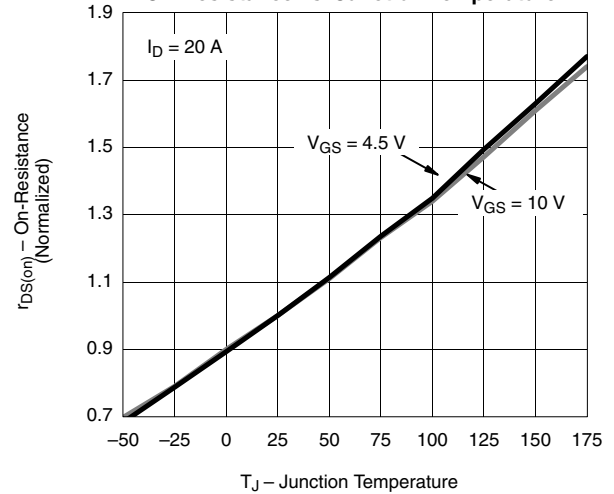
- Based on $T_C = 25^\circ\text{C}$.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ sec
- Maximum under steady state conditions is 50°C/W .
- Calculated based on maximum junction temperature. Package limitation current is 50 A.

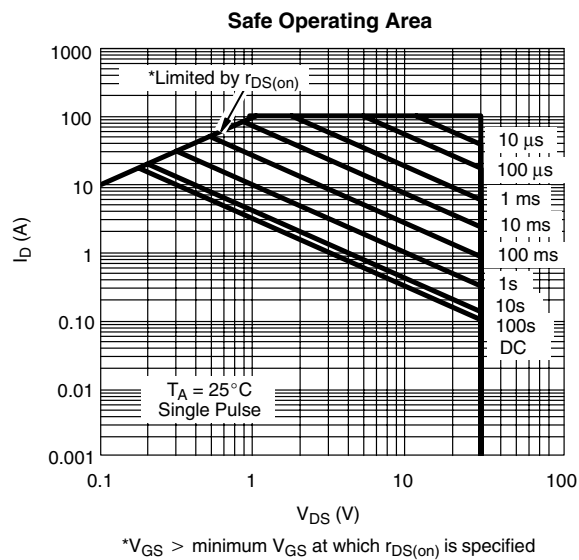
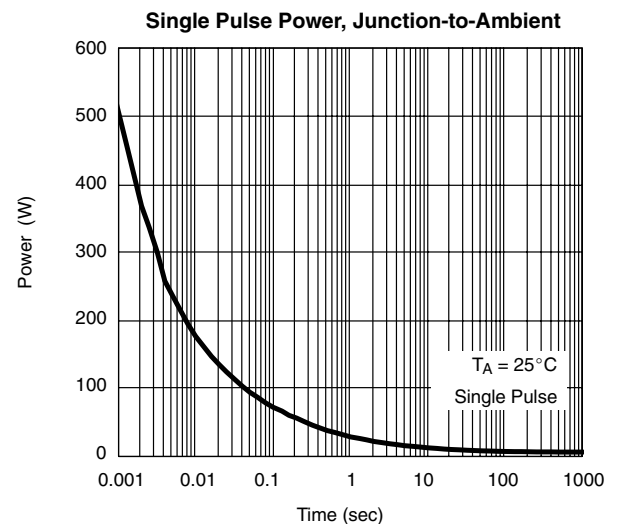
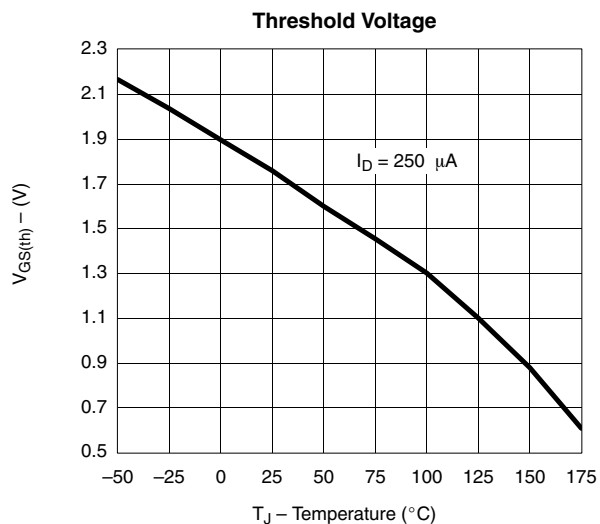
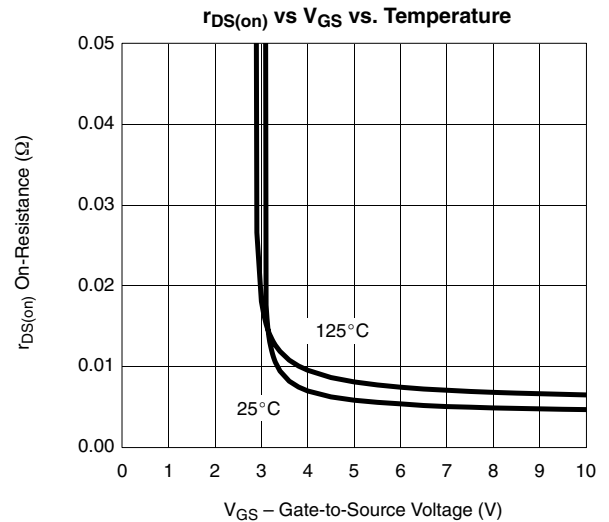
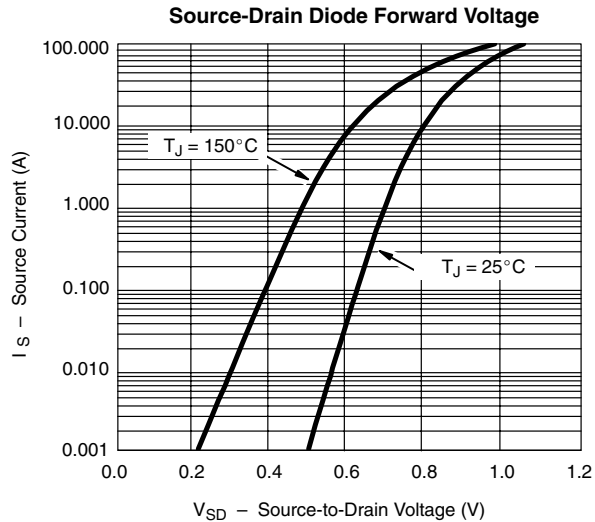
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		25		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			− 6.3		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0046	0.0057	Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.0062	0.0078	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 30 A		70		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		3800		pF
Output Capacitance	C _{oss}			615		
Reverse Transfer Capacitance	C _{rss}			305		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 30 A		62	95	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 25 A		30	45	
Gate-Source Charge	Q _{gs}			11		
Gate-Drain Charge	Q _{gd}			9		
Gate Resistance	R _g	f = 1 MHz		0.9	1.4	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 0.5 Ω I _D ≅ 30 A, V _{GEN} = 10 V, R _g = 1 Ω		12	18	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			30	45	
Fall Time	t _f			8	12	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 0.6 Ω I _D ≅ 25 A, V _{GEN} = 4.5 V, R _g = 1 Ω		26	40	
Rise Time	t _r			230	345	
Turn-Off Delay Time	t _{d(off)}			25	40	
Fall Time	t _f			9	14	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			55 ^c	A
Pulse Diode Forward Current ^a	I _{SM}				100	
Body Diode Voltage	V _{SD}	I _S = 6.7 A		0.9	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 6.7 A, di/dt = 100 A/μs, T _J = 25 °C		65	100	ns
Body Diode Reverse Recovery Charge	Q _{rr}			38	60	nC
Reverse Recovery Fall Time	t _a			50		ns
Reverse Recovery Rise Time	t _b			15		

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Calculated based on maximum junction temperature. Package limitation current is 50 A.

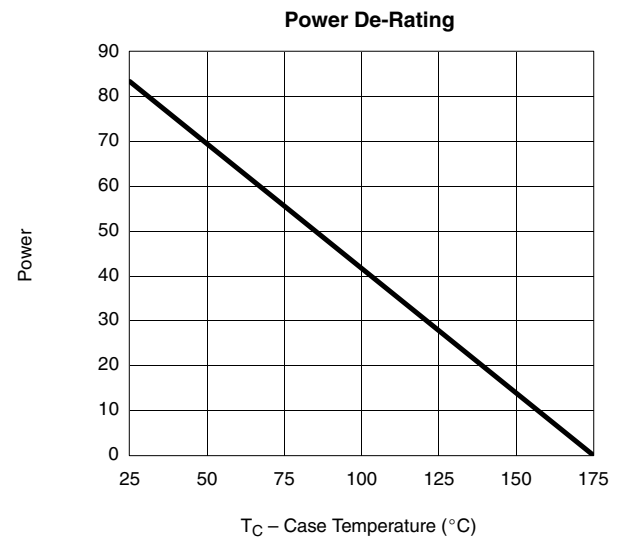
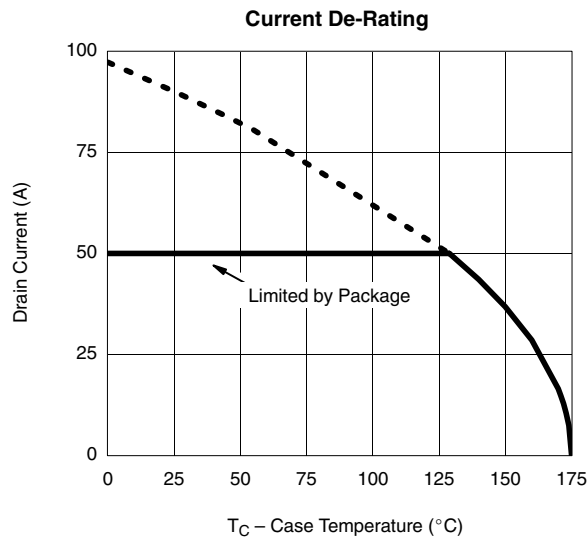
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)


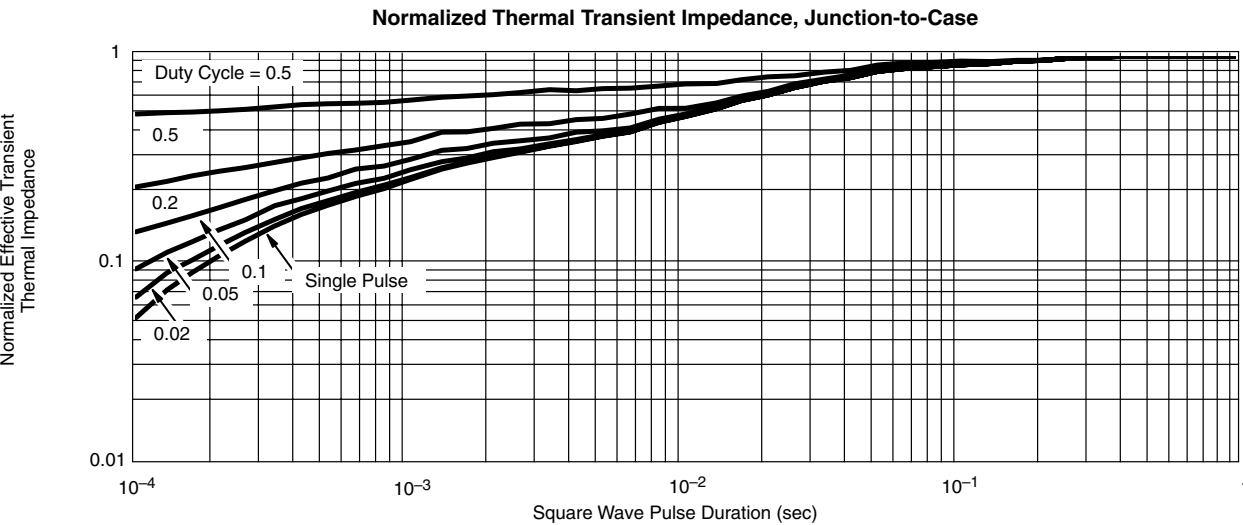
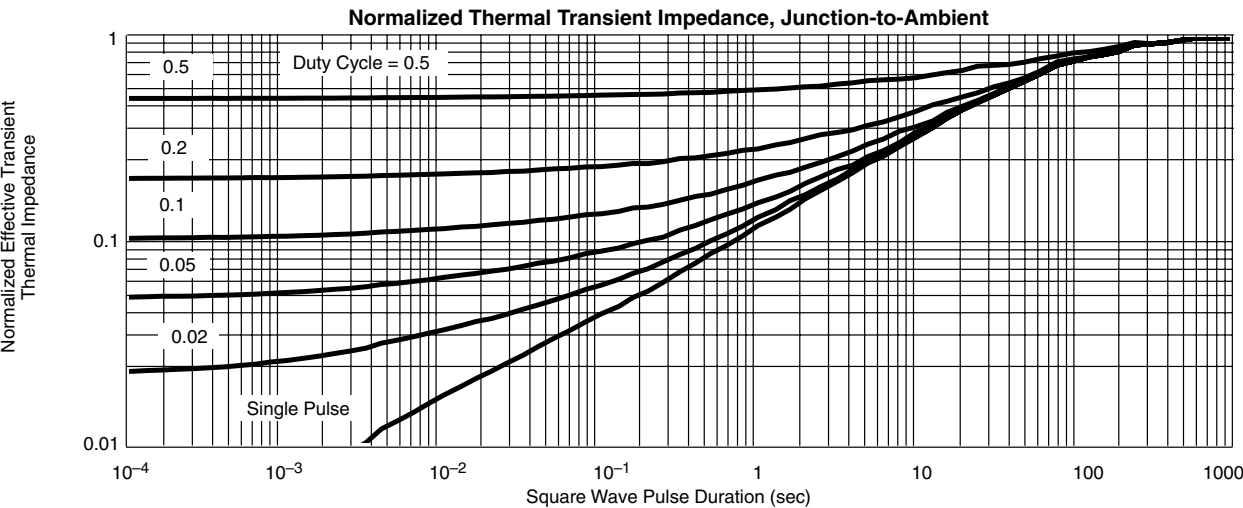


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73540>.



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