P-Channel 100-V (D-S) 175 °C MOSFET

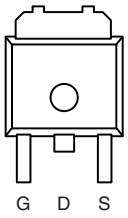
PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)[a]	Q_g (Typ.)
- 100	0.043 at V_{GS} = - 10 V	- 37	54 nC
	0.048 at V_{GS} = - 4.5 V	- 35	

FEATURES

- TrenchFET® Power MOSFET
- Compliant to RoHS Directive 2002/95/EC

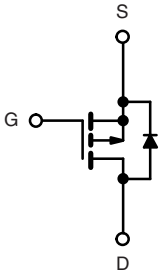
RoHS COMPLIANT

TO-252



Top View

Drain Connected to Tab



P-Channel MOSFET

Ordering Information: SUD50P10-43L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)[b]	T_C = 25 °C	I_D	- 37.1[a]	A
	T_C = 125 °C		- 31[a]	
	T_A = 25 °C		- 9.2[b, c]	
	T_A = 125 °C		- 7.7[b, c]	
Pulsed Drain Current		I_{DM}	- 40	
Continuous Source Current (Diode Conduction)	T_C = 25 °C	I_S	- 50[a]	
	T_A = 25 °C		- 6.9[b, c]	
Avalanche Current	L = 0.1 mH	I_{AS}	- 35	
Single Pulse Avalanche Energy		E_{AS}	61	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	136	W
	T_C = 70 °C		95	
	T_A = 25 °C		8.3[b, c]	
	T_A = 70 °C		5.8[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Junction-to-Case (Drain)		R_{thJC}	0.85	1.1	

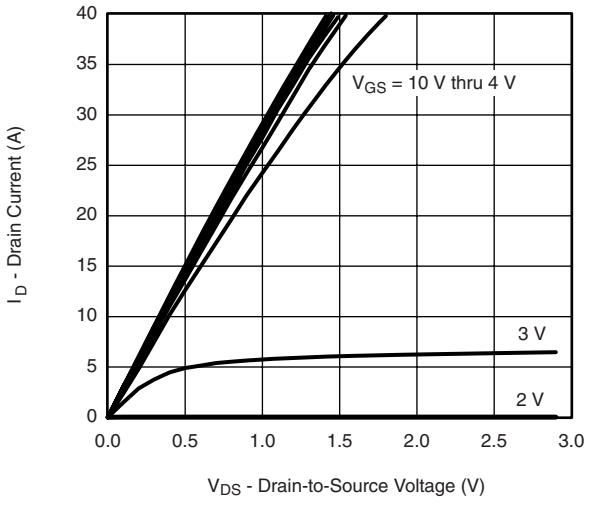
Notes:
a. Package limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. Maximum under Steady State conditions is 40 °C/W.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 109		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			5.9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 1		- 3	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 100 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 100 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = - 10 V	- 40			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V, I_D = - 9.2 A		0.036	0.043	Ω
		V_{GS} = - 4.5 V, I_D = - 7.7 A		0.040	0.048	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 15 V, I_D = - 9.2 A		38		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 50 V, V_{GS} = 0 V, f = 1 MHz		4600		pF
Output Capacitance	C_{oss}			230		
Reverse Transfer Capacitance	C_{rss}			175		
Total Gate Charge	Q_g	V_{DS} = - 50 V, V_{GS} = - 10 V, I_D = - 9.2 A		106	160	nC
		V_{DS} = - 50 V, V_{GS} = - 4.5 V, I_D = - 9.2 A		54	81	
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			26		
Gate Resistance	R_g	f = 1 MHz		4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 6.5 Ω $I_D \cong$ - 7.7 A, V_{GEN} = - 10 V, R_g = 1 Ω		15	25	ns
Rise Time	t_r			20	30	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			100	150	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 6.5 Ω $I_D \cong$ - 7.7 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		42	65	ns
Rise Time	t_r			160	240	
Turn-Off Delay Time	$t_{d(off)}$			100	150	
Fall Time	t_f			100	150	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 50	A
Pulse Diode Forward Current[a]	I_{SM}				- 40	
Body Diode Voltage	V_{SD}	I_S = - 7.7 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 7.7 A, dI/dt = 100 A/µs, T_J = 25 °C		60	90	ns
Body Diode Reverse Recovery Charge	Q_{rr}			150	225	nC
Reverse Recovery Fall Time	t_a			46		ns
Reverse Recovery Rise Time	t_b			14		

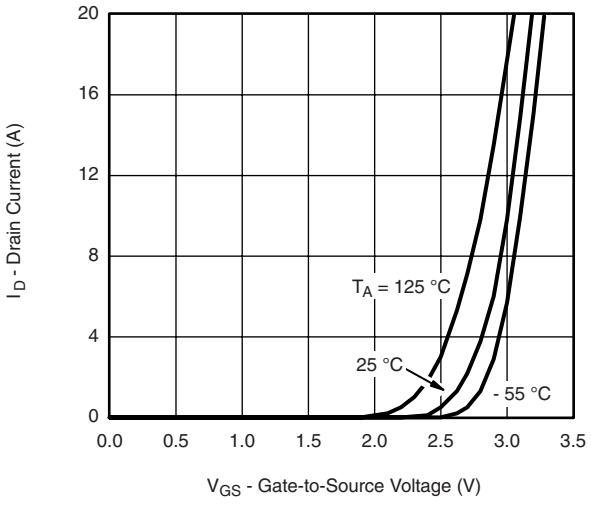
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

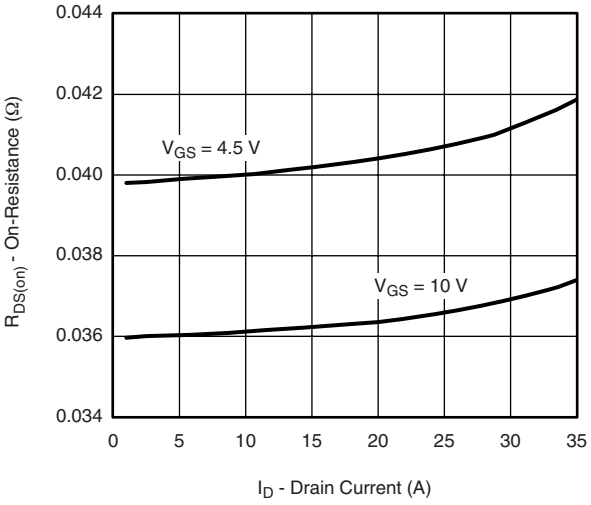
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



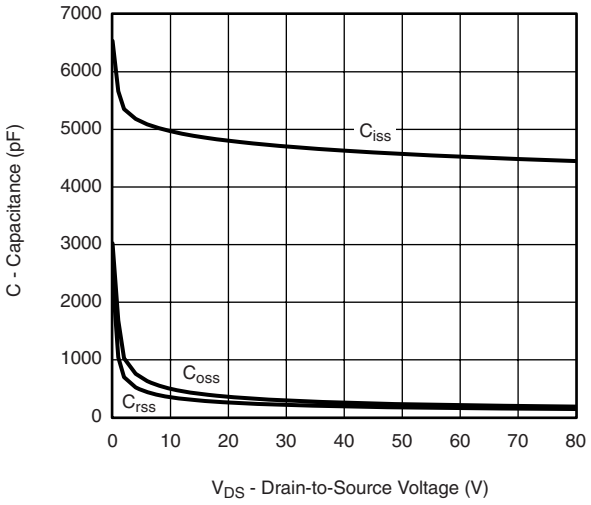
Output Characteristics



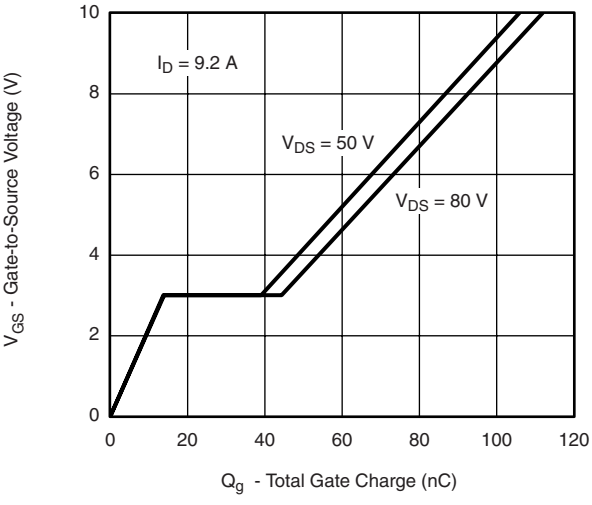
Transfer Characteristics



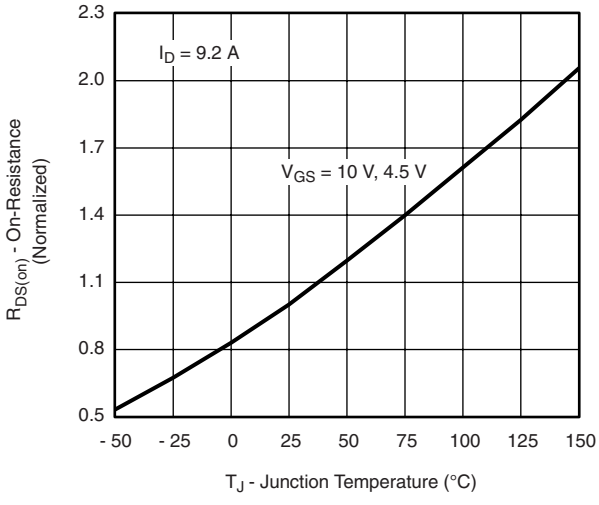
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

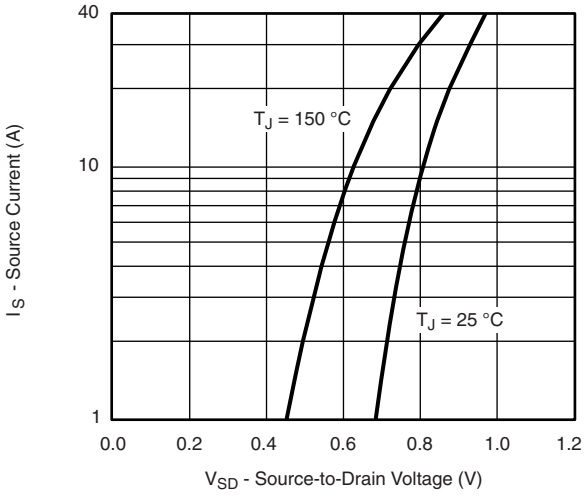


Gate Charge

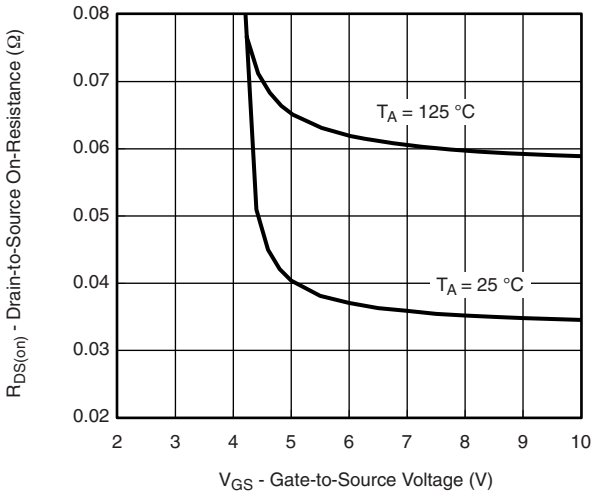


On-Resistance vs. Junction Temperature

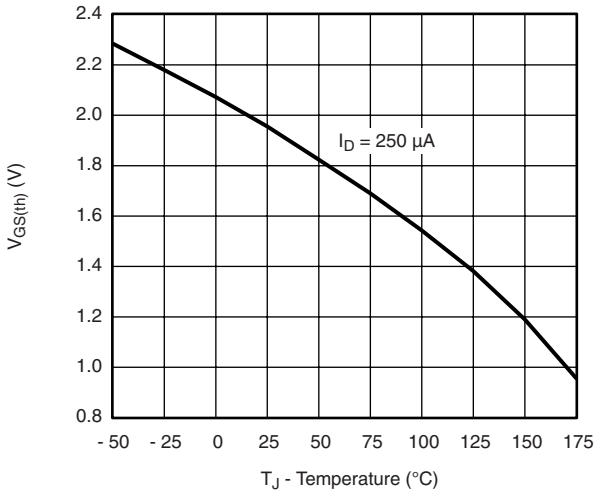
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



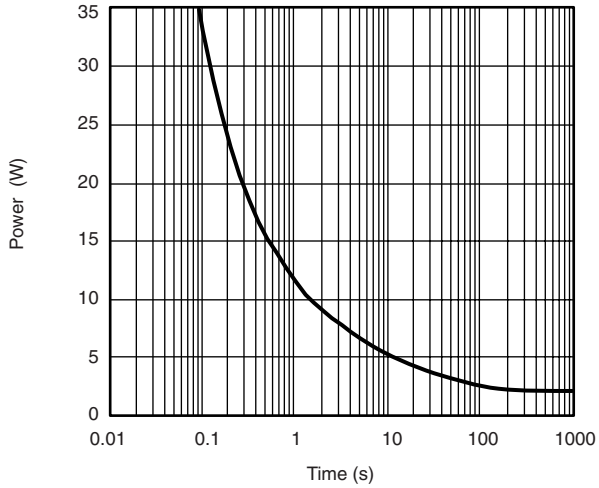
Source-Drain Diode Forward Voltage



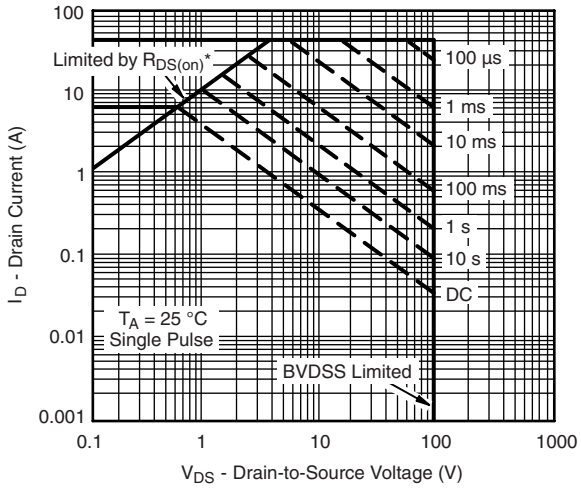
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



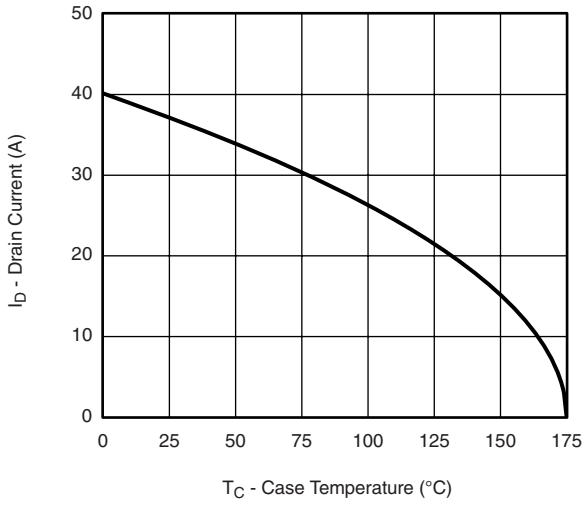
Single Pulse Power, Junction-to-Ambient



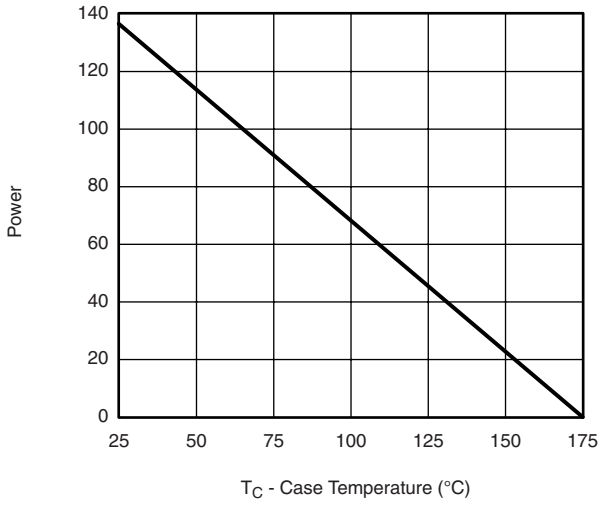
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

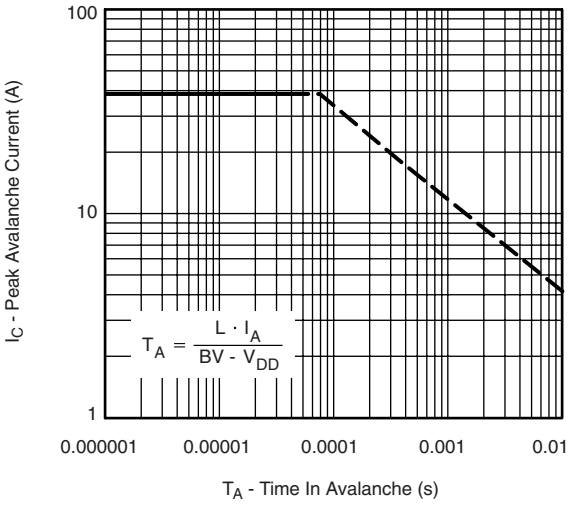
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Current Derating*



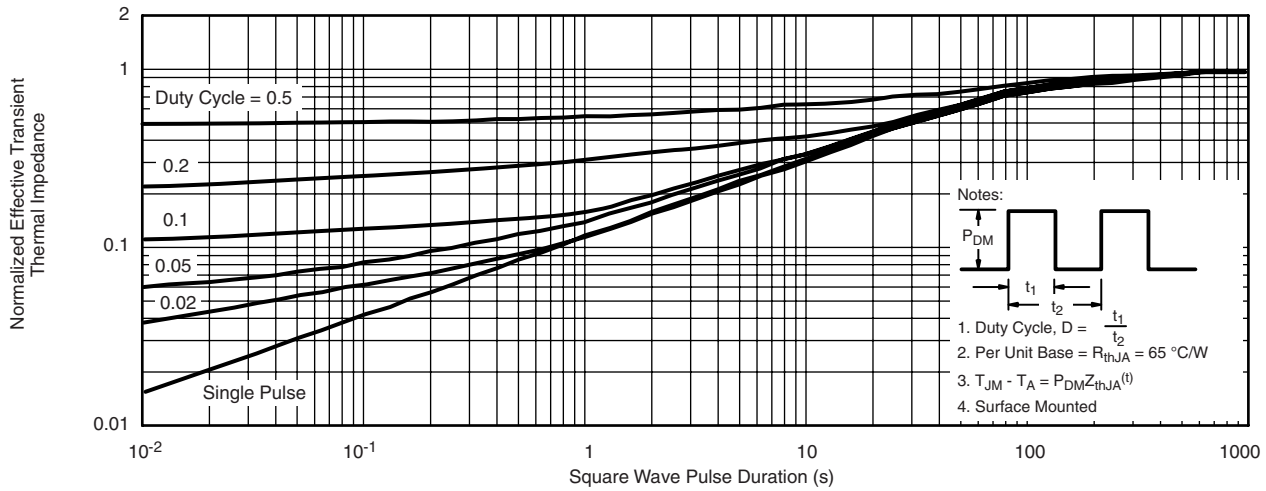
Single Pulse Power, Junction-to-Ambient



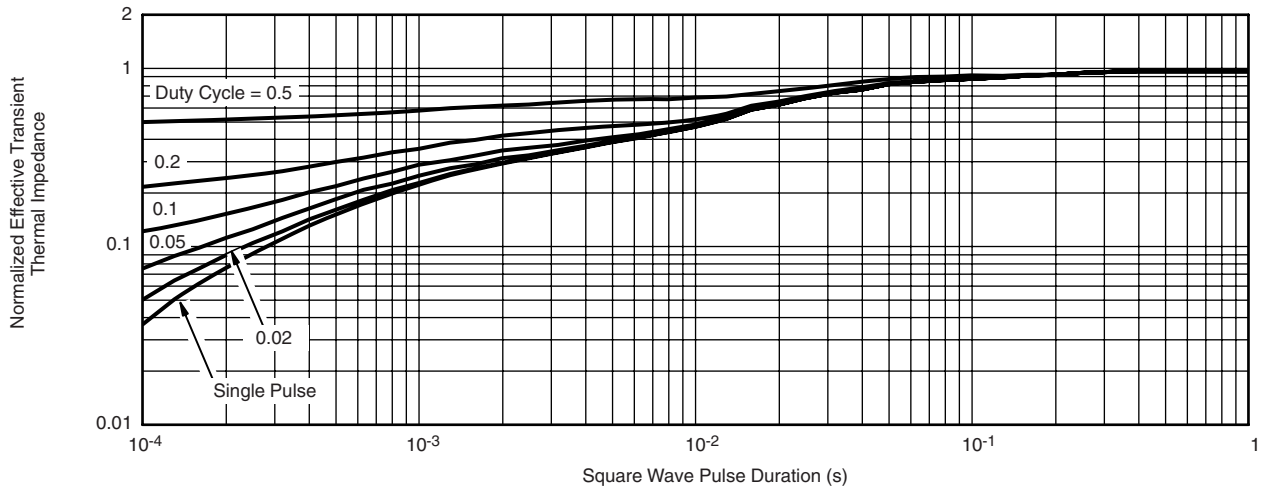
Single Pulse Avalanche Capability

* The power dissipation P_D is based on $T_{J(max)}$ = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



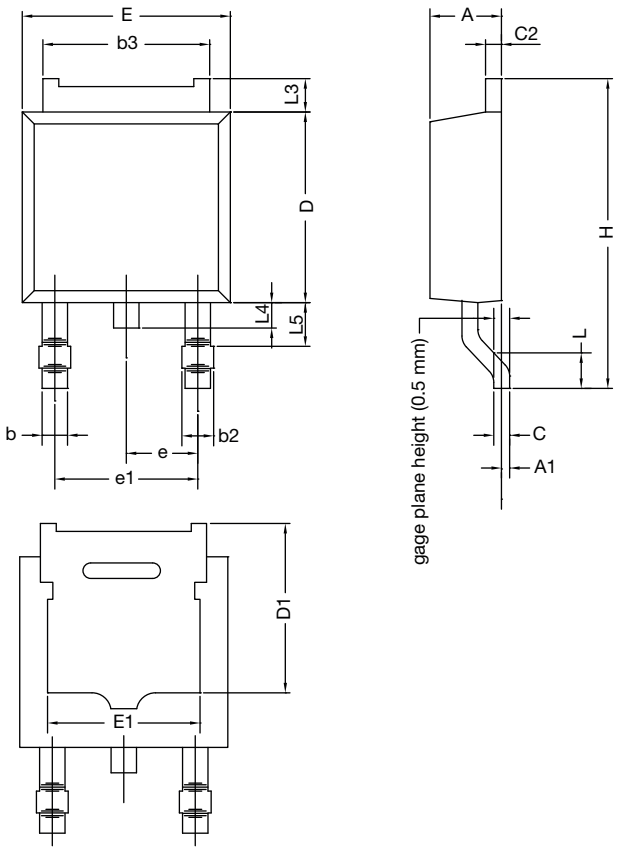
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73444.

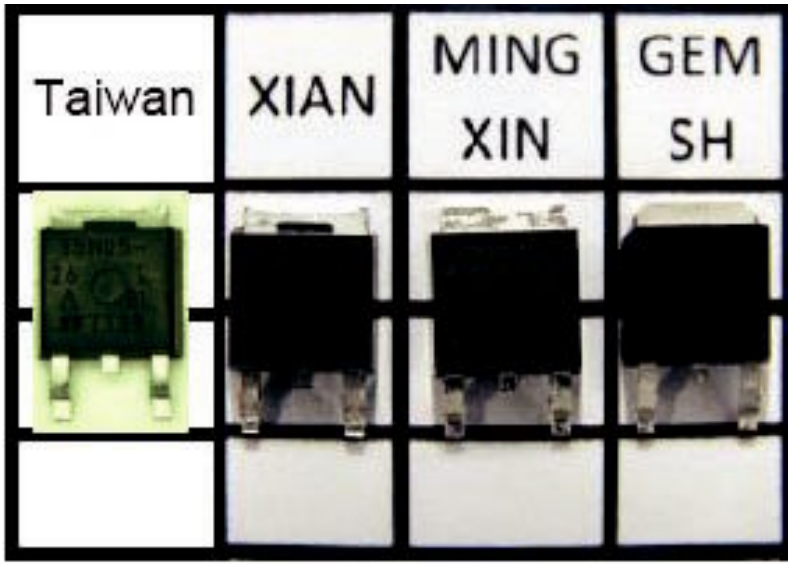
TO-252AA Case Outline



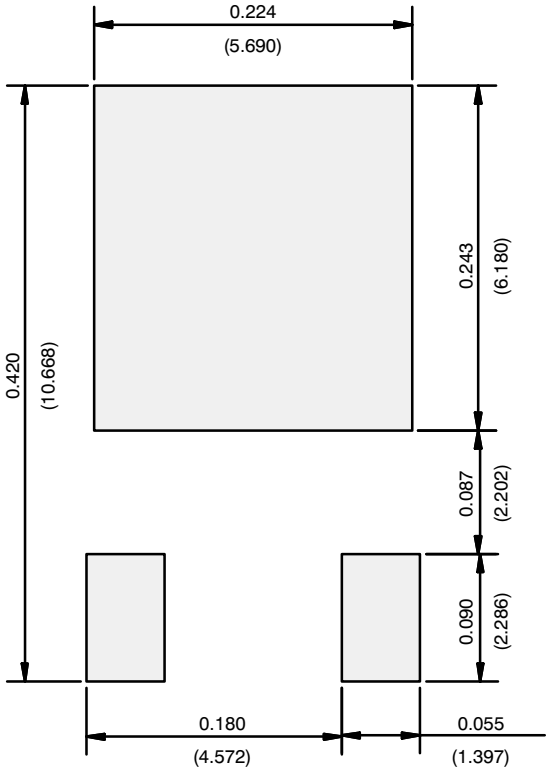
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0359-Rev. O, 03-Jun-13 DWG: 5347				

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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