



## N-Channel 40-V (D-S) 175°C MOSFET

### CHARACTERISTICS

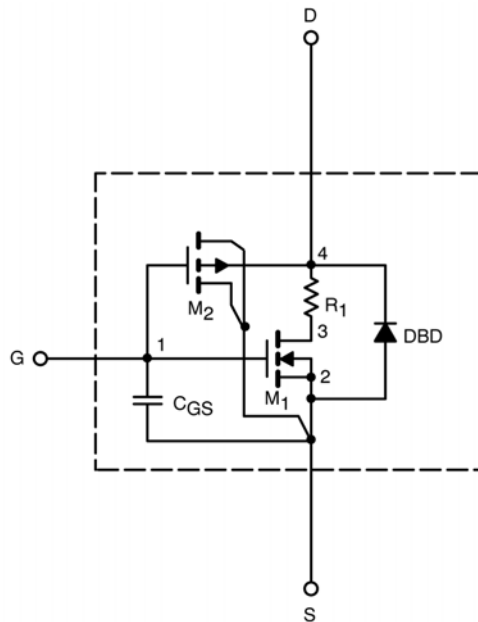
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



| SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED) |                     |  |                |               |      |
|---|---------------------|--|----------------|---------------|------|
| Parameter   | Symbol              | Test Conditions  | Simulated Data | Measured Data | Unit |
| <b>Static</b>   |                     |  |                |               |      |
| Gate Threshold Voltage  | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA  | 3.7            |               | V    |
| On-State Drain Current <sup>a</sup>                           | I <sub>D(on)</sub>  | V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V  | 1170           |               | A    |
| Drain-Source On-State Resistance <sup>a</sup>                 | r <sub>DS(on)</sub> | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A  | 0.0022         | 0.0022        | Ω    |
|   |                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 125°C  | 0.0031         |               |      |
|   |                     | V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A, T <sub>J</sub> = 175°C  | 0.0036         |               |      |
| Forward Transconductance <sup>a</sup>                         | g <sub>fs</sub>     | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A  | 87             |               | S    |
| Forward Voltage <sup>a</sup>                                  | V <sub>SD</sub>     | I <sub>S</sub> = 85 A, V <sub>GS</sub> = 0 V   | 1              | 1.1           | V    |
| <b>Dynamic<sup>b</sup></b>                                    |                     |  |                |               |      |
| Input Capacitance   | C <sub>iss</sub>    | V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz   | 12450          | 15720         | Pf   |
| Output Capacitance  | C <sub>oss</sub>    |  | 1429           | 1400          |      |
| Reverse Transfer Capacitance                                  | C <sub>rss</sub>    |  | 786            | 800           |      |
| Total Gate Charge <sup>c</sup>                                | Q <sub>g</sub>      | V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 110 A   | 262            | 250           | NC   |
| Gate-Source Charge <sup>c</sup>                               | Q <sub>gs</sub>     |  | 95             | 95            |      |
| Gate-Drain Charge <sup>c</sup>                                | Q <sub>gd</sub>     |  | 57             | 57            |      |
| Turn-On Delay Time <sup>c</sup>                               | t <sub>d(on)</sub>  | V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.27 Ω<br>I <sub>D</sub> ≅ 110 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 2.5 Ω | 43             | 50            | Ns   |
| Rise Time <sup>c</sup>  | t <sub>r</sub>      |  | 101            | 150           |      |
| Turn-Off Delay Time <sup>c</sup>                              | t <sub>d(off)</sub> |  | 75             | 70            |      |
| Fall Time <sup>c</sup>  | t <sub>f</sub>      |  | 43             | 25            |      |

**Notes**

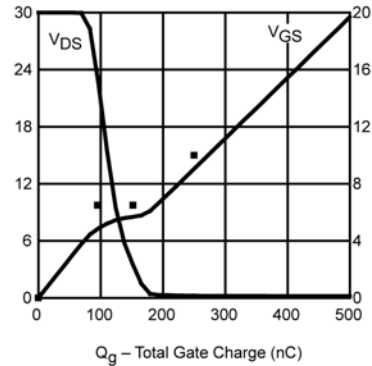
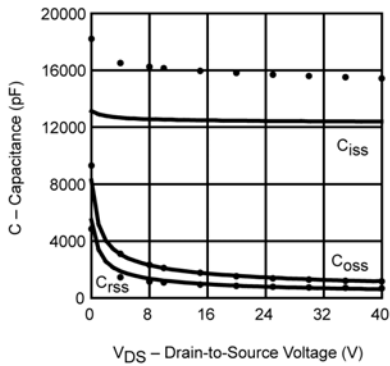
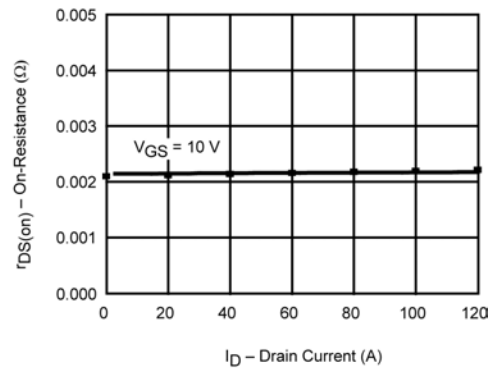
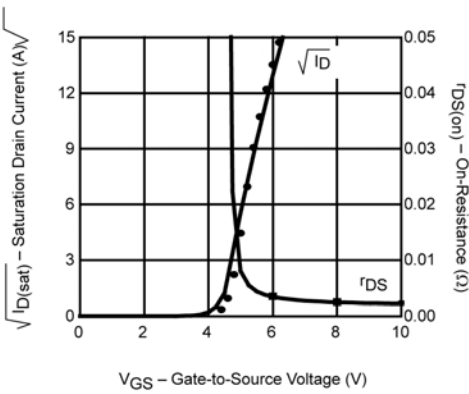
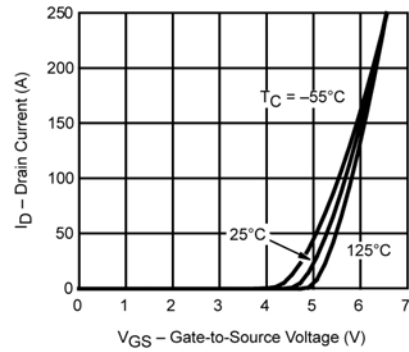
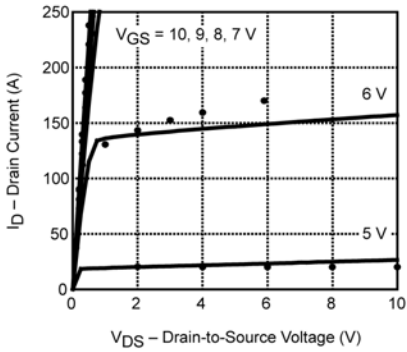
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



# SPICE Device Model SUM110N04-2m7H

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.