



N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^{a, e}	Q _g (Typ)
25	0.0052 @ V _{GS} = 10 V	89	30 nC
	0.0076 @ V _{GS} = 4.5 V	80	

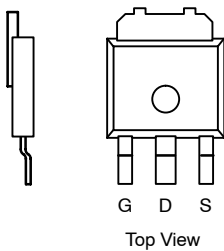
FEATURES

- TrenchFET® Power MOSFET
- 100% R_g Tested
- RoHS Compliant



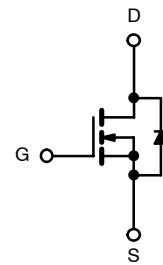
APPLICATIONS

- DC/DC Conversion, Low-Side
 - Desktop PC
 - Notebook PC

TO-252
Reverse Lead DPAK

Drain Connected to Tab

Ordering Information:
 SUR50N025-05P—E3 (Lead (Pb)-Free)
 SUR50N025-05P-T4—E3 (Lead (Pb)-Free, alternate tape orientation)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	25	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	T _C = 25 °C	I _D	89 ^{a, e}	A
	T _C = 70 °C		75 ^{a, e}	
	T _A = 25 °C		36 ^{b, c}	
	T _A = 70 °C		30 ^{b, c}	
Pulsed Drain Current		I _{DM}	100	A
Continuous Source-Drain Diode Current		I _S	55	
			7.7 ^{b, c}	
Avalanche Current Pulse		I _{AS}	45	mJ
Single Pulse Avalanche Energy		E _{AS}	101	
				W
Maximum Power Dissipation		P _D	83 ^a	
			58 ^a	
			11.5 ^{b, c}	
			8.0 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 sec	R _{thJA}	10	13	°C/W
Maximum Junction-to-Case	Steady State	R _{thJC}	1.5	1.8	

Notes:

- Based on T_C = 25 °C.
- Surface mounted on 1" x 1" FR4 board.
- t = 10 sec
- Maximum under steady state conditions is 90 °C/W.
- Calculated based on maximum junction temperature. Package limitation current is 50 A.

SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	25			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		20		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			-6.0		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.4		2.4	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 25 V, V _{GS} = 0 V			1	μA
		V _{DS} = 25 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0042	0.0052	Ω
		V _{GS} = 4.5 V, I _D = 15 A		0.0062	0.0076	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A		65		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = 12 V, V _{GS} = 0 V, f = 1 MHz		3600		pF
Output Capacitance	C _{oss}			790		
Reverse Transfer Capacitance	C _{rss}			430		
Total Gate Charge	Q _g	V _{DS} = 12 V, V _{GS} = 10 V, I _D = 50 A		63	95	nC
		V _{DS} = 12 V, V _{GS} = 4.5 V, I _D = 50 A		30	45	
Gate-Source Charge	Q _{gs}			10.5		
Gate-Drain Charge	Q _{gd}		10.5			
Gate Resistance	R _g	f = 1 MHz	0.5	1.0	1.5	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 12 V, R _L = 0.24 Ω I _D ≅ 50 A, V _{GEN} = 4.5 V, R _g = 1 Ω		24	36	ns
Rise Time	t _r			13	20	
Turn-Off Delay Time	t _{d(off)}			24	36	
Fall Time	t _f			7.5	12	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 12 V, R _L = 0.24 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 1 Ω		11	17	
Rise Time	t _r			11	17	
Turn-Off Delay Time	t _{d(off)}			29	44	
Fall Time	t _f			8	12	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			55	A
Pulse Diode Forward Current ^a	I _{SM}				100	
Body Diode Voltage	V _{SD}	I _S = 30 A		0.9	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 20 A, di/dt = 100 A/μs, T _J = 25 °C		34	51	ns
Body Diode Reverse Recovery Charge	Q _{rr}			25	38	nC
Reverse Recovery Fall Time	t _a			17		ns
Reverse Recovery Rise Time	t _b			17		

Notes

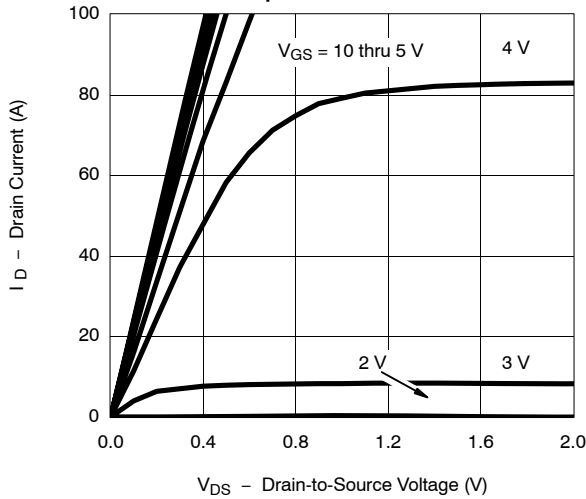
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

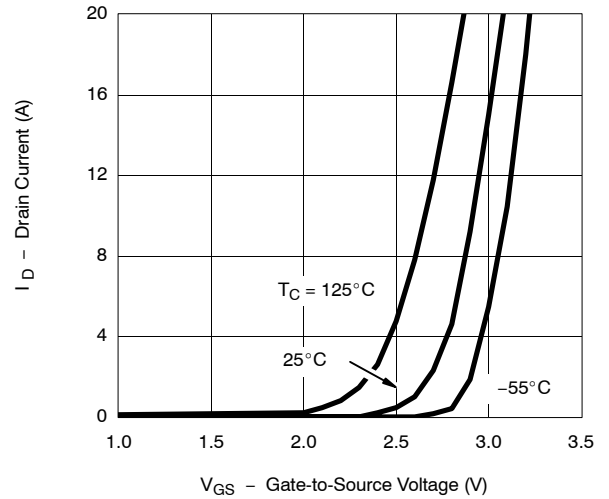


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

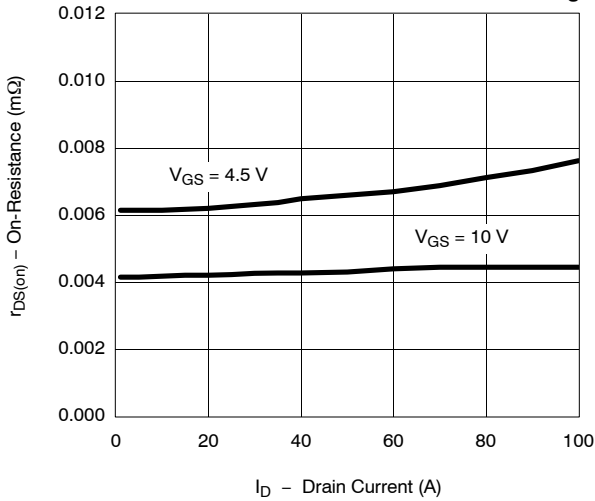
Output Characteristics



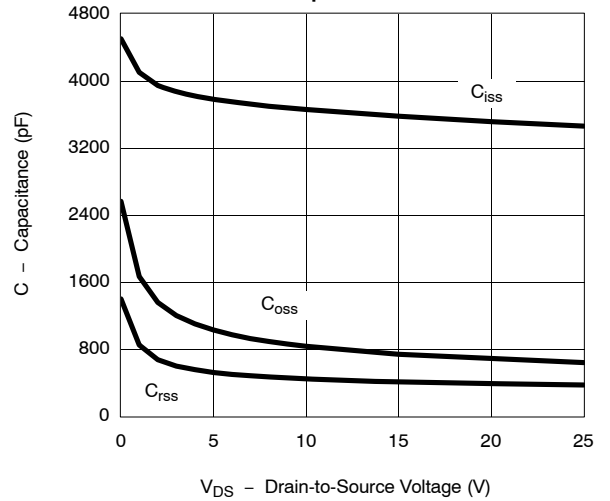
Transfer Characteristics



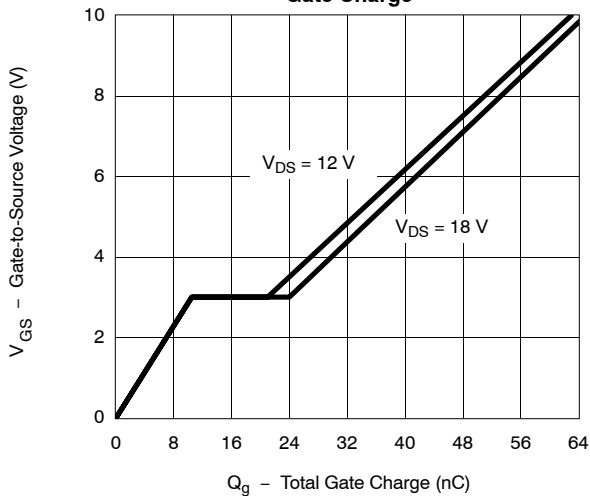
On-Resistance vs. Drain Current and Gate Voltage



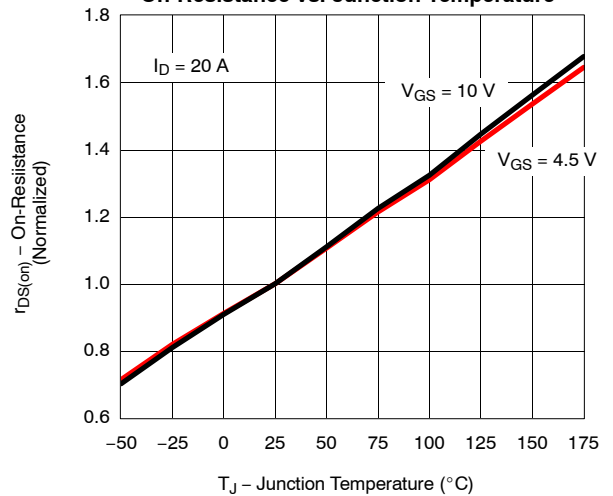
Capacitance



Gate Charge



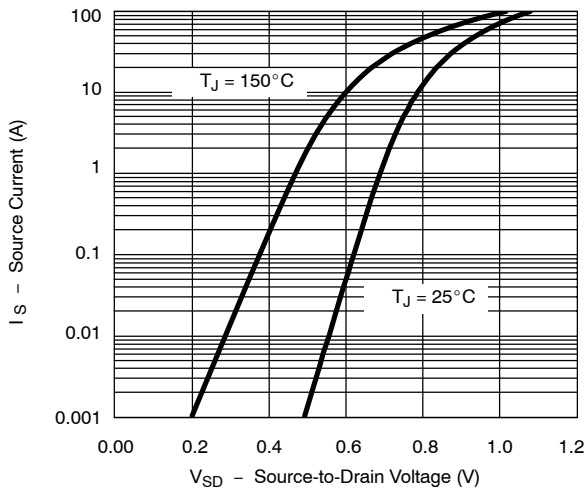
On-Resistance vs. Junction Temperature



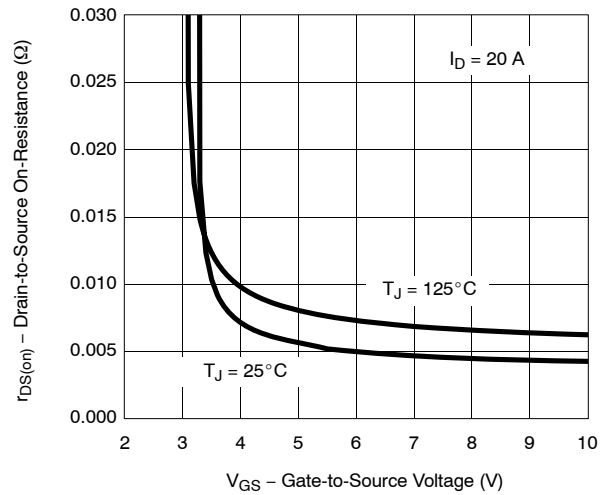


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

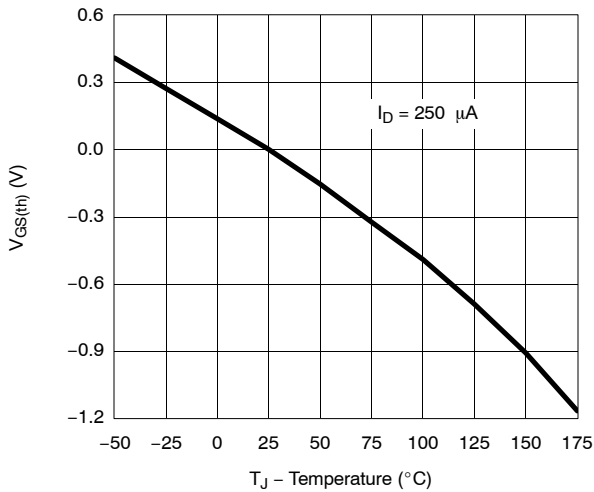
Source-Drain Diode Forward Voltage



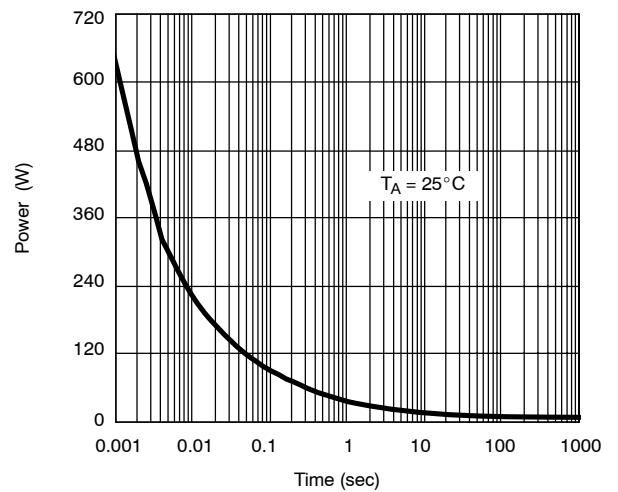
On-Resistance vs. Gate-to-Source Voltage



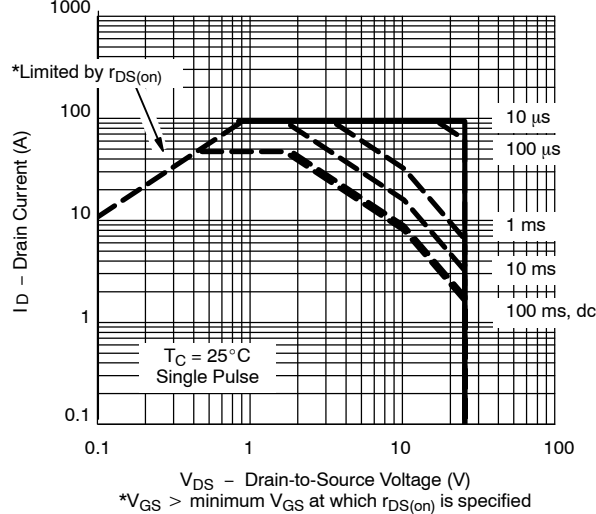
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

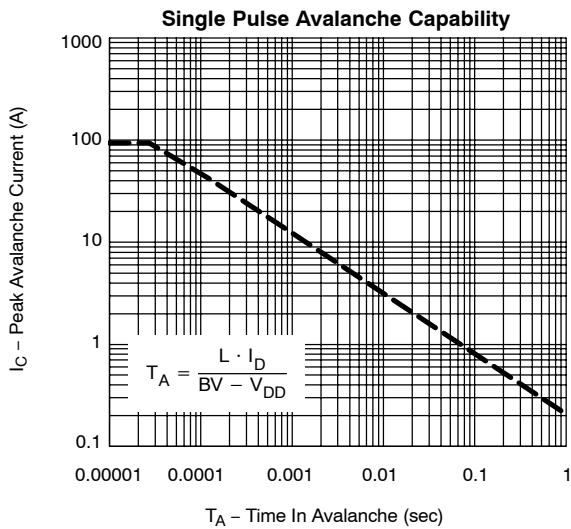
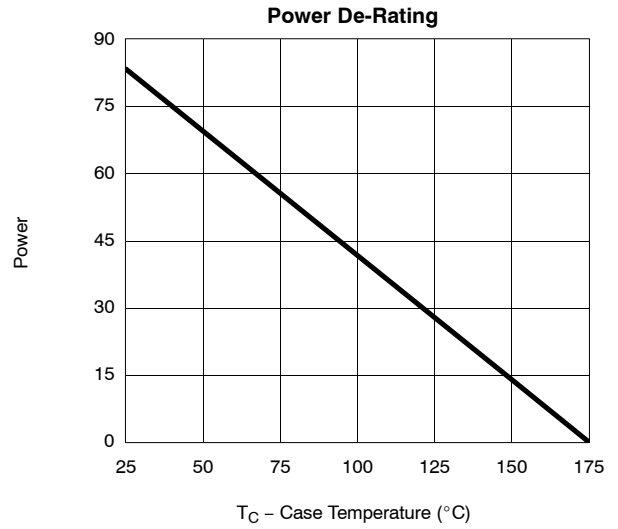
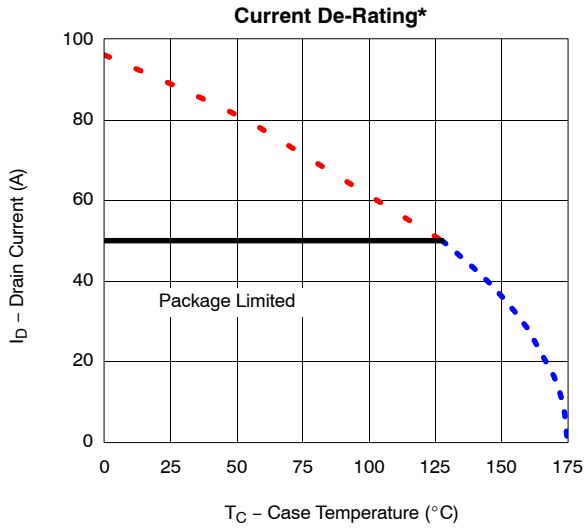


Safe Operating Area, Junction-to-Case





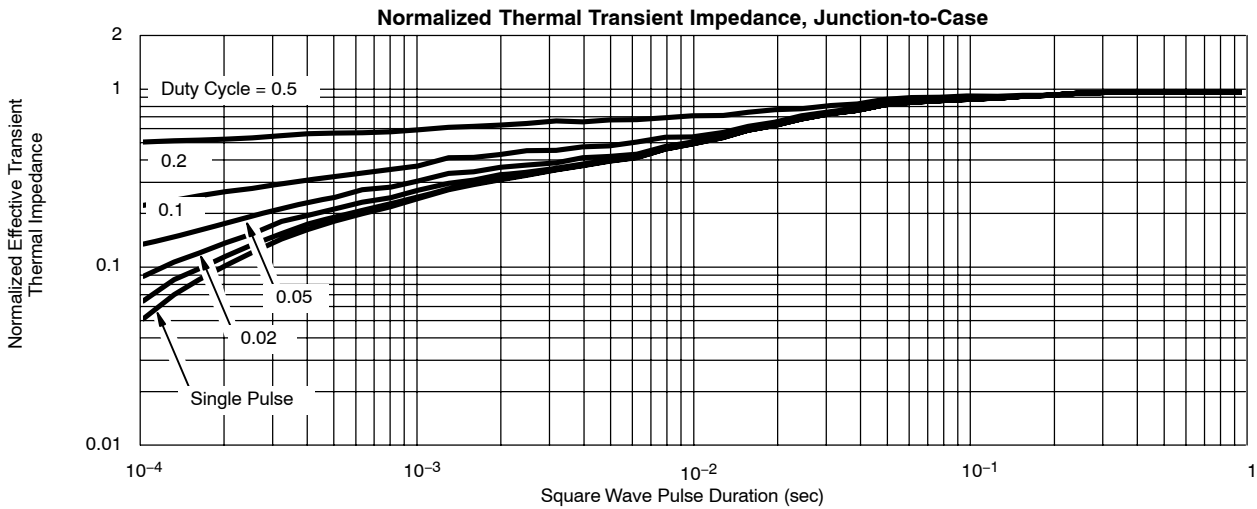
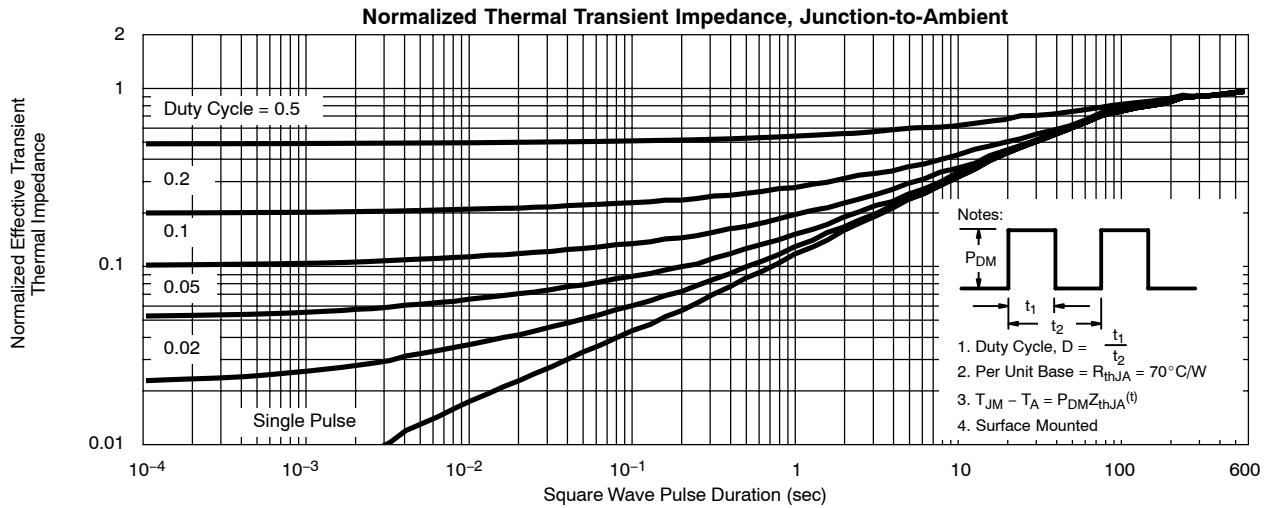
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



*The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73379>.