



New Product

SUR50N03-06P

Vishay Siliconix

## N-Channel 30-V (D-S) 175°C MOSFET

### PRODUCT SUMMARY

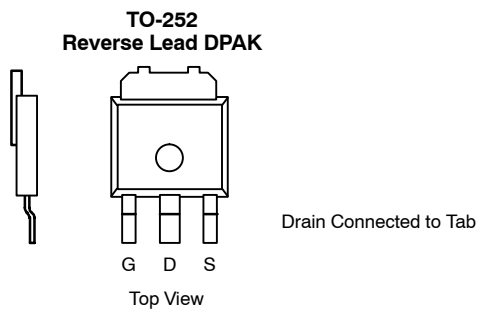
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>b</sup>
30	0.0065 @ $V_{GS} = 10$ V	84 <sup>b</sup>
	0.0095 @ $V_{GS} = 4.5$ V	59 <sup>b</sup>

### FEATURES

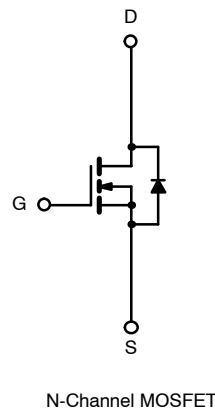
- TrenchFET® Power MOSFET
- 175°C Junction Temperature
- Optimized for Low-Side Synchronous Rectifier Operation
- 100%  $R_g$  Tested

### APPLICATIONS

- DC/DC Converters
  - Desktop CPU Core
- Synchronous Rectifiers



Ordering Information:  
 SUR50N03-06P—E3  
 SUR50N03-06P-T4—E3 (alternate tape orientation)



N-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	$T_A = 25^\circ\text{C}$	27
		$T_C = 25^\circ\text{C}$	84 <sup>b</sup>
		$T_C = 100^\circ\text{C}$	59 <sup>b</sup>
Pulsed Drain Current	$I_{DM}$	100	A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	25	
Maximum Power Dissipation	$P_D$	$T_C = 25^\circ\text{C}$	88
		$T_A = 25^\circ\text{C}$	8.3 <sup>a</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	15	$^\circ\text{C}/\text{W}$
		Steady State	40	
Maximum Junction-to-Case	$R_{thJC}$	1.4	1.7	

#### Notes

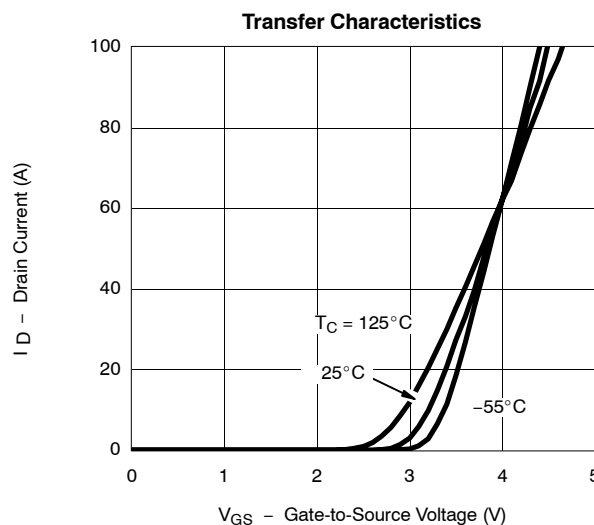
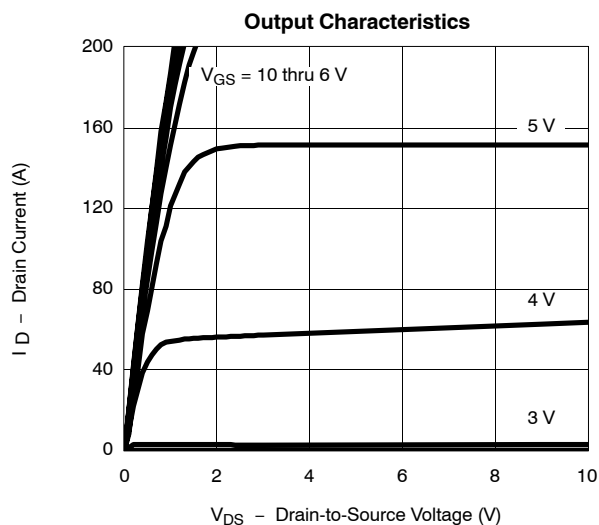
- Surface Mounted on FR4 Board,  $t \leq 10$  sec.
- Based on maximum allowable junction temperature, package limitation current is 50 A.

SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C			50	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0053	0.0065	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125°C			0.0105	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		0.0078	0.0095	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	20			S
<b>Dynamic<sup>a</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		3100		pF
Output Capacitance	C <sub>oss</sub>			565		
Reverse Transfer Capacitance	C <sub>rss</sub>			255		
Gate Resistance	R <sub>g</sub>		1	1.9	3.1	Ω
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A		21	30	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			10		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			7.5		
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			12	20	
Rise Time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 0.3 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		12	20	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			30	45	
Fall Time <sup>c</sup>	t <sub>f</sub>			10	15	
<b>Source-Drain Diode Ratings and Characteristic (T<sub>C</sub> = 25°C)</b>						
Pulsed Current	I <sub>SM</sub>				100	A
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V		1.2	1.5	V
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 50 A, di/dt = 100 A/μs		35	70	ns

Notes

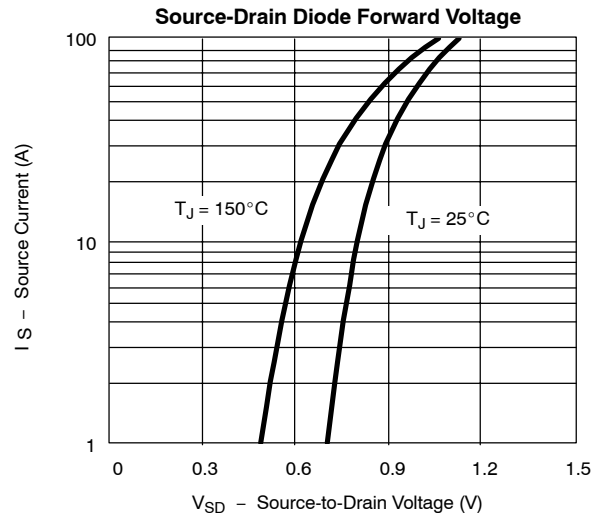
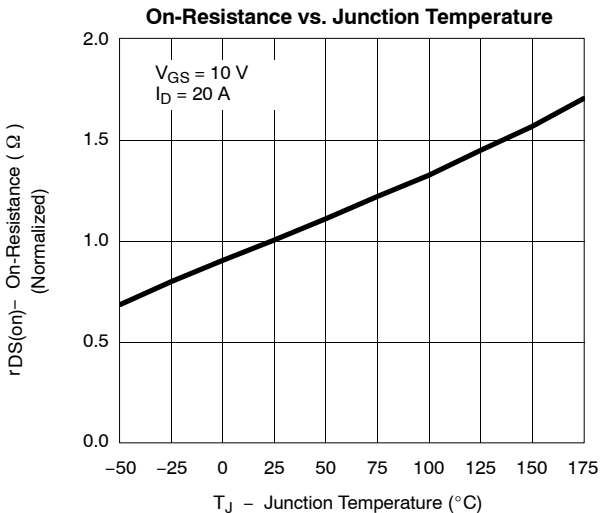
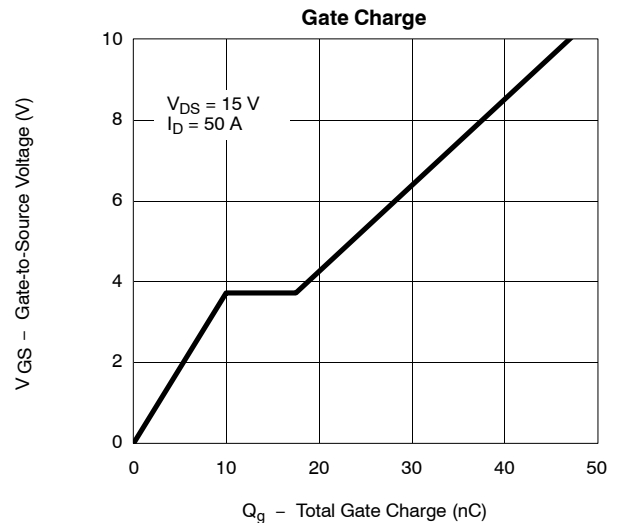
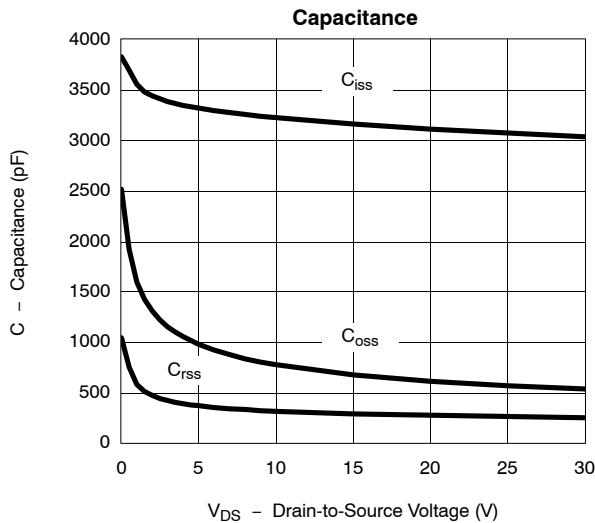
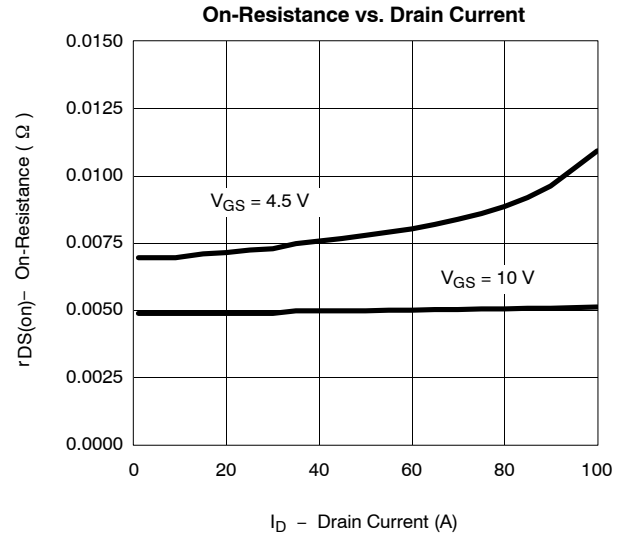
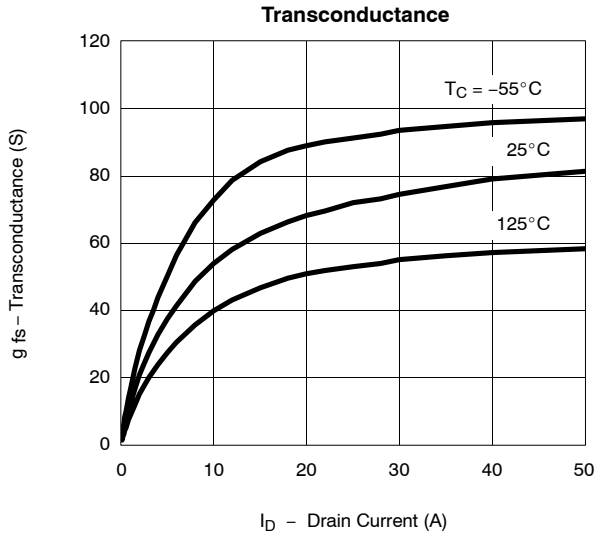
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- c. Independent of operating temperature.

**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



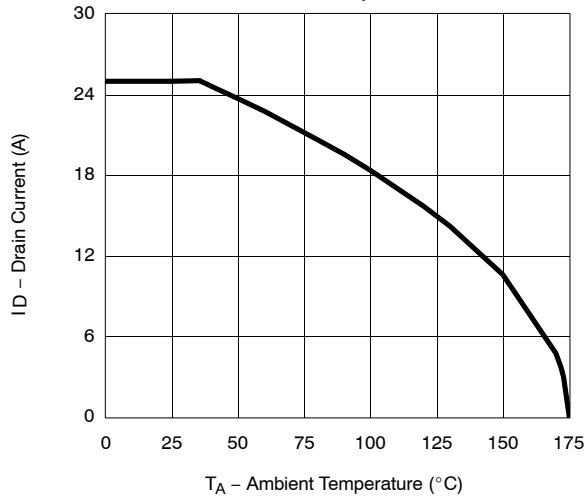


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

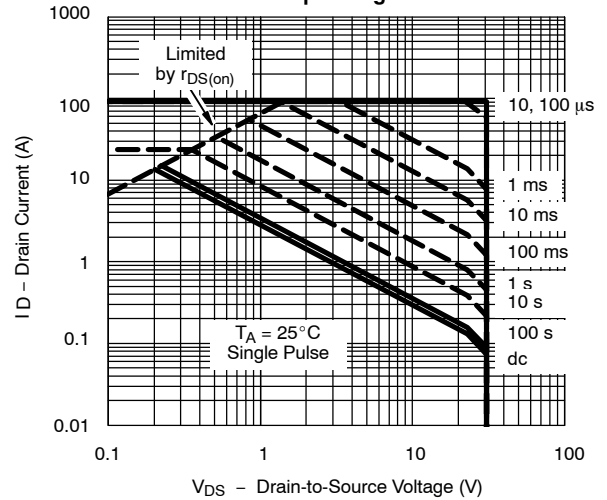


**THERMAL RATINGS**

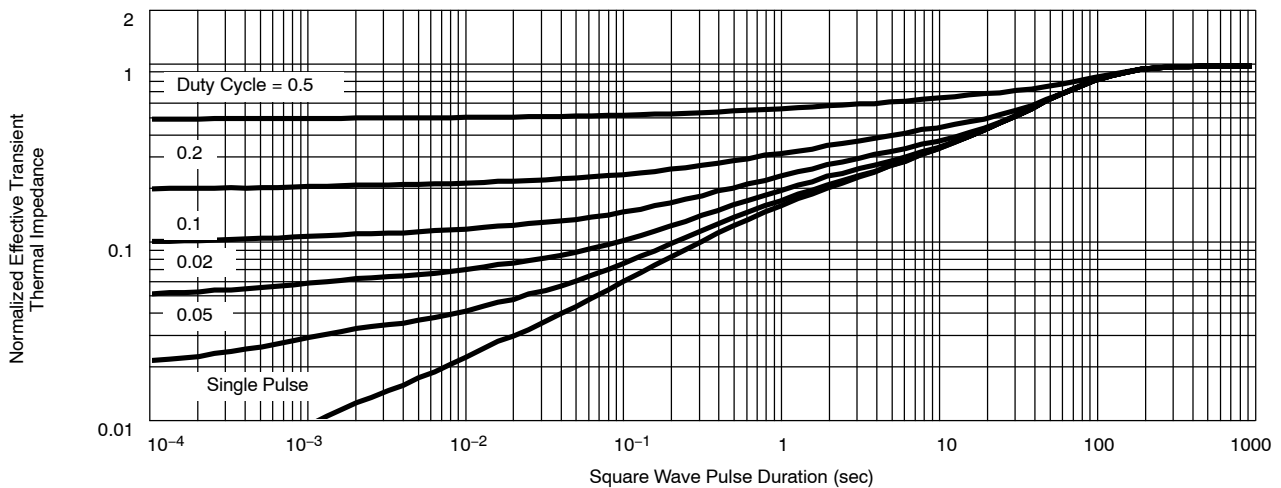
**Maximum Drain Current vs. Ambient Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

