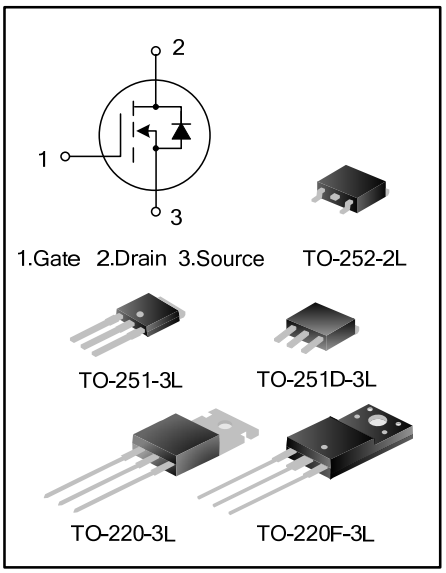
2A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD2N60M/F/T/D is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



FEATURES

* 2A,600V,$R_{DS(on)(typ.)}$=4.0Ω@V_{GS}=10V
* Low gate charge
* Low C_{rss}
* Fast switching
* Improved dv/dt capability

NOMENCLATURE

S V D X N E X X X

Silan VDMOS Code

Nominal current,using 1 or2 digits:
Example:4 denotes 4A,
10 denotes 10A,
08 denotes 0.8A

N denotes N Channel

Special Features indication, May be omitted.
Example: E denotes embeded ESD structure

Nominal Voltage,using 2 digits
Example: 60 denotes 600V,
65 denotes 650V.

Package information.
Example:T:TO-220;F:TO-220F;
M:TO-251,TO-251D;D:TO-252.

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVD2N60M	TO-251-3L	SVD2N60M	Pb free	Tube
SVD2N60M	TO-251D-3L	SVD2N60M	Pb free	Tube
SVD2N60F	TO-220F-3L	SVD2N60F	Pb free	Tube
SVD2N60T	TO-220-3L	SVD2N60T	Pb free	Tube
SVD2N60D	TO-252-2L	SVD2N60D	Pb free	Tube
SVD2N60DTR	TO-252-2L	SVD2N60D	Pb free	Tape & Reel

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Characteristics	Symbol	Rating			Unit
		SVD2N60M/D	SVD2N60T	SVD2N60F	
Drain-Source Voltage	V_{DS}	600			V
Gate-Source Voltage	V_{GS}	±30			V
Drain Current	I_D	2.0			A
Drain Current Pulsed	I_{DM}	8.0			A
Power Dissipation(T_C=25°C)	P_D	34	44	23	W
-Derate above 25°C		0.27	0.35	0.18	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	118			mJ
Operation Junction Temperature	T_J	-55～+150			°C
Storage Temperature	Tstg	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating			Unit
		SVD2N60M/D	SVD2N60T	SVD2N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.7	2.86	5.56	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=1.0A	--	4.0	4.6	Ω
Input Capacitance	Ciss	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	320	380	pF
Output Capacitance	Coss		--	30	45	
Reverse Transfer Capacitance	Crss		--	3	5.6	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=2.0A, RG=25Ω (Note 2,3)	--	13	30	ns
Turn-on Rise Time	t_r		--	12	60	
Turn-off Delay Time	$t_{d(off)}$		--	73	100	
Turn-off Fall Time	t_f		--	14.3	70	
Total Gate Charge	Qg	V_{DS}=480V,I_D=2.0A, V_{GS}=10V (Note 2,3)	--	9.3	13	nC
Gate-Source Charge	Qgs		--	2.0	--	
Gate-Drain Charge	Qgd		--	3.3	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	2.0	A
Pulsed Source Current	I_{SM}		--	--	8.0	
Diode Forward Voltage	V_{SD}	I_S=2.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=2.0A,V_{GS}=0V, dIF/dt=100A/μS	--	230	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.0	--	μC

Notes:

1. L=30mH, I_{AS}=2.58ª, V_{DD}=123V, R_G=25Ω, starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

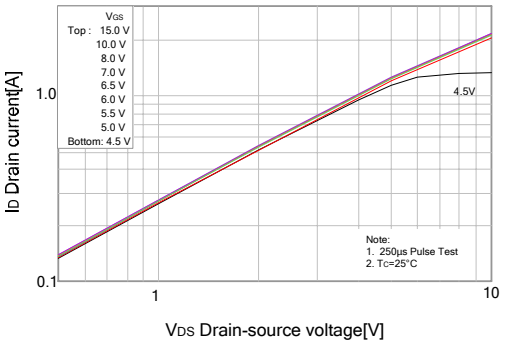


Figure 2. Transfer Characteristics

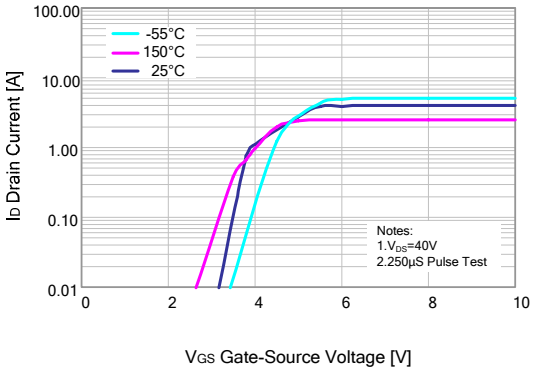


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

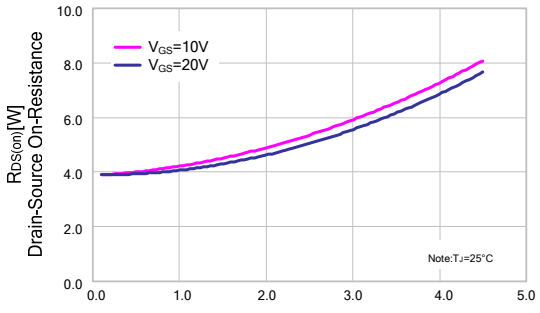


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

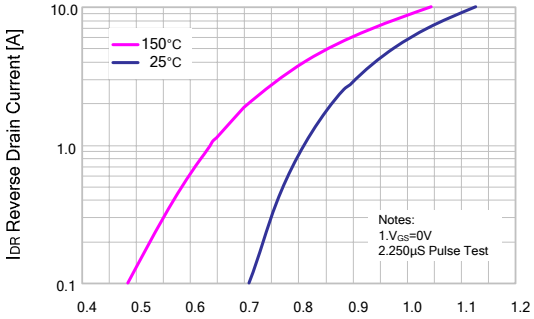


Figure 5. Capacitance Characteristics

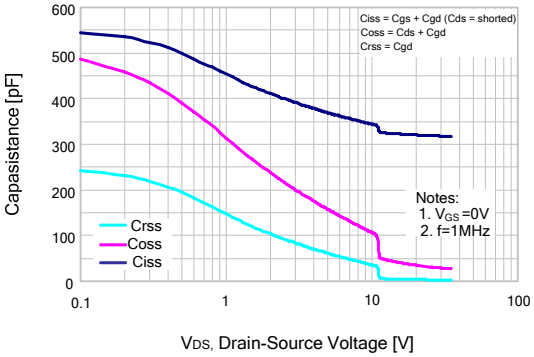
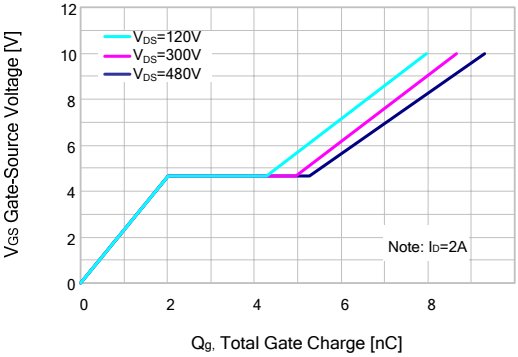


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS （continued）

Figure 7. Breakdown Voltage Variation vs. Temperature

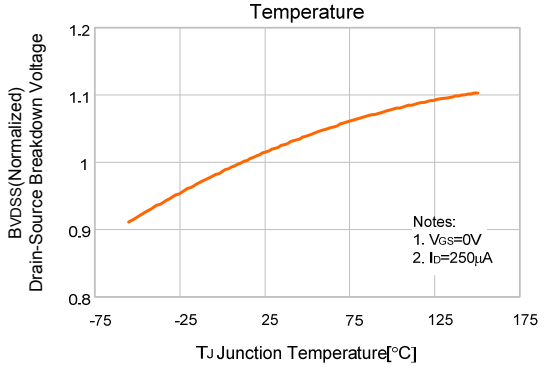


Figure 8. On-resistance Variation vs Temperature

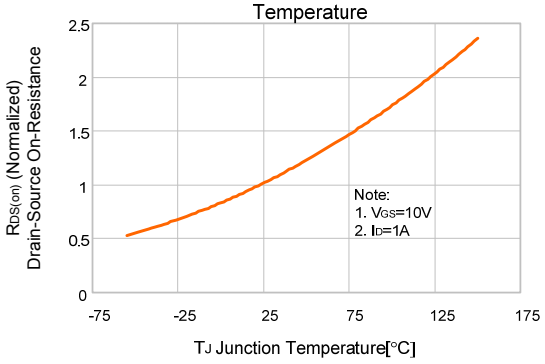


Figure 9-1. Max. Safe Operating Area(SVD2N60M/D)

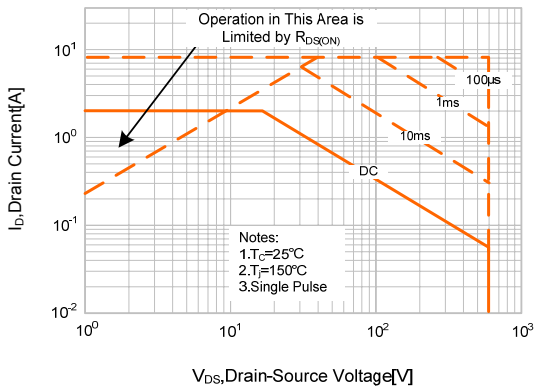


Figure 9-2. Max. Safe Operating Area(SVD2N60T)

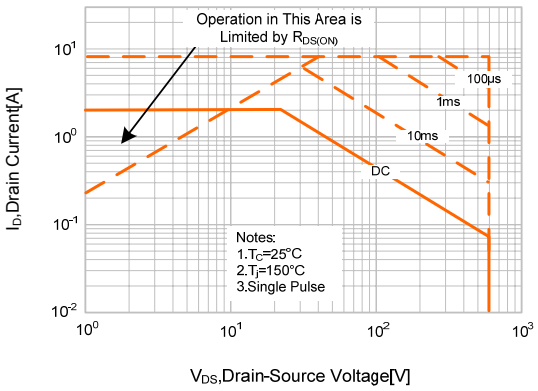


Figure 9-3. Max. Safe Operating Area(SVD2N60F)

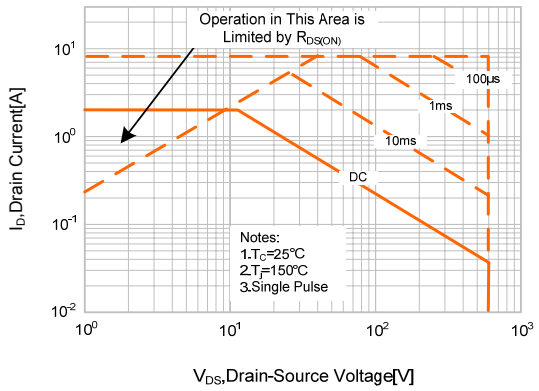
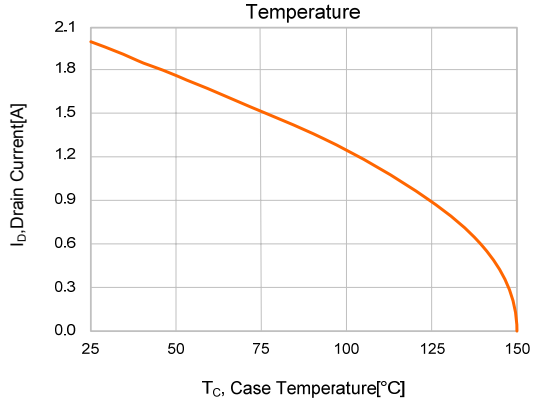
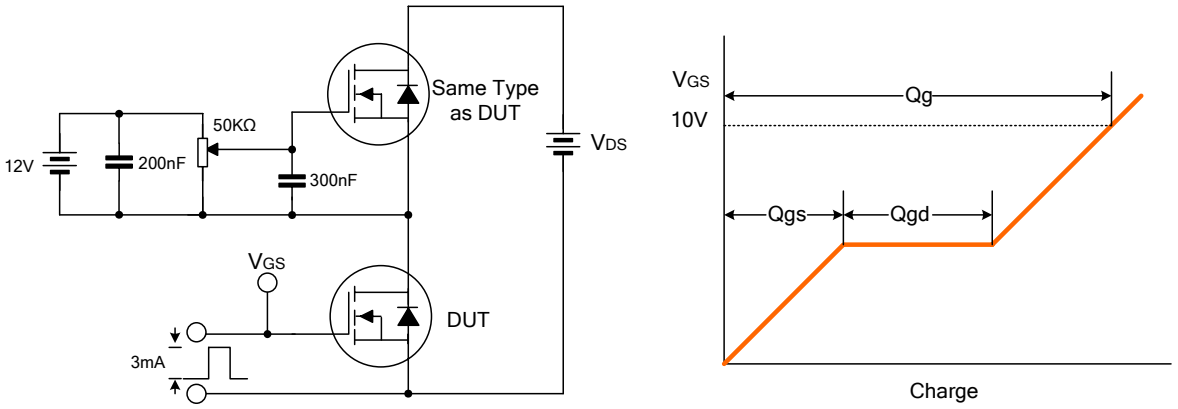


Figure 10. Maximum Drain Current vs. Case Temperature

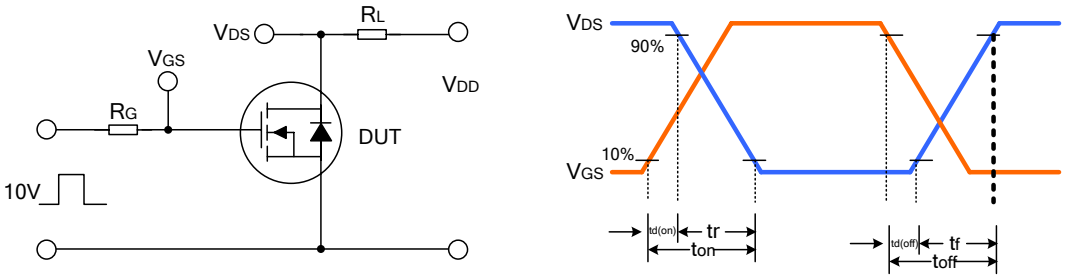


TYPICAL TEST CIRCUIT

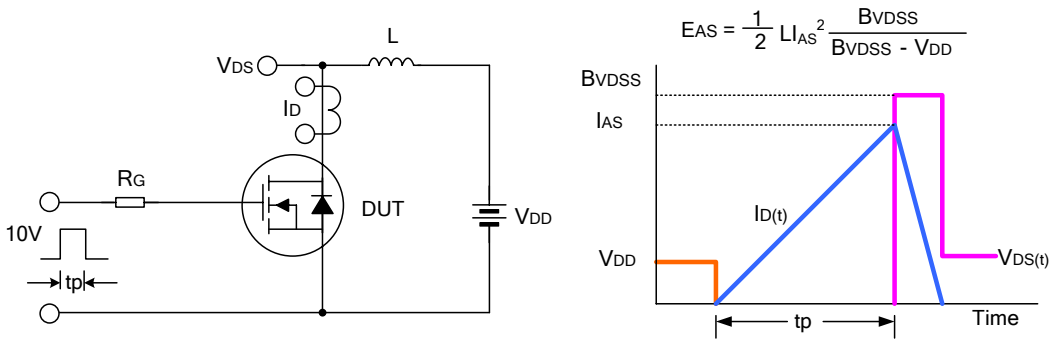
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

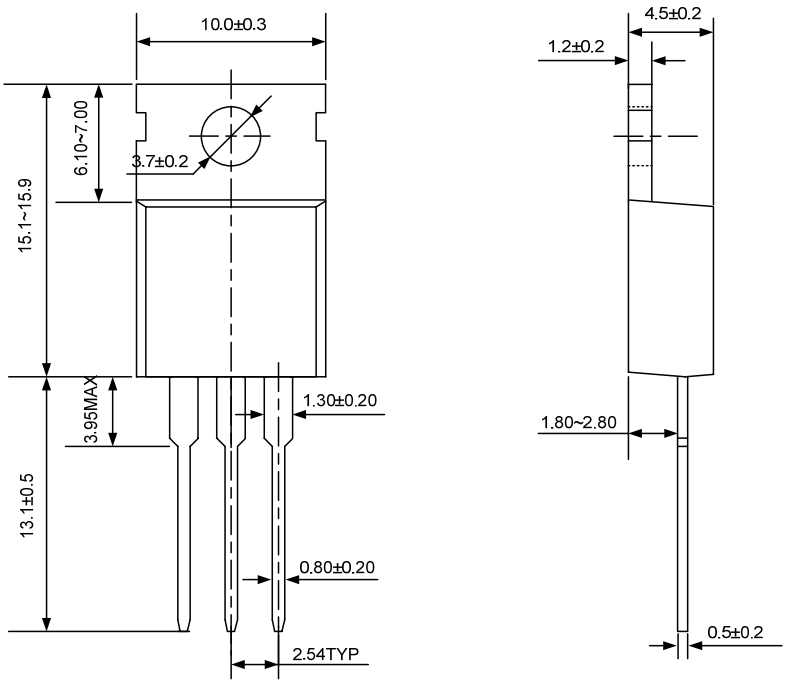


Unclamped Inductive Switching Test Circuit & Waveform

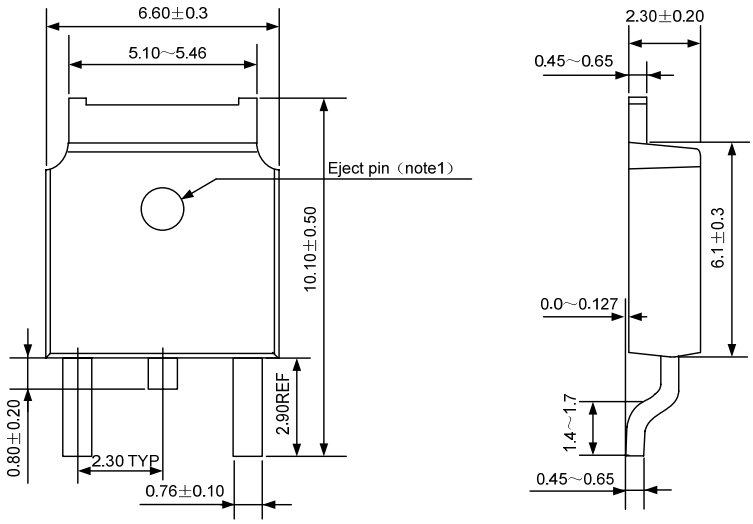


PACKAGE OUTLINE

TO-220-3L UNIT: mm



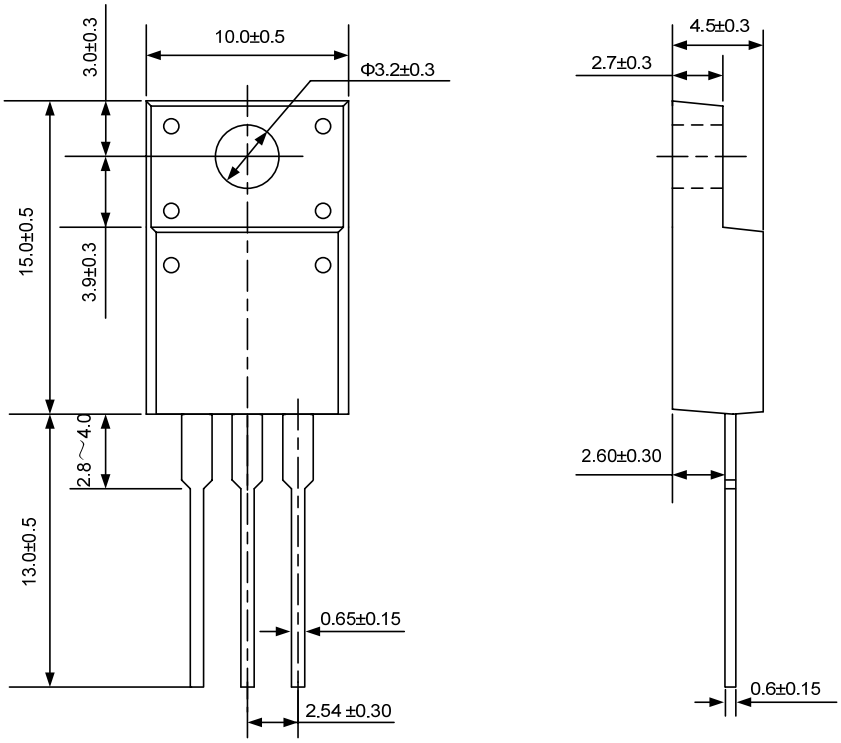
TO-252-2L UNIT: mm



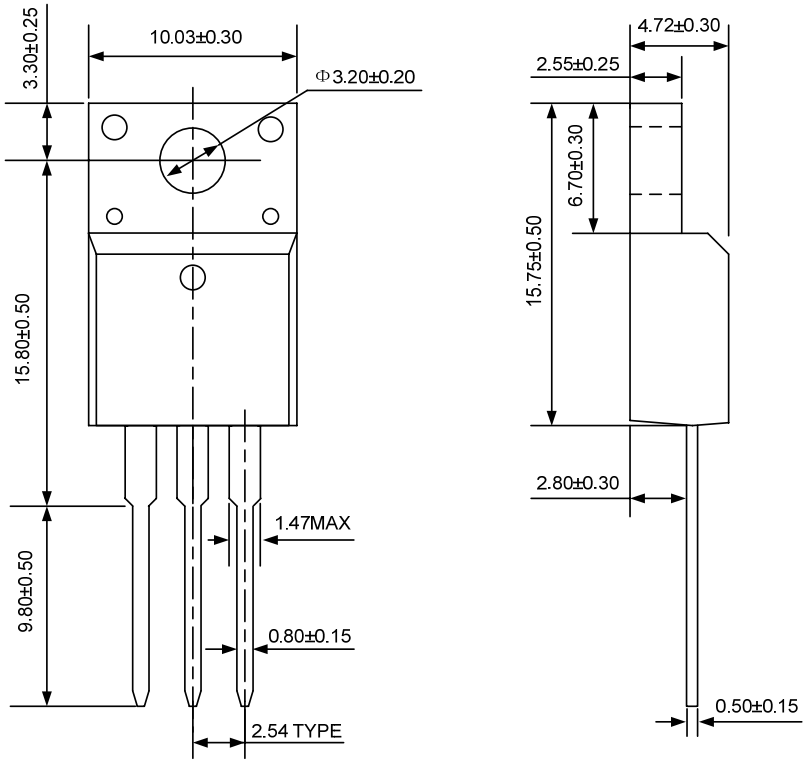
NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE (continued)

TO-220F-3L(One) UNIT: mm

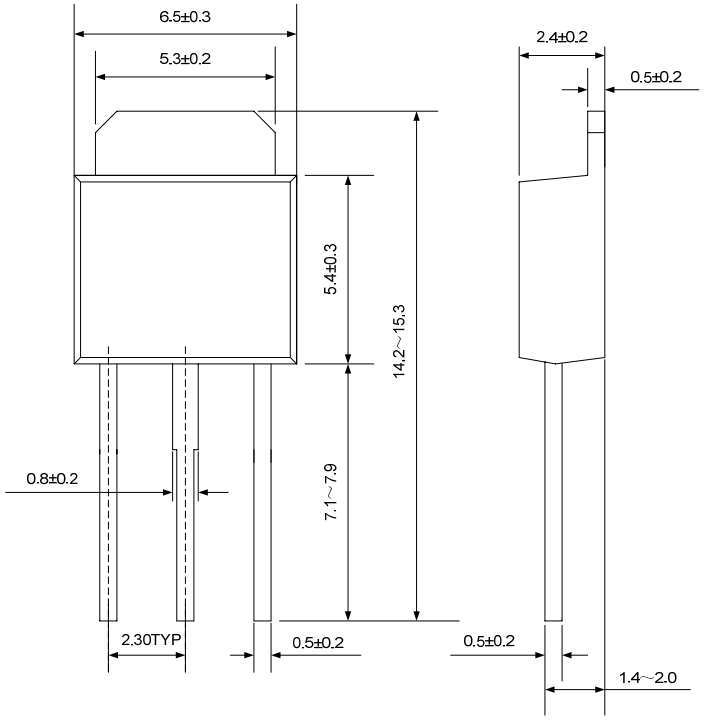


TO-220F-3L(Two) UNIT: mm

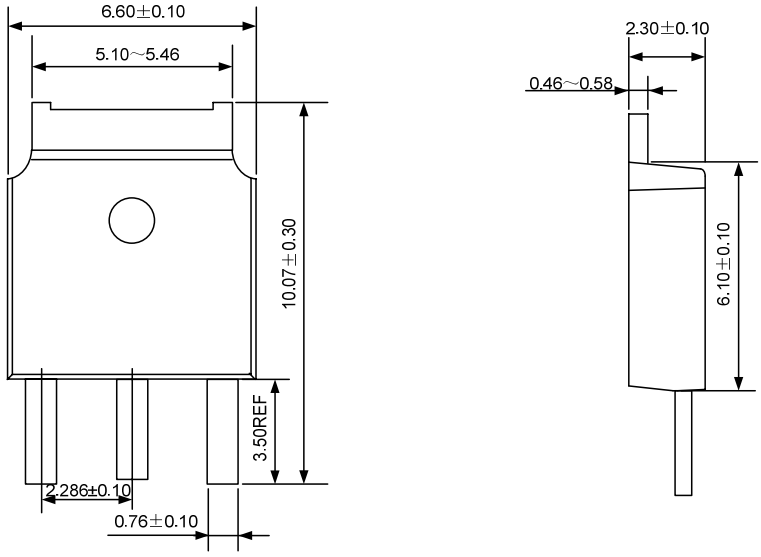


PACKAGE OUTLINE (continued)

TO-251-3L UNIT: mm



TO-251D-3L UNIT: mm



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ATTACHMENT

Revision History

Date	REV	Description	Page
2010.05.13	1.0	Original	
2010.08.20	1.1	Modify" ABSOLUTE MAXIMUM RATINGS", "THERMAL CHARACTERISTICS"; Add SOA &ID-TC	
2010.10.18	1.2	Modify "TYPICAL CHARACTERISTICS", "PACKAGE OUTLINE", the template of Datasheet	
2011.06.28	1.3	Modify the "PACKAGE OUTLINE(continued)" Add the package of TO-251D-3L	8 9