

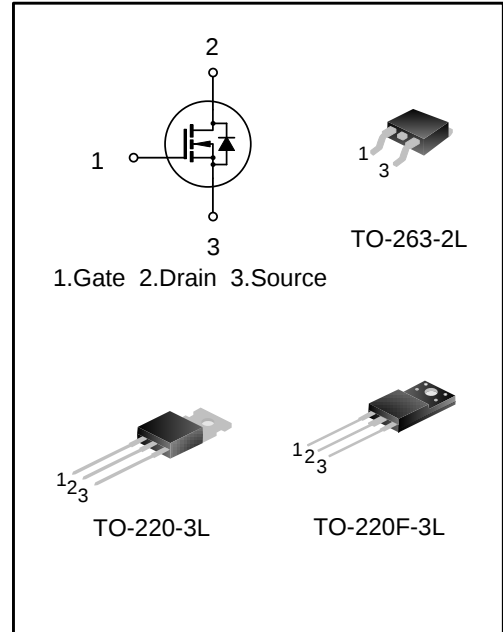
## 110A, 55V N-CHANNEL MOSFET

### DESCRIPTION

SVD3205T/F/S is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary flat low-voltage structure VDMOS technology. The improved process and cell structure have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. It can be widely used in electronic ballast, low-power SWPS.

### FEATURES

- ◆ 110A, 55V,  $R_{DS(on)(typ.)}=7.5m\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low  $C_{rss}$
- ◆ Fast switching
- ◆ Improved dv/dt capability



### ORDERING INFORMATION

| Part No.   | Package    | Marking  | Hazardous Substance Control | Packing Type |
|------------|------------|----------|-----------------------------|--------------|
| SVD3205T   | TO-220-3L  | SVD3205T | Pb free                     | Tube         |
| SVD3205F   | TO-220F-3L | SVD3205F | Pb free                     | Tube         |
| SVD3205S   | TO-263-2L  | SVD3205S | Halogen free                | Tube         |
| SVD3205STR | TO-263-2L  | SVD3205S | Halogen free                | Tape&Reel    |

### ABSOLUTE MAXIMUM RATINGS (UNLESS OTHERWISE NOTED, $T_A=25^{\circ}C$ )

| Characteristics                                                |                       | Symbol           | Ratings  |          |          | Unit |
|----------------------------------------------------------------|-----------------------|------------------|----------|----------|----------|------|
|                                                                |                       |                  | SVD3205T | SVD3205F | SVD3205S |      |
| Drain-Source Voltage                                           |                       | V <sub>DS</sub>  | 55       |          |          | V    |
| Gate-Source Voltage                                            |                       | V <sub>GS</sub>  | ±20      |          |          | V    |
| Drain Current                                                  | T <sub>C</sub> =25°C  | I <sub>D</sub>   | 110      |          |          | A    |
|                                                                | T <sub>C</sub> =100°C |                  | 70       |          |          |      |
| Drain Pulsed Current                                           |                       | I <sub>DM</sub>  | 390      |          |          | A    |
| Power Dissipation (T <sub>C</sub> =25°C)<br>-Derate above 25°C |                       | P <sub>D</sub>   | 200      | 58       | 190      | W    |
|                                                                |                       |                  | 1.6      | 0.46     | 1.52     | W/°C |
| Single Pulsed Avalanche Energy (Note 1)                        |                       | E <sub>AS</sub>  | 909      |          |          | MJ   |
| Operation Junction Temperature Range                           |                       | T <sub>J</sub>   | -55~+150 |          |          | °C   |
| Storage Temperature Range                                      |                       | T <sub>stg</sub> | -55~+150 |          |          | °C   |

## THERMAL CHARACTERISTICS

| Characteristics                         | Symbol          | Ratings  |          |          | Unit |
|-----------------------------------------|-----------------|----------|----------|----------|------|
|                                         |                 | SVD3205T | SVD3205F | SVD3205S |      |
| Thermal Resistance, Junction-to-Case    | $R_{\theta JC}$ | 0.63     | 2.16     | 0.66     | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5     | 62.5     | 62.5     | °C/W |

## ELECTRICAL CHARACTERISTICS (UNLESS OTHERWISE NOTED, $T_J=25^{\circ}\text{C}$ )

| Characteristics                             | Symbol       | Test conditions                                  | Min. | Typ. | Max.      | Unit       |
|---------------------------------------------|--------------|--------------------------------------------------|------|------|-----------|------------|
| Drain-Source Breakdown Voltage              | $BV_{DSS}$   | $V_{GS}=0V, I_D=250\mu A$                        | 55   | --   | --        | V          |
| Drain-Source Leakage Current                | $I_{DSS}$    | $V_{DS}=55V, V_{GS}=0V$                          | --   | --   | 1.0       | $\mu A$    |
| Gate-Source Leakage Current                 | $I_{GSS}$    | $V_{GS}=\pm 20V, V_{DS}=0V$                      | --   | --   | $\pm 100$ | nA         |
| Gate Threshold Voltage                      | $V_{GS(th)}$ | $V_{GS}=V_{DS}, I_D=250\mu A$                    | 2.0  | --   | 3.5       | V          |
| Static Drain- Source<br>On State Resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=62A$                            | --   | 7.5  | 8.0       | m $\Omega$ |
| Input Capacitance                           | $C_{iss}$    | $V_{DS}=25V, V_{GS}=0V, f=1.0MHz$                | --   | 2365 | --        | pF         |
| Output Capacitance                          | $C_{oss}$    |                                                  | --   | 740  | --        |            |
| Reverse Transfer Capacitance                | $C_{rss}$    |                                                  | --   | 169  | --        |            |
| Turn-on Delay Time                          | $t_{d(on)}$  | $V_{DD}=28V, V_{GS}=10V, I_D=62A$<br>(Notes 2,3) | --   | 28   | --        | ns         |
| Turn-on Rise Time                           | $t_r$        |                                                  | --   | 110  | --        |            |
| Turn-off Delay Time                         | $t_{d(off)}$ |                                                  | --   | 159  | --        |            |
| Turn-off Fall Time                          | $t_f$        |                                                  | --   | 138  | --        |            |
| Total Gate Charge                           | $Q_g$        | $V_{DS}=44V, V_{GS}=10V, I_D=62A$<br>(Notes 2,3) | --   | 67   | --        | nC         |
| Gate-Source Charge                          | $Q_{gs}$     |                                                  | --   | 13   | --        |            |
| Gate-Drain Charge                           | $Q_{gd}$     |                                                  | --   | 35   | --        |            |

## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

| Characteristics           | Symbol   | Test conditions                                      | Min. | Typ. | Max. | Unit    |
|---------------------------|----------|------------------------------------------------------|------|------|------|---------|
| Continuous Source Current | $I_S$    | Integral Reverse p-n Junction<br>Diode in the MOSFET | --   | --   | 110  | A       |
| Pulsed Source Current     | $I_{SM}$ |                                                      | --   | --   | 390  |         |
| Diode Forward Voltage     | $V_{SD}$ | $I_S=110A, V_{GS}=0V$                                | --   | --   | 1.3  | V       |
| Reverse Recovery Time     | $T_{rr}$ | $I_S=110A, V_{GS}=0V$<br>$di/dt=100A/\mu s$ (Note 2) | --   | 67   | --   | ns      |
| Reverse Recovery Charge   | $Q_{rr}$ |                                                      | --   | 0.17 | --   | $\mu C$ |

### Notes:

1.  $L=0.30mH, I_{AS}=63A, V_{DD}=28V, R_G=25\Omega$ , starting  $T_J=25^{\circ}\text{C}$ ;
2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ ;
3. Essentially independent of operating temperature.

**TYPICAL CHARACTERISTICS**

Figure 1. On-Region Characteristics (25°C)

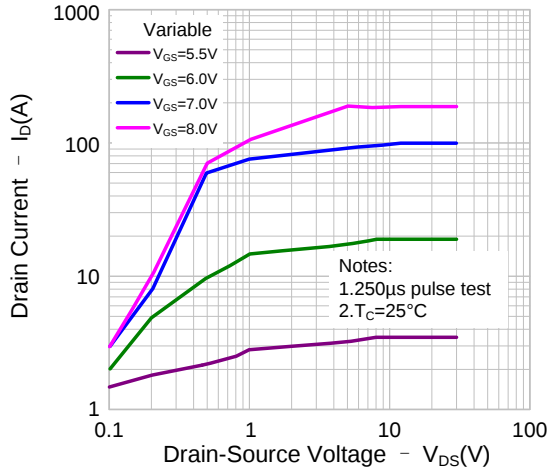


Figure 2. On-Region Characteristics (175°C)

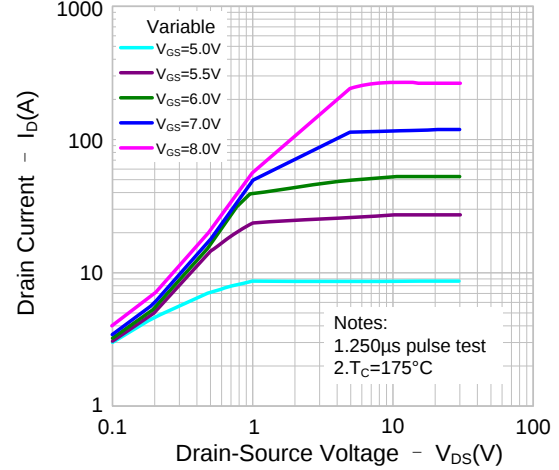


Figure 3. Transfer Characteristics

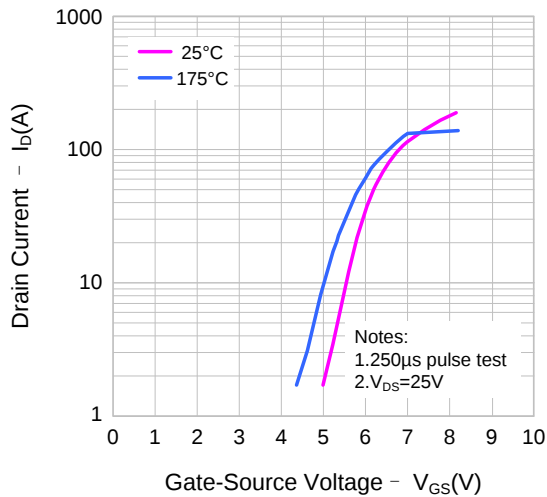


Figure 4. Source Drain Diode Forward Voltage Variation

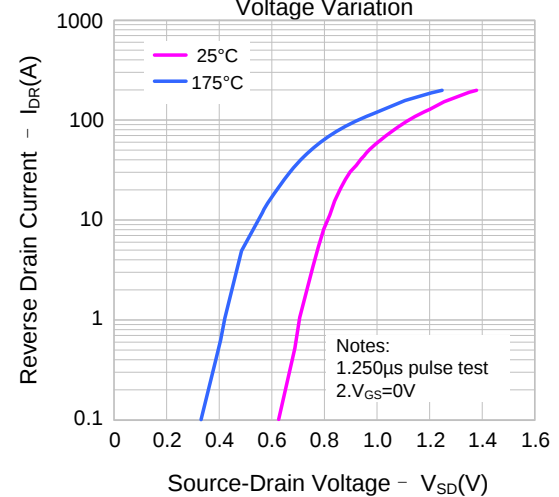


Figure 5. Capacitance Characteristics

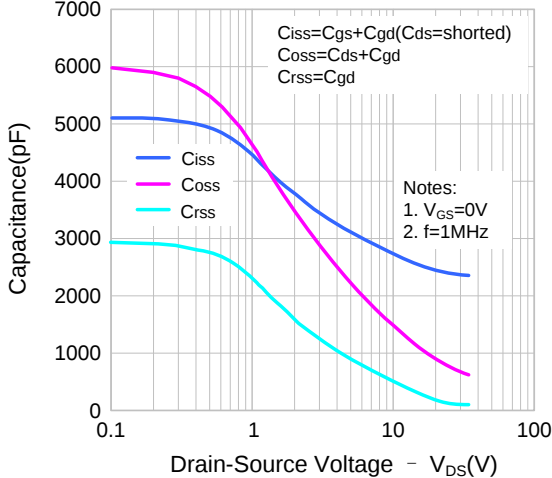
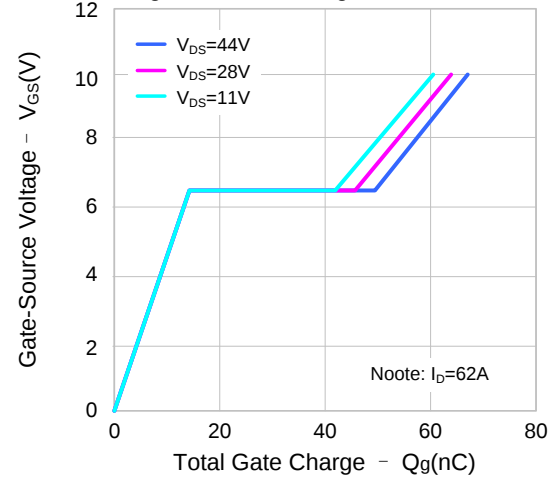
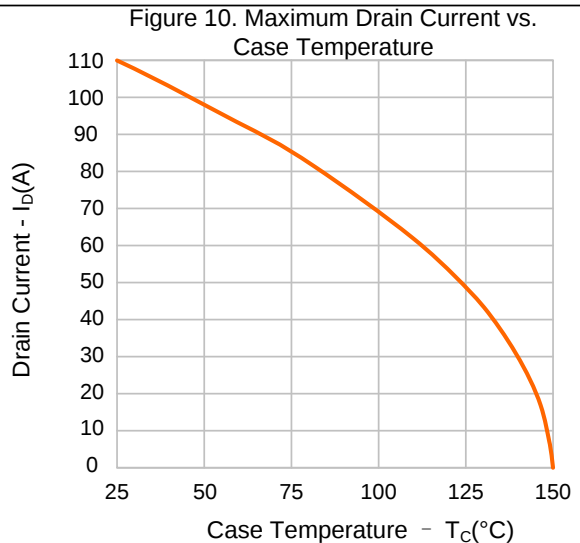
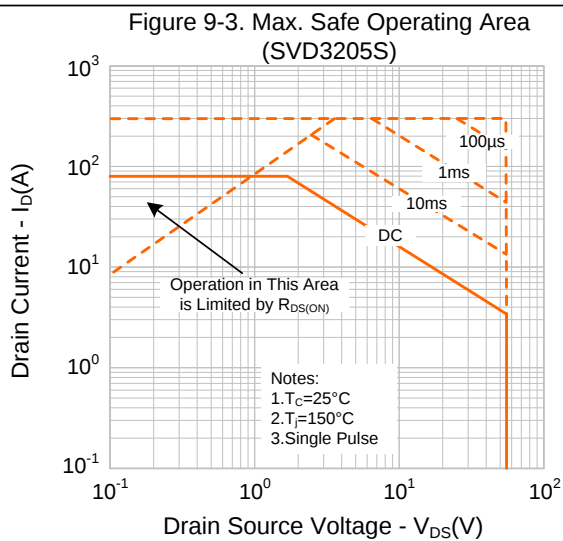
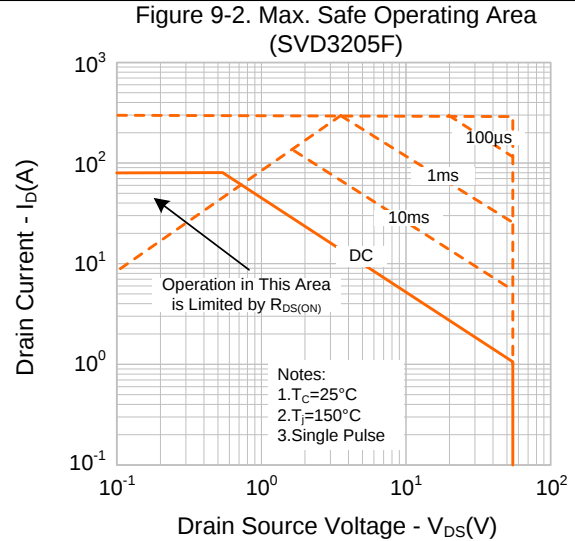
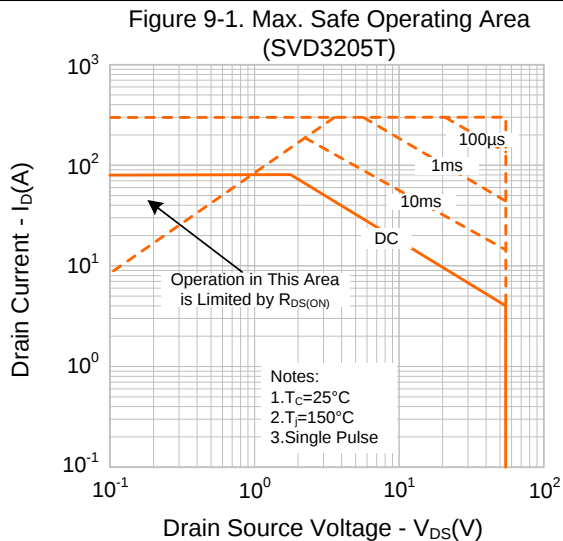
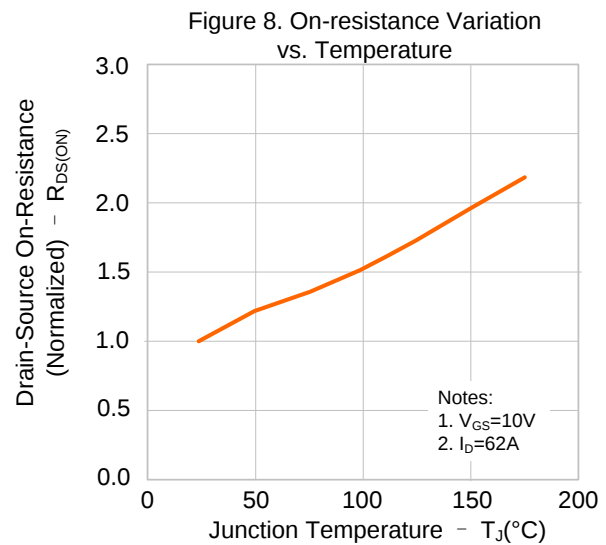
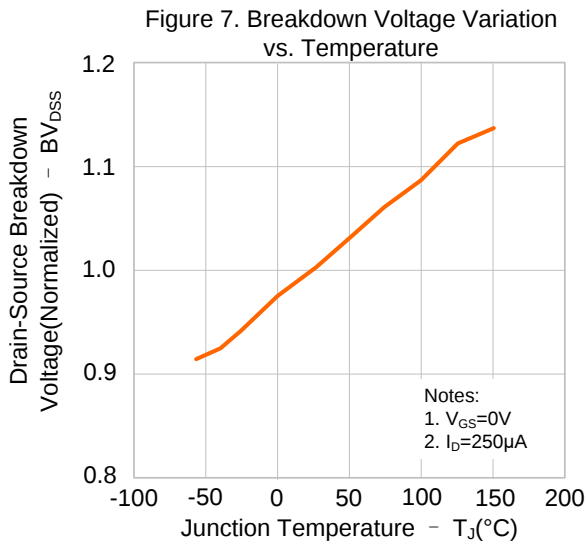


Figure 6. Gate Charge Characteristics

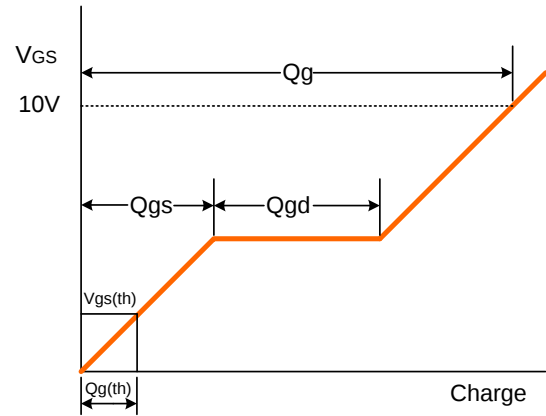
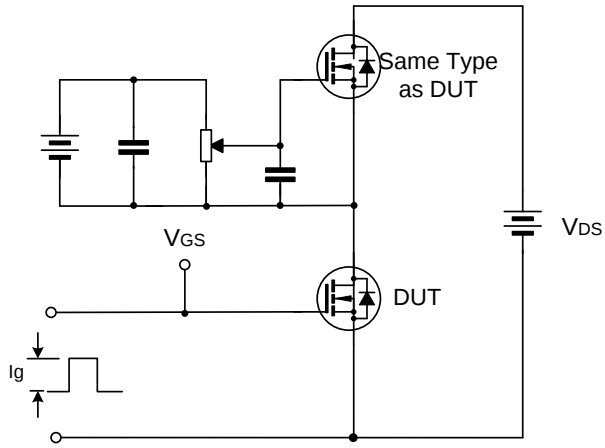


**TYPICAL CHARACTERISTICS (CONTINUED)**

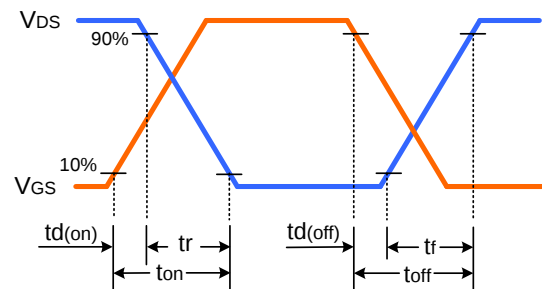
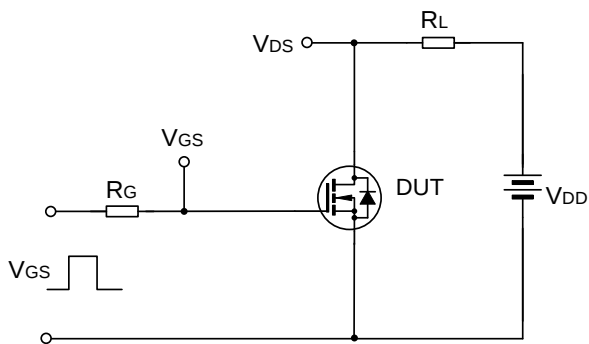


## TYPICAL TEST CIRCUIT

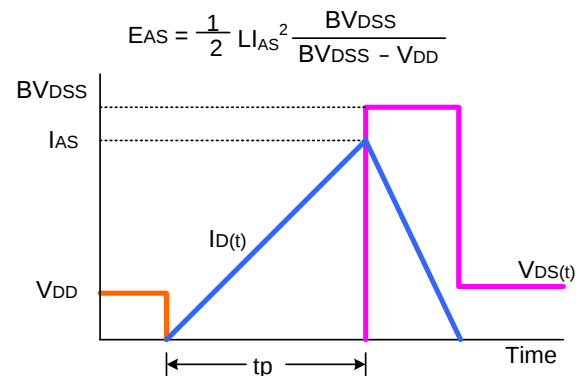
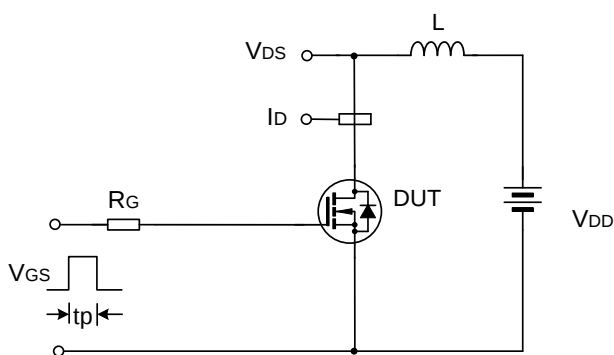
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



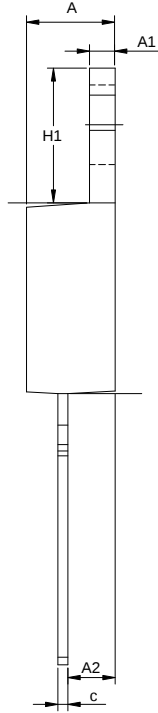
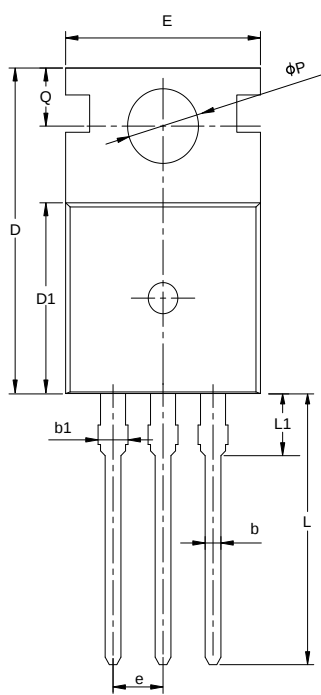
Unclamped Inductive Switching Test Circuit & Waveform



## PACKAGE OUTLINE

### TO-220-3L

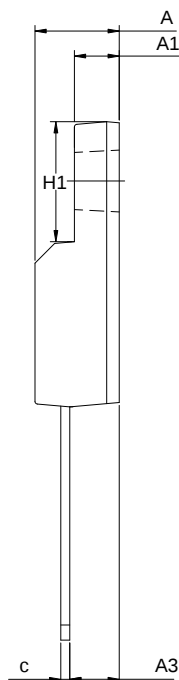
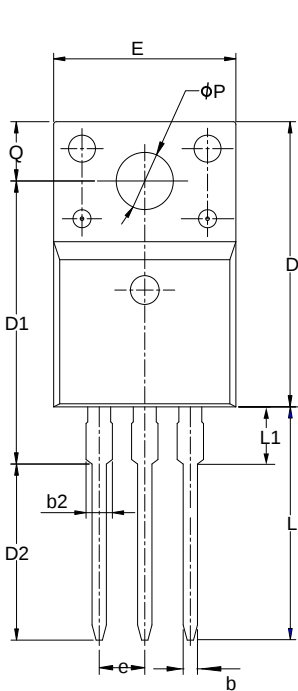
UNIT: mm



| SYMBOL   | MILLIMETER |       |       |
|----------|------------|-------|-------|
|          | MIN        | NOM   | MAX   |
| A        | 4.30       | 4.50  | 4.70  |
| A1       | 1.00       | 1.30  | 1.50  |
| A2       | 1.80       | 2.40  | 2.80  |
| b        | 0.60       | 0.80  | 1.00  |
| b1       | 1.00       | —     | 1.60  |
| c        | 0.30       | —     | 0.70  |
| D        | 15.10      | 15.70 | 16.10 |
| D1       | 8.10       | 9.20  | 10.00 |
| E        | 9.60       | 9.90  | 10.40 |
| e        | 2.54BSC    |       |       |
| H1       | 6.10       | 6.50  | 7.00  |
| L        | 12.60      | 13.08 | 13.60 |
| L1       | —          | —     | 3.95  |
| $\phi P$ | 3.40       | 3.70  | 3.90  |
| Q        | 2.60       | —     | 3.20  |

### TO-220F-3L

UNIT: mm

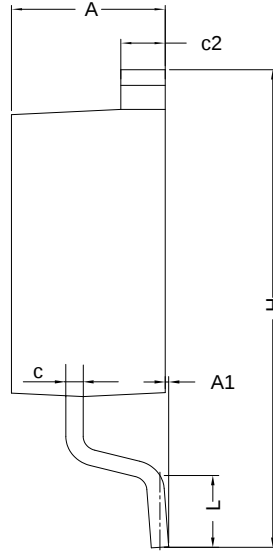
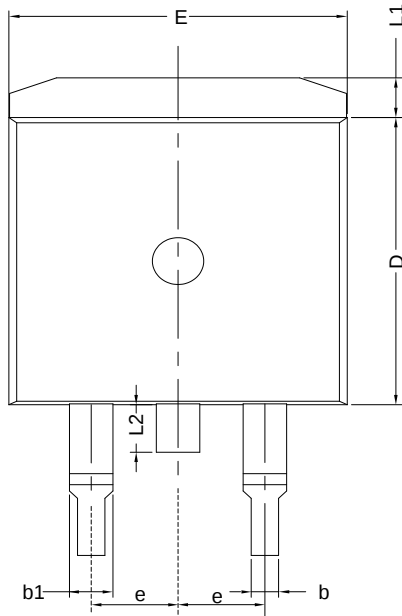


| SYMBOL   | MILLIMETER |       |       |
|----------|------------|-------|-------|
|          | MIN        | NOM   | MAX   |
| A        | 4.42       | 4.70  | 5.02  |
| A1       | 2.30       | 2.54  | 2.80  |
| A3       | 2.50       | 2.76  | 3.10  |
| b        | 0.70       | 0.80  | 0.90  |
| b2       | —          | —     | 1.47  |
| c        | 0.35       | 0.50  | 0.65  |
| D        | 15.25      | 15.87 | 16.25 |
| D1       | 15.30      | 15.75 | 16.30 |
| D2       | 9.30       | 9.80  | 10.30 |
| E        | 9.73       | 10.16 | 10.36 |
| e        | 2.54BSC    |       |       |
| H1       | 6.40       | 6.68  | 7.00  |
| L        | 12.48      | 12.98 | 13.48 |
| L1       | —          | —     | 3.50  |
| $\phi P$ | 3.00       | 3.18  | 3.40  |
| Q        | 3.05       | 3.30  | 3.55  |

## PACKAGE OUTLINE (CONTINUED)

TO-263-2L

UNIT: mm



| SYMBOL | MILLIMETER |      |       |
|--------|------------|------|-------|
|        | MIN        | NOM  | MAX   |
| A      | 4.30       | 4.57 | 4.72  |
| A1     | 0          | 0.10 | 0.25  |
| b      | 0.71       | 0.81 | 0.91  |
| b1     | 1.17       | —    | 1.50  |
| c      | 0.30       | —    | 0.60  |
| c2     | 1.17       | 1.27 | 1.37  |
| D      | 8.50       | —    | 9.35  |
| E      | 9.80       | —    | 10.45 |
| e      | 2.54BSC    |      |       |
| H      | 14.70      | —    | 15.75 |
| L      | 2.00       | 2.30 | 2.74  |
| L1     | 1.12       | 1.27 | 1.42  |
| L2     | —          | —    | 1.75  |

### Important notice :

1. The instructions are subject to change without notice!
2. Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current. Please read the instructions carefully before using our products, including the circuit operation precautions.
3. Our products are consumer electronic products or the other civil electronic products.
4. When using our products, please do not exceed the maximum rating of the products, otherwise the reliability of the whole machine will be affected. There is a certain possibility of failure or malfunction of any semiconductor product under specific conditions. The buyer is responsible for complying with safety standards and taking safety measures when using our products for system design, sample and whole machine manufacturing, so as to avoid potential failure risk that may cause personal injury or property loss.
5. It is strongly recommended to identify the trademark when buying our products. Please contact us if there is any question.
6. Product promotion is endless, our company will wholeheartedly provide customers with better products!
7. Website: <http://www.silan.com.cn>

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Rev.: **2.1**

Revision History:

1. Update turn-on/off time

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Rev.: **2.0**

Revision History:

1. Update electrical diagram and typical circuit diagram
2. Update curve template and important notice

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Rev.: **1.9**

Revision History:

1. Modify the  $I_D$  condition of Fig 8
2. Update the package outline of TO-220-3L, TO-220F-3L and TO-263-2L

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Rev.: **1.8**

Revision History:

1. Modify the test condition

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Rev.: **1.7**

Revision History:

1. Modify the package outline of TO-263-2L

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Rev.: **1.6**

Revision History:

1. Modify the package information of TO-220F-3L and TO-220-3L

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Rev.: **1.5**

Revision History:

1. Modify the thermal characteristics

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Rev.: **1.4**

Revision History:

1. Modify the electrical characteristics

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Rev.: **1.3**

Revision History:

1. Add the typical test circuit

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Rev.: **1.2**

Revision History:

1. Add the package of TO-220F-3L and TO-263-2L

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Rev.: **1.1**

Revision History:

1. Change the schematic diagram of MOS

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Rev.: **1.0**

Revision History:

1. Initial release
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