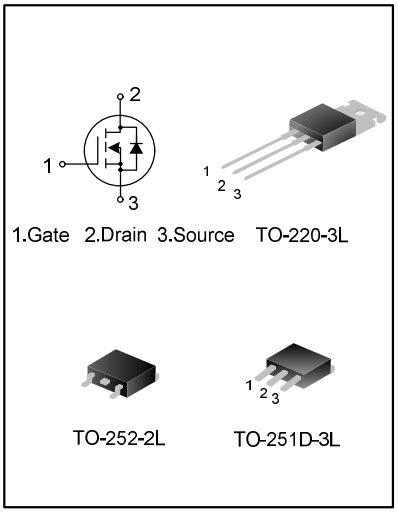
17A, 100V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD3410D/M/T is an N-channel enhancement mode high voltage MOS field effect transistor which is produced using Silan new structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

It is widely used in vehicle voltage regulator etc.



FEATURES

- 17A,100V,$R_{DS(on)(typ.)}$=68mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVD3410D	TO-252-2L	SVD3410D	Halogen free	Tube
SVD3410DTR	TO-252-2L	SVD3410D	Halogen free	Tape & Reel
SVD3410M	TO-251D-3L	SVD3410M	Halogen free	Tube
SVD3410T	TO-220-3L	SVD3410T	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating		Unit
			SVD3410D/M	SVD3410T	
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±16		V
Drain Current	T_C=25°C	I_D	17		A
	T_C=100°C		12		
Drain Current Pulsed		I_{DM}	60		A
Power Dissipation(T_C=25°C)		P_D	83	100	W
-Derate above 25°C			0.66	0.80	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	150		mJ
Operation Junction Temperature Range		T_J	-55～+175		°C
Storage Temperature Range		T_{stg}	-55～+175		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating		Unit
		SVD3410D/M	SVD3410T	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.51	1.25	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	100	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	1.0	--	2.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A	--	68	105	mΩ
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	772	--	pF
Output Capacitance	C_{oss}		--	161	--	
Reverse Transfer Capacitance	C_{rss}		--	40.3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V, V_{GS}=5V R_G=6Ω, I_D=9A	--	8.0	--	ns
Turn-on Rise Time	t_r		--	47	--	
Turn-off Delay Time	$t_{d(off)}$		--	40.67	--	
Turn-off Fall Time	t_f		--	20.2	--	
Total Gate Charge	Q_g	V_{DS}=80V, I_D=9A, V_{GS}=5V	--	17.52	--	nC
Gate-Source Charge	Q_{gs}		--	2.42	--	
Gate-Drain Charge	Q_{gd}		--	10.32	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	17	A
Pulsed Source Current	I_{SM}		--	--	60	
Diode Forward Voltage	V_{SD}	I_S=17A, V_{GS}=0V	--	--	1.3	V
Reverse Recovery Time	T_{rr}	I_S=9A, V_{DD}=50V, dI_F/dt=100A/μs (Note 2)	--	85.5	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.24	--	μC

Notes:

1. L=3.1mH,I_{AS}=9.0A, R_G=25Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

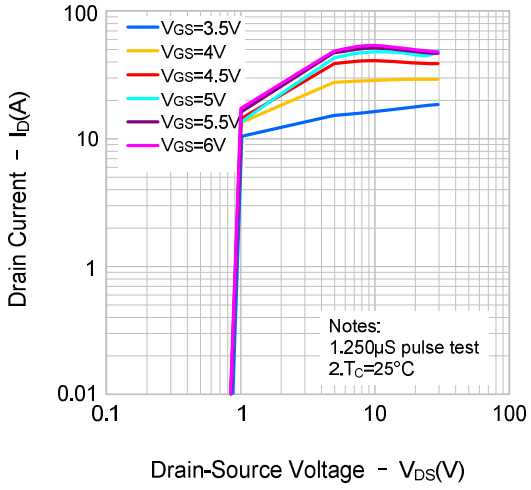


Figure 2. Transfer Characteristics

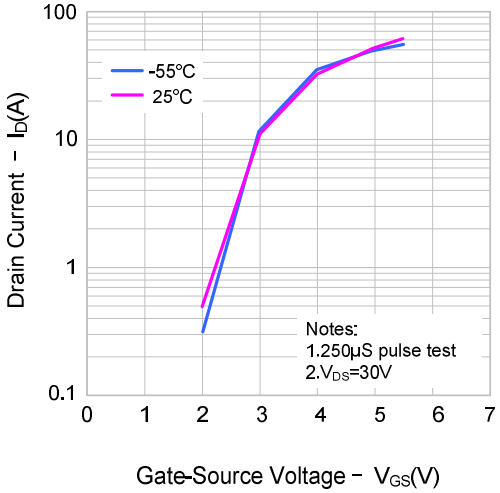


Figure 3. On-Resitance Variation vs. Drain Current

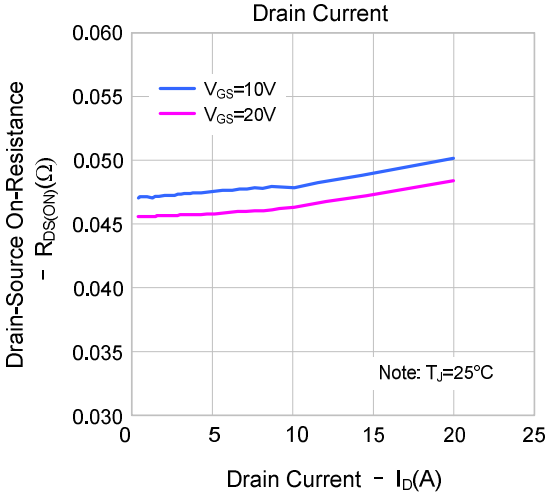


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

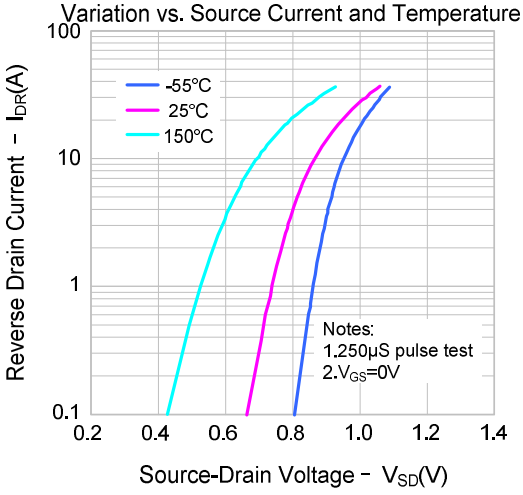


Figure 5. Capacitance Characteristics

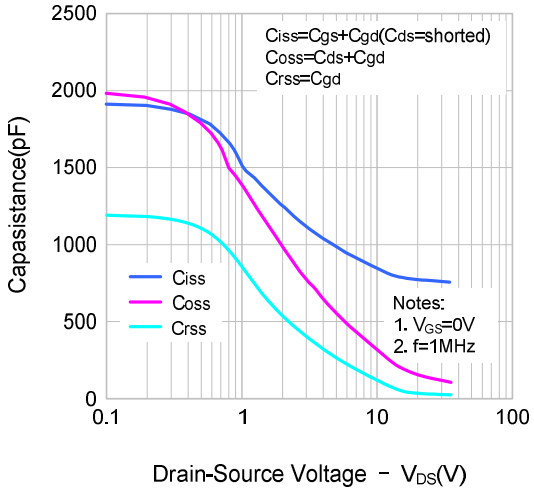
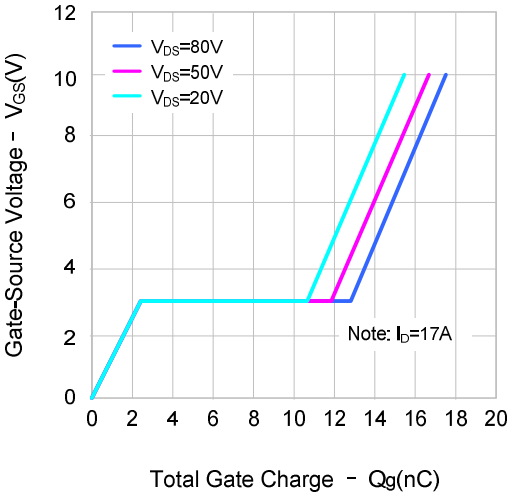


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

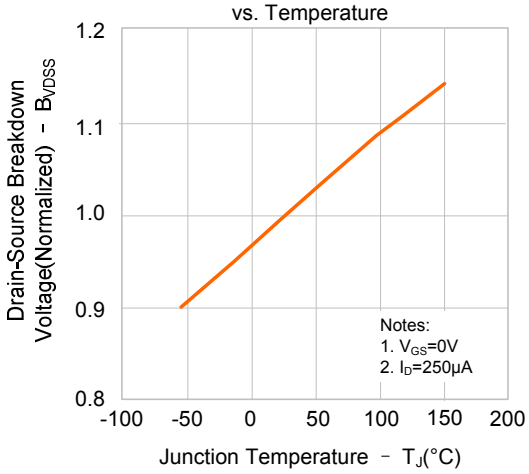


Figure 8. On-resistance Variation vs. Temperature

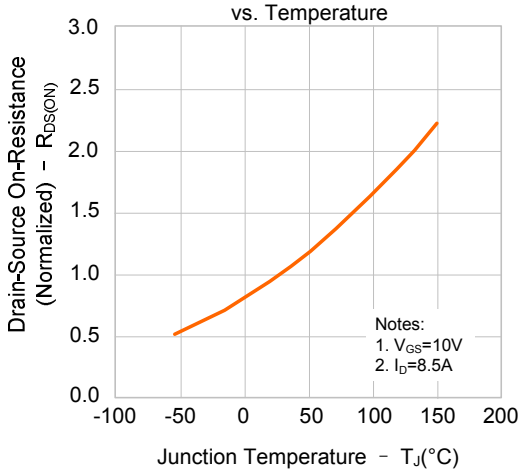


Figure 9-1. Max. Safe Operating Area(SVD3410D/M)

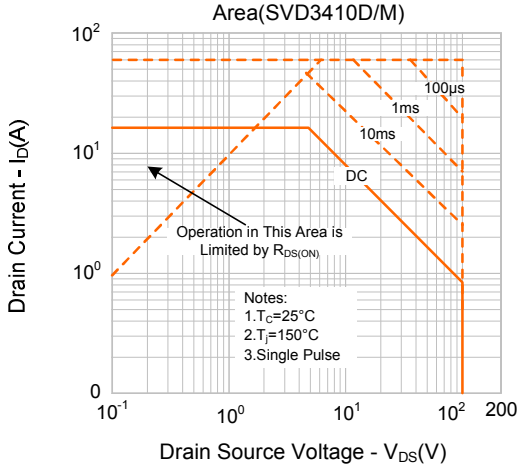


Figure 9-2. Max. Safe Operating Area(SVD3410T)

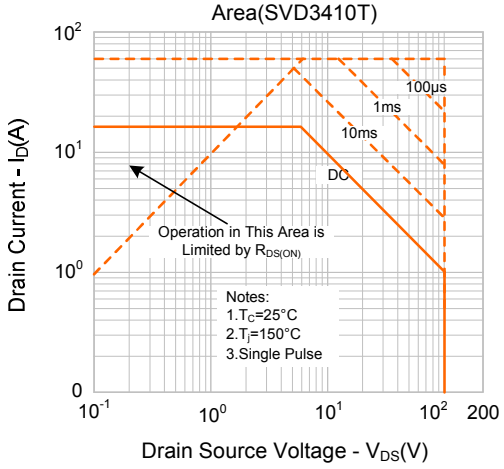
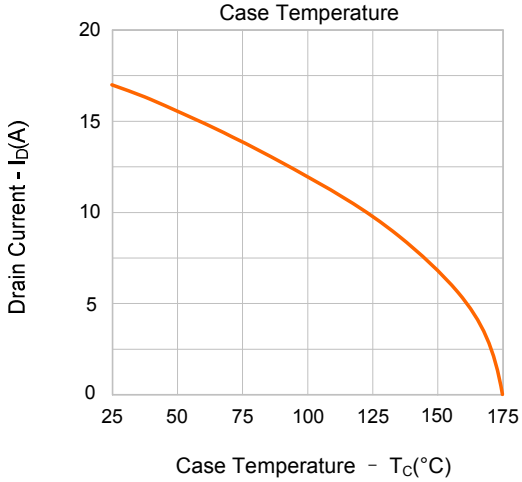
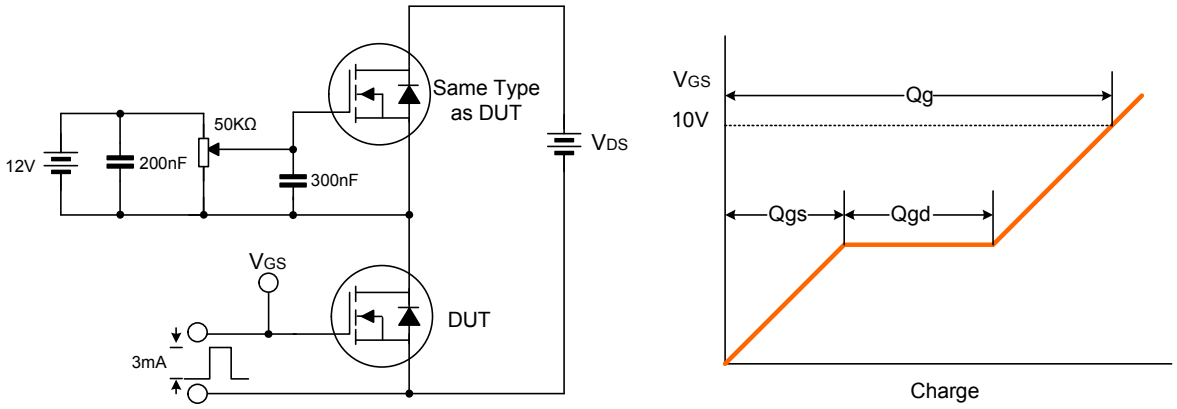


Figure 10. Maximum Drain Current vs. Case Temperature

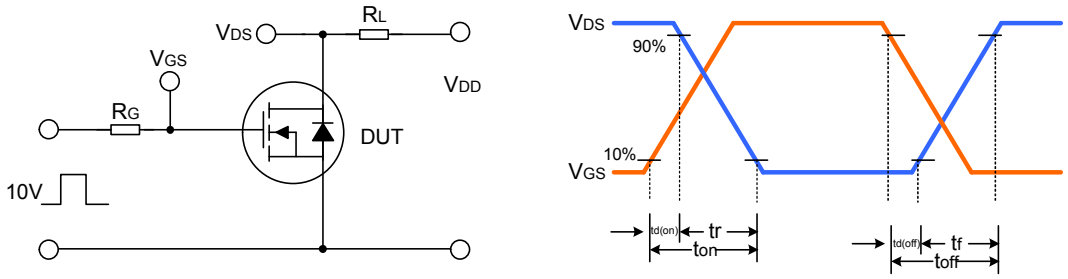


TYPICAL TEST CIRCUIT

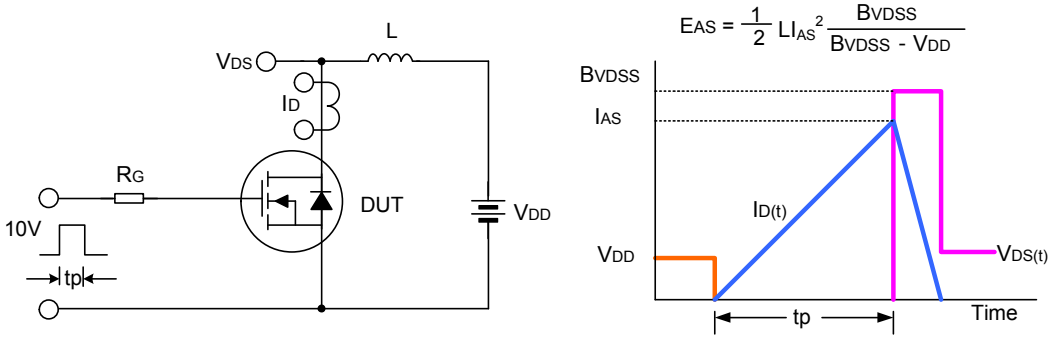
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



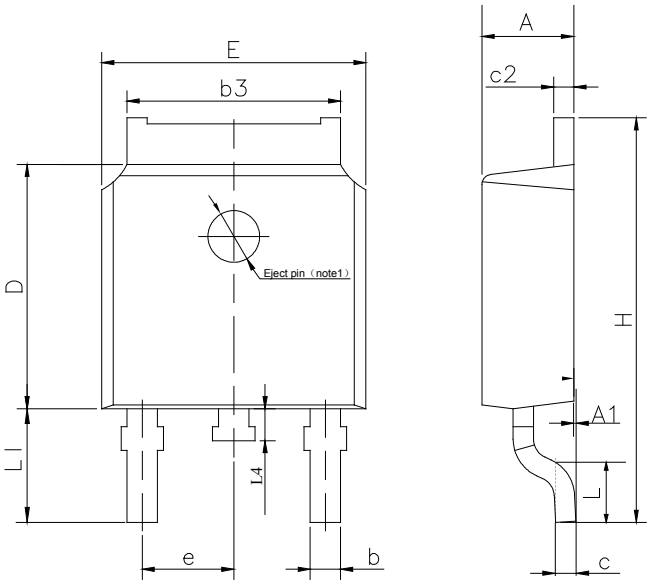
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-252-2L

UNIT: mm

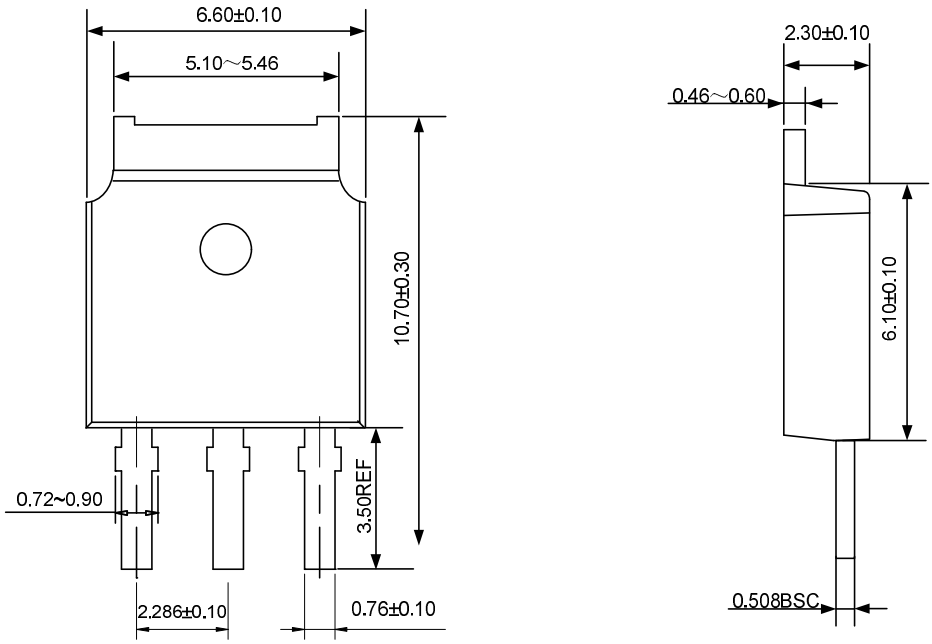


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	---	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	---	0.65
c2	0.45	---	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

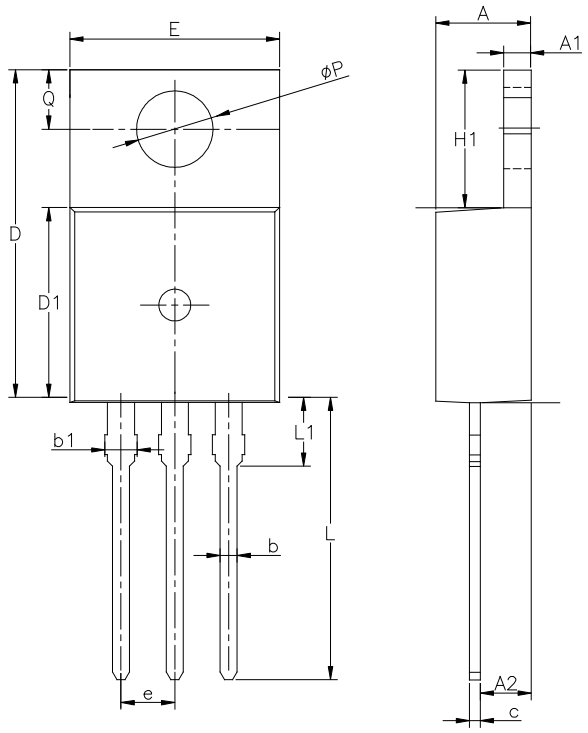
NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-251D-3L

UNIT: mm



TO-220-3L **UNIT: mm**



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

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Part No.:	SVD3410D/M/T	Document Type:	Datasheet
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Rev.:	1.5	Author:	Yin Zi

Revision History:

1. Modify the package information of TO-252-2L
2. Modify the package information of TO-220-3L

Rev.:	1.4	Author:	Yin Zi

Revision History:

1. Add the package of TO-220-3L

Rev.:	1.3	Author:	Yin Zi

Revision History:

1. Modify the thermal characteristics

Rev.:	1.2	Author:	Yin Zi

Revision History:

1. Add the package of TO-251D-3L

Rev.:	1.1	Author:	Yin Zi

Revision History:

1. Modify the electrical characteristics

Rev.:	1.0	Author:	Ma Liqing

Revision History:

1. First release