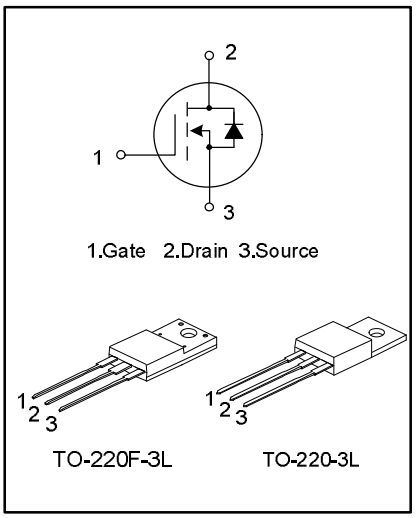
# 4A, 650V N-CHANNEL MOSFET

## GENERAL DESCRIPTION

SVD4N65T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure DMOS technology. The improved planar stripe cell and the improved guarding ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.




## FEATURES

- 4A,650V,$R_{DS(on)}$（typ）=2.3Ω@$V_{GS}$=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

## ORDERING SPECIFICATIONS

| Part No. | Package | Marking | Shipping |
|---|---|---|---|
| SVD4N65T | TO-220-3L | SVD4N65T | 50Unit/Tube |
| SVD4N65F | TO-220F-3L | SVD4N65F | 50Unit/Tube |

## ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

| Parameter | Symbol | SVD4N65T | SVD4N65F | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 650 | | V |
| Gate-Source Voltage | $V_{GS}$ | ±30 | | V |
| Drain Current | $I_D$ | 4.0 | | A |
| Drain Current Pulsed | $I_{DM}$ | 16 | | A |
| Power Dissipation($T_C$=25°C) | $P_D$ | 100 | 33 | W |
| -Derate above 25°C | | 0.8 | 0.26 | W/°C |
| Single Pulsed Avalanche Energy (Note 1) | $E_{AS}$ | 240 | | mJ |
| Repetitive Avalanche Energy | $E_{AR}$ | 10.6 | | mJ |
| Operation Junction Temperature | $T_J$ | -55～+150 | | °C |
| Storage Temperature | $T_{stg}$ | -55～+150 | | °C |

## THERMAL CHARACTERISTICS

| Parameter | Symbol | SVD4N65T | SVD4N65F | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 1.25 | 3.79 | °C/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | 62.5 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_C$=25°C unless otherwise noted)

| Parameter | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain -Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250μA | 650 | -- | -- | V |
| Drain-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=650V, $V_{GS}$=0V | -- | -- | 10 | μA |
| Gate-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±30V, $V_{DS}$=0V | -- | -- | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS}$= $V_{DS}$, $I_D$=250μA | 2.0 | -- | 4.0 | V |
| Static Drain- Source On State Resistance | $R_{DS(on)}$ | $V_{GS}$=10V, $I_D$=2A | -- | 2.3 | 3.0 | Ω |
| Forward Transconductance | $g_{FS}$ | VDS = 50 V, ID = 2 A | -- | 5.34 | -- | S |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=25V,$V_{GS}$=0V, f=1.0MHZ | -- | 556 | 710 | pF |
| Output Capacitance | $C_{oss}$ | | -- | 50 | 80 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | -- | 3 | 11 | |
| Turn-on Delay Time | $t_{d(on)}$ | $V_{DD}$=325V,$I_D$=4.0A, $R_G$=25Ω (Note 2,3) | -- | 20 | 30 | ns |
| Turn-on Rise Time | $t_r$ | | -- | 19.3 | 80 | |
| Turn-off Delay Time | $t_{d(off)}$ | | -- | 128 | 180 | |
| Turn-off Fall Time | $t_f$ | | -- | 20 | 90 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$=520V,$I_D$=4.0A, $V_{GS}$=10V (Note 2,3) | -- | 15.8 | 20 | nC |
| Gate-Source Charge | $Q_{gs}$ | | -- | 3.5 | -- | |
| Gate-Drain Charge | $Q_{gd}$ | | -- | 5.6 | -- | |

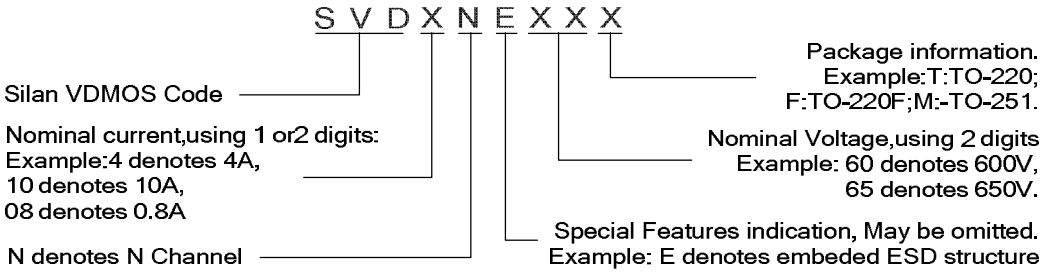
## SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

| Parameter | Symbol | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Continuous Source Current | $I_S$ | Integral Reverse P-N Junction Diode in the MOSFET | -- | -- | 4.0 | A |
| Pulsed Source Current | $I_{SM}$ | | -- | -- | 16 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=4.0A,$V_{GS}$=0V | -- | -- | 1.4 | V |
| Reverse Recovery Time | $T_{rr}$ | $I_S$=4.0A,$V_{GS}$=0V, $dI_F/dt$=100A/μs | -- | 300 | -- | ns |
| Reverse Recovery Charge | $Q_{rr}$ | | -- | 2.2 | -- | μC |

Notes:

1. L=27.5mH,$I_{AS}$=4.0A,$V_{DD}$=50V,$R_G$=25Ω,starting $T_J$=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

## NOMENCLATURE




## TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

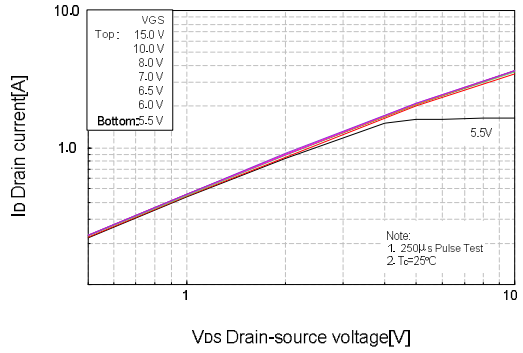



Figure 2. Transfer Characteristics

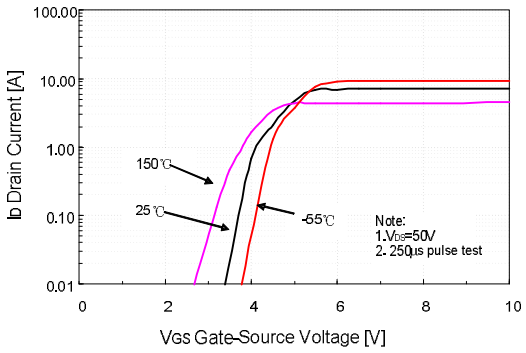



Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

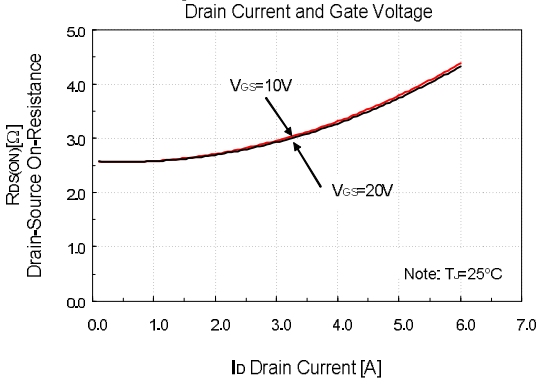
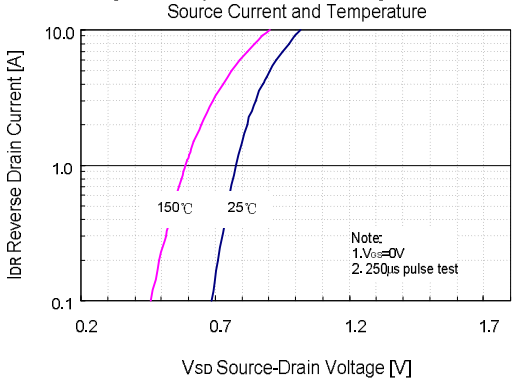



Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature



## TYPICAL CHARACTERISTICS (continued)

Figure 5. Capacitance Characteristics

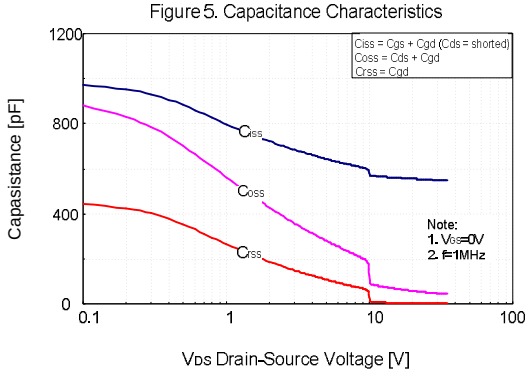



Figure 6. Gate Charge Characteristics

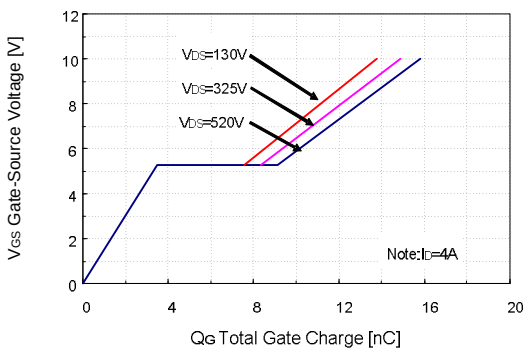



Figure 7. Breakdown Voltage Variation vs. Temperature

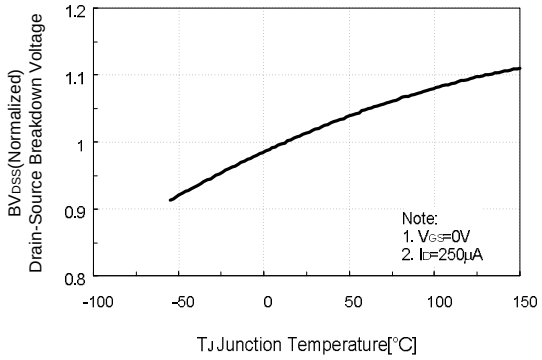
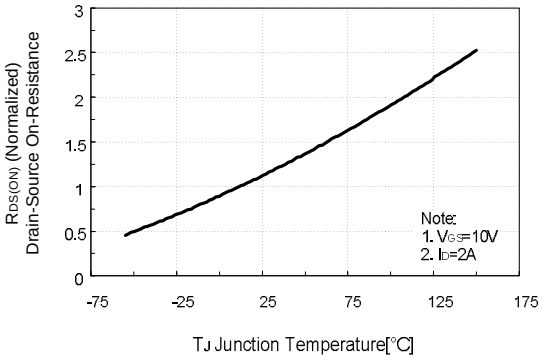
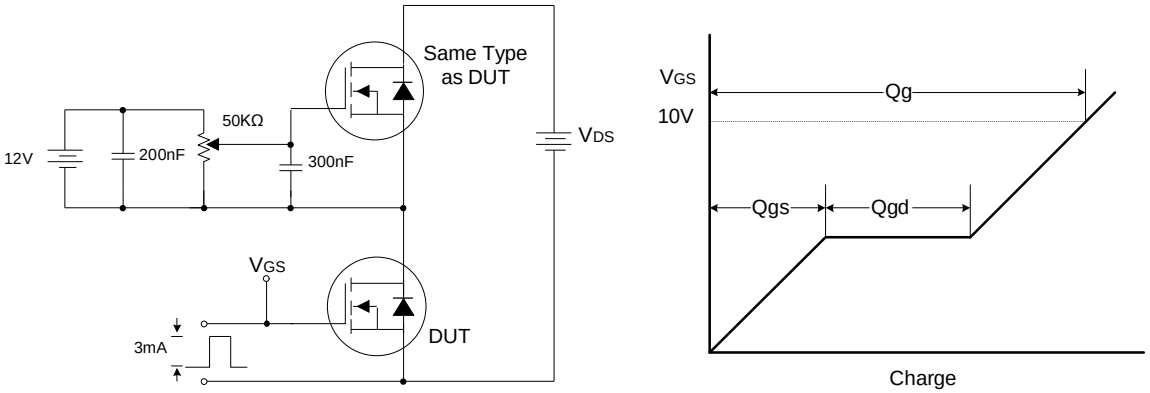



Figure 8. On-resistance Variation vs Temperature

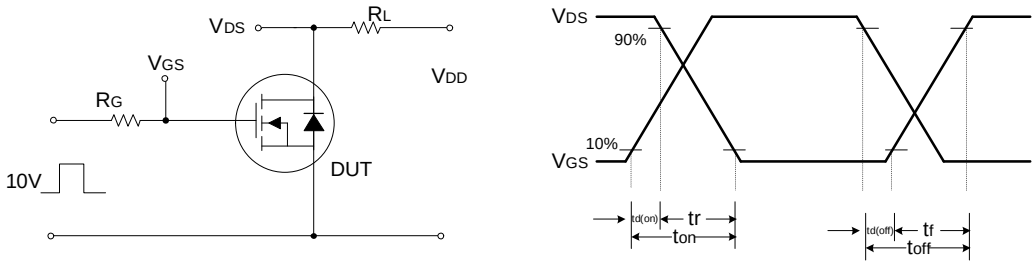


## TYPICAL TEST CIRCUIT

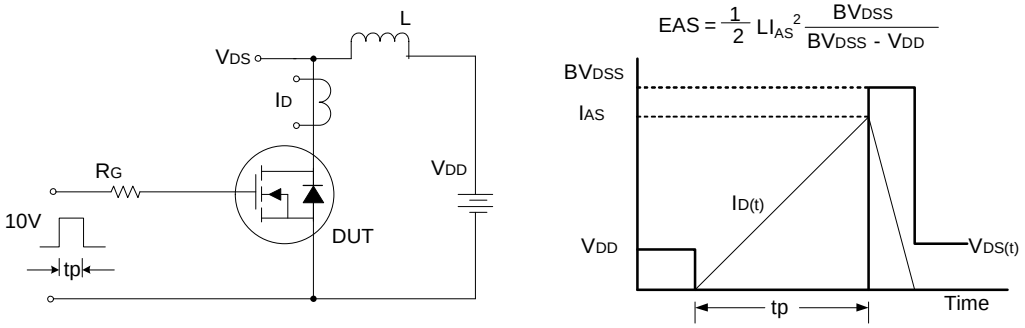
Gate Charge Test Circuit & Waveform




Resistive Switching Test Circuit & Waveform

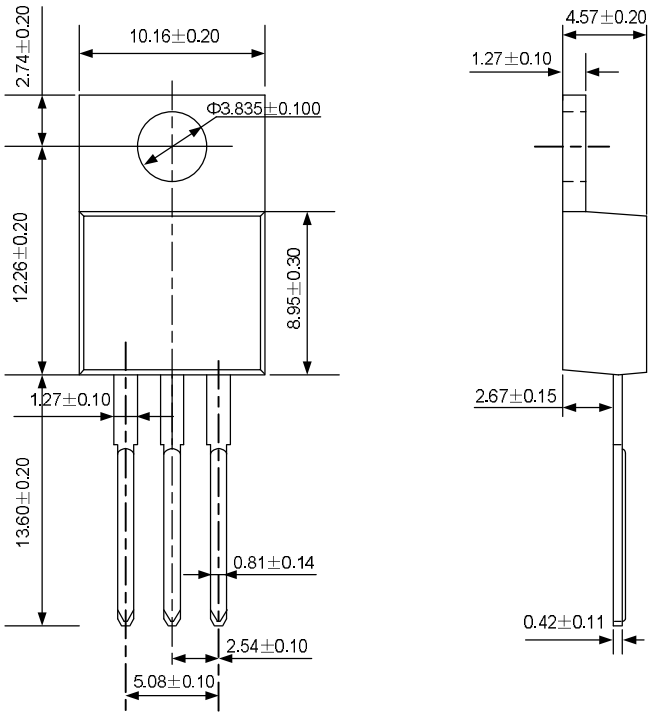



Unclamped Inductive Switching Test Circuit & Waveform

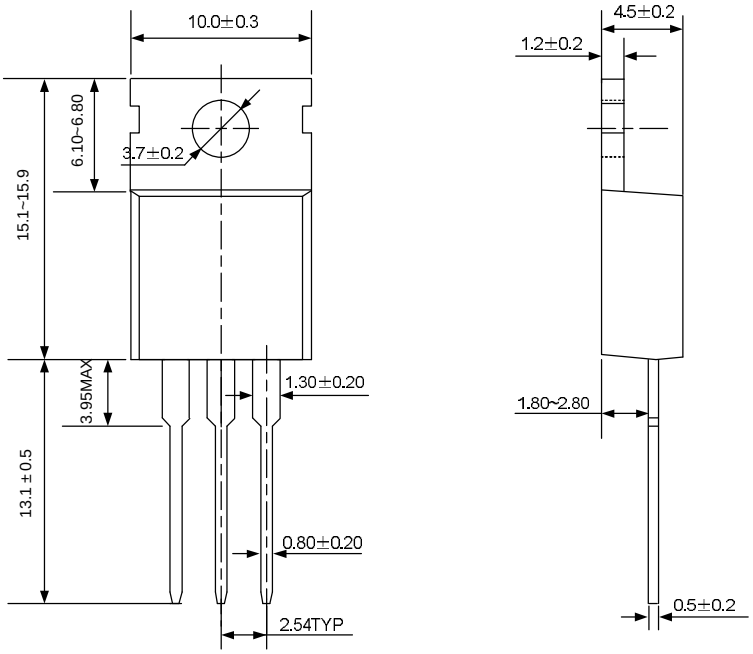


## PACKAGE OUTLINE

### TO-220-3L(One) UNIT:mm

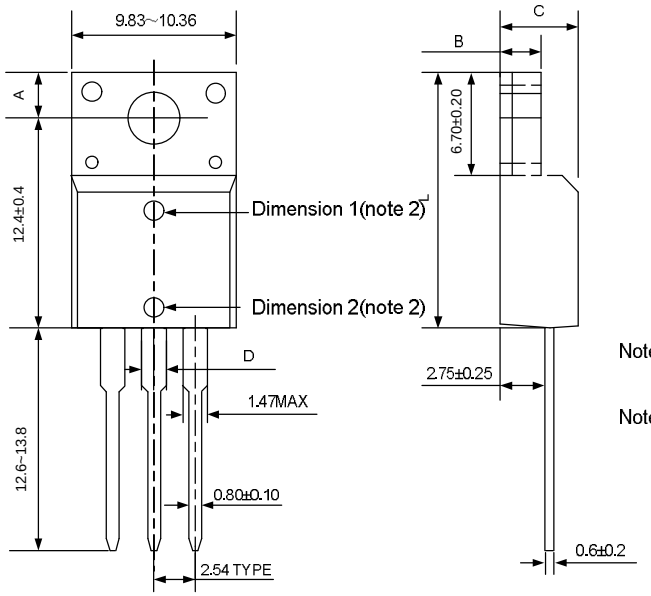



### TO-220-3L（Two） UNIT: mm



## PACKAGE OUTLINE (continued)

### TO-220F-3L(One) UNIT:mm




| Symbol(note1) | Dimension1 | Dimension2 |
|---|---|---|
| A | 3.30±0.15 | 2.70±0.15 |
| B | 2.55±0.20 | 3.0±0.20 |
| C | 4.72±0.2 | 4.50±0.20 |
| D | 1.47MAX | 1.75MAX |
| L | 15.75±0.30 | 15.00±0.30 |

Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;
Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.

### TO-220F-3L（Two） UNIT: mm