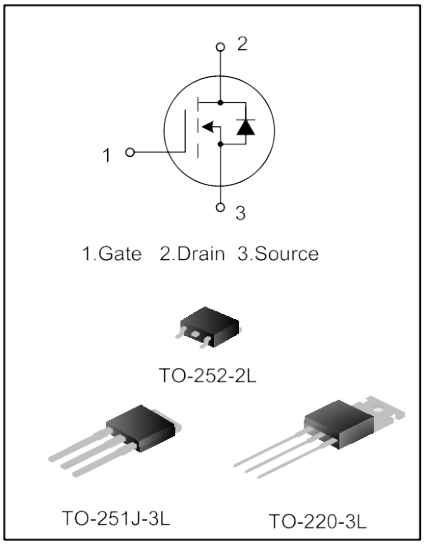
50A, 60V N-CHANNEL MOSFET

GENERAL DESCRIPTION

SVD50N06T is an N-channel enhancement mode high voltage MOS field effect transistor which is produced using Silan new structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

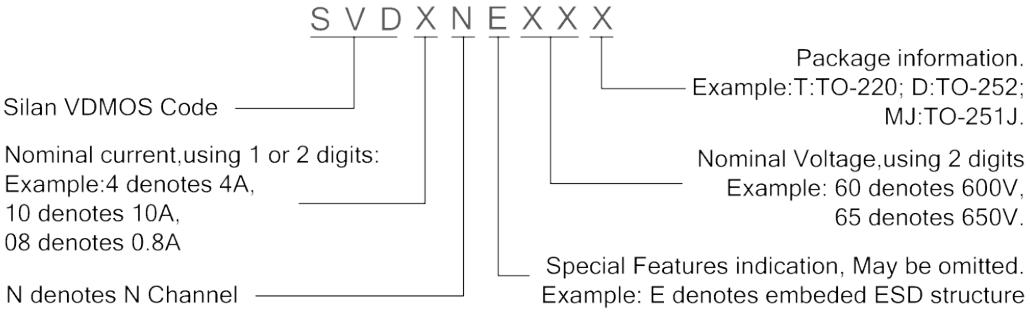
It's widely used in electronic ballasts and low power SMPS.



FEATURES

- 50A,60V,$R_{DS(on)}$ (typ) =18mΩ@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVD50N06T	TO-220-3L	SVD50N06T	Pb free	Tube
SVD50N06D	TO-252-2L	SVD50N06D	Pb free	Tube
SVD50N06DTR	TO-252-2L	SVD50N06D	Pb free	Tape & Reel
SVD50N06MJ	TO-251J-3L	SVD50N06MJ	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Characteristics		Symbol	Rating			Unit
			SVD50N06T	SVD50N06D	SVD50N06MJ	
Drain-Source Voltage		V_{DS}	60			V
Gate-Source Voltage		V_{GS}	±20			V
Drain Current	T_C=25°C	I_D	50			A
	T_C=100°C		31.62			
Drain Current Pulsed		I_{DM}	200			A
Power Dissipation(T_C=25°C)		P_D	110	72	83	W
-Derate above 25°C			0.88	0.58	0.66	W/°C
Single Pulsed Avalanche Energy(Note 1)		E_{AS}	272			mJ
Operation Junction Temperature Range		T_J	-55～+150			°C
Storage Temperature Range		T_{stg}	-55～+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Rating			Unit
		SVD50N06T	SVD50N06D	SVD50N06MJ	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.14	1.74	1.51	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.50	110	110	°C/W

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B_{VDSS}	V_{GS}=0V, I_D=250μA	60	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V	--	--	1.0	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=25A	--	18	23	mΩ
Input Capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	--	1375.8	--	pF
Output Capacitance	C_{oss}		--	393.2	--	
Reverse Transfer Capacitance	C_{rss}		--	102.6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_G=25Ω I_D=50A	--	21.67	--	ns
Turn-on Rise Time	t_r		--	86.67	--	
Turn-off Delay Time	$t_{d(off)}$		--	32.33	--	
Turn-off Fall Time	t_f		--	93	--	
Total Gate Charge	Q_g	V_{DS}=48V, I_D=50A, V_{GS}=10V	--	43.25	--	nC
Gate-Source Charge	Q_{gs}		--	8.11	--	
Gate-Drain Charge	Q_{gd}		--	23.76	--	
Gate resistance	R_G	f=1MHz, Drain Open, OSC Level: 20mv	--	2.2	--	Ω

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	50	A
Pulsed Source Current	I_{SM}		--	--	200	
Diode Forward Voltage	V_{SD}	I_S=50A, V_{GS}=0V	--	--	1.5	V
Reverse Recovery Time	T_{rr}	I_S=50A, V_{GS}=0V, dI_F/dt=100A/μs	--	67.2	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.2	--	μC

Notes:

1. L=0.1mH, I_{AS}=53A, V_{DD}=35V, R_G=20Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

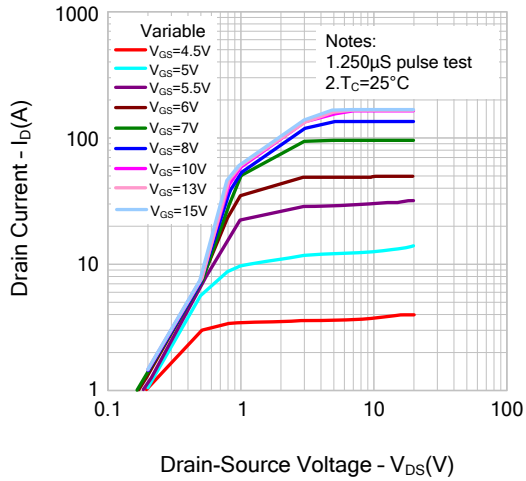


Figure 2. Transfer Characteristics

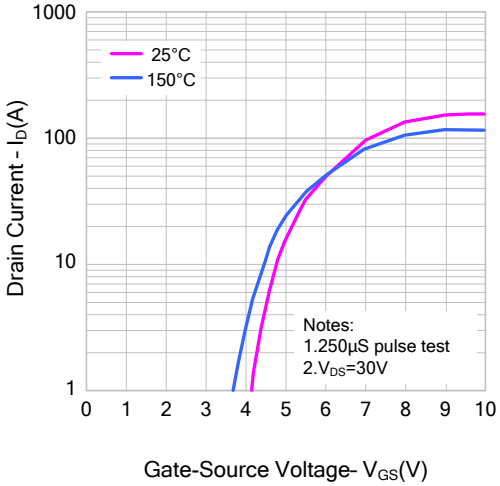


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

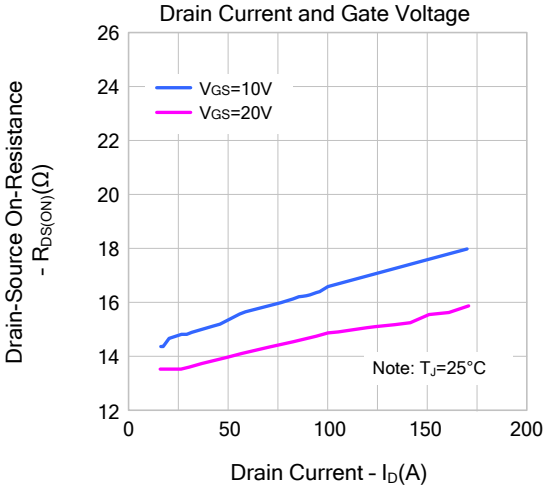


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

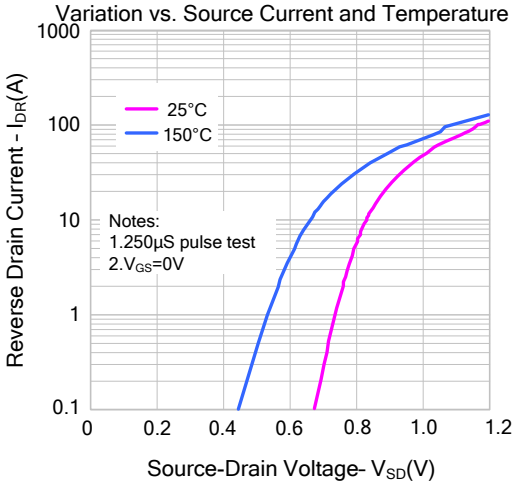


Figure 5. Capacitance Characteristics

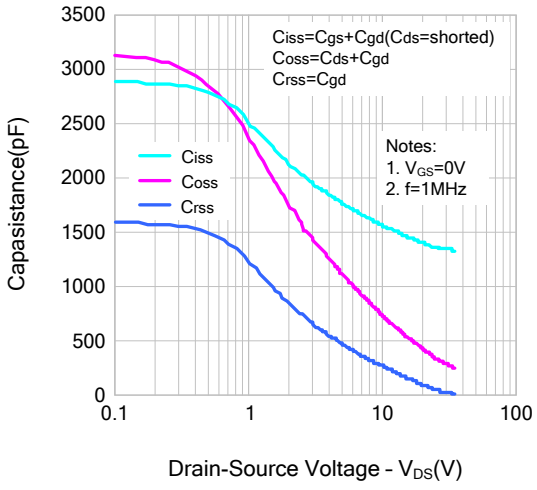
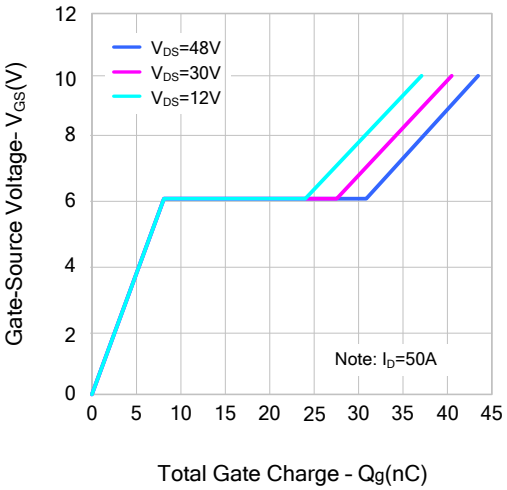


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

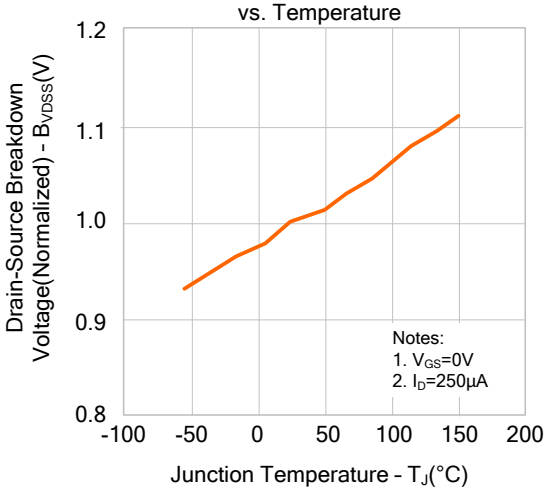


Figure 8. On-resistance Variation vs. Temperature

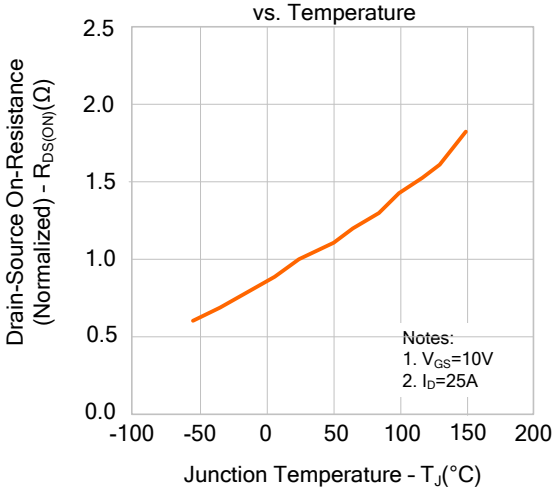


Figure 9-1. Max. Safe Operating Area(SVD50N06T)

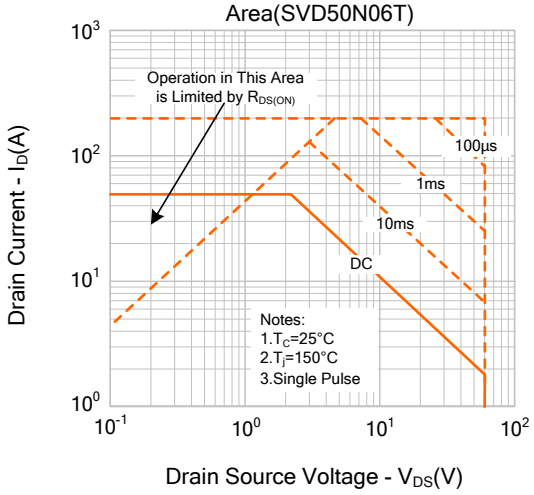


Figure 9-2. Max. Safe Operating Area(SVD50N06D)

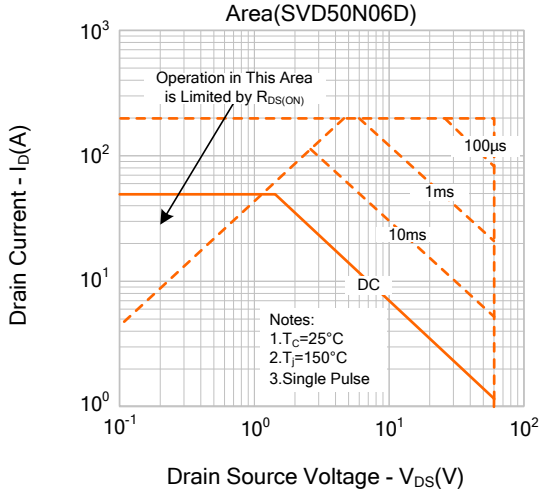


Figure 9-3. Max. Safe Operating Area(SVD50N06MJ)

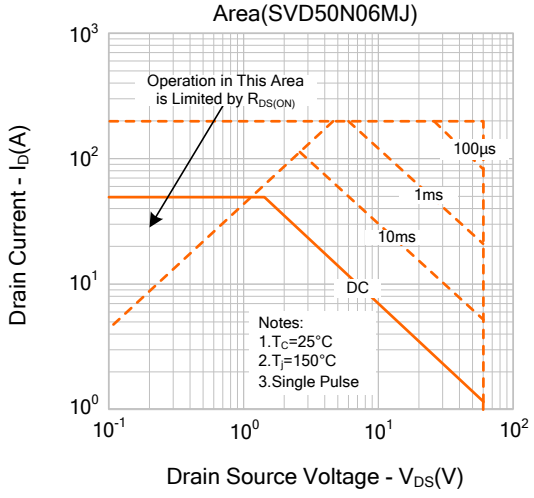
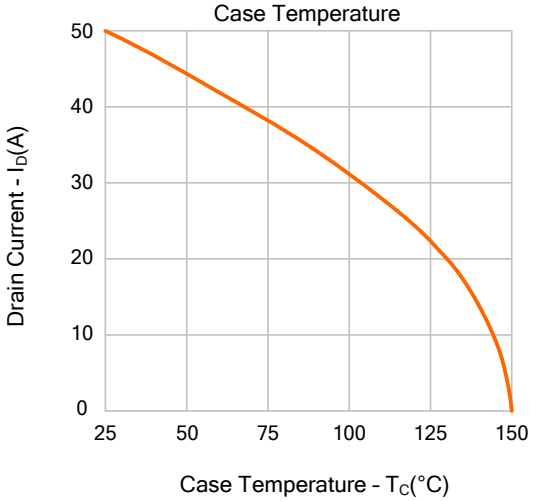
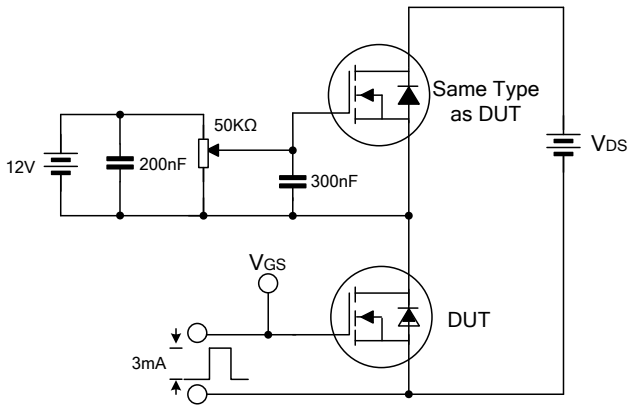


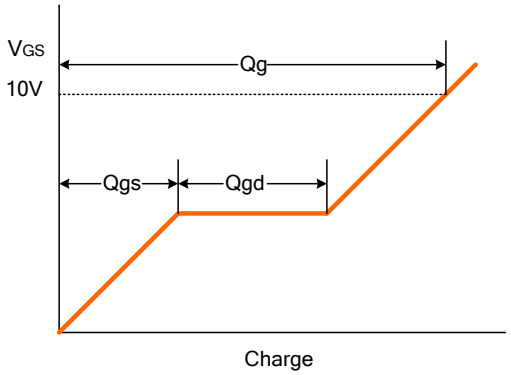
Figure 10. Maximum Drain Current vs. Case Temperature



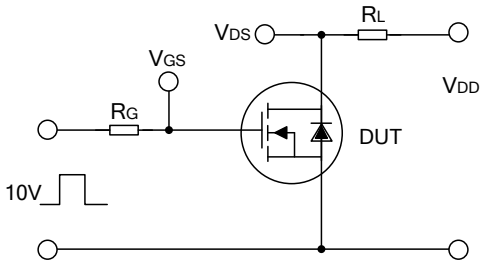
TYPICAL TEST CIRCUIT

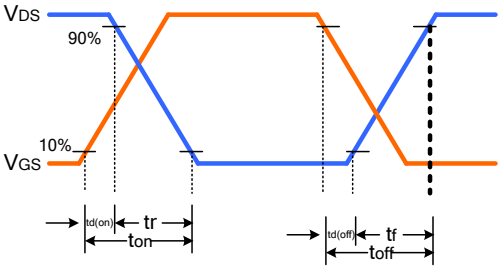
Gate Charge Test Circuit & Waveform



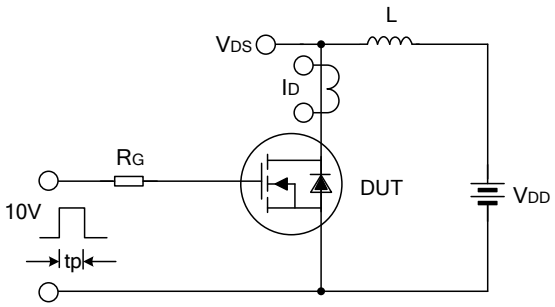


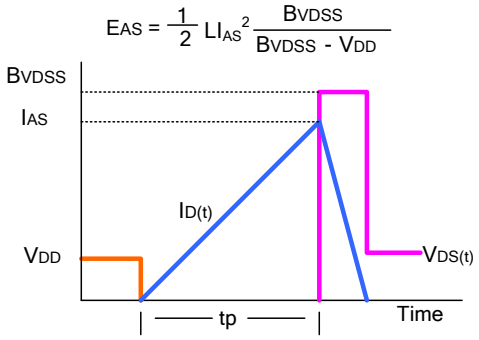
Resistive Switching Test Circuit & Waveform





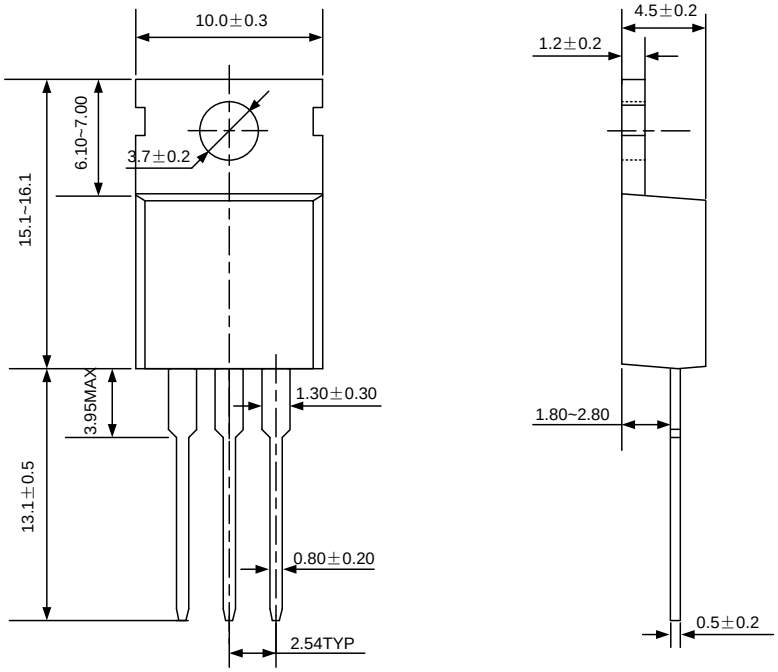
Unclamped Inductive Switching Test Circuit & Waveform



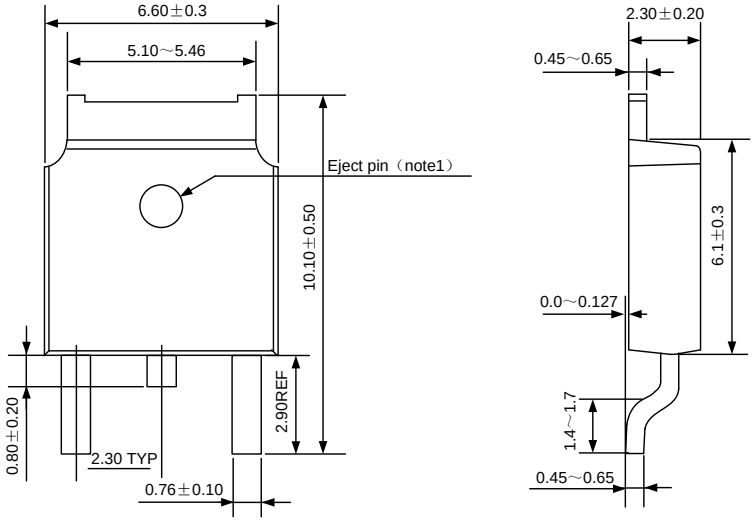


PACKAGE OUTLINE

TO-220-3L UNIT: mm



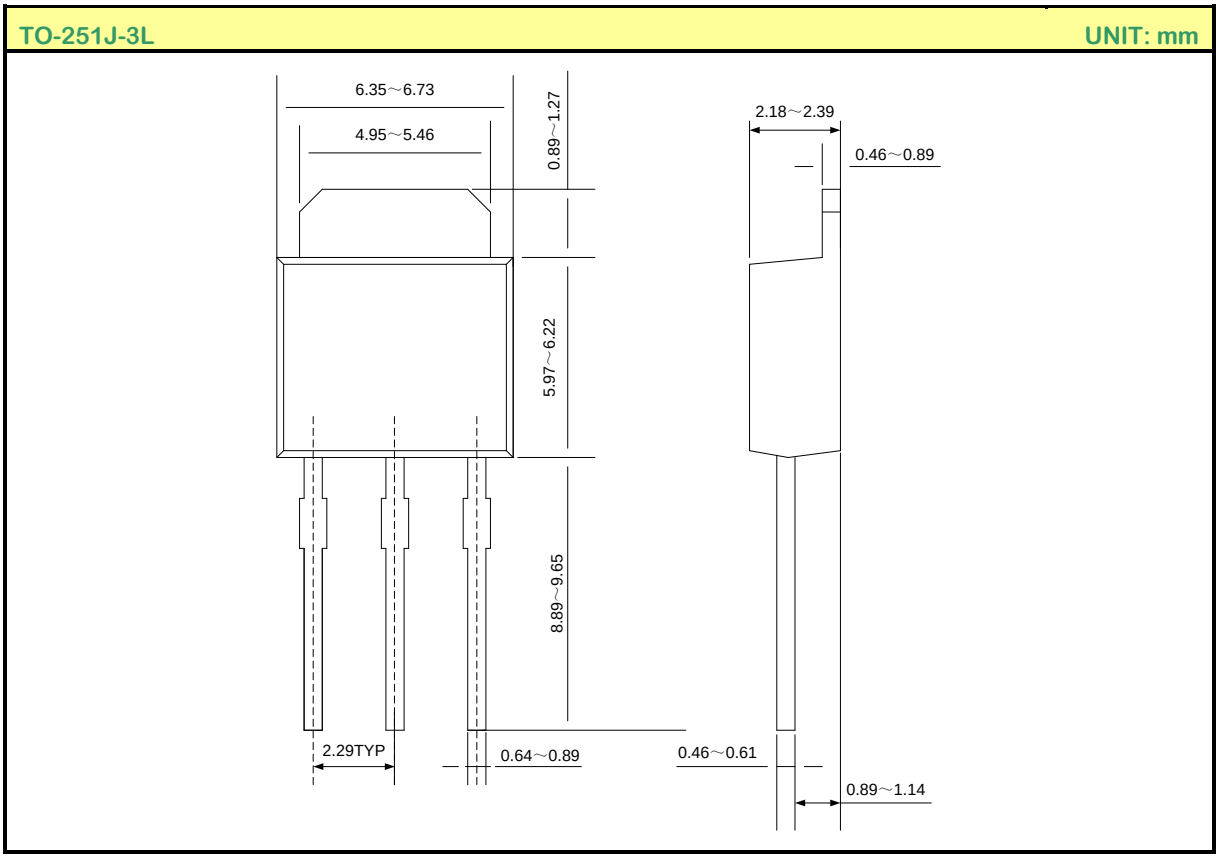
TO-252-2L UNIT: mm



NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

PACKAGE OUTLINE (continued)

TO-251J-3L UNIT: mm



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- **Silan will supply the best possible product for customers!**

ATTACHMENT

Revision History

Date	REV	Description	Page
2012.05.30	1.0	Initial release	
2013.01.21	1.1	Modify “SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS”	