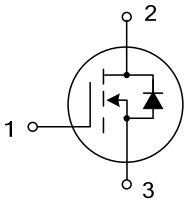
5A, 600V N-CHANNEL MOSFET

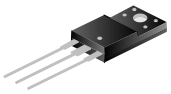
GENERAL DESCRIPTION

SVD5N60T/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin^{TM} structure DMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

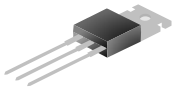
These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.



1.Gate 2.Drain 3.Source



TO-220F-3L

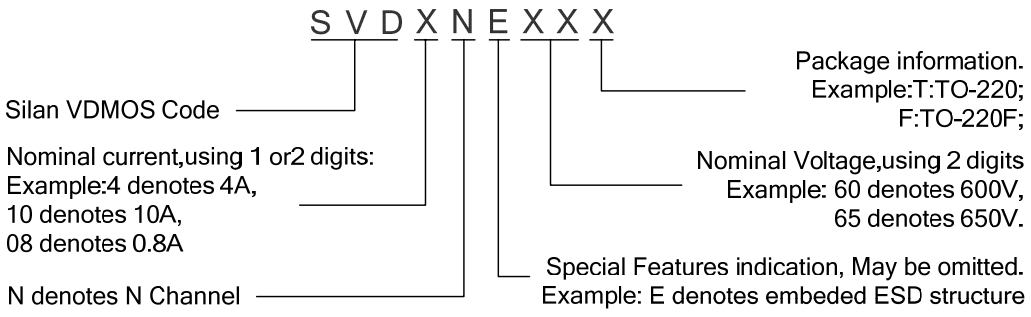


TO-220-3L

FEATURES

- 5A,600V,$R_{DS(on)}$（typ）=1.7Ω@V_{GS}=10V
- Low gate charge
- Low Crss
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING SPECIFICATIONS

Part No.	Package	Marking	Material	Packing
SVD5N60T	TO-220-3L	SVD5N60T	Pb free	Tube
SVD5N60F	TO-220F-3L	SVD5N60F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Rating		Unit
		SVD5N60T	SVD5N60F	
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	±30		V
Drain Current	I_D	5		A
Drain Current Pulsed	I_{DM}	20		A
Power Dissipation(T_C=25°C)	P_D	120	40	W
-Derate above 25°C		0.96	0.32	W/°C
Single Pulsed Avalanche Energy (Note 1)	E_{AS}	352		mJ
Operation Junction Temperature	T_J	-55～+150		°C
Storage Temperature	T_{stg}	-55～+150		°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Rating		Unit
		SVD5N60T	SVD5N60F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.04	3.13	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	120	°C/W

ELECTRICAL CHARACTERISTICS (Tc=25°C unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	600	--	--	V
Drain-Source Leakage Current	I_{DSS}	V_{DS}=600V, V_{GS}=0V	--	--	10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	--	--	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}= V_{DS}, I_D=250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2.5A	--	1.7	2.1	Ω
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHZ	--	681	--	pF
Output Capacitance	C_{oss}		--	62	--	
Reverse Transfer Capacitance	C_{rss}		--	7	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=300V,I_D=5.0A, R_G=25Ω (Note 2,3)	--	26.7	--	ns
Turn-on Rise Time	t_r		--	19	--	
Turn-off Delay Time	$t_{d(off)}$		--	160	--	
Turn-off Fall Time	t_f		--	22	--	
Total Gate Charge	Q_g	V_{DS}=480V,I_D=5.0A, V_{GS}=10V (Note 2,3)	--	19.9	--	nC
Gate-Source Charge	Q_{gs}		--	4.09	--	
Gate-Drain Charge	Q_{gd}		--	7.21	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction Diode in the MOSFET	--	--	5.0	A
Pulsed Source Current	I_{SM}		--	--	20	
Diode Forward Voltage	V_{SD}	I_S=5.0A,V_{GS}=0V	--	--	1.4	V
Reverse Recovery Time	T_{rr}	I_S=5.0A,V_{GS}=0V, dIF/dt=100A/μs	--	270	--	ns
Reverse Recovery Charge	Q_{rr}		--	1.9	--	μC

Notes:

1. L=30 mH, I_{AS}=4.23A, V_{DD}=195V, R_G=25Ω,starting T_J=25°C;
2. Pulse Test: Pulse width ≤300μs,Duty cycle≤2%;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-region Characteristics

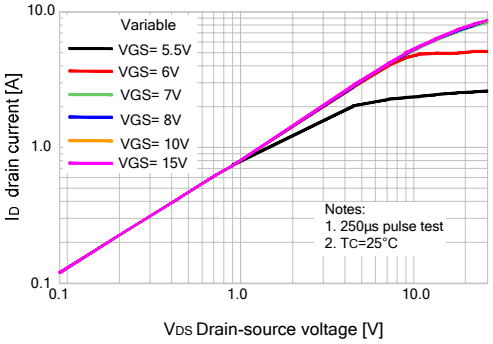


Figure 2. Transfer Characteristics

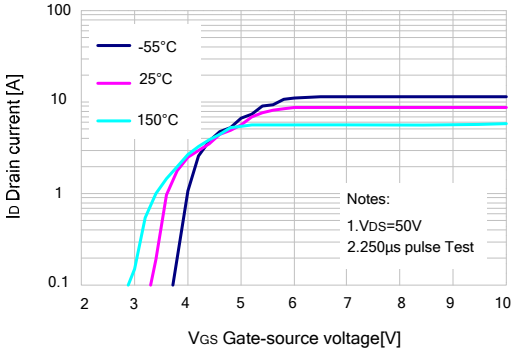


Figure 3. On-resistance variation vs. Drain current

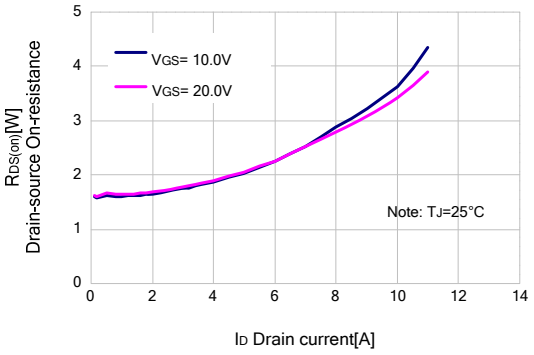
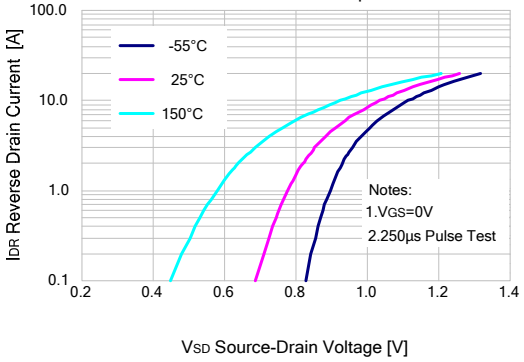


Figure 4. Body Diode Forward Voltage Variation Vs. Source Current and Temperature



TYPICAL CHARACTERISTICS(continued)

Figure 5. Breakdown Voltage Variation vs. Temperature

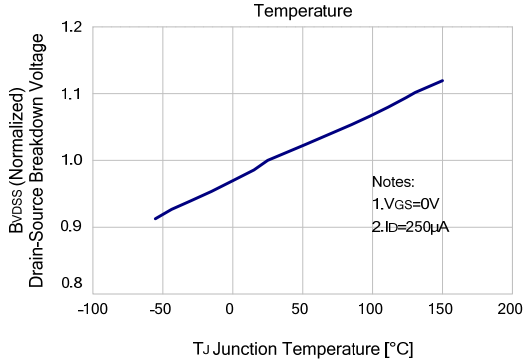


Figure 6. On-resistance Variation vs. Temperature

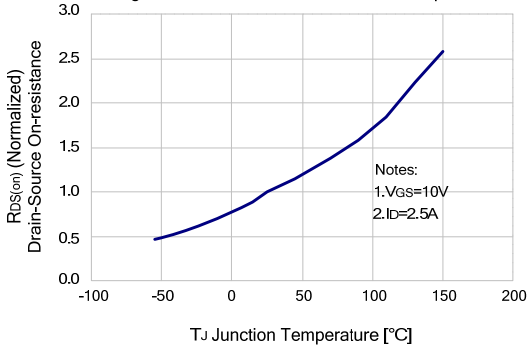


Figure 7. Capacitance Characteristics

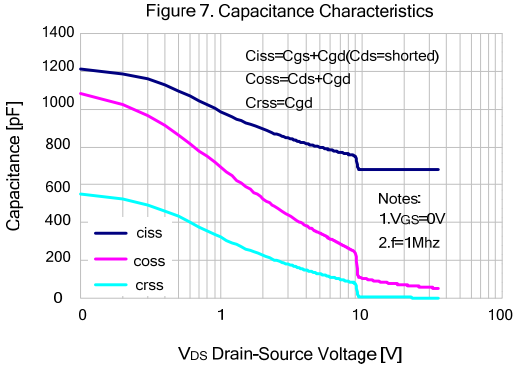


Figure 8-1. Max. Safe Operating Area(SVD5N60T)

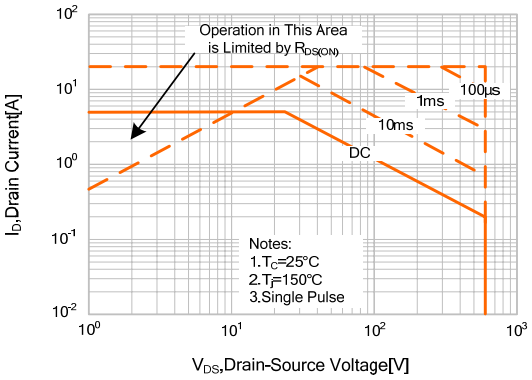


Figure 8-2. Max. Safe Operating Area(SVD5N60F)

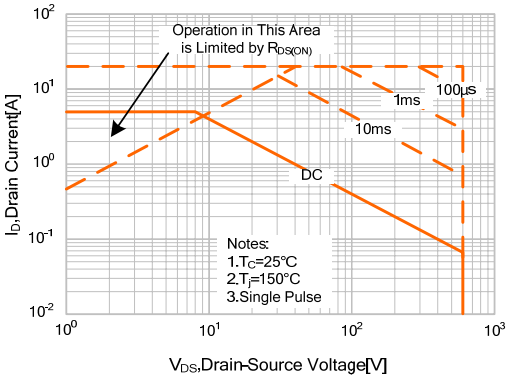
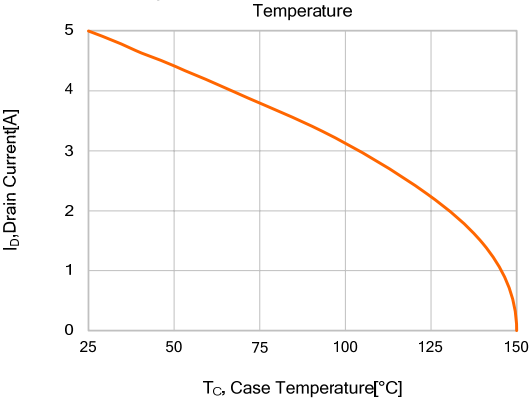
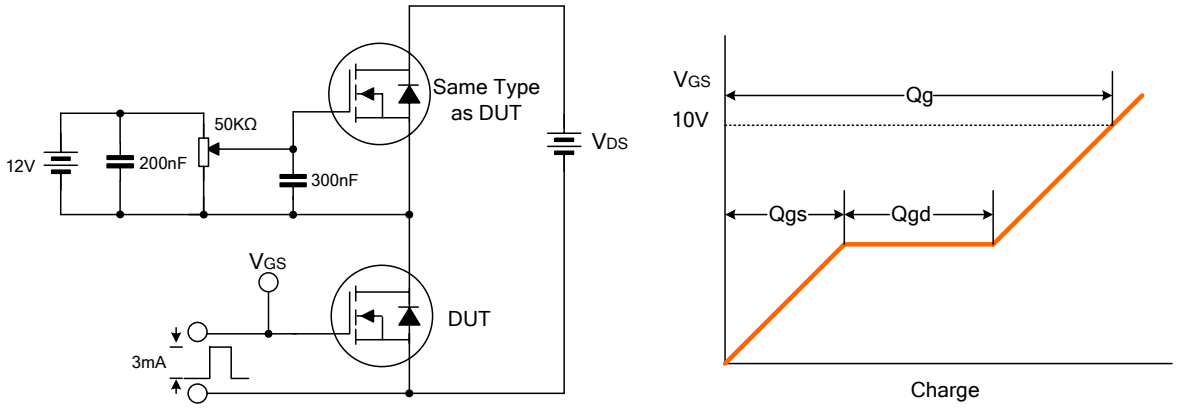


Figure 9. Maximum Drain Current vs. Case Temperature

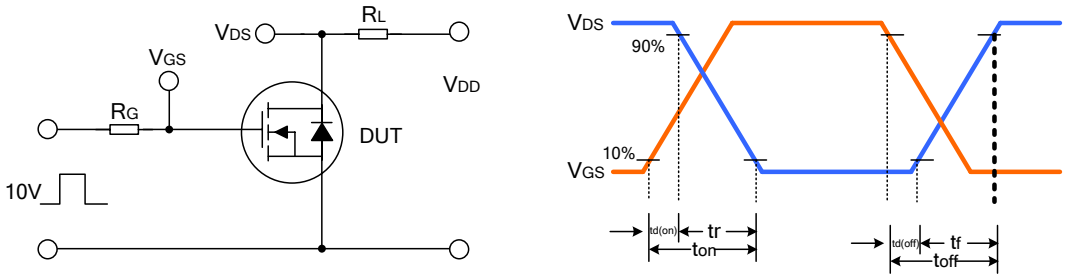


TYPICAL TEST CIRCUIT

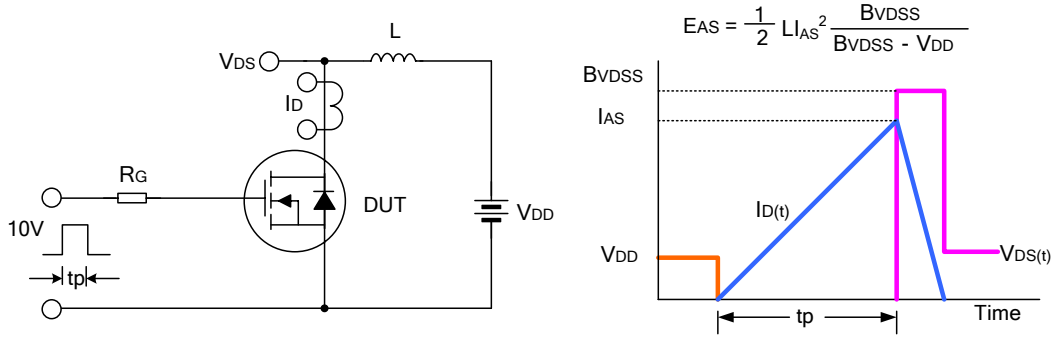
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform

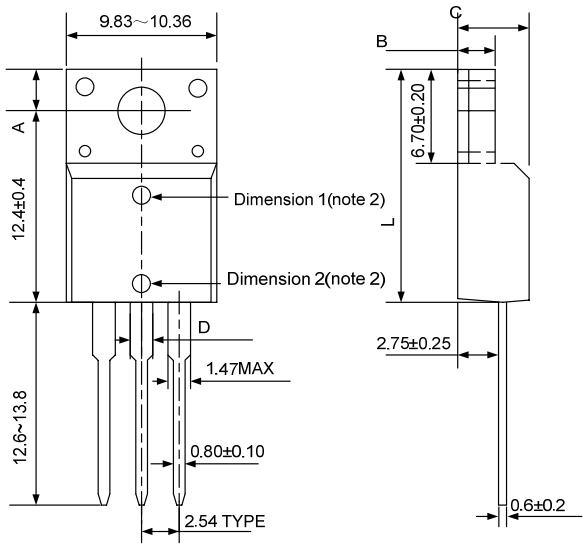


Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

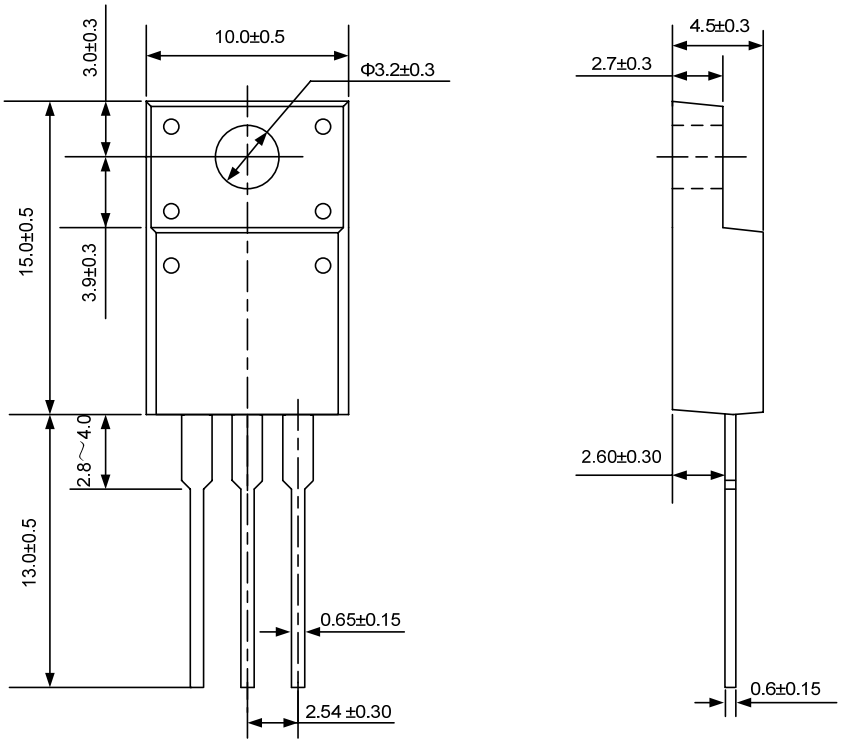
TO-220F-3L(ONE) UNIT: mm



Symbol(note1)	Dimension1	Dimension2
A	3.30±0.15	2.70±0.15
B	2.55±0.20	3.0±0.20
C	4.72±0.2	4.50±0.20
D	1.47MAX	1.75MAX
L	15.75±0.30	15.00±0.30

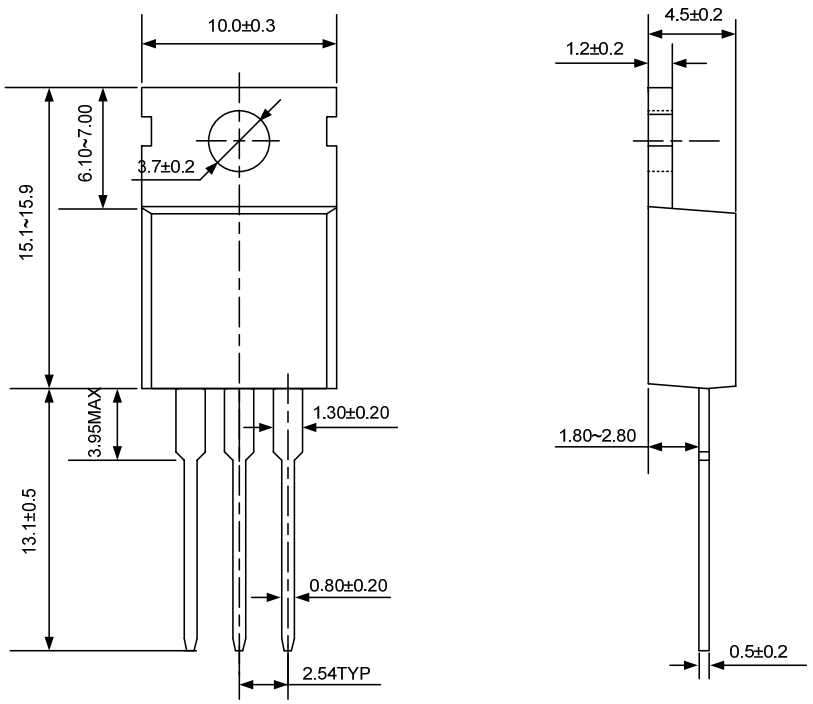
Note1: There may be two values for some products due to different plastic mould machine, so two dimensions of the same position are listed;
Note2: When the product size is Dimension1, the thimble hole is on top of the surface; when the size is Dimension2, the center hole is on bottom of the surface.

TO-220F-3L(TWO) UNIT: mm



PACKAGE OUTLINE(continued)

TO-220-3L UNIT: mm



Disclaimer:

- Silan reserves the right to make changes to the information herein for the improvement of the design and performance without further notice! Customers should obtain the latest relevant information before placing orders and should verify that such information is complete and current.
- All semiconductor products malfunction or fail with some probability under special conditions. When using Silan products in system design or complete machine manufacturing, it is the responsibility of the buyer to comply with the safety standards strictly and take essential measures to avoid situations in which a malfunction or failure of such Silan products could cause loss of body injury or damage to property.
- Silan will supply the best possible product for customers!

ATTACHMENT

Revision History

Date	REV	Description	Page
2010.05.13	1.0	Original	
2010.09.15	1.1	Add lanjian TO-220F-3L package; Add SOA and ID-TC curve	
2010.10.18	1.2	Modify"TYPICAL CHARACTERISTICS"	
2010.10.19	1.3	Modify the template of Datasheet	