

18A, 200V N-CHANNEL MOSFET

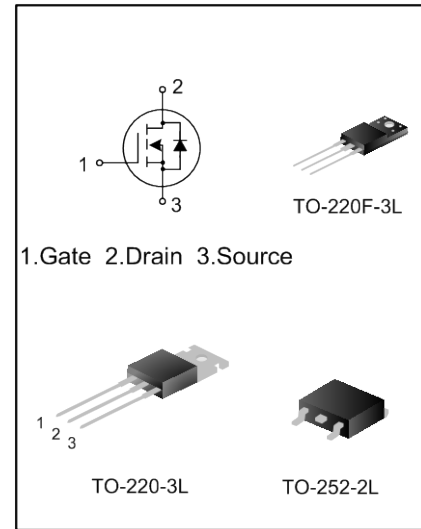
GENERAL DESCRIPTION

SVD640T/D/F is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary S-Rin™ structure middle/low-voltage VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- ◆ 18A,200V, $R_{DS(on)(typ.)}=0.12\Omega@V_{GS}=10V$
- ◆ Low gate charge
- ◆ Low Crss
- ◆ Fast switching
- ◆ Improved dv/dt capability



ORDERING INFORMATION

Part No.	Package	Marking	Material	Packing
SVD640T	TO-220-3L	SVD640T	Pb free	Tube
SVD640D	TO-252-2L	SVD640D	Halogen free	Tube
SVD640DTR	TO-252-2L	SVD640D	Halogen free	Tape & Reel
SVD640F	TO-220F-3L	SVD640F	Pb free	Tube

ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Characteristics		Symbol	Ratings			Unit
			SVD640T	SVD640D	SVD640F	
Drain-Source Voltage		V _{DS}	200			V
Gate-Source Voltage		V _{GS}	±20			V
Drain Current	T _C =25°C	I _D	18			A
	T _C =100°C		11			
Drain Pulsed Current		I _{DM}	72			A
Power Dissipation(T _C =25°C)		P _D	150	110	35	W
-Derate above 25°C			1.2	0.88	0.28	W/°C
Single Pulsed Avalanche Energy (Note 1)		E _{AS}	635			MJ
Operation Junction Temperature Range		T _J	150			°C
Storage Temperature Range		T _{stg}	-65~+150			°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Typ.			Unit
		SVD640T	SVD640D	SVD640F	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.83	1.14	3.57	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	62.0	62.5	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	$B_{V_{DS}}$	$V_{GS}=0V, I_D=250\mu A$	200	--	--	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS}=200V, V_{GS}=0V$	--	--	1	μA
		$V_{DS}=200V, V_{GS}=0V, T_c=125^{\circ}\text{C}$	--	--	1.0	
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	--	--	± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	3.0	4.0	V
Static Drain- Source On State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=9A$	--	0.12	0.15	Ω
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0\text{MHz}$	--	1108	--	pF
Output Capacitance	C_{oss}		--	160	--	
Reverse Transfer Capacitance	C_{rss}		--	34	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=100V, V_{GS}=10V,$ $R_G=2.5\Omega, I_D=11A$	--	15	--	ns
Turn-on Rise Time	t_r		--	47	--	
Turn-off Delay Time	$t_{d(off)}$		--	110	--	
Turn-off Fall Time	t_f		--	36	--	
Total Gate Charge	Q_g	$V_{DD}=160V, V_{GS}=10V,$ $I_D=11A$	--	41	--	nC
Gate-Source Charge	Q_{gs}		--	6.0	--	
Gate-Drain Charge	Q_{gd}		--	20	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse p-n Junction Diode in the MOSFET	--	--	18	A
Pulsed Source Current	I_{SM}		--	--	72	
Diode Forward Voltage	V_{SD}	$I_S=11A, V_{GS}=0V$	--	--	1.5	V
Reverse Recovery Time	T_{rr}	$V_{DD}=50V, di/dt=100A/\mu S,$ $I_F=11A$ (Note 2)	--	160	--	ns
Reverse Recovery Charge	Q_{rr}		--	0.98	--	μC

Notes:

1. $L=30\text{mH}, I_{AS}=5.0A, V_{DD}=100V, R_G=25\Omega$, starting $T_J=25^{\circ}\text{C}$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

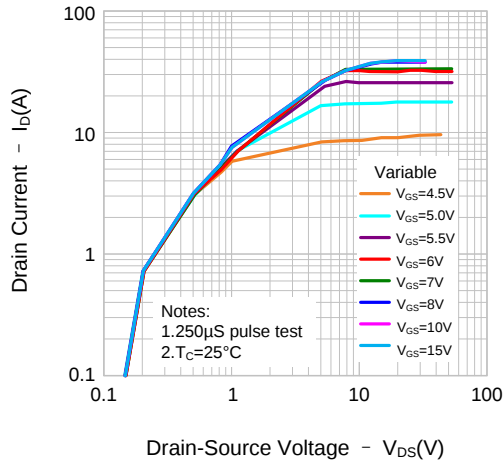


Figure 2. Transfer Characteristics

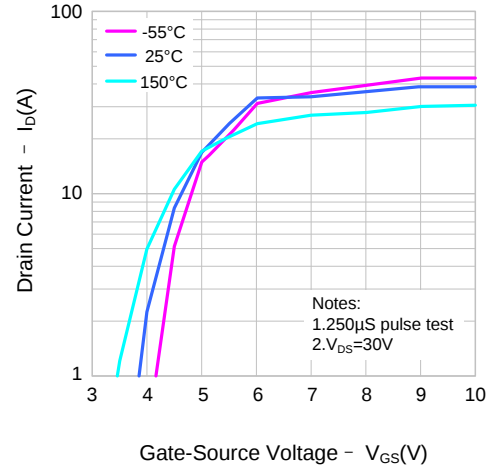


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

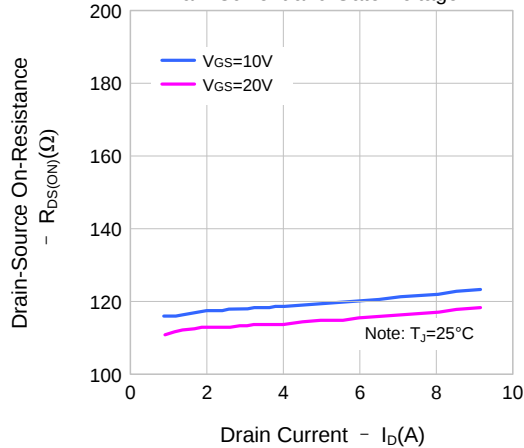


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

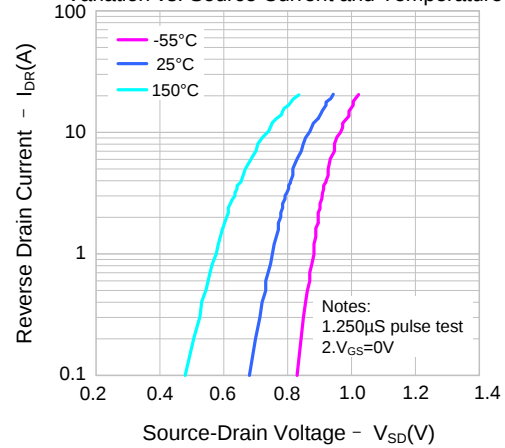


Figure 5. Capacitance Characteristics

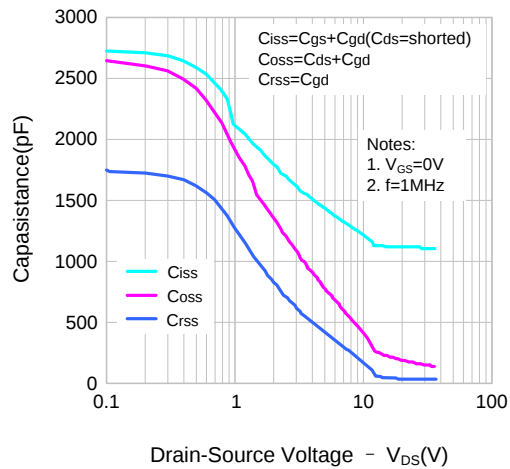
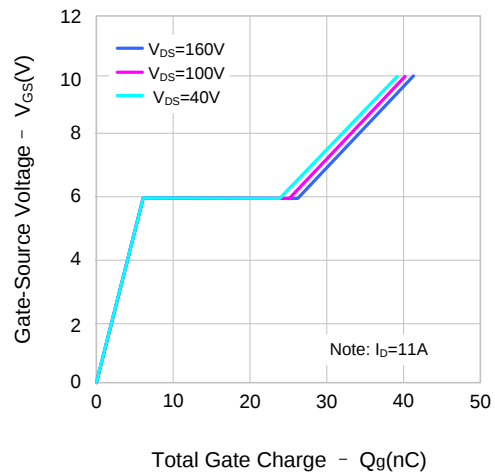


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continue)

Figure 7. Breakdown Voltage Variation vs. Temperature

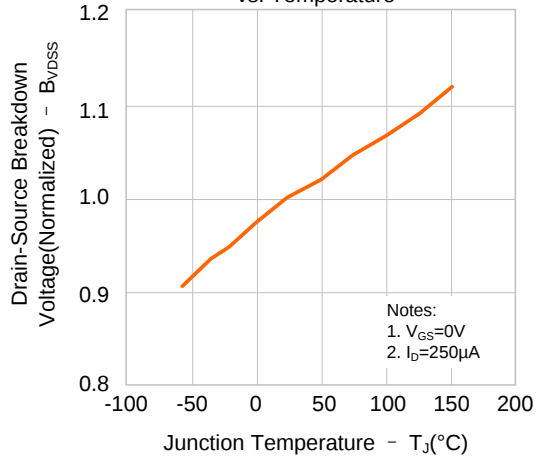


Figure 8. On-resistance Variation vs. Temperature

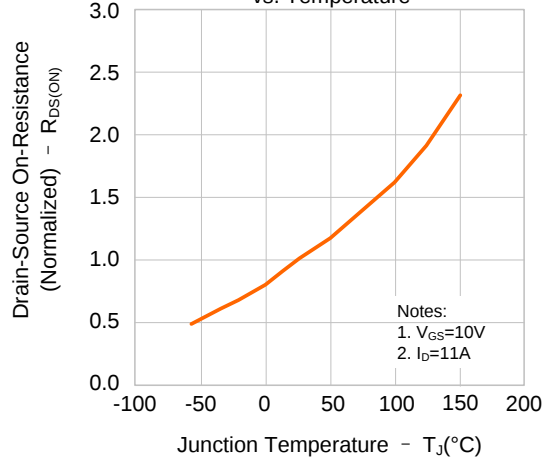


Figure 9-1. Max. Safe Operating Area(SVD640T)

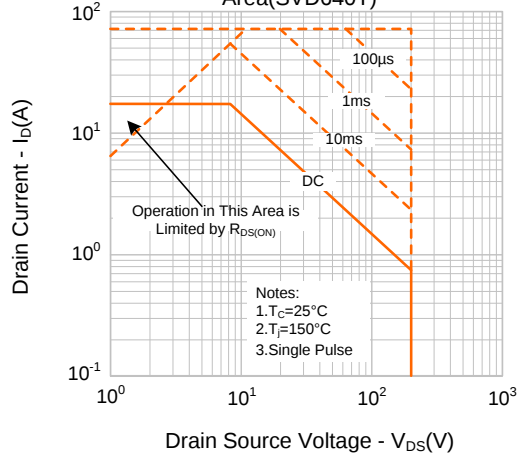


Figure 9-2. Max. Safe Operating Area(SVD640D)

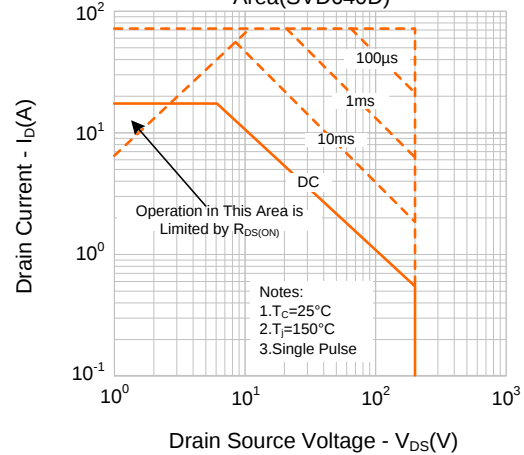


Figure 9-3. Max. Safe Operating Area(SVD640F)

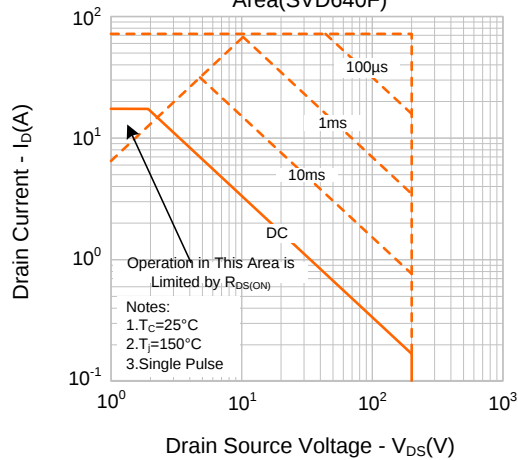
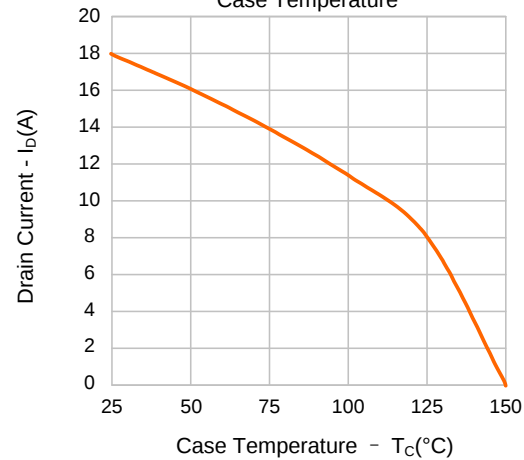
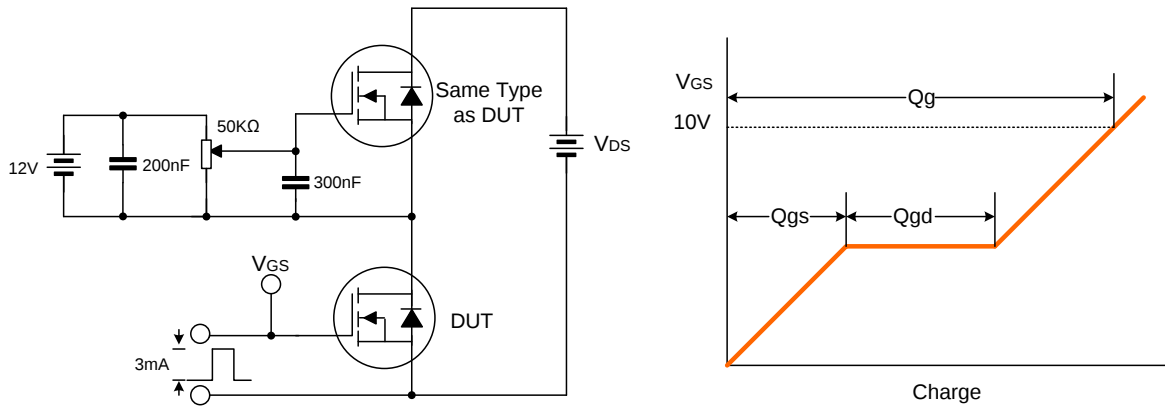


Figure 10. Maximum Drain Current vs. Case Temperature

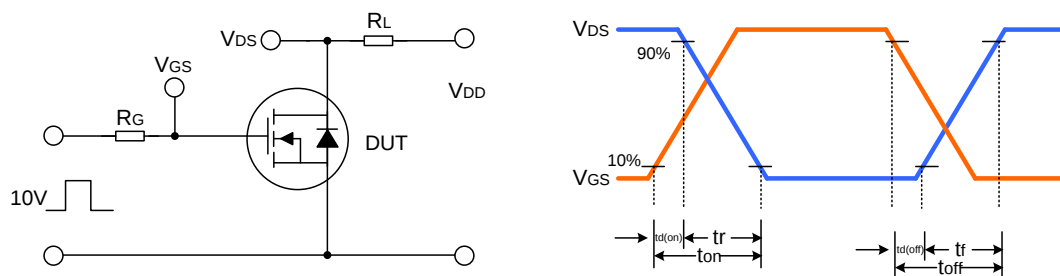


TYPICAL TEST CIRCUIT

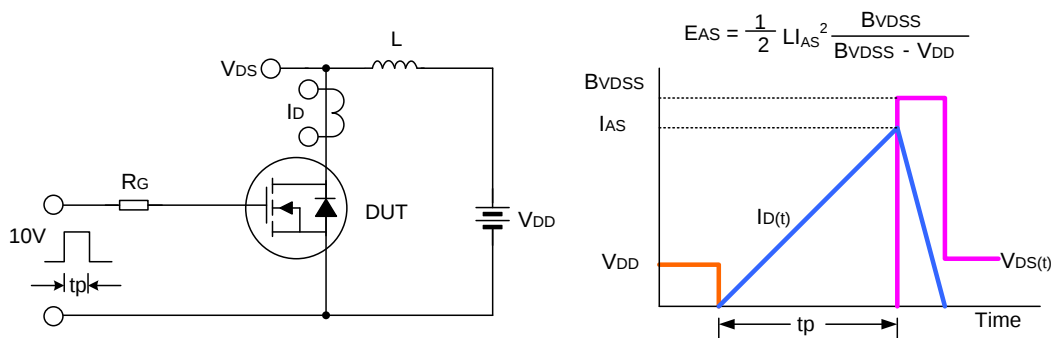
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



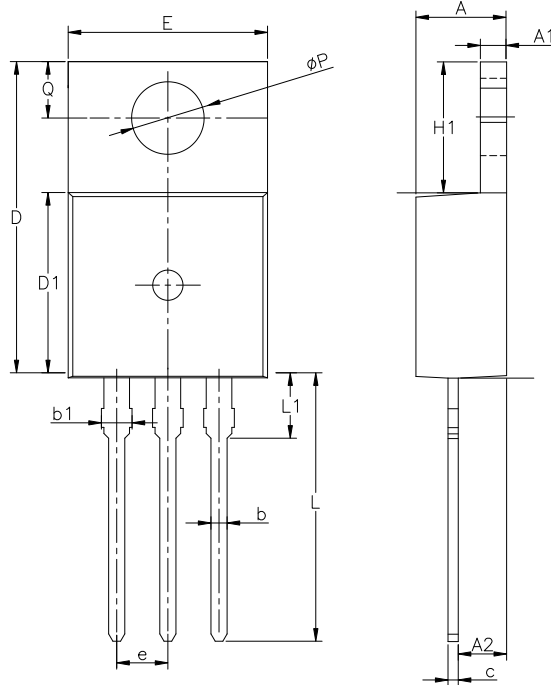
Unclamped Inductive Switching Test Circuit & Waveform



PACKAGE OUTLINE

TO-220-3L

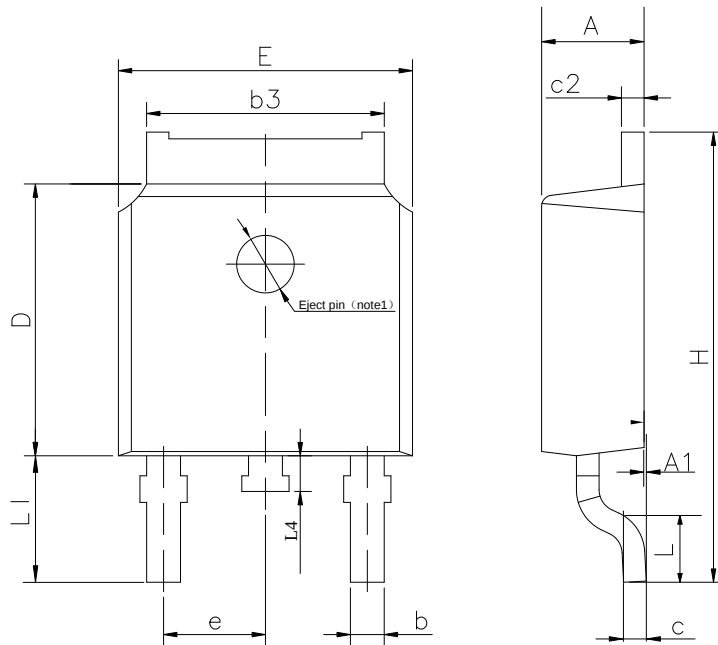
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	1.00	1.30	1.50
A2	1.80	2.40	2.80
b	0.60	0.80	1.00
b1	1.00	—	1.60
c	0.30	—	0.70
D	15.10	15.70	16.10
D1	8.10	9.20	10.00
E	9.60	9.90	10.40
e	2.54BSC		
H1	6.10	6.50	7.00
L	12.60	13.08	13.60
L1	—	—	3.95
ϕP	3.40	3.70	3.90
Q	2.60	—	3.20

TO-252-2L

UNIT: mm

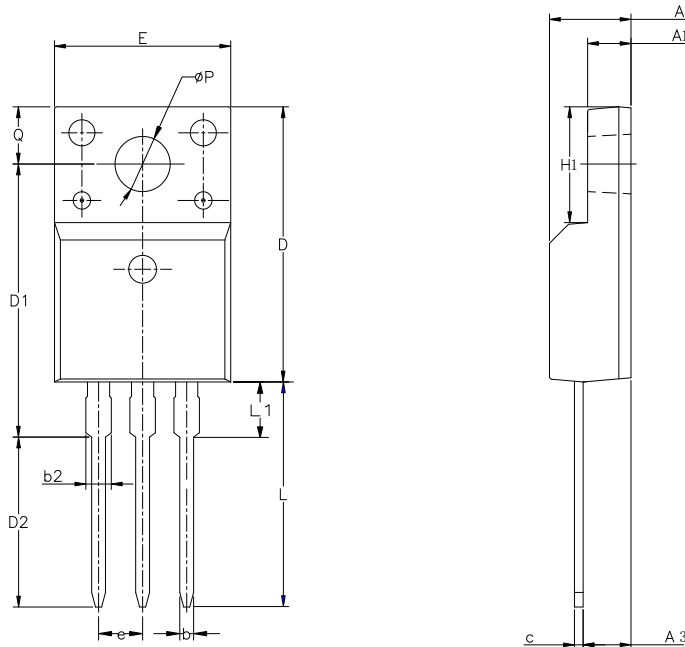


SYMBOL	MIN	NOM	MAX
A	2.10	2.30	2.50
A1	0	—	0.127
b	0.66	0.76	0.89
b3	5.10	5.33	5.46
c	0.45	—	0.65
c2	0.45	—	0.65
D	5.80	6.10	6.40
E	6.30	6.60	6.90
e	2.30TYP		
H	9.60	10.10	10.60
L	1.40	1.50	1.70
L1	2.90REF		
L4	0.60	0.80	1.00

NOTE1 : There are two conditions for this position:has an eject pin or has no eject pin.

TO-220F-3L

UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

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Part No.:	SVD640T/D/F	Document Type:	Datasheet
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Rev.:	1.1	Author:	Yin Zi
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Revision History:

1. Modify the package information of TO-220F-3L
 2. Modify the package information of TO-252-2L
 3. Modify the package information of TO-220-3L
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Rev.:	1.0	Author:	Yin Zi
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Revision History:

1. First release
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